Semiconductor packaging

Weekly Intelligence Report

2026-05-18 | 10 articles | 2 countries

troy-technical.jp

This Week's Keyword

AI Packaging Bottlenecks

Capacity, Materials, & Tech Lead Shifts

10	2	140,000	11.7
articles	countries	wafers/month	Gbps
Total Articles Analyzed	Source Countries	TSMC CoWoS Target (2027)	Samsung HBM4 Speed

All 10 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	TSMC Accelerates Adv Pkg	Corp Strategy	●●●○○	●●●●●	●●●●●	●●●○○	●●●●●	TSMC rapidly scales CoWoS/SoIC capacity with 18 new facilities to meet surging AI chip demand.
#02	TSMC CoWoS Bottleneck	Market Analysis	●●○○○	●●●●●	●●●●●	●●●●○	●●●●●	CoWoS bottleneck delays Google TPU mass production to 2027; Apple secures 2026 capacity.
#03	TSMC CoPoS Exclusivity	Corp Strategy	●●●●○	●●●○○	●●●●●	●●●○○	●●●●○	TSMC secures exclusive CoPoS supply chain to dominate next-gen panel-level AI packaging.
#04	TSMC SoIC 3D Roadmap	Research Roadmap	●●●●○	●●○○○	●●●●○	●●●●○	●●●●○	TSMC's SoIC roadmap targets 4.5μm pitch by 2029, enabling F2F chiplet integration for Fujitsu Monaka CPU.
#05	ABF Substrate Bottleneck	Market Analysis	●●○○○	●●●●●	●●●●●	●●●●○	●●●●●	Ajinomoto's ABF substrate near-monopoly creates critical bottleneck for AI hardware; customers pre-fund capacity.
#06	Hanmi 2nd-Gen Hybrid Bonder	New Product	●●●●○	●●●○○	●●●●○	●●●●○	●●●○○	Hanmi unveils 2nd-gen hybrid bonder for >20-layer HBM, investing $67M in new factory.
#07	SK Hynix HBM Pkg Hub	Corp Strategy	●●○○○	●●●●○	●●●●○	●●●○○	●●●●○	SK Hynix breaks ground on new HBM packaging hub in Cheongju to boost AI memory capacity.
#08	Samsung HBM4 Hybrid Bond	New Product	●●●●○	●●●●○	●●●●●	●●●●○	●●●●○	Samsung pioneers HBM4 mass production with hybrid bonding, achieving 11.7Gbps, securing market lead.
#09	SK Hynix 12-Die HBM Stack	Research	●●●●○	●●○○○	●●●●○	●●●○○	●●●●○	SK Hynix validates 12-die hybrid bonded HBM stack, pushing limits for HBM4/HBM5, but yield undisclosed.
#10	Samsung/Sumitomo Glass JV	Corp Strategy	●●●●○	●●●○○	●●●●○	●●●●○	●●●○○	Samsung Electro-Mechanics and Sumitomo Chemical JV for glass core substrates, critical for next-gen AI packaging.

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI product roadmap exposed to TSMC's CoWoS/SoIC capacity bottlenecks?

TSMC's aggressive expansion (140k wafers/month by 2027) is still insufficient, delaying Google TPUs to 2027. Apple's early capacity reservation highlights intense competition. Does your procurement strategy account for this critical bottleneck?

❷ How vulnerable is your AI hardware supply chain to the ABF substrate monopoly?

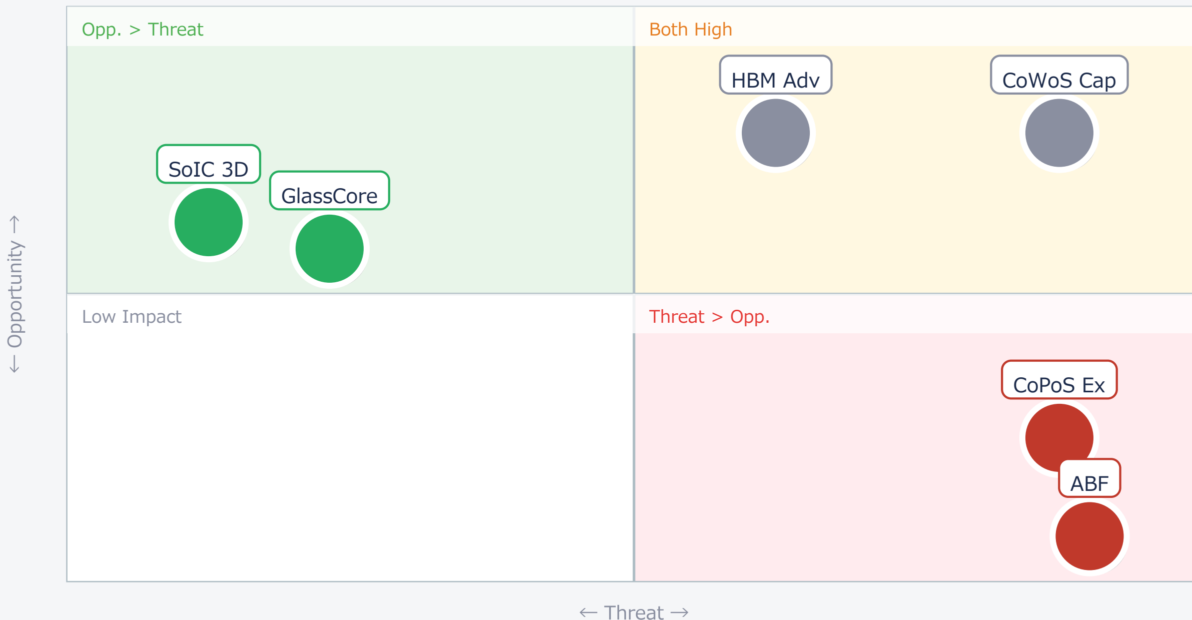
Ajinomoto's near-monopoly on ABF film is a critical bottleneck for AI server chips, consuming 10x more ABF than PC chips. Major chipmakers are pre-funding supplier capacity. Have you diversified or invested in alternative materials?

❸ Does Samsung's HBM4 hybrid bonding lead make your next-gen AI platforms obsolete?

Samsung's early mass production of HBM4 with hybrid bonding achieves 11.7Gbps, 46% above JEDEC standards, shipping to NVIDIA. SK Hynix is also validating 12-die stacks. How will this impact your HBM integration and competitive strategy?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
● CoWoS Cap	Critical	AI chip supply	Supply bottleneck
● HBM Adv	Critical	HBM performance	Tech/Cap lag
● SoIC 3D	Opp.	3D chiplets	Integration gap
● GlassCore	Opp.	New materials	Organic subs.
● CoPoS Ex	Threat	—	Tech lock-out
● ABF	Threat	Alt. materials	Supply bottleneck

Deep Dive ① — TSMC Accelerates Advanced Packaging Capacity

#01 | 2026/05/14 | 専門メディア | Tech Novelty●●●○○ Proximity●●●●● Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●●

TSMC is aggressively expanding its CoWoS and SoIC advanced packaging capacity with 18 new global facilities. This aims to alleviate critical bottlenecks in the AI/HPC supply chain and support next-gen AI accelerator performance.

The expansion is a direct response to surging AI demand, with CoWoS crucial for HBM integration and SoIC enabling higher density 3D chip stacking for ultra-compact, high-bandwidth designs.

▶ Strategic Analyst's Perspective

> Strategic Analyst's Perspective: TSMC's expansion is realistic given market demand, but equipment lead times and skilled labor remain technical barriers. [Opportunity] for US/EU OEMs to secure advanced AI chip supply and for US/EU equipment/materials suppliers to engage with TSMC's build-out. [Threat] is increased reliance on a single dominant supplier, potentially exacerbating future supply chain concentrations. Next actions: [Procurement] Diversify advanced packaging partners beyond TSMC; [Strategy] Investigate domestic/regional advanced packaging R&D; initiatives by Q3 2026.

Deep Dive ② — ABF Substrate: Critical AI Bottleneck

#05 | 2026/04/07 | 専門メディア (分析) | Tech Novelty●●○○○ Proximity●●●●● Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●●

Ajinomoto Build-up Film (ABF), a key dielectric for high-performance substrates, has become a critical bottleneck in the AI hardware supply chain due to Ajinomoto Fine-Techno's near-monopoly.

AI server chips consume over ten times more ABF than PC chips. Major AI chip customers like Nvidia and Intel are pre-funding ~50% of top substrate suppliers' capacity expansions to secure supply.

▶ Strategic Analyst's Perspective

> Strategic Analyst's Perspective: This bottleneck is highly realistic and a known industry challenge. Technical barriers include Ajinomoto's proprietary IP and the complex manufacturing process for ABF. [Opportunity] for US/EU materials & chemical companies to develop alternative high-performance dielectric films or for new entrants to challenge Ajinomoto's dominance. [Threat] is significant production delays and increased costs for US/EU OEMs reliant on AI hardware, and severe supply chain vulnerability. Next actions: [Procurement] Conduct an immediate audit of ABF exposure in your AI hardware supply chain; [R&D;] Fund R&D; into alternative advanced dielectric materials by Q2 2026.

Deep Dive ③ — Samsung Pioneers HBM4 with Hybrid Bonding

#08 | Date unknown | 専門メディア | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●○

Samsung Electronics is deploying dedicated hybrid bonding lines for HBM4, claiming world-first mass production with shipments to NVIDIA. This achieves 11.7Gbps, 46% above JEDEC standards.

Hybrid bonding directly connects copper lines, reducing inter-chip spacing, mitigating heat, and boosting data transfer. This is critical for next-gen HBM performance in AI/HPC applications.

> ▶ Strategic Analyst's Perspective
>
> Strategic Analyst's Perspective: Samsung's claim of HBM4 mass production with hybrid bonding is realistic, cementing its lead. Technical barriers include achieving high yield for multi-layer hybrid bonding and effective thermal management. [Opportunity] for US/EU AI chip designers to leverage higher-performance HBM4 for next-gen platforms and for US/EU equipment/tooling suppliers to support hybrid bonding processes. [Threat] for US/EU memory and AI chip companies falling behind in advanced HBM integration, increasing reliance on Asian suppliers for leading-edge memory. Next actions: [R&D;] Evaluate HBM4 integration strategies and engage with Samsung/SK Hynix on future HBM roadmaps by Q3 2026; [Business Dev] Explore partnerships with hybrid bonding equipment providers.

Other Notable Articles

TSMC Forges Exclusive CoPoS Supply Chain (専門メディア)

Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●●

TSMC's exclusive CoPoS strategy aims to lock out competitors from next-gen panel-level packaging. US/EU firms must assess IP and supply chain risks.

TSMC Unveils SoIC 3D Stacking Roadmap (専門メディア)

Tech Novelty●●●●○ Proximity●●○○○ Market Impact●●●●○

TSMC's SoIC roadmap to 4.5μm pitch by 2029 enables advanced F2F chiplet integration, crucial for future AI/HPC architectures.

Samsung Electro-Mechanics and Sumitomo Chemical Group Partner to Establish Glass Core Substrate Joint Venture (企業発表)

Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○

JV for glass core substrates addresses warpage and signal integrity for large-area AI packages, a key material shift for advanced packaging.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Conduct an urgent audit of ABF substrate exposure across all AI hardware supply chains, identifying single points of failure.
- [Executive] Schedule a strategic review to assess the impact of TSMC's CoWoS/SoIC capacity bottlenecks on current and future AI product roadmaps.

Short-term (1 month)

- [R&D;] Initiate exploratory research into alternative high-performance dielectric materials to reduce reliance on Ajinomoto's ABF film.
- [Strategy] Analyze TSMC's CoPoS exclusivity strategy and its potential long-term impact on access to next-generation panel-level packaging technologies.
- [Business Dev] Engage with Samsung and SK Hynix to understand their HBM4 hybrid bonding roadmaps and secure future supply allocations.

Medium-long term (quarter+)

- [Strategy] Develop a multi-year plan to diversify advanced packaging partners and explore domestic/regional advanced packaging R&D; and manufacturing capabilities.
- [R&D;] Invest in internal R&D; or strategic partnerships for 3D chiplet integration (e.g., SoIC) and glass core substrate technologies to maintain competitive edge.
- [Legal/IP] Review IP landscape for hybrid bonding and advanced packaging materials to identify licensing opportunities or potential infringement risks.

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Semiconductor_BackEnd — Selected Articles

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Articles: 10

Table of Contents

#01 TSMC Accelerates Advanced Packaging Capacity Expansion to Meet Exploding AI Demand

#02 TSMC's CoWoS Bottleneck Threatens to Delay Google TPU Mass Production to 2027

#03 TSMC Forges Exclusive CoPoS Supply Chain to Secure Next-Gen AI Packaging Dominance

#04 TSMC Unveils SoIC 3D Stacking Roadmap: Achieving 4.5μm Pitch by 2029, Enabling Face-to-Face Chiplet Integration for Fujitsu Monaka CPU

#05 ABF Substrate Becomes Critical Bottleneck in AI Hardware Supply Chain, Driven by Ajinomoto's Dominance

#06 Hanmi Semiconductor Unveils Second-Gen Hybrid Bonder for Advanced HBM Stacking, Investing $67M in New Factory

#07 SK Hynix Initiates HBM Packaging Hub Construction in Cheongju to Bolster AI Memory Capacity

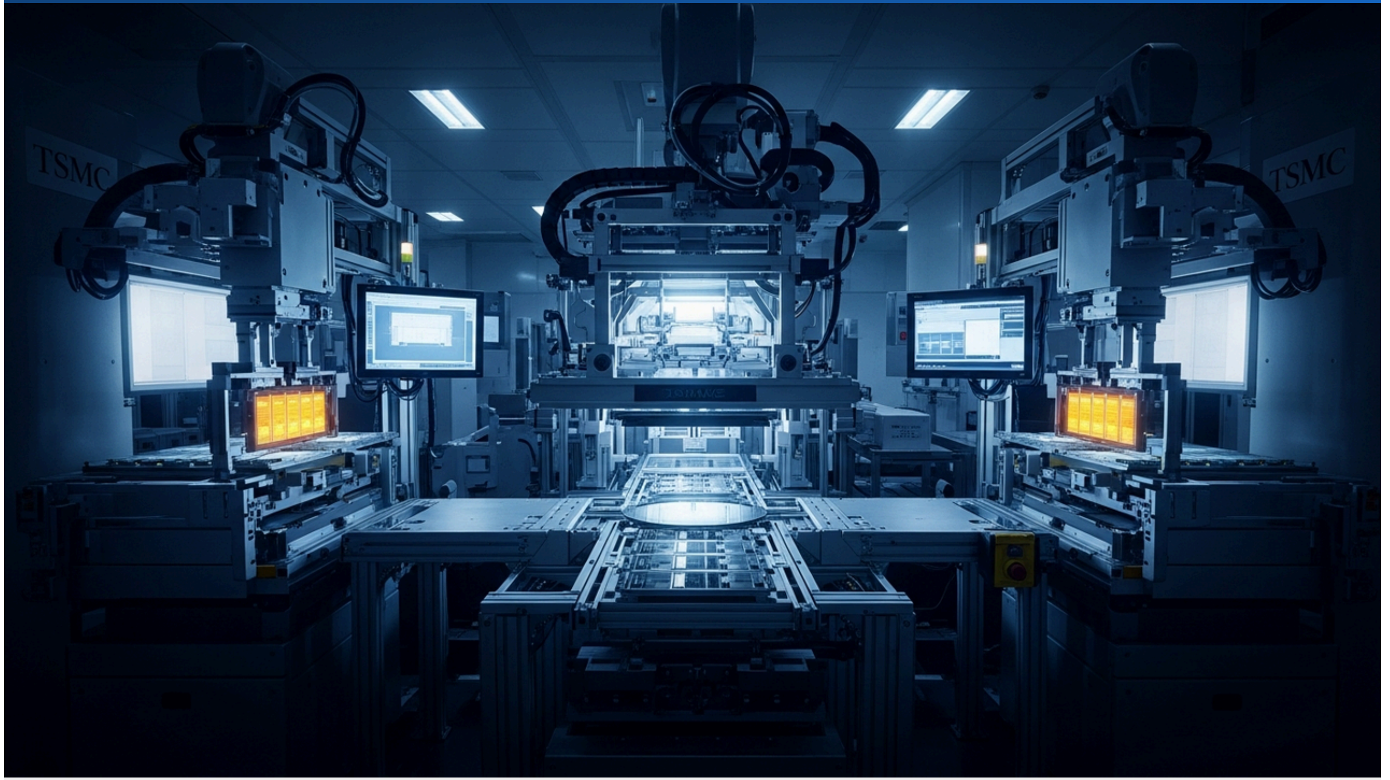
#08 Samsung Electronics Pioneers HBM4 Mass Production with Hybrid Bonding, Solidifying Market Lead

#09 SK Hynix Validates 12-Die Hybrid Bonded HBM Stack Amidst Heated AI Memory Race

#10 Samsung Electro-Mechanics and Sumitomo Chemical Group Partner to Establish Glass Core Substrate Joint Venture

TSMC Accelerates Advanced Packaging Capacity Expansion to Meet Exploding AI Demand

Published May 14, 2026　　専門メディア　　Taiwan



OVERVIEW

TSMC is rapidly scaling its advanced CoWoS and SoIC packaging capacity to address the surging demand for AI chips. With 18 new fabs and advanced packaging facilities under construction globally, this expansion aims to alleviate critical bottlenecks in the AI/HPC supply chain and sustain the performance trajectory of next-generation AI accelerators.

IN DEPTH

Background

The insatiable demand for artificial intelligence (AI) and high-performance computing (HPC) has fundamentally reshaped the semiconductor industry, shifting focus beyond traditional transistor scaling to advanced packaging solutions. As AI chips become increasingly complex and data-intensive, integrating multiple dies into a single package, such as with CoWoS (Chip on Wafer on Substrate) and SoIC (System on Integrated Chips), has become paramount for achieving performance and power efficiency targets. TSMC, a dominant player in foundry services, has been at the forefront of developing and deploying these sophisticated packaging technologies.

Key Findings / Results

TSMC announced a significant acceleration of its advanced packaging capacity expansion for both CoWoS and SoIC, directly responding to the robust AI market growth. During its 2026 Technology Symposium, the company detailed advancements in its leading-edge process nodes, showcased its comprehensive 3DFabric advanced packaging roadmap, and highlighted its global manufacturing footprint strategy, including the deployment of AI-powered smart manufacturing. A staggering 18 new fabs and advanced packaging facilities are currently under construction worldwide, underscoring TSMC's commitment to bolstering supply. This aggressive build-out is critical for accommodating the increasingly intricate architectures of AI/HPC chips that rely heavily on dense inter-die connections and superior power delivery facilitated by these advanced packaging schemes.

Technical Significance & Outlook

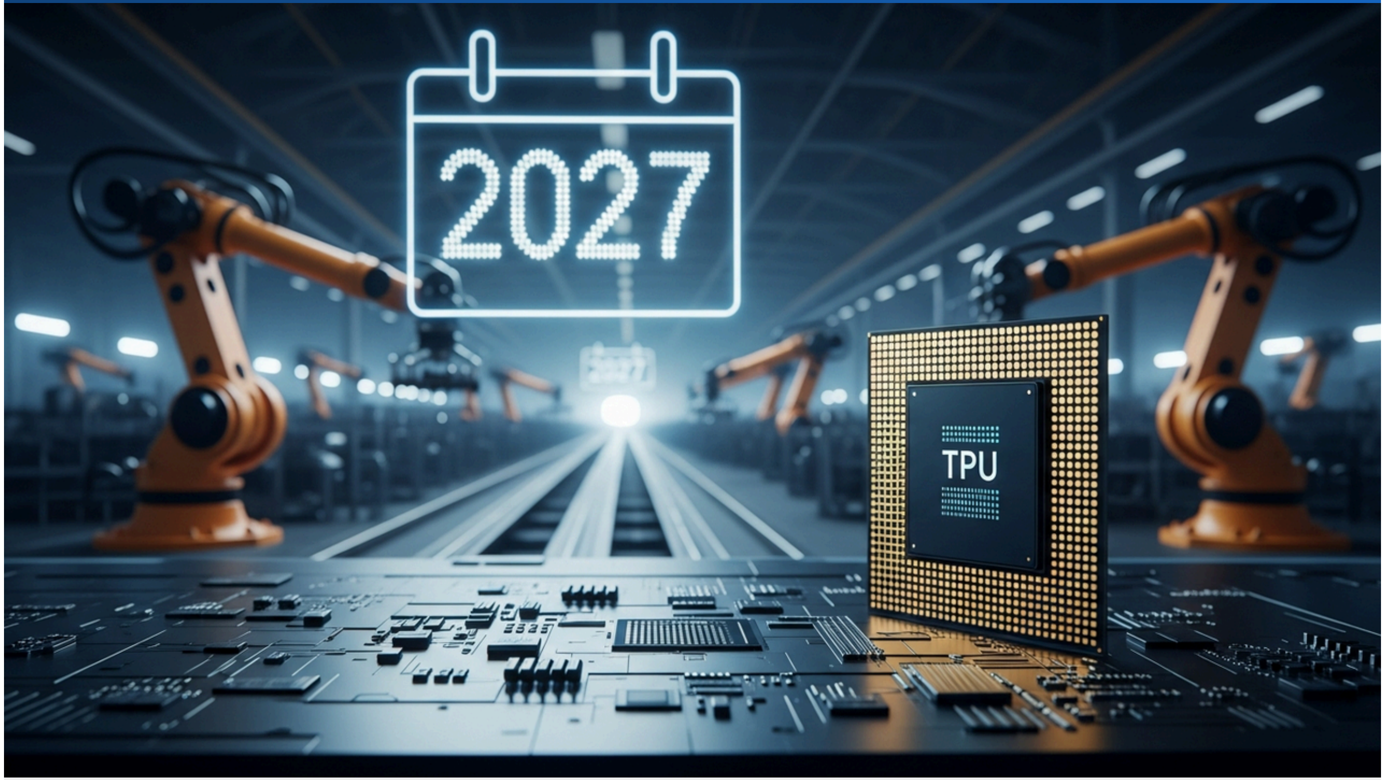
The rapid expansion of CoWoS and SoIC capacity carries profound technical and industrial significance. CoWoS, a 2.5D packaging solution, is essential for integrating logic dies with HBM stacks, a configuration central to leading AI accelerators. SoIC, a 3D chip stacking technology, offers even higher inter-die connection density by enabling face-to-face bonding, paving the way for ultra-compact and high-bandwidth chiplet designs. This capacity ramp-up directly addresses a critical bottleneck in the AI semiconductor supply chain, which has seen extended lead times for advanced packaged components. By expanding globally and integrating AI into manufacturing, TSMC aims to enhance efficiency, reduce time-to-market, and provide a more resilient supply network. This strategic investment is poised to unlock further innovation in AI hardware, enabling the development of even more powerful and efficient computing platforms.

Source: #

Collected: May 15, 2026 | Automated Research System (Gemini API)

TSMC's CoWoS Bottleneck Threatens to Delay Google TPU Mass Production to 2027

Published May 14, 2026 専門メディア Taiwan



OVERVIEW

Chronic shortages in TSMC's CoWoS advanced packaging capacity are projected to delay mass production of Google's custom AI chips (TPU) until 2027. Despite TSMC's aggressive expansion plans targeting 120,000 wafers/month by late 2026 and 140,000 by late 2027, Apple's reservation of initial 2026 capacity leaves limited bandwidth for Google, highlighting the intense competition for critical packaging resources in the AI market.

IN DEPTH

Background

The burgeoning demand for artificial intelligence (AI) has spurred major technology companies like Google to develop specialized AI accelerators, such as their Tensor Processing Units (TPUs). These high-performance chips necessitate sophisticated packaging technologies like CoWoS (Chip on Wafer on Substrate) to integrate multiple logic dies with high-bandwidth memory (HBM), ensuring maximum computational efficiency. However, the unprecedented surge in AI chip demand has strained the supply of these advanced packaging solutions, creating a significant bottleneck in the semiconductor supply chain.

Key Findings / Results

Industry analysis indicates that TSMC's constrained CoWoS packaging capacity may defer the mass production of Google's custom AI chip, the TPU, until 2027. TSMC is actively expanding its CoWoS capacity, aiming for 120,000 wafers per month by the end of 2026 and 140,000 wafers per month by the end of 2027, a substantial increase from 45,000 wafers/month in early 2025. Nevertheless, Apple is reportedly securing a significant portion of TSMC's early 2026 CoWoS capacity for its next-generation processors, consequently limiting the availability for Google's TPUs. This allocation strategy is expected to cap Google's TPU production at 3.1-3.2 million units in 2026, with a projected increase to 5-6 million units in 2027. The current demand for CoWoS significantly outstrips supply, impacting major customers and their product timelines.

Technical Significance & Outlook

The CoWoS capacity bottleneck underscores the critical role of advanced packaging in the AI era. As a 2.5D integration technology, CoWoS facilitates high-density integration of logic and memory, a cornerstone for high-performance AI accelerators. The delay in TPU mass production due to packaging constraints highlights that advanced packaging, rather than frontend wafer fabrication, has become a key determinant for AI product time-to-market. TSMC's aggressive capacity ramp-up, while necessary, reveals the structural challenges in meeting exploding AI demand. The anticipated easing of CoWoS supply in 2027, driven by TSMC's investments, is expected to benefit not only Google but also other major clients like Broadcom and MediaTek, enabling broader deployment of advanced AI hardware. This situation also prompts hyper-scalers to potentially explore diversified supply chains or alternative packaging solutions to mitigate future single-vendor dependencies.

Source: #

TSMC Forges Exclusive CoPoS Supply Chain to Secure Next-Gen AI Packaging Dominance

Published May 08, 2026　専門メディア　Taiwan

OVERVIEW

TSMC is reportedly implementing a highly exclusive supply chain strategy for CoPoS, its next-generation panel-level packaging technology, to solidify its leadership in AI semiconductors. This move, involving strict non-disclosure agreements and supply restrictions with Taiwanese equipment and material partners post-mass production, aims to prevent technology leakage and ensure TSMC's proprietary edge over rivals in advanced AI packaging.

IN DEPTH

Background

As the performance demands of AI semiconductors continue to escalate, advanced packaging technologies are becoming as critical as leading-edge wafer fabrication. TSMC has already established a strong lead with its CoWoS (Chip on Wafer on Substrate) platform, but it is now aggressively pursuing CoPoS (Chip on Panel on Substrate), a panel-level packaging technology, as the next frontier. CoPoS promises greater efficiency and scalability for larger AI chip packages by processing multiple chips on larger panel substrates, moving beyond traditional wafer-based methods.

Key Findings / Results

Reports indicate that TSMC is not only accelerating its CoWoS capacity expansion but is also strategically consolidating its lead in CoPoS technology. To secure its dominance in this critical next-generation AI packaging solution, TSMC is reportedly imposing stringent confidentiality and exclusivity agreements on its Taiwanese equipment and material suppliers. These agreements are said to mandate strict control over intellectual property and restrict these partners from supplying CoPoS-related technologies to competitors for several years after mass production commences. This aggressive strategy aims to protect TSMC's technological advancements and ensure a proprietary edge in the highly competitive AI semiconductor market.

Technical Significance & Outlook

The push for CoPoS exclusivity highlights the immense strategic value TSMC places on advanced packaging as a differentiator for AI hardware. CoPoS, with its potential for higher throughput and lower cost per chip compared to wafer-level processes like CoWoS, is envisioned to be crucial for the large-scale production of future AI accelerators. By locking down its supply chain, TSMC is proactively mitigating risks of technology transfer to competitors, thereby extending its lead in an area increasingly critical for AI performance. This strategy also implies a significant investment in R&D and manufacturing infrastructure for CoPoS, likely influencing the development trajectory of the entire AI semiconductor industry. Competitors will face steeper barriers to entry, potentially solidifying TSMC's long-term position as the premier advanced packaging provider for high-end AI and HPC applications.

Source: https://www.digitimes.com/news/a20260508PD207/tsmc-packaging-cowos-expansion-capacity.html

Collected: May 15, 2026 | Automated Research System (Gemini API)

TSMC Unveils SoIC 3D Stacking Roadmap: Achieving 4.5μm Pitch by 2029, Enabling Face-to-Face Chiplet Integration for Fujitsu Monaka CPU

Published April 29, 2026 専門メディア Taiwan

OVERVIEW

TSMC has revealed its SoIC (System on Integrated Chips) 3D stacking roadmap, targeting a 4.5-micron pitch by 2029, down from today's 6 microns. This advanced face-to-face (F2F) chiplet stacking technology, part of the second-generation SoIC, is poised to benefit high-performance CPUs like Fujitsu's Monaka, significantly boosting vertical interconnect density for next-generation AI/HPC chips.

IN DEPTH

Background

The relentless pursuit of higher performance in AI and High-Performance Computing (HPC) has driven the semiconductor industry beyond traditional 2D scaling, making 3D integration technologies increasingly vital. TSMC's System on Integrated Chips (SoIC) is a foundational 3D stacking solution that enables ultra-fine pitch inter-die bonding, offering superior bandwidth and lower latency compared to conventional packaging methods that rely on wire bonding or microbumps. This vertical integration is crucial for assembling complex chiplet-based architectures that demand maximum density and minimal communication overhead between constituent dies.

Key Findings / Results

TSMC has published an ambitious roadmap for its SoIC 3D stacking technology, detailing plans to shrink the inter-die connection pitch from the current 6 micrometers (μm) to an impressive 4.5 μm by 2029. This pitch reduction directly translates to a significant increase in vertical interconnect density, enhancing data throughput and overall system performance. A cornerstone of this advancement is the second-generation SoIC technology, which introduces face-to-face (F2F) stacking. F2F bonding allows direct electrical connection between the active surfaces of two dies, minimizing wiring layers and optimizing electrical characteristics. Fujitsu's upcoming Monaka supercomputer CPU is expected to be an early adopter of this F2F chiplet stacking, leveraging its benefits for enhanced performance. For instance, the A14-to-A14 SoIC, slated for mass production in 2029, is projected to deliver 1.8 times the inter-die I/O density compared to N2-on-N2 SoIC.

Technical Significance & Outlook

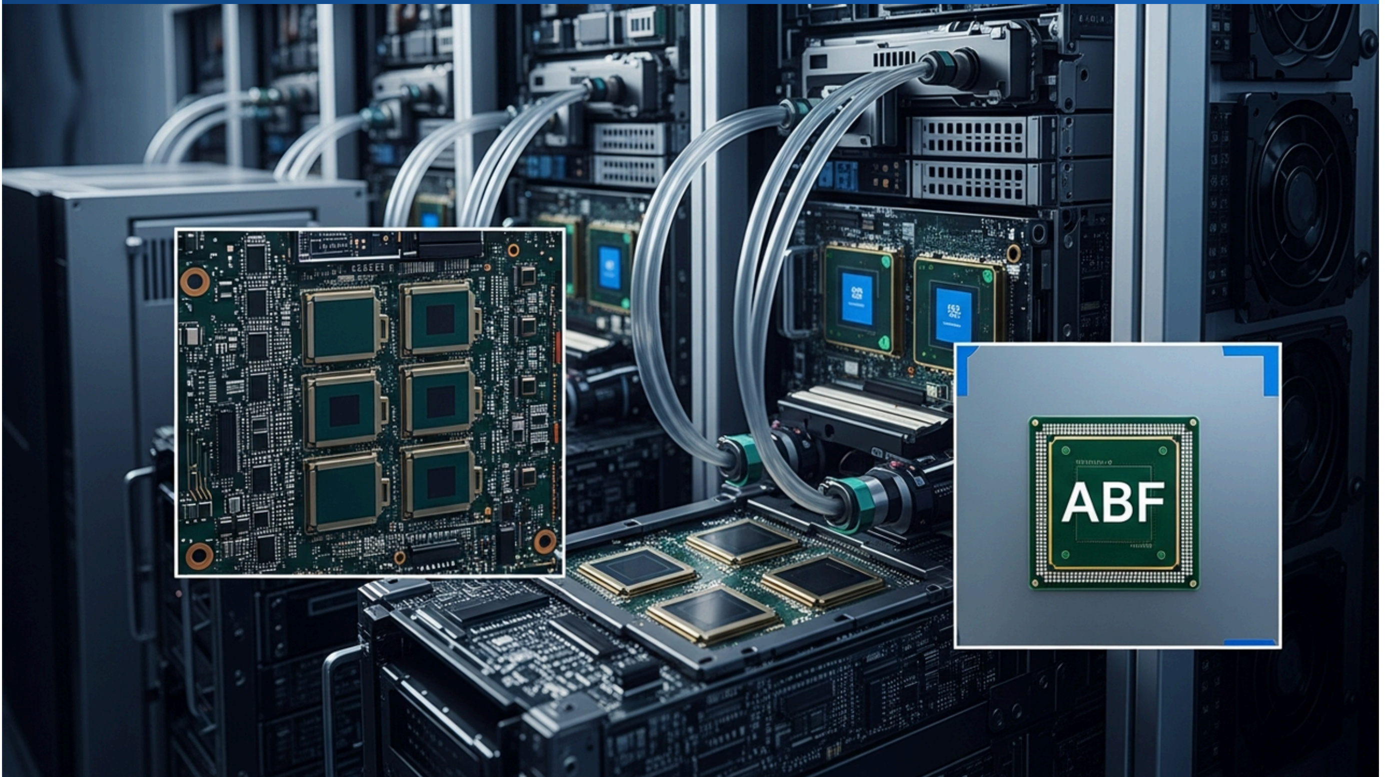
The continued pitch miniaturization of SoIC represents a critical technical leap for AI/HPC architectures. Higher density vertical interconnects facilitate the creation of more sophisticated Systems-on-Chips (SoCs) that integrate various logic chiplets or logic with memory in a tightly coupled manner. This enables improvements in computational power, reductions in power consumption, and smaller form factors, driving innovation across data centers, edge AI, and supercomputing applications. TSMC's SoIC technology is already implemented in products like AMD's Instinct MI300 series, indicating its proven viability for high-end applications. This roadmap reinforces the trend towards heterogeneous integration and the chiplet ecosystem, allowing designers to fabricate specialized functional blocks on optimal process nodes and integrate them seamlessly through advanced packaging. The success of SoIC will be a key enabler for the next generation of AI hardware, pushing the boundaries of what is possible in computing.

Source: https://www.tomshardware.com/tech-industry/semiconductors/tsmc-soic-3d-stacking-roadmap-outlines-path-from-6-micron-pitches-today-to-4-5-micron-in-2029-fujitsus-monaka-cpu-to-benefit-from-face-to-face-chiplet-stacking

Collected: May 15, 2026 | Automated Research System (Gemini API)

ABF Substrate Becomes Critical Bottleneck in AI Hardware Supply Chain, Driven by Ajinomoto's Dominance

Published April 07, 2026　専門メディア (分析)　Taiwan



OVERVIEW

Ajinomoto Build-up Film (ABF), an essential insulating dielectric for high-performance substrates, has emerged as an unexpected bottleneck in the AI hardware ecosystem due to Ajinomoto Fine-Techno's near-monopoly. Leading substrate manufacturers like Ibiden are making massive capital investments, with AI chip giants such as Nvidia and Intel directly pre-funding approximately 50% of the top four suppliers' capacity expansions to secure supply.

IN DEPTH

Background

The explosive growth of artificial intelligence (AI) across all sectors, from data centers to edge devices, mandates increasingly powerful and complex semiconductor chips. AI accelerators and High-Performance Computing (HPC) processors, with their intricate architectures and high power densities, require advanced packaging substrates that can facilitate high-speed, high-density signal transmission beyond the capabilities of traditional materials. Ajinomoto Build-up Film (ABF) has become the material of choice for the most advanced Flip-Chip Ball Grid Array (FC-BGA) substrates due to its superior dielectric properties and processing compatibility.

Key Findings / Results

ABF substrates have unexpectedly become a critical bottleneck in the AI hardware supply chain. Ajinomoto Fine-Techno, a Japanese company, holds a near-monopoly on ABF film production, and its capacity has struggled to keep pace with the exponential surge in AI demand. Reports indicate that substrates for AI server chips consume over ten times more ABF film than those for PC chips, creating a structural demand imbalance. To address this, major ABF substrate manufacturers, including Ibiden, have announced massive capital expenditure plans. Ibiden, for instance, is investing ¥500 billion ($3.2 billion) to expand its AI substrate capacity. Notably, a significant portion of these investments, approximately 50% of the top four substrate suppliers' capital expenditure, is being pre-funded by leading AI chip customers like Nvidia, Intel, and hyperscalers developing custom AI chips. This direct financial involvement underscores the urgency and strategic importance of securing ABF supply.

Technical Significance & Outlook

The ABF shortage has direct implications for the production and market availability of AI semiconductors. Ajinomoto Fine-Techno's dominant position and the inherent limitations in its production capacity are constraining the growth of the entire AI industry. However, the collaborative funding model, where major customers pre-invest in supplier capacity, represents an evolving dynamic in the semiconductor supply chain. This approach provides strong incentives for suppliers to expand and helps to mitigate long-term supply risks. It suggests a shift towards deeper, shared-risk partnerships between chip designers and material/substrate manufacturers. Future efforts will likely focus on developing alternative ABF suppliers, diversifying material science innovations for advanced packaging, and exploring new entrants to stabilize supply. Ensuring a stable and sufficient supply of ABF substrates is paramount for the continued proliferation and advancement of AI technologies.

Source: #

Collected: May 15, 2026 | Automated Research System (Gemini API)

Hanmi Semiconductor Unveils Second-Gen Hybrid Bonder for Advanced HBM Stacking, Investing $67M in New Factory

Published April 10, 2026   専門メディア   South Korea

OVERVIEW

Hanmi Semiconductor is set to introduce its second-generation hybrid bonder prototype this year, crucial for next-generation HBM mass production with over 20 stacked layers. Concurrently, the company is investing approximately ₩100 billion ($67.6 million) to build a dedicated hybrid bonder factory in Incheon, slated for completion by H1 2025, aiming to lead the market with bump-less copper-to-copper bonding technology.

IN DEPTH

Background

The proliferation of artificial intelligence (AI) necessitates High-Bandwidth Memory (HBM) that can process vast amounts of data at unprecedented speeds. HBM achieves this by vertically stacking multiple DRAM dies, but further increasing stack height and performance demands more advanced, higher-density, and more reliable inter-die bonding technologies than traditional microbump approaches. Hybrid bonding, which directly connects copper lines without bumps, has emerged as a promising solution to meet these stringent requirements.

Key Findings / Results

Hanmi Semiconductor, a leading South Korean semiconductor equipment manufacturer, announced the development of its second-generation hybrid bonder, designed to support multi-layer stacking for next-generation HBM. The company plans to unveil a prototype later this year and initiate collaborations with key customers. To support mass production, Hanmi is investing approximately ₩100 billion (around $67.6 million USD) in a new hybrid bonder factory within the Juan National Industrial Complex in Incheon. This 14,570 square meter facility is expected to be completed by the first half of 2025, dedicated to manufacturing HBM hybrid bonders. The core technological innovation of this second-generation system is its ability to perform bump-less, direct copper-to-copper (Cu-to-Cu) bonding between chips and wafers. This significantly reduces connection pitch, enabling HBM stacks with over 20 DRAM layers, which is crucial for HBM3E and future HBM4/HBM5 generations.

Technical Significance & Outlook

Hanmi Semiconductor's investment in its second-generation hybrid bonder marks a significant advancement for the HBM market. As a dominant player with approximately 70% global market share in HBM-specific TC bonders, Hanmi aims to replicate this leadership in the nascent hybrid bonding segment. This technology is vital for pushing the boundaries of HBM performance, particularly in data transfer rates and power efficiency, which directly translates to more powerful AI accelerators. Amidst ongoing HBM supply shortages, securing advanced bonding equipment capacity is paramount for HBM manufacturers' competitiveness and time-to-market. Hanmi's strategic move underscores the expanding role of back-end equipment suppliers in the AI era and reinforces South Korea's position as a critical innovation hub within the HBM ecosystem.

Source: https://www.chosun.com/english/industry-en/2026/04/10/2EZEOAMZUVAFPGWWTMCDZIZBZU/

Collected: May 15, 2026 | Automated Research System (Gemini API)

SK Hynix Initiates HBM Packaging Hub Construction in Cheongju to Bolster AI Memory Capacity

Published April 23, 2026　専門メディア　South Korea

OVERVIEW

SK Hynix has broken ground on a substantial advanced packaging facility in Cheongju Technopolis, signaling a strategic shift in AI semiconductor competition from wafer fabrication to performance-critical back-end processes. This new hub aims to significantly augment HBM production and advanced packaging capabilities, directly addressing the burgeoning demand for AI memory.

IN DEPTH

Background

The relentless expansion of artificial intelligence (AI) applications has profoundly transformed the semiconductor landscape. For demanding AI workloads requiring immense data processing and high-speed computation, the bandwidth of memory supporting CPUs and GPUs has become as crucial as the processors themselves. High-Bandwidth Memory (HBM) achieves superior data transfer rates by vertically stacking multiple DRAM dies and connecting them through a wide interface to logic chips like GPUs. In the production of HBM, the post-wafer fabrication packaging process is a critical stage that dictates final product performance and yield.

Key Findings / Results

SK Hynix has commenced construction of a new, large-scale advanced packaging facility in Cheongju Technopolis, South Korea, to substantially expand its production capacity for HBM and other AI-centric memory. This investment epitomizes an industry-wide trend where the competitive battleground in AI semiconductors is shifting from leading-edge frontend wafer fabrication to the complexities and performance-determining aspects of back-end advanced packaging technologies. Through this new packaging hub, SK Hynix aims to fortify its HBM stacking, thermal management, and testing capabilities, thereby reinforcing its leadership in the AI memory market. Cheongju is a key manufacturing base for SK Hynix, and the new facility is expected to leverage synergies with existing infrastructure.

Technical Significance & Outlook

The establishment of SK Hynix's HBM packaging hub in Cheongju holds significant implications for the global AI memory market. In an environment of persistent HBM supply shortages driven by escalating AI demand, this facility will be instrumental in ensuring stable HBM supply and alleviating bottlenecks in AI accelerator production. This enhanced supply could bolster deliveries to major AI chip manufacturers such as Nvidia and AMD, potentially accelerating the growth of the broader AI ecosystem. Furthermore, this investment can be seen as part of a broader "IDM 2.0" strategy, where integrated device manufacturers strengthen their in-house back-end technologies and capacities. Strategic investments in advanced packaging are increasingly becoming a pivotal factor in determining the performance, cost, and time-to-market of future AI semiconductors.

Source: https://www.digitimes.com/news/a20260422VL212/sk-hynix-packaging-hbm-capacity-production.html

Samsung Electronics Pioneers HBM4 Mass Production with Hybrid Bonding, Solidifying Market Lead

Published Date unknown　専門メディア　South Korea

OVERVIEW

Samsung Electronics is strategically deploying dedicated hybrid bonding lines in its domestic facilities for HBM4, aiming to secure market leadership. The company has successfully commenced mass production of HBM4 using this advanced technique, which significantly reduces inter-chip spacing, mitigates heat generation, and boosts data transfer speeds, achieving 11.7Gbps—46% above JEDEC standards for HBM4.

IN DEPTH

Background

The escalating demands of AI and High-Performance Computing (HPC) are driving rapid advancements in High-Bandwidth Memory (HBM). HBM dramatically increases data transfer speeds by vertically stacking multiple DRAM chips. However, for next-generation HBM4, achieving further performance gains while addressing critical physical challenges like heat dissipation necessitates an evolution beyond traditional microbump bonding. Hybrid bonding, with its finer pitch and superior electrical characteristics, is emerging as the essential technology to meet these stringent requirements.

Key Findings / Results

Samsung Electronics has announced the progressive installation of dedicated hybrid bonding lines for HBM4 in its South Korean manufacturing facilities, a strategic move to cement its leadership in the HBM4 market. This technology involves directly bonding DRAM dies and logic dies using copper-to-copper connections, eliminating the need for traditional bumps and significantly reducing the distance between chips. This shortens signal paths, leading to higher data transfer speeds and more effective heat dissipation. Samsung claims to be the first in the world to successfully commence mass production of HBM4 using this hybrid bonding technique, with shipments reportedly already underway to key customers including NVIDIA. Samsung's HBM4 achieves an operating speed of 11.7Gbps, approximately 46% higher than the JEDEC standard of 8Gbps, with HBM4E potentially reaching data processing speeds from 3.3 TB/s to 4.0 TB/s.

Technical Significance & Outlook

Samsung Electronics' early adoption of hybrid bonding for HBM4 significantly enhances its competitiveness and technological advantage in the HBM market. This enables Samsung to offer higher-performance and more reliable HBM solutions to AI chip manufacturers like NVIDIA. Competitors such as SK Hynix and Micron are also accelerating their development and deployment of hybrid bonding, intensifying the market share battle for HBM4 and future generations. Hybrid bonding is a pivotal technology for solving the core challenges of the AI semiconductor era—multi-layer HBM stacking, performance enhancement, and thermal management. The progress in its mass production will dictate the pace of evolution for the entire AI ecosystem. This technology's widespread adoption could ultimately lead to denser 3D integration and establish new standards for semiconductor packaging.

Source: https://economy.ac/news/2026/02/202602288324

SK Hynix Validates 12-Die Hybrid Bonded HBM Stack Amidst Heated AI Memory Race

Published April 28, 2026 専門メディア South Korea

OVERVIEW

SK Hynix has successfully verified a 12-die HBM stack using hybrid bonding, demonstrating significant progress in its next-generation packaging technology for HBM4 and HBM5. While actively improving yield for mass production, the company is withholding specific figures, highlighting the technical challenges and competitive intensity as hybrid bonding becomes crucial for achieving higher-speed, more efficient, and denser HBM stacks without traditional bumps.

IN DEPTH

Background

The continuous advancement of artificial intelligence (AI) has positioned High-Bandwidth Memory (HBM) as a critical enabler for high-performance AI accelerators. HBM achieves dramatic improvements in data transfer speeds by vertically stacking multiple DRAM dies. However, next-generation HBM demands even higher layer counts and greater bandwidth, pushing the limits of traditional microbump bonding technologies. Hybrid bonding, with its finer pitch and superior electrical properties, is therefore indispensable. This technology directly connects copper lines between chips, increasing connection density and enhancing signal integrity.

Key Findings / Results

SK Hynix announced significant progress in its hybrid bonding packaging technology for HBM modules. The company has successfully verified a 12-die HBM stack using hybrid bonding, marking a substantial step towards achieving the multi-layer goals for next-generation HBM (HBM4 and HBM5). SK Hynix is currently dedicating efforts to improve the yield of this technology to levels suitable for mass production, although specific yield figures have not been disclosed. Hybrid bonding eliminates the need for traditional bumps by directly joining memory layers, thereby minimizing the distance between chips and contributing to higher data transfer speeds and reduced power consumption. This capability is crucial for accommodating the increasingly fast and complex AI workloads.

Technical Significance & Outlook

SK Hynix's successful verification of a 12-die HBM stack via hybrid bonding underscores the escalating technological competition in the HBM market. If SK Hynix, a leading HBM supplier, can establish this technology and improve its mass production yield, it will accelerate the market introduction of next-generation AI memory like HBM4 and HBM5, bolstering its market leadership. However, the non-disclosure of specific yield figures suggests that technical challenges persist, particularly concerning cleanliness and thermal management in multi-layer stacks. The commercialization of hybrid bonding will not only impact AI chip performance but also cost efficiency and product reliability. The maturity of this technology is vital for the development of the entire AI hardware ecosystem, and continuous monitoring of HBM market trends remains essential.

Source: https://wccftech.com/sk-hynix-verifies-12-die-hybrid-bonded-hbm-stack-but-wont-disclose-yield-figures-as-next-gen-hbm4-ai-memory-race-heats-up/

Samsung Electro-Mechanics and Sumitomo Chemical Group Partner to Establish Glass Core Substrate Joint Venture

Published November 05, 2025　企業発表　South Korea

OVERVIEW

Samsung Electro-Mechanics and Sumitomo Chemical Group have signed an MOU to establish a joint venture for manufacturing "glass core" substrates, a critical material for next-generation advanced packaging. Aiming to mass-produce these substrates from Dongwoo Fine-Chem's Pyeongtaek facility, this collaboration addresses the need for superior flatness and lower thermal expansion, essential for high-density, large-area AI and HPC packages.

IN DEPTH

Background

The evolution of AI and High-Performance Computing (HPC) chips presents new challenges for semiconductor packaging technology. As chips become larger, more integrated, and consume more power, conventional organic-based package substrates are encountering limitations in terms of warpage, signal integrity degradation, and thermal management. To overcome these hurdles and support next-generation high-performance semiconductors, the development of glass core substrates, boasting superior material properties, has become an urgent priority. Glass core substrates are garnering attention as a promising solution for advanced packaging due to their low coefficient of thermal expansion (CTE), excellent flatness, and electrical stability.

Key Findings / Results

Samsung Electro-Mechanics has entered into a strategic partnership with Sumitomo Chemical Group, a Japanese chemical giant, for the mass production of "glass core" — a core material for next-generation semiconductor package substrates. The two companies have signed a non-binding Memorandum of Understanding (MOU) to establish a joint venture (JV) aimed at building a supply chain and bringing glass core substrates to market. The JV's headquarters and initial production site for glass core are planned to be at Dongwoo Fine-Chem's Pyeongtaek facility, a subsidiary of Sumitomo Chemical Group. Glass core substrates are considered a crucial technology that overcomes the limitations of conventional organic substrates, particularly for high-density, large-area advanced semiconductor packages for AI and HPC. They enable the reduction of warpage-induced defects and the formation of finer circuit patterns.

Technical Significance & Outlook

The collaboration between Samsung Electro-Mechanics and Sumitomo Chemical Group represents a significant move in the advanced packaging materials market and is expected to greatly accelerate the commercialization of glass core substrates. Through this JV, Samsung is anticipated to secure a stable supply of glass core substrates and enhance its competitiveness in advanced semiconductor packaging technology. Sumitomo Chemical Group will leverage its extensive expertise in material science to explore new growth areas within the semiconductor industry. The widespread adoption of glass core substrates will contribute to further performance enhancements and reliability for AI chips, ultimately enabling more sophisticated electronic devices. In the future, glass core substrates hold the potential to become the standard material for HBM stacking, chiplet integration, and other applications requiring advanced high-density interconnections, thus forming a new paradigm in semiconductor packaging technology.

Source: https://www.samsungsem.com/global/newsroom/news/view.do?id=9850

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