Semiconductor packaging

Weekly Intelligence Report

2026-05-31 | 15 articles | 8 countries

troy-technical.jp

This Week's Keyword

AI Advanced Packaging

HBM, Hybrid Bonding, Regionalization

15	8	$150B	200nm
articles	countries	USD	pitch
Total Articles Analyzed	Source Countries	NVIDIA Taiwan Invest.	Hybrid Bonding Record

All 15 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	Amkor's $7B Arizona Pkg	Corporate Strategy	●●○○○	●●●○○	●●●●○	●●●●○	●●●●●	Amkor invests $7B in Arizona for advanced packaging, aiming for $11B revenue by 2030, supported by CHIPS Act.
#02	TSMC CoWoS Capacity Shift	Corporate Strategy	●●●○○	●●●●○	●●●●●	●●●○○	●●●●○	TSMC shifts mature node capacity to CoWoS for AI accelerators, easing packaging bottleneck but impacting automotive/PMIC supply.
#03	AMD's $10B Taiwan Pkg	Corporate Strategy	●●●○○	●●●○○	●●●●○	●●●●○	●●●●●	AMD invests over $10B in Taiwan's AI ecosystem, focusing on EFB 2.5D packaging with local partners for next-gen AI chips.
#04	HBM4 with Hybrid Bonding	New Product	●●●●○	●●●●○	●●●●●	●●●●○	●●●●○	SK Hynix and Samsung unveil HBM4 with hybrid bonding, targeting H2 2026 mass production for AI/HPC applications.
#05	Malaysia Adv. Pkg Consort.	Corporate Strategy	●●○○○	●●●○○	●●●○○	●●●○○	●●●○○	Malaysia launches a $39M consortium to develop advanced semiconductor packaging capabilities within two years, boosting domestic IP.
#06	ASE Panel-Level Packaging	New Product	●●●●○	●●●○○	●●●●○	●●●●○	●●●●○	ASE unveils industry-first automated 310mm panel-level packaging line for AI and chiplet integration, targeting H1 2027 production.
#07	Imec/EVG 200nm Hybrid B.	Research	●●●●●	●○○○○	●●●●●	●●●●●	●●●●●	Imec and EVG achieve record 200nm interconnect pitch in wafer-to-wafer hybrid bonding, advancing 3D-IC for future AI/HPC.
#08	Hanmi HBM4 Bonder Rebound	Corporate Strategy	●●○○○	●●●●○	●●●●○	●●●●○	●●●●●	Hanmi Semiconductor forecasts HBM4 TC bonder rebound in Q2 2026, plans US expansion to support Micron, SK Hynix, and Tesla.
#09	NVIDIA HBM Bottleneck	Market Analysis	●○○○○	●●●●○	●●●●●	●●●○○	●●●●●	CoWoS bottleneck for AI accelerators eases with TSMC expansion, but HBM supply from limited vendors becomes the new critical constraint.
#10	NVIDIA $150B Taiwan Invest	Corporate Strategy	●○○○○	●●●●○	●●●●●	●●●●○	●●●●●	NVIDIA CEO projects $150B annual investment in Taiwan's AI supply chain, benefiting TSMC's 3nm and CoWoS, with demand still exceeding supply.
#11	TEL/Samsung Hybrid Bond	Corporate Strategy	●●●○○	●●●○○	●●●●○	●●●○○	●●●●○	Tokyo Electron and Samsung boost capex for hybrid bonding equipment, crucial for HBM4 and advanced packaging for AI/GPU.
#12	Hetero. Integration Adv.	Research	●●●○○	●●○○○	●●●○○	●●○○○	●●●○○	Heterogeneous integration with hybrid bonding advances AI/5G/6G, but faces critical power, thermal, and reliability challenges.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#13	Huawei's "Tao Law" 1.4nm	Research	●●●●●	●●○○○	●●●●●	●●○○○	●●●●○	Huawei's "Tao Law" aims for 1.4nm-equivalent chip density via "Logic Folding" and ultra-fine hybrid bonding, targeting mobile SoC by late 2026.
#14	Korea HBM Test Equip.	Corporate Strategy	●●○○○	●●●●○	●●●○○	●●●○○	●●●●○	South Korea addresses HBM test equipment bottleneck by fostering domestic suppliers, with Digital Frontier mass-producing HBM4 wafer testers.
#15	AMD FOPLP for Zen 7	Corporate Strategy	●●●○○	●●○○○	●●●●○	●●○○○	●●●●●	AMD explores Powertech's FOPLP for next-gen Zen 7 CPUs to diversify packaging, build complex chiplets, and reduce TSMC reliance.

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your HBM supply chain resilient enough for AI?

With TSMC's CoWoS bottleneck easing, HBM supply is now the primary constraint for AI accelerators (#09). SK Hynix and Samsung are targeting HBM4 mass production by H2 2026 (#04), but only three major vendors exist. Does your procurement strategy account for this critical dependency?

❷ How will advanced hybrid bonding redefine your product roadmap?

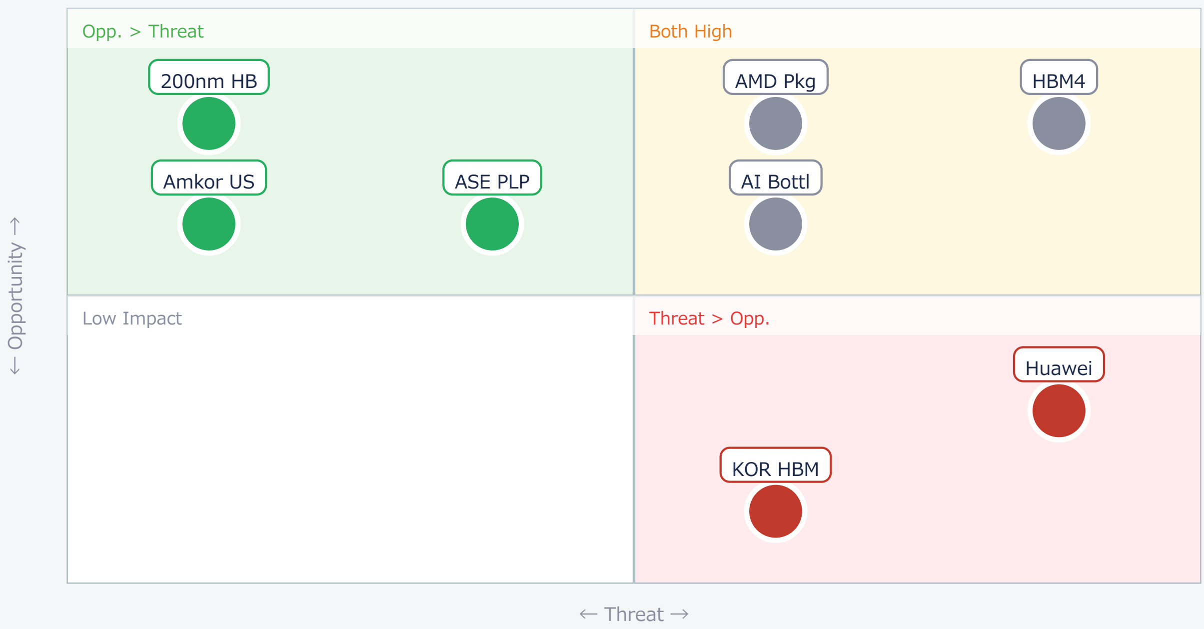
Imec and EV Group achieved a record 200nm interconnect pitch in hybrid bonding (#07), while Huawei's 'Tao Law' proposes 1.4nm-equivalent density via 'Logic Folding' (#13). Are your R&D; teams actively exploring these ultra-fine 3D integration techniques, or risk being left behind?

❸ Are you diversifying advanced packaging beyond Taiwan?

Amkor's $7B Arizona investment (#01) and AMD's exploration of FOPLP for Zen 7 (#15) signal a push for packaging diversification. Given geopolitical risks and concentration in Taiwan (#03, #10), are you strategically investing in or partnering with alternative advanced packaging ecosystems?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
● 200nm HB	Opp.	Future 3D-IC IP	Long-term tech gap
● Amkor US	Opp.	Resilient supply	Non-US OSATs
● ASE PLP	Opp.	Cost-eff. AI	WLP obsoles.
● HBM4	Critical	Next-gen AI/HPC	Lagging adoption
● AI Bottl	Critical	CoWoS access	HBM shortage
● AMD Pkg	Critical	Supply flex.	TSMC reliance
● Huawei	Threat	—	China tech leap

● KOR HBM	Threat	—	Market share loss

Deep Dive ① — HBM4 with Hybrid Bonding Nears Production

#04 | 2026/05/22 | Techfund | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●○

SK Hynix and Samsung unveiled production-ready HBM4 devices at CES 2026, targeting mass production in H2 2026. SK Hynix showcased a 16-layer, 48GB HBM4 using hybrid bonding, while Samsung presented a 12-layer, 36GB stack focusing on thermal management. This marks a critical industry shift towards hybrid bonding as HBM stacks exceed 16 layers, promising enhanced performance and reliability for next-generation AI and HPC applications.

Hybrid bonding offers significantly finer interconnect pitches and superior connection reliability compared to traditional micro-bump bonding, which is becoming challenging for higher HBM stacking densities. This technology is indispensable for meeting the data transfer speeds and efficiency required by intensive AI workloads, pushing the boundaries of future AI and HPC systems.

▶ Strategic Analyst's Perspective

> Strategic Analyst's Perspective: The HBM4 announcements are realistic given the rapid pace of AI development. The technical barrier lies in scaling hybrid bonding for high-volume manufacturing while ensuring yield and thermal performance. [Opportunity] for US/EU OEMs to integrate cutting-edge memory, enabling next-gen AI platforms. [Threat] for those reliant on older HBM generations or without robust HBM4 supply agreements. Next actions: [Procurement] Secure HBM4 supply agreements immediately. [R&D;] Begin HBM4 integration design and thermal management studies for future products by next quarter.

Deep Dive ② — Record 200nm Hybrid Bonding Achieved

#07 | 2026/05/28 | imec | Tech Novelty●●●●● Proximity●○○○○ Market Impact●●●●● Data Reliability●●●●● US/EU Relevance●●●●●

Imec and EV Group (EVG) demonstrated wafer-to-wafer hybrid bonding with an unprecedented 200nm copper interconnect pad pitch on a 300mm wafer, achieving a post-bond overlay vector below 40 nanometers. This breakthrough, presented at ECTC 2026, significantly advances the hybrid bonding roadmap for future logic-to-logic and memory-to-logic tier stacking.

The co-optimization of process flow, including SiCN as a dielectric and chemical mechanical polishing, was crucial. This achievement enables unprecedented high-density interconnects for 3D-ICs, addressing data transmission bottlenecks and dramatically enhancing AI and HPC performance, serving as a fundamental technology for more functional and lower-power devices.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The reported 200nm pitch is a genuine academic breakthrough, pushing the limits of hybrid bonding. However, commercialization is 5+ years away due to remaining technical barriers like yield at scale, thermal management, and integration into complex manufacturing flows. [Opportunity] for US/EU technology licensors and IP holders to invest in fundamental research and co-development with Imec/EVG to secure future 3D-IC intellectual property. [Threat] for companies not engaging in advanced research, risking a long-term technology gap. Next actions: [R&D;] Establish joint development programs with Imec/EVG by year-end. [Strategy] Evaluate long-term implications for chip design paradigms by next quarter.

Deep Dive ③ — TSMC Shifts Capacity to CoWoS for AI

#02 | 2026/05/28 | Tom's Hardware | Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●○

TSMC is reallocating 40-90nm mature node capacity to expand its CoWoS advanced packaging and silicon interposer fabrication, directly addressing a critical supply bottleneck for AI accelerators. This strategic shift prioritizes the escalating demand for high-performance AI chips, underscoring CoWoS's indispensable role in AI chip manufacturing.

This move impacts the availability of mature-node wafers for other industries, including automotive and power management ICs, which may face supply shortages and potential cost increases. It highlights a significant shift in priorities across the semiconductor industry, driven by the profound impact of AI technology.

> ▶ Strategic Analyst's Perspective
>
> Strategic Analyst's Perspective: TSMC's capacity reallocation is a realistic response to market demand, but the impact on mature node supply is a significant concern. The technical barrier is managing the transition and ensuring stable supply for affected industries. [Opportunity] for US/EU OEMs in AI/HPC to potentially access more CoWoS capacity. [Threat] for US/EU automotive and industrial companies reliant on mature nodes, facing potential shortages and price hikes. Next actions: [Procurement] Immediately assess exposure to mature node shortages and diversify suppliers. [Strategy] Re-evaluate long-term sourcing strategies for automotive and PMICs by next month.

Other Notable Articles

Amkor Technology Targets $11B Revenue by 2030, Anchored by $7 Billion Arizona Advanced Packaging Investment (MarketBeat)
Tech Novelty●●○○○ Proximity●●●○○ Market Impact●●●●○

Amkor's $7B Arizona investment, supported by CHIPS Act, boosts US advanced packaging capacity for AI/HPC, critical for supply chain resilience.

AMD Commits Over $10 Billion to Taiwan's AI Ecosystem for Advanced Packaging and EFB Technology Expansion (EE Times)
Tech Novelty●●●○○ Proximity●●●○○ Market Impact●●●●○

AMD's $10B+ investment in Taiwan's EFB 2.5D packaging with ASE/SPIL/PTI strengthens its chiplet strategy for next-gen AI.

ASE Unveils Industry-First Automated 310mm Panel-Level Packaging Line for AI and Chiplet Integration (AnySilicon)
Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○

ASE's new automated 310mm PLP line offers superior efficiency for AI/chiplets, targeting H1 2027 production, reducing packaging costs.

Hanmi Semiconductor Forecasts HBM4 TC Bonder Rebound in Q2, Announces US Expansion Plans (BigGo Finance)
Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●○

Hanmi expects HBM4 TC bonder rebound in Q2 2026 and plans US expansion to support key customers like Micron and Tesla.

Huawei's "Tao Law" Proposes 1.4nm-Equivalent Chip Density via Logic Folding and Ultra-Fine Hybrid Bonding (China as a System)
Tech Novelty●●●●● Proximity●●○○○ Market Impact●●●●●

Huawei's ambitious 'Tao Law' aims for 1.4nm-equivalent density via 'Logic Folding' and hybrid bonding, potentially reshaping chip design.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Review HBM supply contracts and forecasts, especially for HBM3E/HBM4, given the emerging bottleneck (#09).
- [Strategy] Assess impact of Amkor's Arizona investment on US advanced packaging supply chain and potential for domestic partnerships (#01).

Short-term (1 month)

- [R&D;] Investigate Huawei's "Tao Law" and Logic Folding claims; evaluate potential for similar 3D integration approaches outside China (#13).
- [Business Dev] Engage with Imec/EVG on 200nm hybrid bonding roadmap to understand future 3D-IC capabilities and potential licensing opportunities (#07).
- [Procurement] Evaluate alternative advanced packaging suppliers (e.g., ASE's PLP, Powertech's FOPLP) to diversify beyond TSMC's CoWoS for AI/HPC (#06, #15).

Medium-long term (quarter+)

- [Strategy] Develop a comprehensive HBM supply chain resilience plan, including investment in domestic HBM production or strategic partnerships (#04, #09).
- [R&D;] Increase internal R&D; on hybrid bonding and advanced thermal management solutions to address heterogeneous integration challenges for AI/5G/6G (#12, #07).
- [Legal/IP] Monitor IP developments around advanced packaging (e.g., EFB, FOPLP, hybrid bonding) in Asia to identify potential infringement risks or licensing opportunities (#03, #06, #15).
- [Executive] Re-evaluate global manufacturing footprint and OSAT strategy in light of regionalization efforts in the US (Amkor) and Southeast Asia (Malaysia) (#01, #05).

Semiconductor_BackEnd — Selected Articles

Date: 2026-05-31

Articles: 15

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Amkor Technology Targets $11B Revenue by 2030, Anchored by $7 Billion Arizona Advanced Packaging Investment

Published May 21, 2026 MarketBeat USA

OVERVIEW

Amkor Technology aims to exceed $11 billion in revenue by 2030, driven by a $7 billion, two-phase investment in its Arizona advanced packaging and test campus. High-volume manufacturing is slated to begin in 2028, establishing the first high-volume advanced packaging OSAT facility in the U.S. This strategic move, supported by approximately $400 million from the CHIPS Act, is critical for supporting the burgeoning AI, HPC, automotive, and communications sectors, with the Arizona plant projected to generate $1 billion in revenue at full scale.

IN DEPTH

Background and Strategic Imperatives

Amkor Technology is undertaking a significant strategic pivot towards advanced packaging, aiming to capture growth in critical sectors such as artificial intelligence (AI), high-performance computing (HPC), automotive, and next-generation communications. The company's vision, outlined at its 2026 Investor Day, emphasizes substantial reinforcement of its U.S. manufacturing capabilities, a move designed to bolster supply chain resilience amidst evolving geopolitical landscapes. Government support, particularly through the U.S. CHIPS Act, serves as a crucial accelerator for this ambitious endeavor.

Massive Investment in Arizona Facilities

Central to Amkor’s growth strategy is a colossal $7 billion investment dedicated to its advanced packaging and test campus in Arizona. This investment is planned in two distinct phases, with high-volume manufacturing from the initial phase projected to commence by 2028. The new facility is designed to feature 355,000 square feet of state-of-the-art clean room space. Additionally, Amkor has proactively secured an extra 67 acres of land, ensuring ample capacity for future expansion needs. This project benefits from significant governmental backing, including approximately $400 million in incentives facilitated by the CHIPS Act.

Market Impact and Future Outlook

Upon reaching full operational capacity, the Arizona facility is expected to contribute approximately $1 billion in annual revenue, establishing itself as the first high-volume advanced packaging Outsourced Semiconductor Assembly and Test (OSAT) operation within the United States. This development is pivotal for integrating advanced packaging capabilities into the domestic semiconductor ecosystem, serving as a vital component for AI chips and related high-demand technologies. The investment is a cornerstone of Amkor's broader objective to achieve over $11 billion in annual revenue by 2030. Furthermore, the establishment of advanced packaging capabilities within the U.S. is anticipated to contribute significantly to the diversification and security of the global semiconductor supply chain, addressing growing concerns about geographical concentration of critical manufacturing processes.

Source: https://www.marketbeat.com/instant-alerts/amkor-technology-targets-11b-revenue-by-2030-on-ai-packaging-arizona-ramp-2026-05-21/

TSMC Repurposes Mature Node Capacity to CoWoS for AI Accelerators Amid Critical Supply Shortage

Published May 28, 2026 Tom's Hardware Taiwan

OVERVIEW

TSMC is reallocating 40-90nm mature node capacity to expand its CoWoS advanced packaging and silicon interposer fabrication, directly addressing a critical supply bottleneck for AI accelerators. This strategic shift prioritizes the escalating demand for high-performance AI chips, impacting the availability of mature-node wafers for other industries, including automotive and power management ICs. The move underscores CoWoS's indispensable role in AI chip manufacturing and TSMC's commitment to alleviating production constraints in this high-growth sector.

IN DEPTH

Background and CoWoS Significance

The burgeoning demand for AI accelerators has elevated TSMC's CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging technology to a pivotal role in the fabrication of high-performance AI chips. CoWoS facilitates the integration of multiple dies, including high-bandwidth memory (HBM), onto a silicon interposer, enabling superior interconnect density and shorter signal paths. This architecture is crucial for delivering the data transfer speeds and efficiency required by intensive AI workloads. However, the inherent complexity of CoWoS manufacturing and its reliance on specialized equipment have rendered its supply capacity a primary bottleneck in AI chip production.

Strategic Reallocation of Mature Node Capacity

To mitigate these supply constraints, TSMC has made a strategic decision to repurpose production capacity from its 40nm to 90nm mature manufacturing nodes towards CoWoS packaging and silicon interposer fabrication. Historically, these mature nodes have been extensively utilized for a broad spectrum of general-purpose chips, encompassing automotive electronics, power management ICs, and IoT devices. This reallocation clearly signals TSMC's prioritization of meeting the insatiable demand for AI accelerators, thereby solidifying its leadership in the rapidly expanding AI market.

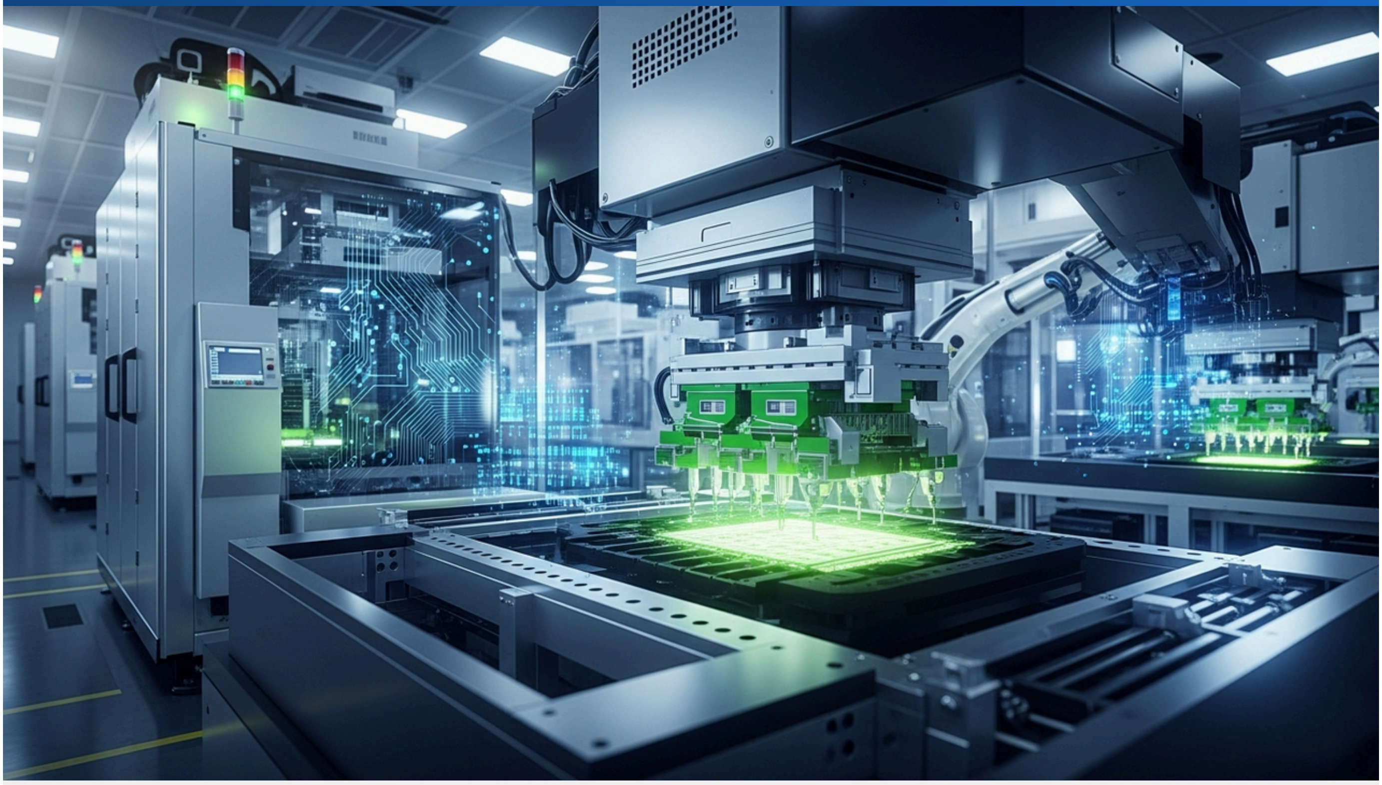
Broader Industry Implications and Outlook

The diversion of mature node capacity to CoWoS production is expected to directly influence wafer supply for other industries, particularly the automotive sector and the growing segment of power management ICs for AI servers. These industries, heavily reliant on mature nodes, may face supply shortages and potential cost increases. In the long term, TSMC's action highlights a significant shift in priorities across the entire semiconductor manufacturing industry, underscoring the profound impact of AI technology at every stage of the value chain. It is anticipated that other foundries may consider similar strategies, prompting customers requiring mature node products to intensify their efforts in diversifying suppliers and securing long-term supply agreements to ensure continuity.

Source: https://www.tomshardware.com/tech-industry/semiconductors/the-trailing-edge-foundry-roadmap-examined

AMD Commits Over $10 Billion to Taiwan's AI Ecosystem for Advanced Packaging and EFB Technology Expansion

Published May 21, 2026   EE Times   Taiwan



OVERVIEW

AMD announced an investment exceeding $10 billion into Taiwan's AI ecosystem, bolstering advanced packaging capabilities and R&D. This initiative specifically targets Elevated Fanout Bridge (EFB) based 2.5D packaging technology, in collaboration with Taiwanese partners like ASE, SPIL, and Powertech Technology. The investment aims to enhance chiplet architectures, high-bandwidth memory integration, and 3D hybrid bonding for next-generation AI systems, with Powertech already qualifying a cost-efficient 2.5D panel-based EFB interconnect technology.

IN DEPTH

Strategic Investment Rationale and Objectives

In response to the rapid advancements in artificial intelligence (AI) and the consequent surge in demand for high-performance computing (HPC), AMD has committed a significant strategic investment of over $10 billion to Taiwan, a pivotal hub in the global semiconductor supply chain. The primary objective of this extensive investment is to fortify Taiwan's entire AI ecosystem and, more specifically, to drastically enhance advanced packaging capabilities, which are indispensable for AMD's forthcoming generation of AI processors. AMD is a leading proponent of chiplet-based designs, an approach that critically relies on high-density, efficient packaging technologies to achieve performance and power targets.

Key Technologies and Collaboration with Taiwanese Partners

AMD's investment primarily focuses on advancing Elevated Fanout Bridge (EFB) based 2.5D packaging technology. This cutting-edge technology serves as a foundational element for the seamless integration of high-bandwidth memory (HBM) and the future realization of advanced 3D hybrid bonding techniques. AMD is actively collaborating with leading Taiwanese Outsourced Semiconductor Assembly and Test (OSAT) providers, including Advanced Semiconductor Engineering (ASE), Siliconware Precision Industries Co., Ltd. (SPIL), and Powertech Technology (PTI). Notably, Powertech Technology has already achieved qualification for the industry's first 2.5D panel-based EFB interconnect technology in partnership with AMD, facilitating cost-effective, high-volume production on large, square panels—a significant manufacturing advantage over traditional wafer-based methods.

Impact on Next-Generation AI Systems and Future Outlook

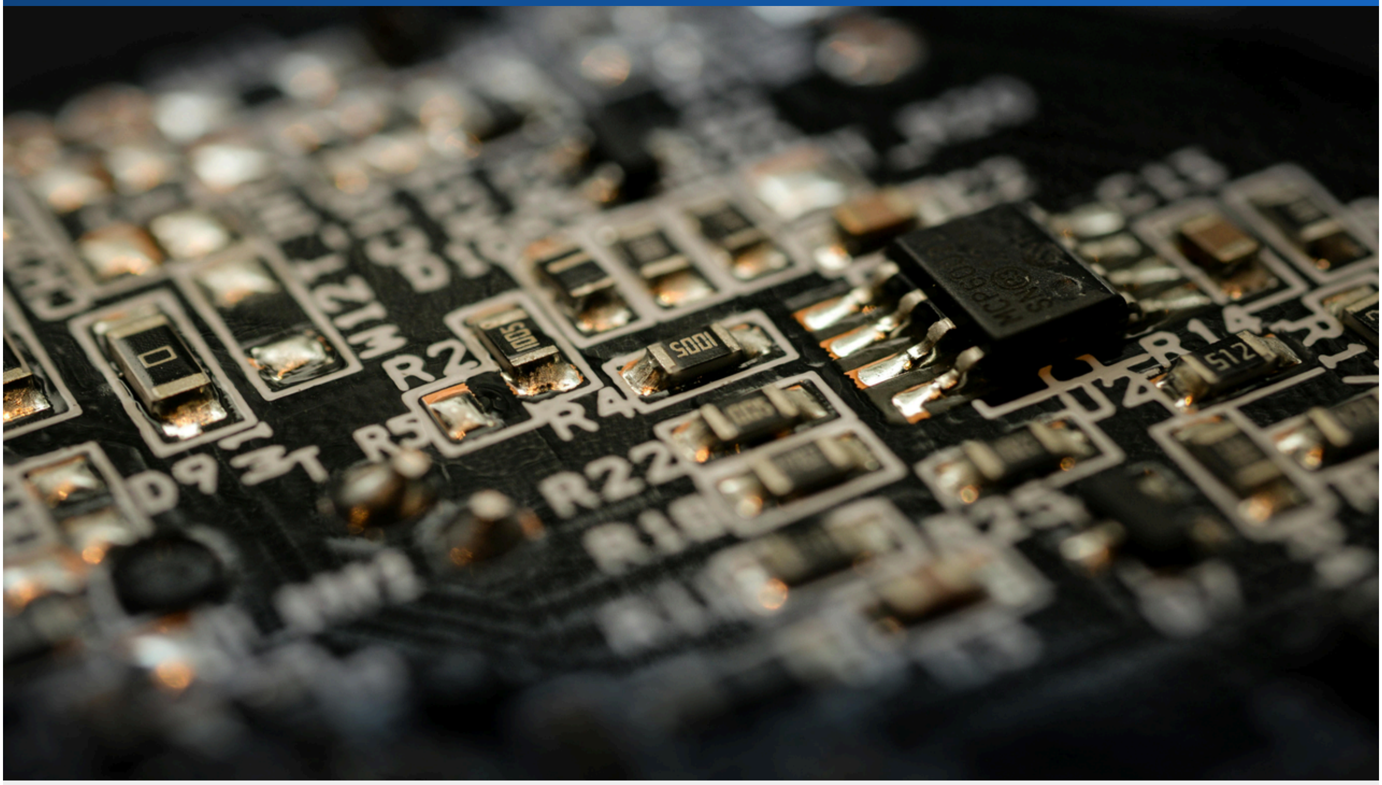
This substantial investment and technological collaboration are poised to directly contribute to the development of AMD's next-generation AI systems, exemplified by products such as the 6th Gen AMD EPYC CPUs, codenamed "Venice." The evolution of EFB and other advanced packaging technologies is critical for strengthening inter-chiplet connectivity and optimizing HBM integration, thereby enabling a significant leap in AI processing capabilities. By leveraging Taiwan's robust semiconductor manufacturing ecosystem, AMD aims to efficiently deliver state-of-the-art AI chips to market at competitive costs, solidifying its leadership in the AI era. In the long term, this investment is expected to further accelerate innovation and growth in advanced packaging technologies within Taiwan's semiconductor industry, fostering a more resilient and advanced global supply chain for AI hardware.

Source: https://www.eetimes.com/amd-plans-10b-investment-in-taiwan-to-boost-ai-infrastructure/

Collected: May 29, 2026 | Automated Research System (Gemini API)

SK Hynix and Samsung Unveil Production-Ready HBM4 with Hybrid Bonding, Targeting H2 2026 Mass Production

Published May 22, 2026 Techfund South Korea



OVERVIEW

At CES 2026, SK Hynix showcased a 16-layer, 48GB HBM4 device leveraging advanced Through-Silicon Via (TSV) and hybrid bonding for high density, while Samsung presented a 12-layer, 36GB HBM4 stack focused on thermal management. Both memory giants are targeting mass production in the second half of 2026. This signals a pivotal industry shift towards hybrid bonding, especially as HBM stacks exceed 16 layers, promising enhanced performance and reliability for next-generation AI and HPC applications.

IN DEPTH

Current State of HBM4 Development and Hybrid Bonding Integration

High Bandwidth Memory (HBM) is an indispensable technology for maximizing chip performance in artificial intelligence (AI) and high-performance computing (HPC) applications. At CES 2026, leading memory manufacturers SK Hynix and Samsung unveiled near-production prototypes of their next-generation HBM4 devices, with a stated goal of commencing mass production in the second half of 2026. This announcement underscores the industry's accelerated transition to HBM4, a generation that necessitates the integration of novel bonding technologies to achieve higher stacking densities and data transfer rates compared to preceding HBM versions.

Technical Demonstrations by SK Hynix and Samsung

- **SK Hynix:** The company exhibited a 16-layer HBM4 device boasting a 48 GB capacity, achieved through the sophisticated application of Through-Silicon Via (TSV) technology and hybrid bonding. This demonstration highlighted significant advancements in stacking density and performance characteristics, crucial for addressing the demands of complex AI workloads.
- **Samsung:** Samsung presented a 12-layer HBM4 stack with a 36 GB capacity, emphasizing enhancements in thermal management and manufacturing yield. As HBM stacking increases, heat dissipation becomes a critical challenge, making Samsung's approach focused on practicality and reliability. The company aims to balance high performance with stability through proprietary thermal dissipation technologies and optimized manufacturing processes.

Industry Trends and Future Outlook

The evolution of HBM technology is precipitating a significant paradigm shift in bonding techniques across the industry. Particularly as HBM stacks push beyond 16 layers, conventional micro-bump bonding methods face increasing difficulties in achieving finer interconnect pitches while maintaining reliability. Consequently, memory manufacturers are actively exploring the phased introduction of hybrid bonding technology for HBM4 and subsequent generations. Hybrid bonding offers the promise of significantly finer pitches and superior connection reliability, expected to contribute to enhanced performance and manufacturing efficiency for next-generation HBM. This technological innovation is poised to be a key enabler for pushing the performance boundaries of future AI and HPC systems.

Source: https://techfund.site/the-state-of-hbm4-chronicled-at-ces-2026/

Collected: May 29, 2026 | Automated Research System (Gemini API)

Malaysia Launches National Consortium to Accelerate Advanced Semiconductor Packaging Development Within Two Years

Published May 25, 2026 SME.asia Malaysia

OVERVIEW

Malaysia has established the Malaysia Advanced Packaging Consortium (MAPC) with a total funding of RM185 million ($39 million USD) to develop domestic advanced semiconductor packaging capabilities within two years. This initiative, a collaboration between government (RM92M R&D grant) and industry (RM93M), involves five local companies. The primary goal is to elevate Malaysia's semiconductor industry from traditional OSAT services to higher-value advanced packaging, thereby strengthening its ecosystem and national intellectual property.

IN DEPTH

National Strategy for Advanced Packaging Advancement

Malaysia has long played a significant role in the semiconductor industry's back-end processes, particularly in Outsourced Semiconductor Assembly and Test (OSAT). However, as global semiconductor demand shifts towards high-value sectors such as AI, 5G/6G, and high-performance computing, there is an urgent need to adapt to more sophisticated packaging technologies. To address this challenge and enhance national competitiveness, the Malaysian government has announced the establishment of the Malaysia Advanced Packaging Consortium (MAPC). This initiative is part of a national strategy aimed at rapidly developing domestic advanced packaging capabilities within a short two-year timeframe and transforming the industrial structure.

Public-Private Partnership and Funding

The MAPC adopts a model of close collaboration between the government and industry. The government has committed an R&D grant of RM92 million (approximately $19.5 million USD), which is augmented by an industry contribution of RM93 million (approximately $19.7 million USD), securing a total fund of RM185 million (approximately $39 million USD). This funding will be allocated to advanced packaging research and development, talent cultivation, and capital expenditure for equipment. The consortium includes five local companies: SkyeChip Bhd, Inari Technology Sdn Bhd, FusionAP Sdn Bhd, Pentamaster Instrumentation Sdn Bhd, and NSW Automation Sdn Bhd, each expected to contribute through their specialized expertise, thereby elevating Malaysia's overall technological capabilities.

Expected Outcomes and Future Outlook

The establishment and activities of MAPC are designed to transform Malaysia's semiconductor industry from a provider of conventional OSAT services into a developer and provider of more complex and high-value advanced packaging solutions. This transition is expected to increase added value within the domestic value chain and foster the creation of new technological intellectual property (IP). In the long term, this initiative represents a crucial step for Malaysia to solidify its position as a more strategic and indispensable player in the global semiconductor supply chain. Furthermore, it is anticipated to contribute to job creation in advanced technology sectors and upskill the domestic workforce, supporting sustainable economic growth.

Source: https://sme.asia/malaysia-to-build-advanced-semiconductor-packaging-in-2-years/

Collected: May 29, 2026 | Automated Research System (Gemini API)

ASE Unveils Industry-First Automated 310mm Panel-Level Packaging Line for AI and Chiplet Integration

Published May 26, 2026   AnySilicon   Taiwan

OVERVIEW

Advanced Semiconductor Engineering (ASE) has developed an automated 310mm x 310mm panel-level packaging (PLP) production line, a significant advancement for AI processors and chiplet architectures. This industry-first platform offers up to 96,100 mm^2 of usable area, vastly improving manufacturing scalability and efficiency compared to traditional wafer-level packaging. Compatible with ASE's FOCoS and FOCoS-Bridge platforms, supporting 2/2μm and 8/8μm line/space capabilities, the line is slated for production in the first half of 2027.

IN DEPTH

Panel-Level Superiority in Advanced Packaging

With the ongoing evolution of AI and high-performance computing (HPC), the integration density and performance of semiconductor chips are rapidly advancing, increasing the significance of advanced packaging technologies. The proliferation of chiplet architectures, in particular, demands packaging solutions that can efficiently and densely integrate multiple smaller chips. ASE's newly developed 310mm x 310mm Panel-Level Packaging (PLP) offers distinct advantages over conventional wafer-level packaging (WLP), which uses circular wafers. By utilizing larger, rectangular substrates, PLP enhances material utilization efficiency and dramatically increases the number of chips that can be processed simultaneously. This approach is expected to lead to significant reductions in manufacturing costs and improvements in throughput.

Technical Specifications and Production Capabilities

This innovative automated PLP production line provides an expansive usable packaging area of up to 96,100 mm^2. This represents a substantial improvement in area efficiency compared to WLP, offering particular benefits for large AI processors and complex chiplet integrations. The new line ensures compatibility with ASE's existing advanced packaging platforms, FOCoS (Fan-Out Chip-on-Substrate) and FOCoS-Bridge (Fan-Out Chip-on-Substrate with Bridge), supporting line/space capabilities of 2/2μm and 8/8μm respectively. Such fine-pitch wiring capabilities are essential for achieving high-density interconnections and enabling high-speed data transfer between chiplets. ASE aims to commence mass production on this groundbreaking PLP line by the first half of 2027.

Market Impact and Future Outlook

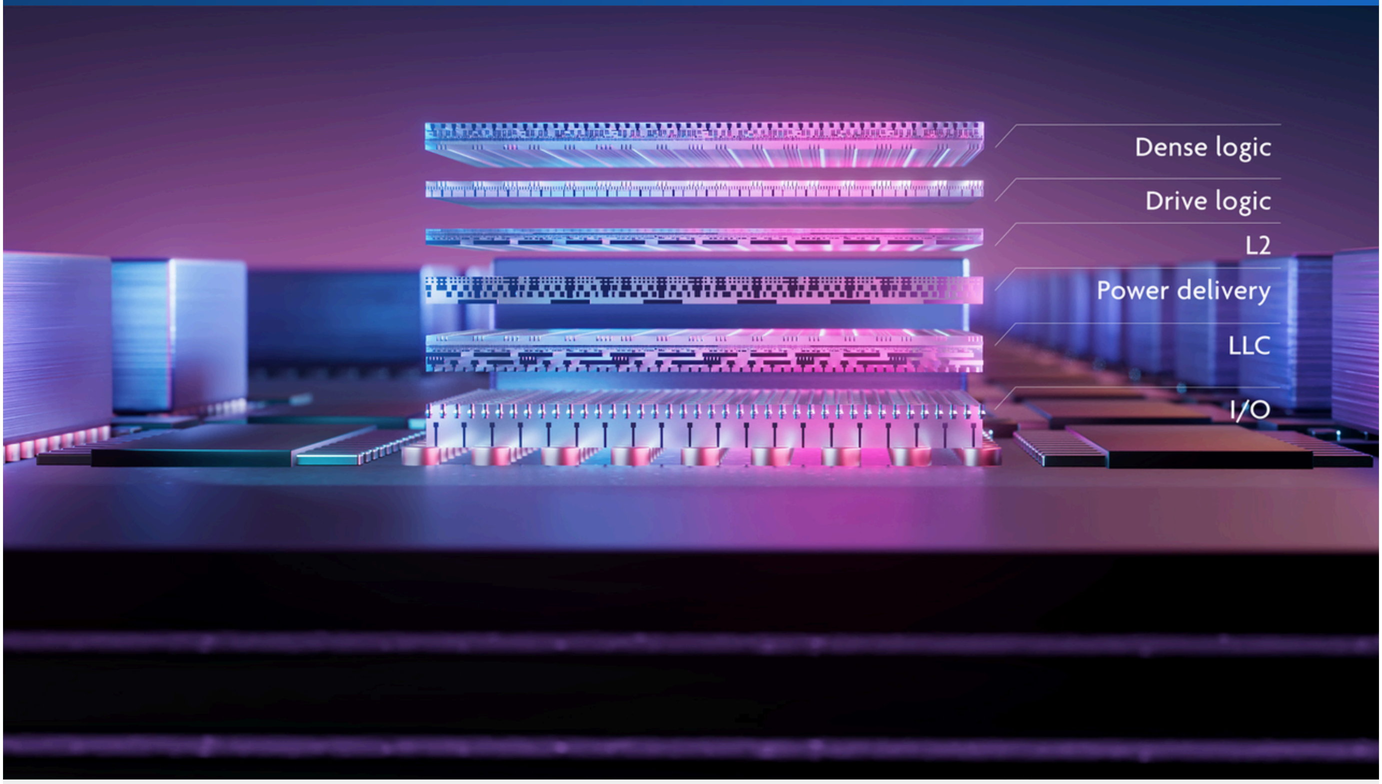
The introduction of panel-level packaging by ASE is expected to significantly contribute to reducing manufacturing costs and expanding the supply capacity of AI chips and chiplet-based semiconductor products. More efficient manufacturing processes will accelerate the widespread adoption of high-performance AI hardware, thereby fostering further advancements in AI technology. Furthermore, this technology has the potential for broad adoption across various sectors, including HPC, data centers, and autonomous vehicle chips, where high-density integration is crucial. ASE's move is anticipated to further solidify its leadership in the advanced packaging market and serve as a crucial step in driving innovation across the entire semiconductor industry.

Source: https://anysilicon.com/news/ase-launches-310mm-panel-level-packaging-line-for-ai-and-chiplet-applications/

Collected: May 29, 2026 | Automated Research System (Gemini API)

Pushing the Limits of 3D Integration: Imec and EVG Achieve Record 200nm Hybrid Bonding Pitch

Published Published May 28, 2026 imec ベルギー



OVERVIEW

Imec and EV Group (EVG) have announced a major breakthrough in 3D integration, demonstrating wafer-to-wafer hybrid bonding with an unprecedented 200nm copper interconnect pad pitch on 300mm wafers. Achieved with a remarkable post-bond overlay vector below 40 nanometers across all dies, this advance, unveiled at ECTC 2026, significantly accelerates the hybrid bonding roadmap for future logic-to-logic and memory-to-logic tier stacking. The meticulous co-optimization of process flow, including SiCN dielectrics and precision chemical mechanical polishing, was key to enabling such high interconnect densities vital for next-generation computing architectures.

IN DEPTH

The Imperative for High-Density Integration

In the vanguard of high-performance semiconductors, particularly for demanding applications like AI accelerators and data center processors, maximizing chip-to-chip connection density while concurrently minimizing data transmission latency and power consumption represents a critical challenge. To address this imperative, 3D integration — the vertical stacking of chips — has emerged as a cornerstone architectural strategy. Among its diverse methodologies, hybrid bonding distinguishes itself as a frontrunner, enabling direct, high-density copper-to-copper interconnects between stacked tiers. Transcending the scaling limitations of traditional micro-bump bonding to achieve ever-finer interconnect pitches is pivotal for unlocking future performance frontiers.

Breakthrough: 200nm Pitch Hybrid Bonding

Imec and EV Group (EVG) have announced a groundbreaking advancement in this critical field. Unveiled at ECTC 2026, their collaborative research successfully demonstrated wafer-to-wafer hybrid bonding on 300mm wafers with an extraordinarily fine copper interconnect pad pitch of just 200 nanometers. This achievement not only sets a new industry benchmark but significantly surpasses existing records for interconnect density. Crucially, the post-bond overlay vector was achieved with remarkable accuracy, remaining consistently below 40 nanometers across the entire 300mm wafer. This level of precision is paramount for guaranteeing the robustness, reliability, and optimal electrical performance of the interconnected structures. This unprecedented feat was enabled by meticulous co-optimization of the entire process flow, including the strategic use of SiCN as a high-performance dielectric material and a precisely controlled chemical mechanical polishing (CMP) step meticulously engineered prior to the bonding process.

Technical Significance and Future Outlook

The successful demonstration of 200nm pitch hybrid bonding is poised to profoundly impact the architectural landscape of next-generation computing. It unlocks the capability for unprecedented high-density interconnects in vertically stacked logic-to-logic and memory-to-logic tiers. This breakthrough is expected to dramatically alleviate data transmission bottlenecks, consequently boosting the performance of demanding AI and High-Performance Computing (HPC) applications. This technology will accelerate the realization of advanced chiplet-based designs and sophisticated 3D-ICs, further cementing hybrid bonding's pivotal role in the broader semiconductor industry roadmap. Looking ahead, it is anticipated to serve as a fundamental enabling technology for engineering more functional, compact, and energy-efficient devices across various domains.

Source: https://www.evgroup.com/company/news/detail/imec-and-ev-group-demonstrate-wafer-to-wafer-hybrid-bonding-with-200nm-interconnect-pitch-and-record-high-overlay-accuracy

Collected: May 29, 2026 | Automated Research System (Gemini API)

Hanmi Semiconductor Forecasts HBM4 TC Bonder Rebound in Q2, Announces US Expansion Plans

Published May 22, 2026 BigGo Finance South Korea

OVERVIEW

Hanmi Semiconductor anticipates a significant rebound in HBM4 TC bonder orders from Q2 2026, driven by accelerating AI semiconductor demand, despite a Q1 slump during the HBM3E-to-HBM4 transition. The company projects record full-year revenues and operating profits. To support global supply chains, including Micron, SK Hynix, and Tesla's US fabs, Hanmi plans a ₩100 billion ($66 million) investment in its Plant 7 and the establishment of "Hanmi USA" in San Jose, reinforcing its position as a global leader in HBM TC bonder technology.

IN DEPTH

Surging HBM4 Demand and Hanmi Semiconductor's Strategy

High Bandwidth Memory (HBM) is experiencing explosive demand as a core component of AI accelerators. The next generation, HBM4, requires advanced Thermo-Compression (TC) bonding technology to achieve even higher bandwidth and stacking density. Hanmi Semiconductor, a global leader in the TC bonder market, forecasts a substantial rebound in HBM4 TC bonder orders starting from Q2 2026. This resurgence is attributed to the continuous growth of the AI semiconductor market and the accelerating transition to HBM4 technology. Despite a temporary dip in Q1 revenues due to a transition gap from HBM3E to HBM4, the company maintains a bullish full-year outlook, projecting record financial performance.

Global Expansion and Focus on the US Market

To meet the escalating HBM demand, Hanmi Semiconductor is pursuing a strategy to strengthen its global production capacity and service infrastructure. As part of this initiative, the company is making a significant investment of ₩100 billion (approximately $66 million USD) in its Plant 7 in South Korea to expand production capabilities. Furthermore, Hanmi announced plans to establish "Hanmi USA" in San Jose, aiming to bolster its presence in the American market. This US outpost will reinforce support for key customers' American facilities, including Micron, SK Hynix, and Tesla, and deepen collaboration with local supply chains. This expansion in the US aligns with the broader trend of semiconductor supply chain re-alignment driven by geopolitical considerations.

Importance of HBM TC Bonder Technology and Future Outlook

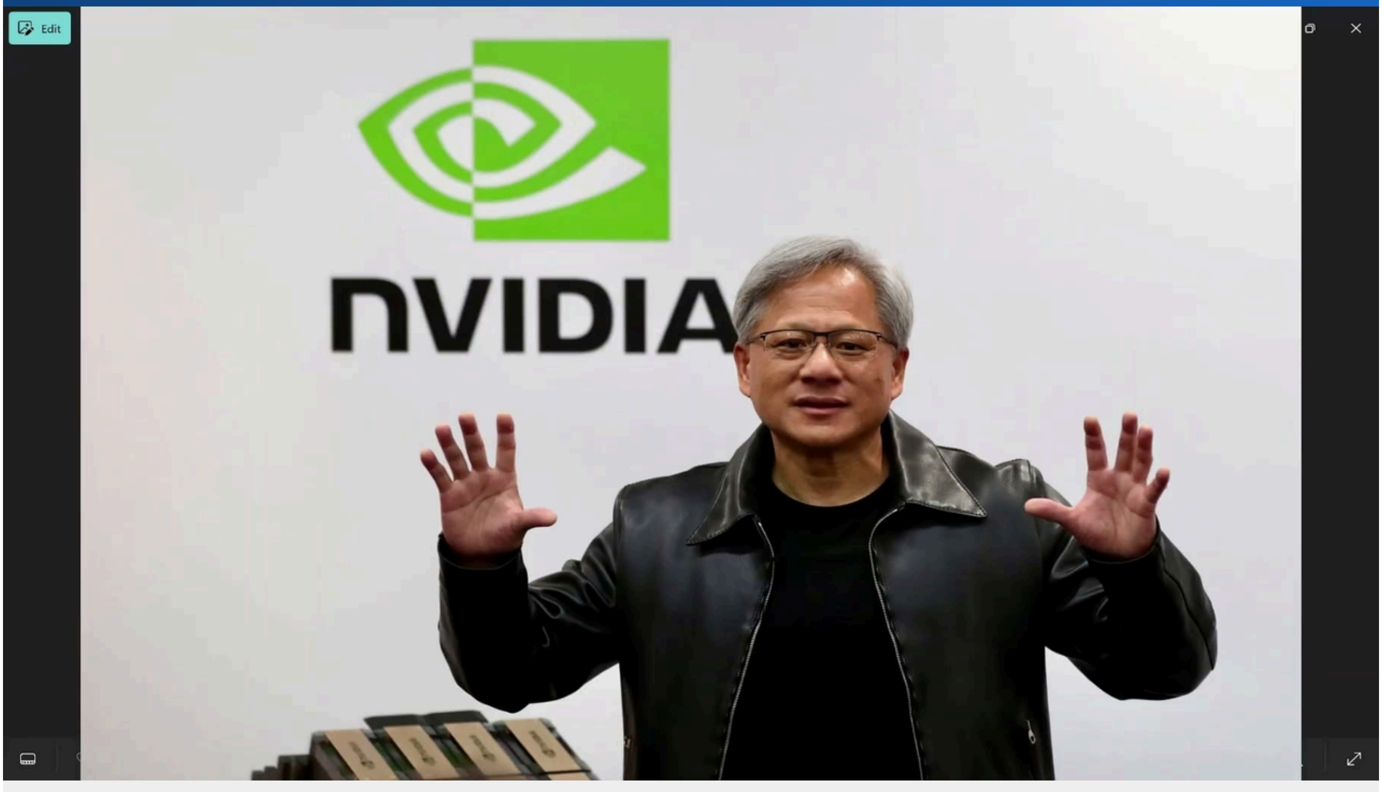
As HBM stacking density increases and requires finer-pitch chip integration, TC bonders are critical equipment for determining HBM performance and reliability. Hanmi Semiconductor's technology is key to meeting these advanced requirements and enabling high-volume HBM production. The company's aggressive investment and global expansion strategy aim to capitalize on the growth of the HBM market, seeking future revenue growth and further market share expansion. As long as AI technology continues to evolve, HBM demand is expected to remain robust, and consequently, the importance of advanced packaging equipment manufacturers like Hanmi Semiconductor will continue to rise. Specifically, the ability to address next-generation HBM beyond HBM4 will be a major determinant of the company's long-term growth.

Source: https://finance.biggo.com/news/md1vTZ4BmHHDnbgy_8Ej

Collected: May 29, 2026 | Automated Research System (Gemini API)

NVIDIA's CoWoS Bottleneck Eases, HBM Supply Emerges as Primary Constraint for AI Accelerators

Published May 21, 2026 24/7 Wall St. USA



OVERVIEW

TSMC's CoWoS advanced packaging capacity for AI accelerators is expanding, projected to reach 35,000 wafers/month by late 2026 and up to 140,000 wafers/month by 2027, alleviating a long-standing bottleneck. However, high-bandwidth memory (HBM) supply, particularly HBM3E and HBM4 for next-gen NVIDIA GPUs, has emerged as the new primary constraint. HBM production consumes significantly more wafer capacity than conventional DRAM, with only three major manufacturers (SK Hynix, Samsung, Micron) operating at scale, directly limiting AI accelerator shipments and forcing hyperscalers into long-term supply agreements.

IN DEPTH

CoWoS Bottleneck Alleviates, HBM Presents New Challenges

For several years, the TSMC CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity had been the primary bottleneck in the production of NVIDIA's high-performance AI accelerators. However, due to significant capital investments by TSMC, the tightness in CoWoS supply is gradually easing. Reports indicate that TSMC is expanding CoWoS capacity to approximately 35,000 wafers per month by the end of 2026, with potential to reach 120,000 to 140,000 wafers per month by late 2026 or 2027. While this is positive news for AI chip supply, as CoWoS constraints ease, a new and more severe bottleneck has emerged: the supply shortage of High Bandwidth Memory (HBM).

Current State and Constraints of HBM Supply

NVIDIA's next-generation GPUs, such as the Blackwell Ultra (B300) and Rubin, which are designed for high-performance AI accelerators, require vast quantities of HBM, specifically HBM3E and HBM4. However, HBM production consumes significantly more wafer capacity than conventional DRAM. Furthermore, only three manufacturers globally—SK Hynix, Samsung, and Micron—are capable of mass-producing HBM. This limited number of suppliers, coupled with high manufacturing costs and complex production processes, has made HBM supply the new dominant constraint in the AI accelerator market. Demand continues to far outstrip supply, forcing hyperscalers, including NVIDIA, to enter into long-term agreements with memory manufacturers to secure stable HBM supply.

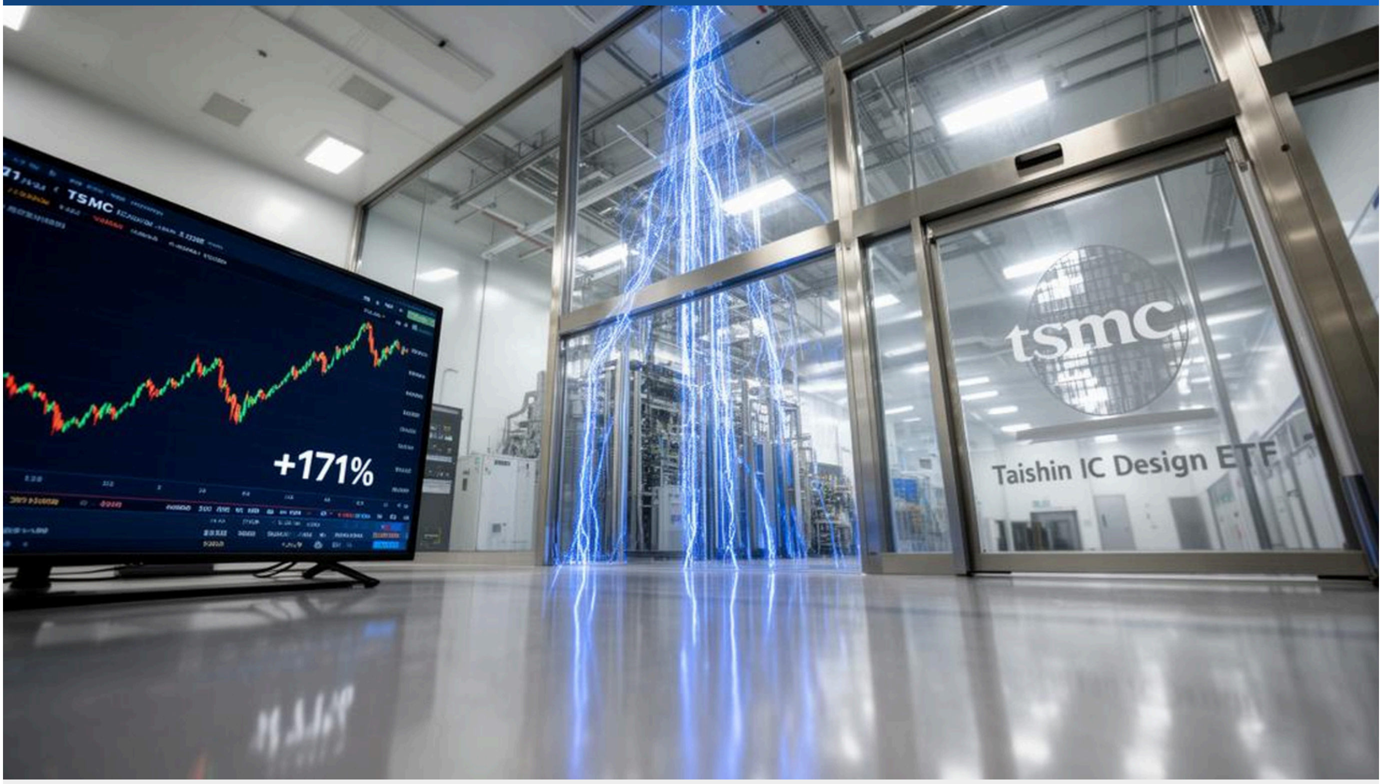
Market Impact and Future Outlook

The HBM supply shortage directly limits the ultimate shipment volumes of AI accelerators, impacting the pace of AI infrastructure build-out. This poses a significant challenge not only for AI chip providers like NVIDIA but also for cloud companies deploying AI services. In the long term, memory manufacturers must accelerate HBM production capacity expansion, a process that requires substantial capital investment and time. Continuous improvements in HBM manufacturing technology, particularly in stacking techniques and thermal management, will also be essential. While the market welcomes the easing of CoWoS supply, it must now confront the new reality of HBM scarcity through collaborative efforts and innovation across the entire supply chain. This approach is necessary to enable the continued widespread adoption and advancement of AI technology.

Source: https://247wallst.com/investing/2026/05/21/nvidia-could-10x-its-sales-one-bottleneck-is-stopping-it/

NVIDIA CEO Jensen Huang Projects $150 Billion Annual Investment in Taiwan's AI Supply Chain

Published May 27, 2026 BigGo Finance Taiwan



OVERVIEW

NVIDIA CEO Jensen Huang announced that the company's annual procurement and investment in Taiwan's AI supply chain is projected to reach $150 billion in the future, a tenfold increase from $10-$15 billion four to five years ago. This substantial commitment underscores Taiwan's critical role in NVIDIA's AI strategy, with TSMC directly benefiting from robust orders for 3nm wafers and CoWoS advanced packaging. TSMC anticipates strong demand for these advanced technologies to continue through 2027, with demand still outstripping available supply.

IN DEPTH

NVIDIA's Unwavering Commitment to Taiwan's Supply Chain

NVIDIA CEO Jensen Huang announced that the company's annual procurement and investment in Taiwan's AI supply chain is projected to reach an astounding $150 billion in the future. This represents a tenfold increase from the $10-$15 billion annual level just four to five years ago, and a significant jump from the current annual spending of approximately $100 billion. This declaration unequivocally highlights NVIDIA's strategic positioning of Taiwan's semiconductor ecosystem as an absolutely critical partner in the age of AI.

TSMC's Gains and Market Ramifications

This enormous commitment from NVIDIA is poised to yield substantial benefits, particularly for Taiwan Semiconductor Manufacturing Company (TSMC). TSMC is expected to continue securing robust orders for 3nm process technology wafer fabrication, which is essential for NVIDIA's next-generation AI chips, and for its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging services. CEO Huang's remarks corroborate TSMC's own outlook, which anticipates strong demand for its cutting-edge manufacturing and packaging technologies to persist through 2027, with demand continuing to outpace available supply for AI accelerators.

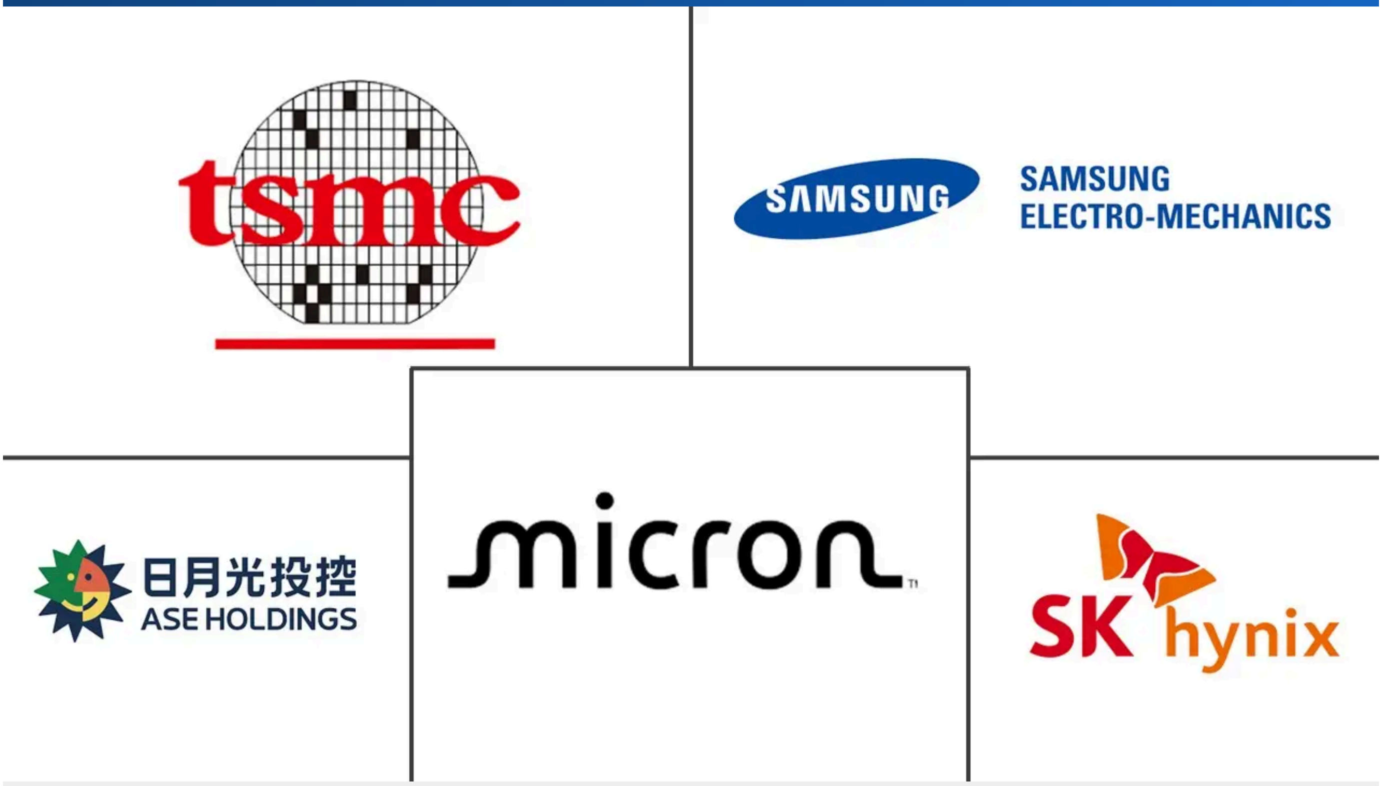
Taiwan's Strategic Position in the Semiconductor Industry

NVIDIA's large-scale investment reaffirms Taiwan's undisputed centrality in the global semiconductor supply chain, especially concerning AI chip manufacturing. Taiwanese companies have cultivated a comprehensive ecosystem, spanning design, manufacturing, packaging, and testing, which underpins innovation in the AI era. This investment serves as a testament to the international confidence in Taiwan's technological innovation capabilities and manufacturing prowess, factors that will further solidify Taiwan's dominance in the semiconductor industry for years to come. Moreover, it explicitly demonstrates that a strong partnership with Taiwan is indispensable for NVIDIA to maintain its leading edge in AI technology.

Source: https://finance.biggo.com/news/Iw93Z54BDXrLZJaArqwN

Tokyo Electron and Samsung Boost Capex for Hybrid Bonding Equipment Amid Advanced Packaging Shift

Published May 26, 2026 Mordor Intelligence Japan, South Korea



OVERVIEW

Tokyo Electron and Samsung are significantly increasing capital expenditures for hybrid bonding and general bonding equipment, targeting long-term growth in the Through-Silicon Via (TSV) market for GPUs and AI accelerators. This investment is crucial for HBM4, as memory vendors outsource base-die logic to leading-edge foundries, demanding tighter TSV alignment tolerances and copper-to-copper bonding—making hybrid bonding indispensable. This strategic move aims to secure their leadership in the evolving advanced packaging landscape.

IN DEPTH

Shift to Advanced Packaging and Investment Rationale

The semiconductor industry is approaching the physical limits of Moore's Law, shifting the primary driver for performance improvement from traditional scaling to advanced packaging, particularly heterogeneous integration. High-performance chips like GPUs and AI accelerators require efficient, high-density integration of multiple dies to maximize data transfer speeds and power efficiency. To meet this demand, giants in semiconductor equipment and chip manufacturing, Tokyo Electron (TEL) and Samsung, are substantially increasing their capital expenditures for hybrid bonding and related bonding equipment. This strategic investment aims to secure long-term leadership in the Through-Silicon Via (TSV) market, a core technology for next-generation semiconductor products.

HBM4 and the Indispensability of Hybrid Bonding

Specifically, the advent of HBM4, the latest generation of High Bandwidth Memory, further elevates the importance of hybrid bonding technology. HBM4 involves more complex stacking of memory and logic base dies, leading to a dramatic increase in interconnection density. This necessitates finer pitches and higher connection reliability, levels that are challenging for traditional micro-bump bonding methods to achieve. Furthermore, there's an accelerating trend for memory vendors to outsource the manufacturing of HBM base-die logic to leading-edge foundries like TSMC. This development increases the demand for stringent TSV alignment tolerances and robust copper-to-copper bonding requirements for integrating dies from different manufacturers with high precision. Hybrid bonding is recognized as the only viable solution capable of meeting these strict requirements.

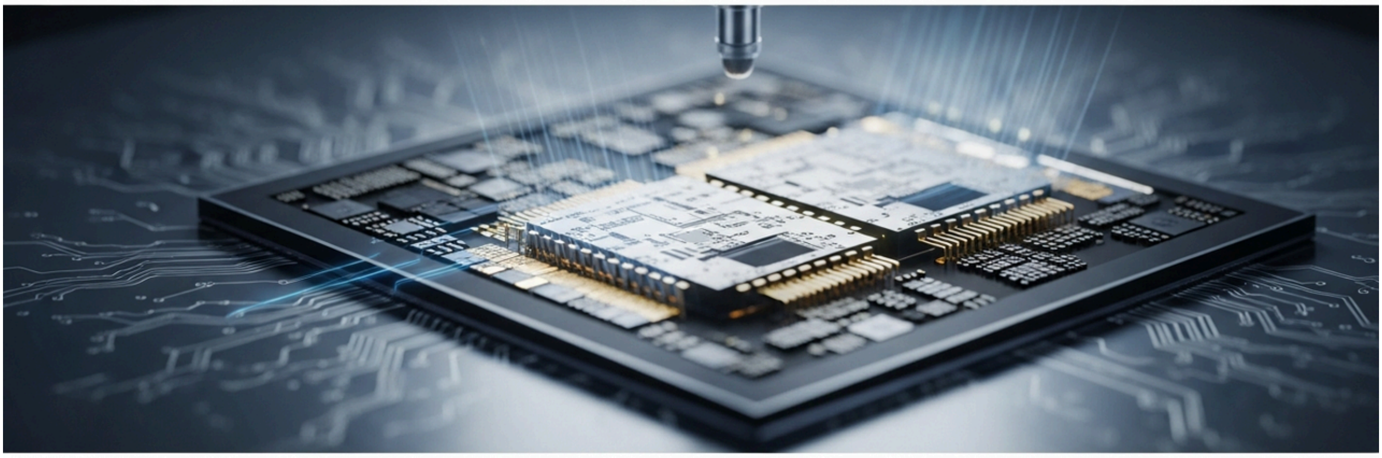
Market Impact and Future Outlook

The substantial capital investments by Tokyo Electron and Samsung are expected to accelerate the industrial adoption of hybrid bonding technology, potentially establishing new standards for semiconductor manufacturing processes. TEL, as a leading supplier of bonding equipment, and Samsung, as a major manufacturer of advanced memory and system LSIs, will leverage their respective strengths to enhance mass production capabilities for HBM4 and subsequent high-performance chips. This move will serve as a foundational support for the continuous growth of the AI and HPC markets, fostering technological innovation across the entire supply chain. In the long term, hybrid bonding is anticipated to further enable the development of 3D-IC and chiplet technologies, solidifying its position as a key technology that pushes the boundaries of performance and efficiency across the semiconductor industry.

Source: https://www.mordorintelligence.com/industry-reports/through-silicon-via-tsv-for-gpu-and-ai-accelerators-market

Heterogeneous Integration Advances with Hybrid Bonding, Tackling Critical Power and Thermal Challenges for AI and 5G/6G

Published May 21, 2026 IndexBox Global



OVERVIEW

Heterogeneous integration, particularly vertical chip stacking with fine-pitch interconnects, is crucial for future AI and 5G/6G electronics, dramatically reducing data travel distances and power consumption. Hybrid bonding is enhancing chip-to-chip interconnect density and efficiency but introduces new reliability concerns at bonding interfaces requiring further research. Power delivery and thermal management are becoming limiting factors for expanding AI workloads, driving interest in integrated voltage regulation within packages and advanced cooling solutions as transistor counts continue to rise.

The Crucial Role of Heterogeneous Integration

Semiconductor chips, forming the core of next-generation electronics for AI, 5G/6G communications, and high-performance computing, demand unprecedented levels of performance and power efficiency. The key to achieving this lies in heterogeneous integration, a technology that combines multiple chips with different functionalities (logic, memory, I/O, etc.) within a single package. By vertically stacking chips using fine-pitch interconnects, this approach dramatically shortens data transmission distances, consequently reducing signal latency and power consumption. This enables performance enhancements and miniaturization levels that are difficult to achieve with traditional monolithic chips.

Advances and Challenges with Hybrid Bonding

At the forefront of heterogeneous integration is hybrid bonding technology. This technique facilitates direct copper-to-copper connections between chips, fused with dielectric layers, achieving significantly finer pitches and higher connection densities compared to conventional micro-bump connections. This leap dramatically improves inter-chip data transfer bandwidth and efficiency. However, hybrid bonding also introduces new technical challenges. Key concerns include mechanical stress at the bonding interface, mismatches in thermal expansion coefficients, and electrical reliability. Addressing these issues necessitates further research and sophisticated approaches in material science, process control, and design optimization.

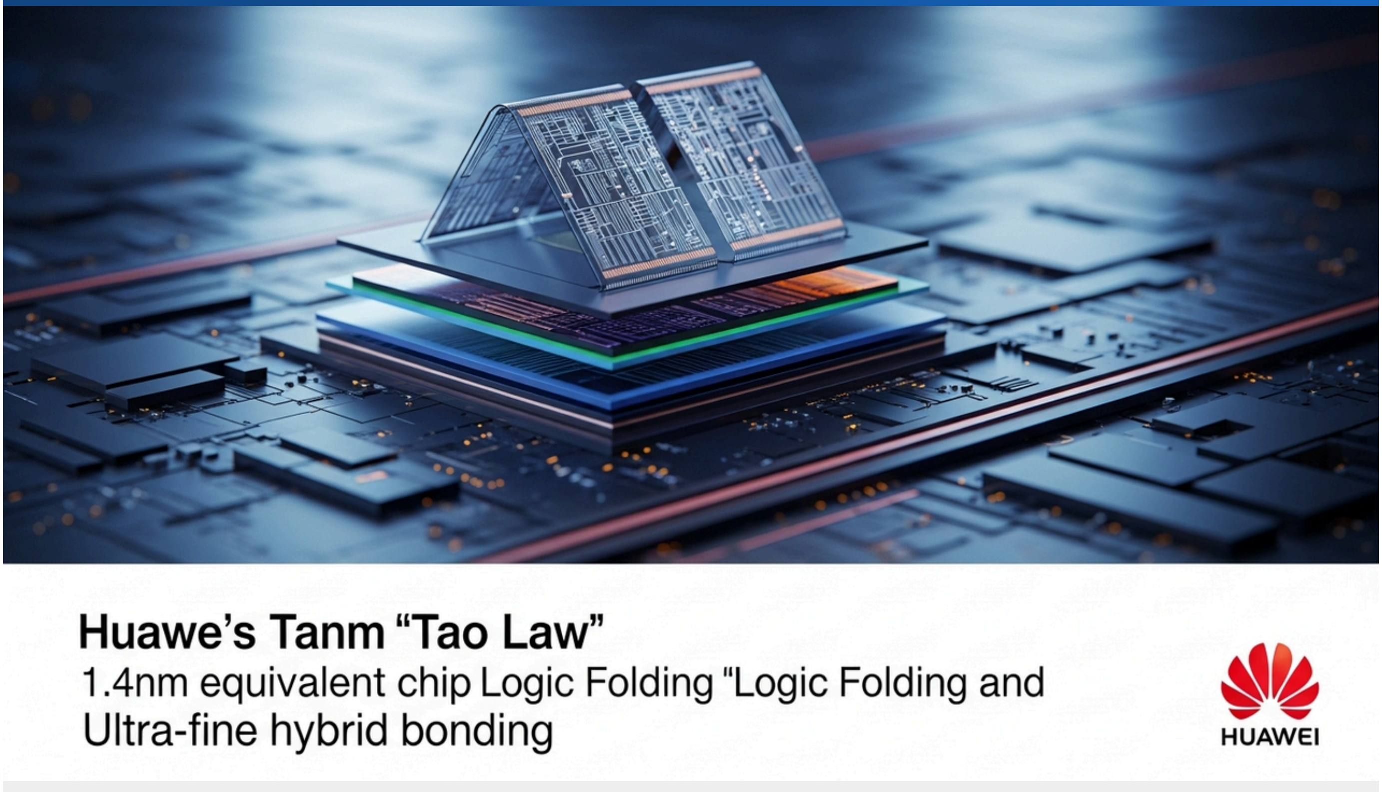
Limits of Power Delivery and Thermal Management

As the scale and complexity of AI workloads expand, the power consumption and heat generation of semiconductor chips are dramatically increasing. Currently, power delivery and thermal management are becoming the most critical limiting factors for further chip performance scaling. Power delivery within densely integrated chip packages faces challenges of voltage drop and noise, which can hinder stable operation. Moreover, if generated heat cannot be efficiently dissipated, it leads to performance degradation and reliability issues. Consequently, the industry is seeing growing interest in technologies that integrate voltage regulators directly within packages, as well as innovative thermal management solutions such as liquid cooling, microfluidic cooling, and 3D cooling. Comprehensive solutions to these challenges are essential to accommodate the continuous increase in transistor counts and enable future advancements.

Source: https://www.indexbox.io/blog/heterogeneous-integration-key-to-ai-5g6g-and-future-electronics/

Huawei's "Tao Law" Proposes 1.4nm-Equivalent Chip Density via Logic Folding and Ultra-Fine Hybrid Bonding

Published May 25, 2026 China as a System China



OVERVIEW

Huawei has introduced the "Tao Law," a novel semiconductor process development aiming for 1.4nm-equivalent chip density within five years through "Logic Folding." This method distributes logic gates across vertically stacked active layers connected by ultra-fine-pitch hybrid bonding and TSV technologies. The Kirin 2026 achieved a 1.5µm hybrid-bonding pitch, with a mobile SoC chip utilizing Logic Folding slated for autumn 2026, targeting a 55% increase in effective transistor density. This strategy demands significant advancements in EDA tools to treat multiple stacked dies as a continuous design entity.

IN DEPTH

Concepts of "Tao Law" and "Logic Folding"

Huawei's proposed "Tao Law" represents a novel scaling approach for semiconductor processes, envisioning an alternative to traditional Moore's Law. It aims to enhance effective chip density not only by scaling down transistor sizes on a single plane but also by extending chips vertically. Central to this strategy is an innovative methodology called "Logic Folding." Logic Folding involves distributing logic gates across multiple vertically stacked active layers instead of confining them to a single silicon layer. This allows for the physical integration of more transistors within the same footprint, effectively delivering performance gains comparable to advanced process node scaling. This approach holds the potential to overcome the physical and economic limitations currently challenging conventional miniaturization techniques.

Role of Ultra-Fine Hybrid Bonding and TSV Technology

The realization of Logic Folding critically depends on highly advanced chip stacking and interconnection technologies. Huawei places ultra-fine-pitch hybrid bonding and Through-Silicon Via (TSV) technology at the core of this endeavor. Hybrid bonding enables direct copper-to-copper connections between chips, achieving significantly finer connection pitches than conventional micro-bumps. This maximizes data transfer speed and efficiency between vertically stacked logic layers. The Kirin 2026 has already demonstrated a groundbreaking hybrid bonding pitch of 1.5μm, showcasing the maturity of this technology.

Next-Generation Mobile SoC and Market Implications

Huawei plans to launch a mobile System-on-Chip (SoC) utilizing this "Tao Law" and Logic Folding technology in autumn 2026. This new chip aims to achieve a 55% increase in effective transistor density compared to traditional designs, which is expected to dramatically enhance the performance of smartphones and other mobile devices. The successful implementation of Logic Folding necessitates significant advancements in Electronic Design Automation (EDA) toolchains, enabling them to treat multiple stacked dies as a single, continuous design entity. Huawei's move demonstrates the strong resolve of the Chinese semiconductor industry to pursue performance gains through innovative packaging technologies, even with limited access to leading-edge foundries due to U.S. export restrictions. This strategy has the potential to introduce a new direction for the global semiconductor roadmap.

Source: https://leonliao.substack.com/p/tau-scaling-law-vs-moores-law-from

Collected: May 29, 2026 | Automated Research System (Gemini API)

Korea Addresses HBM Test Equipment Bottleneck by Fostering Domestic Suppliers

Published May 23, 2026 eferix.substack.com South Korea

OVERVIEW

South Korea has identified the HBM test equipment bottleneck, historically dominated by foreign companies like Advantest and Teradyne, as a national supply chain vulnerability. In response, SK Hynix actively cultivated domestic suppliers, leading to Digital Frontier mass-producing HBM4 wafer testers. Digital Frontier secured approximately KRW 196 billion (~$143 million) in HBM4 contracts in Q1 2026 alone, highlighting the rapid growth of indigenous capabilities in this critical sector and strengthening Korea's HBM production resilience.

IN DEPTH

Importance of HBM Test Equipment and the Bottleneck

High Bandwidth Memory (HBM) is a core component of AI accelerators, and its performance and reliability are guaranteed through rigorous testing procedures. The complex stacked structure of HBM, in particular, necessitates advanced wafer-level and final testing. Historically, the HBM test equipment market has been dominated by a few global players, such as Japan's Advantest and the US's Teradyne. This created a bottleneck for South Korea's HBM production, as it faced high external dependence in this critical area. This dependence was recognized as a national-level vulnerability for Korea from the perspective of supply chain stability and geopolitical risks.

SK Hynix's Strategy to Cultivate Domestic Suppliers

To resolve this bottleneck, SK Hynix, a leading HBM manufacturer in South Korea, has strategically focused on cultivating domestic semiconductor equipment suppliers. This initiative aimed not only at cost reduction but also at strengthening the supply chain's resilience and achieving technological self-reliance. SK Hynix has provided technical cooperation and investment to promising domestic companies, supporting their development of HBM test equipment. These proactive efforts have borne fruit, enabling domestic companies like Digital Frontier to develop advanced testers for HBM4 and enter mass production.

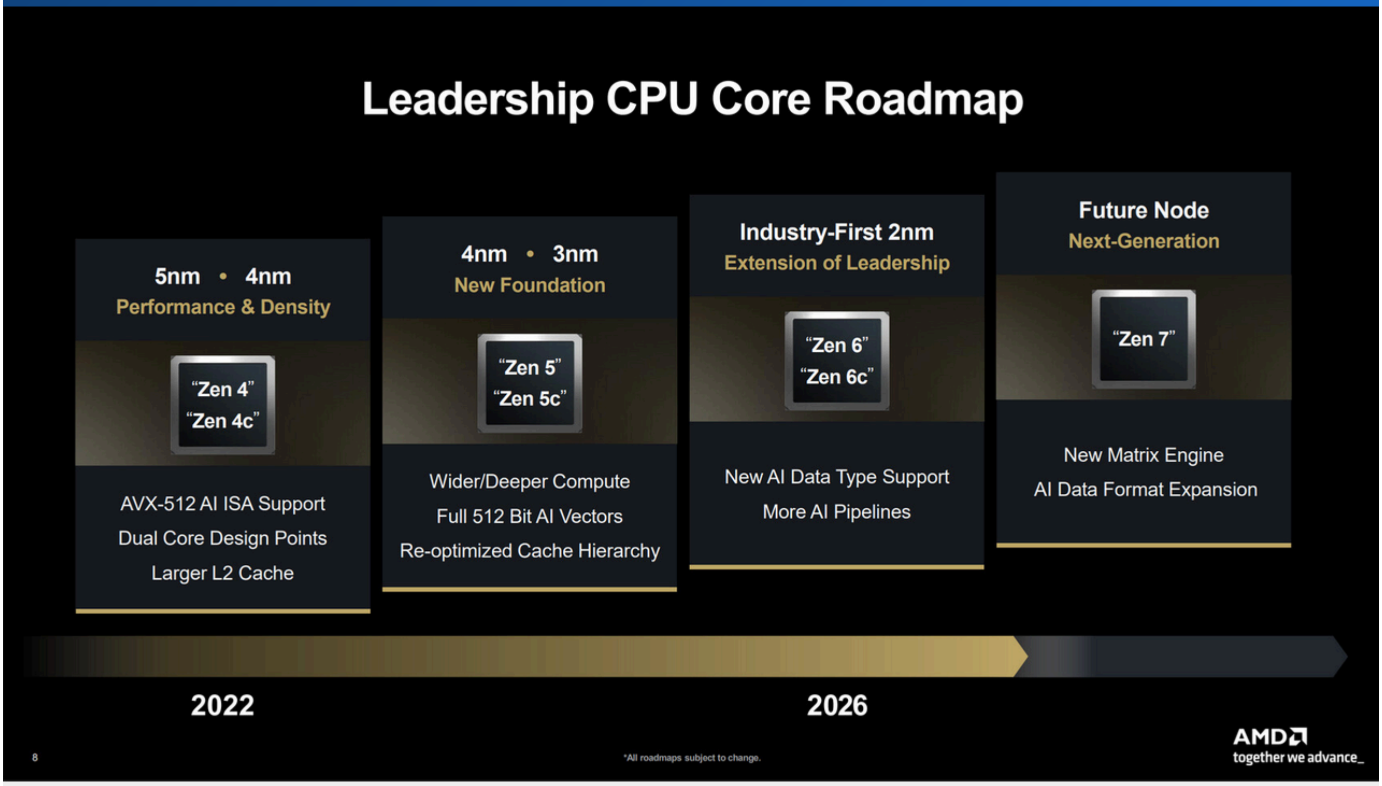
Rise of Digital Frontier and Market Impact

Digital Frontier successfully mass-produced HBM4 wafer testers and secured substantial HBM4-related contracts worth approximately KRW 196 billion (around $143 million USD) in Q1 2026 alone. This achievement demonstrates the company's rapid emergence as a critical player in the global HBM supply chain. Digital Frontier's success holds significant implications for South Korea in overcoming bottlenecks in HBM production and advancing vertical integration of cutting-edge technologies within its domestic ecosystem. This is expected to further enhance Korea's competitiveness in HBM production and strengthen its readiness to stably meet the increasing demand for AI chips in the future. In the long term, this development has the potential to reshape the HBM test equipment market landscape and foster diverse technological innovations.

Source: https://eferix.substack.com/p/korea-and-the-hbm-supply-chain

AMD Explores Powertech's FOPLP for Next-Generation Zen 7 CPUs, Eyeing Packaging Diversification

Published May 25, 2026 TechPowerUp USA



OVERVIEW

AMD is reportedly exploring Powertech Technology's Fan-Out Panel-Level Packaging (FOPLP) for its upcoming "Zen 7" CPUs, codenamed "Grimlock." This move signals AMD's strategic intent to build increasingly complex chiplet configurations and potentially reduce reliance on TSMC for advanced packaging services. The flagship "Grimlock" CCD is speculated to feature 16 cores and, when paired with next-generation 3D V-Cache, could achieve up to 224MB of total L3 cache, leveraging FOPLP's efficiency for high-performance, cost-effective integration.

IN DEPTH

The Necessity of Advanced Packaging in Next-Generation CPUs

The continuous advancement of CPU performance now relies heavily not only on miniaturization technologies but also on sophisticated packaging techniques. Particularly, the chiplet architecture, actively promoted by AMD, integrates multiple smaller chips (chiplets) within a single package, improving manufacturing yields and enhancing design flexibility. For the forthcoming "Zen 7" architecture CPUs, codenamed "Grimlock," further performance improvements and functional integration necessitate the adoption of new solutions that push beyond the limits of current packaging technologies. Against this backdrop, AMD is actively exploring various advanced packaging solutions.

Interest in Powertech Technology's FOPLP Solution

One of the key technologies AMD is reportedly considering is the Fan-Out Panel-Level Packaging (FOPLP) solution provided by Powertech Technology. FOPLP, by utilizing larger, rectangular panels compared to traditional wafer-level packaging, can significantly enhance the manufacturing efficiency and cost-effectiveness of chiplets. This capability could enable AMD to economically produce more complex and higher-performance chiplet configurations. Powertech Technology's FOPLP solution is expected to demonstrate particular advantages in high-performance CPU packaging, especially where high-density redistribution layers (RDL) are required.

AMD's Strategic Objectives and Zen 7 CPU Outlook

AMD's exploration of advanced packaging technologies like FOPLP stems from several strategic objectives. One aim is to efficiently construct even more powerful and complex chiplet configurations for AI and HPC (High-Performance Computing) applications. Another key objective is to potentially reduce its reliance on TSMC for advanced packaging services, thereby diversifying its supply chain. TSMC currently faces high demand for advanced packaging, such as CoWoS, which can lead to supply constraints. By expanding its own packaging options, AMD aims to secure future production capacity and flexibility.

The flagship "Grimlock" CCD of the next-generation "Zen 7" architecture is speculated to feature 16 cores. When combined with next-generation 3D V-Cache technology, the total L3 cache capacity could reach up to 224MB. Such large cache capacities are expected to deliver exceptionally high performance in AI workloads and gaming. The potential adoption of Powertech's FOPLP technology would significantly impact the cost and performance balance of "Grimlock" CPUs, playing a crucial role in AMD's efforts to establish a competitive advantage in the highly contested CPU market.

Source: https://www.techpowerup.com/349330/amd-zen-7-ip-to-use-tsmc-a14-node-and-more-advanced-packaging?cp=3