Semiconductor Back-End

Weekly Intelligence Report

2026-06-20 | 37 articles | 11 countries

troy-technical.jp

This Week's Keyword

Advanced Packaging

AI demand drives capacity & material innovation

37	11	120-140K	$1B+
articles	countries	wafers/month	USD
Total Articles Analyzed	Source Countries/Regions	TSMC CoWoS Capacity (2026)	Intel Glass Substrate R&D

All 37 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	Samsung/SK Honam Fabs	Corporate Strategy	●●○○○	●●●○○	●●●●○	●●●○○	●●●●○	Samsung/SK Hynix plan advanced packaging fabs in S. Korea's Honam for AI memory; Amkor expands.
#02	Glass Core Substrates	Research	●●●●○	●●○○○	●●●●●	●●●●○	●●●●●	Glass core substrates are next-gen packaging; Intel invests $1B+ in R&D; for 2030 HVM.
#03	AT&S; Kulim Expansion	Corporate Strategy	●●○○○	●●●●○	●●●○○	●●●●●	●●●●●	AT&S; invests €2B in Malaysia for IC substrates & advanced PCBs, driven by AMD & AI demand.
#04	TSMC CoWoS/CoPoS	Market Analysis	●●●○○	●●●○○	●●●●●	●●●○○	●●●●●	TSMC to halve CoWoS gap by 2026; NVIDIA to adopt next-gen CoPoS for 2028-2029 mass production.
#05	TSMC CoWoS Shortage	Market Analysis	●○○○○	●●●●●	●●●●●	●●●○○	●●●●●	TSMC's CoWoS capacity still short through 2026 despite expansion; Nvidia reserves 60%.
#06	ABF/Glass Substrates	Trend Article	●●●○○	●●○○○	●●●●○	●●○○○	●●●●○	ABF substrates bottleneck AI accelerators; glass substrates are promising but years from HVM.
#07	TSMC Glass Substrates	Research	●●●●○	●●○○○	●●●●○	●●●○○	●●●●●	TSMC strengthens glass substrate supply chain for CoWoS, achieving 16% warpage reduction.
#08	Henkel HBM Materials	Corporate Strategy	●●○○○	●●●●○	●●●○○	●●●○○	●●●●●	German Henkel expands electronics materials investment in Korea for HBM packaging development.
#09	Glass Substrate Hurdles	Trend Article	●●●○○	●●○○○	●●●●○	●●○○○	●●●●○	Glass core substrates are next-gen packaging for AI/HPC, but face brittleness and TGV hurdles.
#10	ASE LEAP Revenue Up	Corporate Strategy	●●○○○	●●●●○	●●●●○	●●●○○	●●●●○	ASE raises 2026 LEAP revenue outlook to $3.5B+, driven by AI advanced packaging demand.
#11	Park/imec Metrology	Research	●●●●○	○○○○○	●●●○○	●●●●●	●●●●●	Park Systems & imec partner for advanced metrology solutions for next-gen 3D packaging & logic.
#12	CoWoS Eases, New Bottlenecks	Market Analysis	●●○○○	●●●○○	●●●●●	●●○○○	●●●●●	CoWoS shortage eases, but bottleneck shifts to hyper-scale packaging, glass substrates, TGVs.
#13	imec RF Interposer	Research	●●●●●	○○○○○	●●●○○	●●●●●	●●●●●	imec unveils high-density MIMCAP RF interposer for D-band mm-wave, accelerating III-V chiplet integration.
#14	TSMC/Amkor US Deal	Corporate Strategy	●●○○○	●●●●○	●●●●●	●●●○○	●●●●●	TSMC & Amkor sign 10-year advanced packaging deal in Arizona; Amkor invests $7B for CoWoS.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#15	AI Memory Shortage	Market Overview	1	5	5	2	5	AI demand intensifies memory shortage due to TSMC CoWoS constraints and Vietnam labor issues.
#16	Nokia US Packaging Boost	Corporate Strategy	2	5	3	2	5	Nokia boosts US advanced semiconductor test & packaging capacity 10x in Pennsylvania for AI networks.
#17	Malaysia Packaging Cons.	Corporate Strategy	2	3	2	2	3	Malaysia establishes Advanced Packaging Consortium with RM185M to elevate semiconductor value chain.
#18	TSMC CoWoS Gap Narrows	Market Analysis	3	3	5	4	5	TSMC to halve AI chip supply gap to 10% by end-2026 with CoWoS boost; next-gen CoPoS on track.
#19	SE Report: Photonics, Hybrid	Trend Article	4	2	4	3	5	SE report highlights on-chip photonics, hybrid bonding, GaN for AI/HPC, Intel's packaging advancements.
#20	AT&S; Kulim AI Substrates	Corporate Strategy	2	4	3	4	5	AT&S; expands Kulim plant in Malaysia, boosting AI IC substrate capacity under AMD agreements.
#21	KAIST Liquid Cooling	Research	5	2	4	3	4	KAIST develops breakthrough liquid cooling for AI semiconductors, shattering thermal bottlenecks.
#22	Samsung Packaging Lag	Market Analysis	1	5	4	3	4	Samsung's advanced packaging lags TSMC/Intel, clouding its AI chip comeback despite HBM efforts.
#23	Lam Research Packaging	Corporate Strategy	2	4	4	4	5	Lam Research forecasts 50%+ growth in advanced packaging revenue by 2026, key AI "picks and shovels" provider.
#24	SK Hynix HBM4E Samples	New Product	4	4	5	5	5	SK Hynix ships 12-layer HBM4E samples for AI, delivering 16Gbps/pin, 20%+ power efficiency.
#25	SK Hynix US HBM Talks	Corporate Strategy	1	3	4	2	5	SK Hynix holds US talks on HBM supply & investment plans, bolstering domestic semiconductor supply.
#26	Micron HBM Sold Out	Corporate Strategy	2	5	5	3	5	Micron's HBM capacity sold out through 2026, securing position in NVIDIA's "Vera Rubin" AI platform.
#27	Kaynes/AOI India OSAT	Corporate Strategy	2	3	2	3	2	Kaynes Tech partners with AOI Electronics to build ₹3,307 Cr OSAT plant in India for back-end.
#28	TSMC/Amkor US Pact	Corporate Strategy	2	4	5	3	5	TSMC & Amkor forge 10-year strategic partnership to boost US advanced packaging capabilities.
#29	AT&S; Malaysia/China	Corporate Strategy	2	4	3	4	5	AT&S; invests €2B in Malaysia/China to expand high-end IC substrate capacity for AI/HPC.
#30	Amkor AZ Expansion	Corporate Strategy	2	4	5	3	5	Amkor expands Arizona footprint by 67 acres, aiming to be first high-volume advanced packaging OSAT in US.
#31	Intel Hires Lee Seok-hee	Corporate Strategy	3	5	4	3	5	Intel appoints former SK Hynix CEO Lee Seok-hee as SVP of Advanced Packaging to bolster AI systems.
#32	Samsung Honam HBM Plant	Corporate Strategy	2	3	4	3	4	Samsung considers new HBM-focused advanced packaging plant in Honam, S. Korea for AI server demand.
#33	SK Hynix HBM4E Ships	New Product	4	4	5	4	5	SK Hynix ships next-gen HBM4E AI memory chips: 12-layer, 48GB, 16Gbps/pin, 20%+ power efficiency.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#34	TSMC CoPoS/Glass Sub	Research	●●●●	●●○○	●●●●	●●●●	●●●●	TSMC accelerates CoPoS development (310x310mm panel, late 2028 HVM) & glass core for CoWoS.
#35	Nokia US ATP Expansion	Corporate Strategy	●●○○	●●●●	●●●○	●●●●	●●●●	Nokia expands US advanced test & packaging in Pennsylvania, doubling workforce for AI infrastructure.
#36	Amkor SiP Vietnam Shift	Corporate Strategy	●●○○	●●●●	●●○○	●●●○	●●●○	Amkor shifts SiP production to Vietnam to free space for high-value programs, driven by smartphone demand.
#37	imec III-V Chiplet	Research	●●●●	●○○○	●●●○	●●●●	●●●●	imec achieves system-level III-V chiplet integration on RF silicon interposer, boosting capacitance 10-100X.

●●●○ High ●●○○ Med-High ●○○○ Med ○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your advanced packaging roadmap ready for glass?

Intel's $1B+ investment and TSMC's CoPoS/glass substrate plans signal a major shift. US/EU OEMs and materials suppliers must assess if their current organic substrate strategies will be obsolete by 2030.

❷ How exposed is your AI supply chain to HBM bottlenecks?

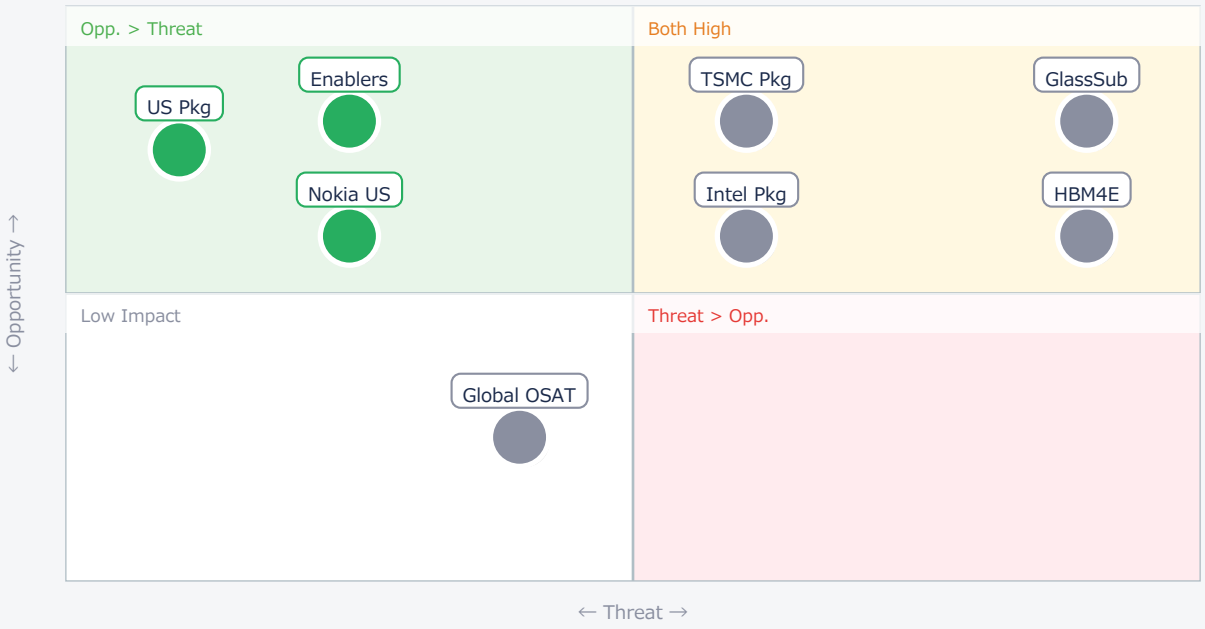
SK Hynix and Micron's HBM capacity is sold out through 2026, with NVIDIA securing major allocations. US/EU AI chip designers and data center operators must secure future HBM supply or risk competitive disadvantage.

❸ Are you leveraging US domestic packaging capacity effectively?

TSMC and Amkor's $7B Arizona deal and Nokia's PA expansion aim to build a robust US advanced packaging ecosystem. US/EU companies should evaluate opportunities for secure, domestic sourcing and partnerships.

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
GlassSub	Critical	New mat'l market	Obsolescence risk
TSMC Pkg	Critical	AI chip supply	New bottlenecks
HBM4E	Critical	AI perf boost	Supply access
Intel Pkg	Critical	Intel partner	Competitor shift
US Pkg	Opp.	Domestic supply	Cost premium
Enablers	Opp.	New tech sales	Lagging R&D;
Nokia US	Opp.	US infra build	Niche market
Global OSAT	Ref.	Diversify chain	Regional comp

Deep Dive ① — Glass Core Substrates: The Next Frontier

#02 | 2026/06/13 | Infra Startups | Tech Novelty●●●●○ Proximity●●○○○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●●

Glass core substrates are emerging as the next physical frontier for advanced packaging, offering superior dimensional stability, lower CTE, and finer wiring than organic substrates. Intel is investing over $1 billion in its Arizona R&D; line, targeting high-volume production between 2026 and 2030 to lead this domain.

This technology promises higher interconnect density, improved power delivery, and superior thermal management, crucial for future AI and HPC chips. It aims to break the current CoWoS bottleneck and revolutionize semiconductor packaging, but faces challenges like glass brittleness and scalable TGV formation.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: Intel's substantial investment signals a serious commitment to glass substrates, making the 2026-2030 HVM target ambitious but credible. Key technical barriers remain in glass processing, TGV formation, and establishing a robust supply chain. [Opportunity] for US/EU materials and equipment suppliers to partner with Intel and other pioneers in developing this new ecosystem. [Threat] for existing organic substrate manufacturers facing long-term obsolescence and for non-Intel foundries/OSATs needing to rapidly develop their own glass substrate roadmaps. Next actions: [R&D;] Initiate internal research on glass substrate processing and TGV technology by Q4 2026. [Business Dev] Explore strategic partnerships with Intel or emerging glass substrate developers by Q1 2027.

Deep Dive ② — SK Hynix Ships HBM4E: AI Memory Breakthrough

#24 | 2026/06/18 | SK hynix Inc. | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●●● US/EU Relevance●●●●●

SK Hynix has begun shipping samples of its 12-layer HBM4E, a next-gen AI DRAM, to key customers. This HBM4E boasts 16Gbps per pin data processing speeds and over 20% improved power efficiency, representing a 30%+ speed increase over HBM4.

Utilizing Advanced MR-MUF technology, it achieves 48GB capacity and a 17% reduction in thermal resistance, critical for high-heat AI environments. NVIDIA CEO Jensen Huang's endorsement at Computex 2026 highlights the industry's high anticipation for this memory.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The published performance numbers from SK Hynix, an industry leader, are highly realistic for samples and set a new benchmark. The primary technical barrier is scaling this advanced 12-layer stack with MR-MUF to high-volume mass production with consistent yields. [Opportunity] for US/EU AI OEMs to design next-gen accelerators leveraging HBM4E's superior performance and efficiency, accelerating AI development. [Threat] for US/EU AI OEMs reliant on HBM from Asian suppliers, facing potential supply chain allocation risks and competitive disadvantage if they cannot secure early access. Next actions: [Procurement] Engage SK Hynix immediately to secure HBM4E sample allocations and understand future supply roadmaps by end of Q3 2026. [R&D;] Begin designing next-gen AI chips to fully exploit HBM4E's specifications by Q4 2026.

Deep Dive ③ — US Advanced Packaging: TSMC & Amkor Deal

#14 | 2026/06/16 | Bignewsnetwork | Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●●

TSMC and Amkor have signed a 10-year strategic agreement to expand semiconductor packaging capabilities in Arizona, USA. Amkor plans a $7 billion investment in its Peoria, Arizona facility to boost CoWoS supply and build out the US domestic semiconductor ecosystem.

This partnership focuses on cutting-edge packaging technologies like TSMC's InFO and CoWoS, critical for AI, HPC, and automotive. It aims to alleviate the CoWoS bottleneck and align with US government policies for domestic semiconductor manufacturing resilience.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The 10-year deal and $7B investment are highly credible, driven by US CHIPS Act incentives and strategic supply chain diversification. Key barriers include securing a skilled workforce in Arizona and ensuring cost competitiveness against established Asian hubs. [Opportunity] for US OEMs and government agencies to gain a more secure, geographically diversified, and domestic advanced packaging supply chain, reducing geopolitical risks. Amkor (a US company) significantly strengthens its position. [Threat] for Asian OSATs potentially seeing reduced demand for US-bound advanced packaging, and the higher cost structure in the US could impact overall AI chip pricing. Next actions: [Supply Chain] Re-evaluate advanced packaging sourcing strategies for US-made products and engage Amkor by Q3 2026. [Executive] Continue advocating for sustained government support for domestic semiconductor manufacturing initiatives.

Other Notable Articles

Intel Appoints Former SK hynix CEO Lee Seok-hee as Senior VP of Advanced Packaging to Bolster AI Systems (The Korea Herald)
Tech Novelty●●●○○ Proximity●●●●● Market Impact●●●●○ US/EU Relevance●●●●●

Intel's strategic hire signals aggressive push into advanced packaging, leveraging HBM expertise to challenge TSMC/Samsung.

TSMC Accelerates CoPoS Packaging Development, Standardizing 310x310mm Panel Format; Introduces Glass Core Substrate for CoWoS Towards Late 2028 Mass Production (TrendForce)
Tech Novelty●●●●○ Proximity●●○○○ Market Impact●●●●● US/EU Relevance●●●●●

TSMC's CoPoS panel format and glass substrate integration are critical for next-gen AI, setting future industry standards.

imec Unveils High-Density MIMCAP RF Interposer for D-Band Millimeter-Wave and Sub-THz Applications, Accelerating III-V Chiplet Integration (imec)
Tech Novelty●●●●● Proximity●○○○○ Market Impact●●●○○ US/EU Relevance●●●●●

imec's breakthrough in RF interposers and III-V chiplet integration is vital for future 6G and high-speed data center links.

KAIST Develops Breakthrough Liquid Cooling Technology to Shatter AI Semiconductor Thermal Bottleneck (Mirage News)
Tech Novelty●●●●● Proximity●●○○○ Market Impact●●●●○ US/EU Relevance●●●●○

KAIST's liquid cooling offers a scalable solution to AI chip thermal bottlenecks, potentially integrating into existing fabs.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [R&D;] Evaluate SK Hynix HBM4E sample specifications for compatibility with next-generation AI accelerator designs.
- [Strategy] Begin assessing the long-term impact of glass core substrates on current advanced packaging roadmaps and material sourcing.
- [Procurement] Review current CoWoS/advanced packaging allocations and future demand projections against easing supply constraints.

Short-term (1 month)

- [Supply Chain] Initiate discussions with Amkor on US advanced packaging capacity and lead times for 2027+ to secure domestic supply options.
- [R&D;] Investigate KAIST's breakthrough liquid cooling technology for potential integration into high-density AI packages.
- [Executive] Analyze Intel's strategic hiring in advanced packaging and its implications for the competitive landscape and partnership opportunities.

Medium-long term (quarter+)

- [R&D;] Establish internal R&D; programs or external partnerships for glass substrate material and process development, targeting 2030 HVM.
- [Strategy] Develop a diversified advanced packaging supply chain strategy, including regional options (US, EU, Asia) to mitigate geopolitical risks.
- [Legal/IP] Monitor IP developments in advanced packaging, especially for glass substrates, novel cooling solutions, and III-V chiplet integration.

Semiconductor_BackEnd — Selected Articles

Date: 2026-06-20

Articles: 37

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#11 Park Systems and imec Partner to Develop Advanced Metrology Solutions for Next-Gen 3D Packaging and Logic Research

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#32 Samsung Considers New HBM-Focused Advanced Semiconductor Packaging Plant in South Korea's Honam Region to Meet AI Server Demand

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Samsung, SK Hynix Eye Honam Region in South Korea for First Advanced Packaging Fabs Amid Soaring AI Memory Demand; Amkor Plans $980M Expansion

Published June 14, 2026 The Elec Inc. South Korea

OVERVIEW

Samsung Electronics and SK Hynix are considering establishing their first advanced semiconductor packaging plants in South Korea's Honam region to meet surging AI infrastructure demand. Samsung is weighing Gwangju and Saemangeum, while SK Hynix is looking at Gwangju or Muan as potential sites. This move is complemented by Amkor Technology's existing Gwangju ecosystem, with Amkor planning a $980 million investment by 2035 to add 1,000 jobs, addressing HBM packaging capacity shortages and aligning with government regional development policies.

IN DEPTH

Key Findings

Samsung Electronics and SK Hynix are actively exploring the establishment of new advanced semiconductor packaging (back-end) facilities in South Korea's Honam region. This strategic initiative aims to address the explosive growth in AI infrastructure demand, particularly for high-bandwidth memory (HBM), and to bolster the companies' competitive edge in the global semiconductor supply chain. The Honam region, including Gwangju, already benefits from an established ecosystem of outsourced semiconductor assembly and test (OSAT) providers like Amkor Technology, which itself plans to invest approximately $980 million in its Gwangju plant by 2035, creating 1,000 new jobs.

Technical & Economic Details

Samsung is considering Gwangju and Saemangeum, while SK Hynix is evaluating Gwangju or Muan as potential locations for their new packaging facilities. While official investment figures remain undisclosed, the combined investment is projected to be in the realm of $1 billion. The Honam region's appeal stems from its advantageous infrastructure, including relatively affordable land, abundant water resources crucial for semiconductor manufacturing, and stable power supply. Leveraging Amkor's existing presence, these new investments are expected to significantly strengthen the regional semiconductor industry cluster, fostering synergies and technological advancements.

Background & Context

Advanced packaging technologies, such as those integrating logic and HBM chips, are critical enablers for next-generation AI processors. Currently, packaging capacity, particularly TSMC's CoWoS, represents a significant bottleneck in AI chip supply chains globally, driving urgent expansion efforts across the industry. The South Korean government's policy of balanced regional development also plays a role, as these investments align with national objectives to distribute industrial growth beyond traditional hubs. This domestic expansion is anticipated to enhance the resilience of Korea's semiconductor ecosystem against external supply chain disruptions.

Outlook

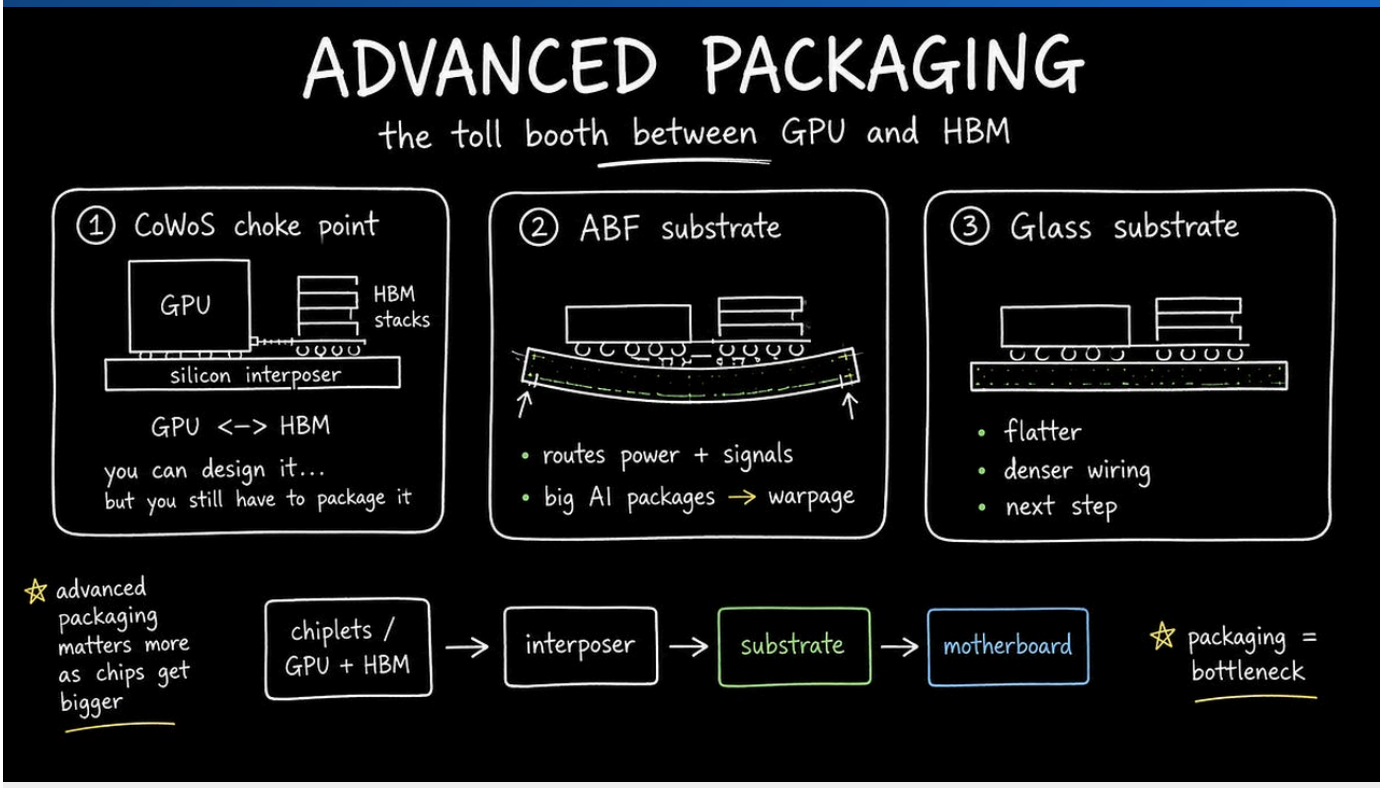
The realization of these investments in the Honam region would solidify South Korea's leadership in the AI semiconductor market. The expanded packaging capacity, coupled with Amkor's contributions, will be vital for accelerating global AI infrastructure build-out. Economically, the initiative is poised to generate substantial employment opportunities and attract ancillary industries to the region. Furthermore, the focus on leveraging local infrastructure, including potential for renewable energy, hints at a broader commitment to sustainable manufacturing practices within the advanced packaging sector.

Source: https://www.thelec.net/news/articleView.html?idxno=11312

Collected: June 19, 2026 | Automated Research System (Gemini API)

Advanced Packaging: Glass Core Substrates Emerge as Next-Gen Frontier; Intel Commits Over $1 Billion to R&D for High-Volume Production by 2030

Published June 13, 2026 Infra Startups USA



OVERVIEW

Advanced packaging is a critical bottleneck in the AI boom, with TSMC's CoWoS capacity dictating the pace of global AI infrastructure build-out. Shipments of CoWoS wafers are projected to reach approximately 40,000 per month by late 2024, escalating to 75,000 in 2025. Glass core substrates are emerging as the next physical frontier for advanced packaging, prompting Intel to invest over $1 billion in its Arizona glass R&D line, targeting high-volume production between 2026 and 2030.

IN DEPTH

Key Findings

The explosive growth of AI and the consequent demand for high-performance chips have positioned advanced packaging as a decisive bottleneck in the semiconductor supply chain. Currently, TSMC's CoWoS (Chip on Wafer on Substrate) capacity is effectively dictating the pace of global AI infrastructure development. However, a next-generation technology poised to break this bottleneck—glass core substrates—is gaining significant traction. Intel is already making strides to lead this domain, investing over $1 billion in its Arizona-based glass R&D line, with ambitions for high-volume production between 2026 and 2030.

Technical & Economic Details

TSMC's CoWoS technology is essential for integrating multiple HBM (High Bandwidth Memory) stacks and logic dies, maximizing the performance of AI accelerators. Its supply remains constrained, with an estimated 40,000 CoWoS wafers shipped per month by the end of 2024, projected to expand to 75,000 per month in 2025. In contrast, glass core substrates offer several technical advantages over traditional organic substrates, including superior dimensional stability, lower coefficient of thermal expansion (CTE), and the ability to fabricate finer wiring patterns. These characteristics promise higher interconnect density, improved power delivery networks, and superior thermal management, expected to push the performance limits of future AI and HPC chips. Intel's investment exceeding $1 billion underscores its commitment to establishing mass production capabilities for glass substrates, aiming to secure long-term market leadership.

Background & Context

The performance enhancement of AI chips increasingly depends not just on transistor count but also on inter-chip and intra-chip data transfer speeds and power efficiency. Advanced packaging serves as a crucial means to address these challenges, and its bottleneck status could potentially limit the growth of the entire AI industry. Glass substrates are being actively researched and developed across the semiconductor industry as a promising solution to these challenges. Intel's strategy involves not only integrating glass substrates into its product roadmap but also driving technological innovation across the supply chain to foster an open ecosystem.

Strategic Significance & Outlook

Intel's substantial investment in glass core substrates and its target for high-volume production by 2026-2030 have the potential to revolutionize the future of semiconductor packaging. As glass substrate technology matures and mass production scales, it is expected to significantly enhance AI chip performance and reduce costs, thereby accelerating the broader adoption of AI technologies. However, persistent challenges such as glass brittleness, the development of scalable Through-Glass Via (TGV) formation processes, and ensuring compatibility with existing supply chains will require continuous R&D and industry-wide collaboration. Glass core substrates are undoubtedly a technology to watch, poised to define next-generation semiconductors in the AI era.

Source: https://www.infrastartups.com/p/advanced-packaging-the-toll-booth

Collected: June 19, 2026 | Automated Research System (Gemini API)

AT&S Unveils €2 Billion Kulim Expansion to Fuel AI Boom with Advanced IC Substrates and PCBs

Published Published June 15, 2026　AT&S Official Press Release　オーストリア

OVERVIEW

AT&S is undertaking a monumental €1.5 billion to €2 billion expansion of its Kulim, Malaysia, manufacturing facility. Driven by long-term commitments from industry leaders like AMD, this investment directly addresses the explosive demand for advanced semiconductor packaging and IC substrates crucial for global AI infrastructure development. The multi-phase project, encompassing new construction and upgrades, is set to significantly bolster AT&S's capacity for high-performance computing and AI applications.

IN DEPTH

Background

The exponential growth of artificial intelligence (AI) is creating unprecedented demand for advanced data processing capabilities, making high-performance substrates and sophisticated packaging technologies indispensable in modern semiconductor design and manufacturing. Malaysia's Kulim Hi-Tech Park, often dubbed one of the nation's 'Silicon Valleys,' plays a critical role in the global semiconductor supply chain. This strategic positioning, coupled with the industry's broader trend towards supply chain diversification, sets the stage for AT&S's significant expansion. Long-term partnerships with leading customers like AMD are pivotal for AT&S to cement its position as a key enabler of the AI era.

Key Findings

AT&S has announced a landmark expansion plan for its Kulim manufacturing site, backed by long-term commitments from key customers including AMD and other technology leaders. This substantial investment, projected to range from €1.5 billion to €2 billion, underscores AT&S's strategic commitment to addressing the surging demand for advanced semiconductor packaging, primarily fueled by the global build-out of AI infrastructure.

The multi-phase expansion will significantly enhance AT&S's production capacity for complex IC substrates and advanced packaging solutions vital for high-performance computing (HPC) and AI applications. This includes bolstering the capabilities of the already operational Plant 1, undertaking significant renovation of Plant 2's existing structures, and constructing state-of-the-art new manufacturing sites specifically for IC substrate cores and advanced Printed Circuit Boards (PCBs). High-density, reliable substrates are critical for advanced packages integrating AI accelerators and High Bandwidth Memory (HBM), and AT&S is driving technological innovation and process optimization to meet these exacting requirements.

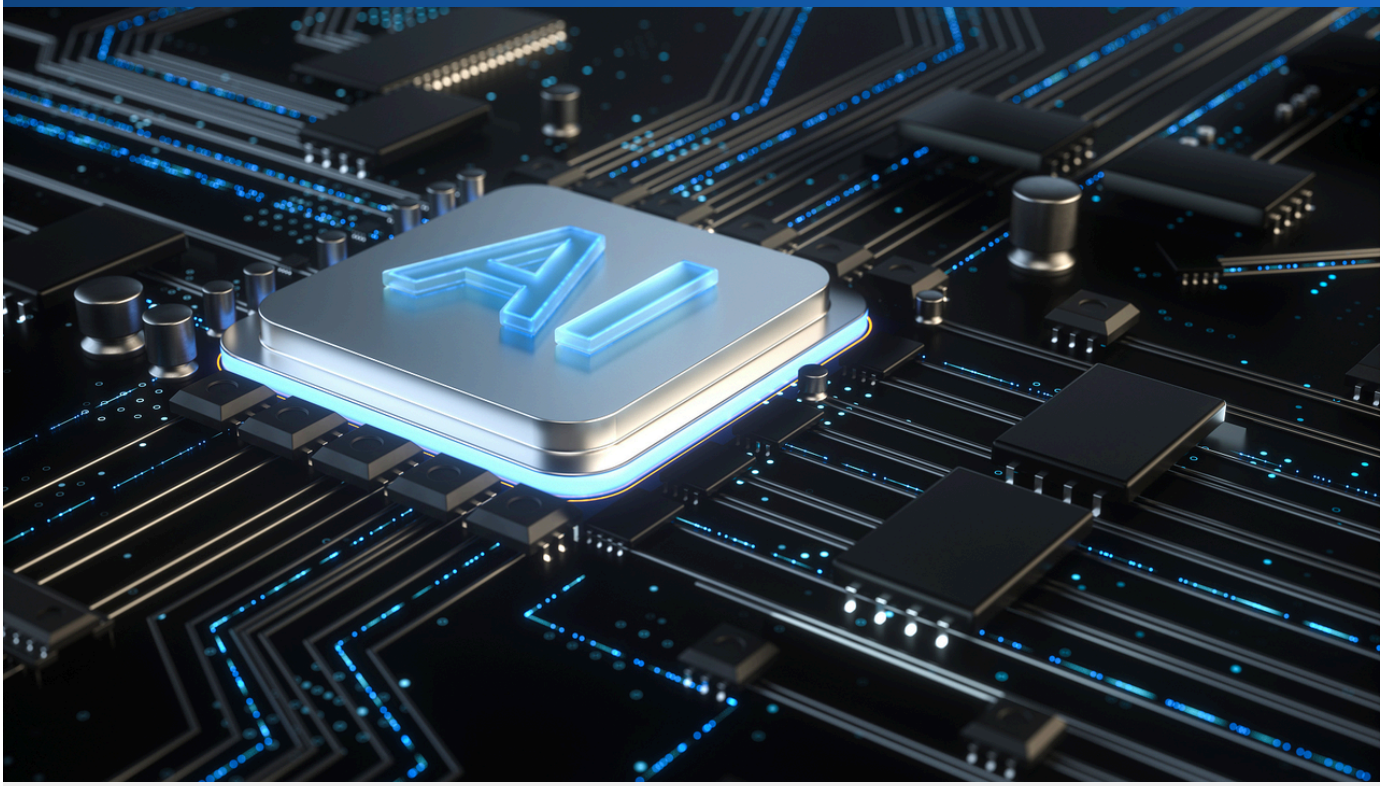
This investment, one of Malaysia's largest foreign direct investments, is expected to have a substantial positive impact on the regional economy. Underpinned by long-term customer contracts, the expansion is set to ensure AT&S's competitive advantage and revenue stability. Strategically, enhanced production capabilities and technological innovations will enable AT&S to maintain its leadership in advanced IC substrates and PCBs, capture new market opportunities in the burgeoning AI and HPC sectors, and further contribute to supply chain resilience. As AI technology continues its rapid evolution, the demand for increasingly complex and higher-performance substrate and packaging solutions will only intensify, solidifying AT&S's critical role in the future of computing.

Source: https://ats.net/en/press/ats-expands-kulim-site-to-support-long-term-customer-demand-and-deepen-strategic-technology-partnerships/

Collected: June 19, 2026 | Automated Research System (Gemini API)

TSMC Narrows CoWoS Supply-Demand Gap from 20% to 10% by End of 2026; NVIDIA to Adopt Next-Gen CoPoS for 2028-2029 Mass Production

Published June 15, 2026 Moomoo Singapore



OVERVIEW

TSMC is accelerating advanced packaging capacity expansion, projecting its CoWoS supply-demand gap to significantly narrow from approximately 20% to 10% by the end of 2026. Concurrently, research and development for its next-generation CoPoS (Chip-on-Panel-on-Substrate) packaging platform are progressing, with NVIDIA's Feynman platform reportedly becoming the first customer for CoPoS, targeting mass production by 2028-2029. TrendForce forecasts TSMC's monthly CoWoS production capacity to reach 120,000-140,000 wafers by 2026.

IN DEPTH

Key Findings

TSMC is aggressively expanding its CoWoS (Chip on Wafer on Substrate) advanced packaging capacity, aiming to significantly reduce the current supply-demand gap of approximately 20% to around 10% by the end of 2026. Simultaneously, the company is making substantial progress in the research and development of its next-generation packaging platform, CoPoS (Chip-on-Panel-on-Substrate). Reports indicate that NVIDIA's Feynman platform is slated to be the first customer to adopt CoPoS, with mass production targeted for 2028-2029, promising to further advance AI chip performance and stabilize supply.

Technical & Economic Details

The projected narrowing of the CoWoS supply-demand gap is attributed to TSMC's massive investments across multiple sites and optimization of its production processes. According to TrendForce, TSMC's monthly CoWoS production capacity is expected to reach 120,000-140,000 wafers by 2026, which will partially catch up with the escalating AI chip demand. CoPoS technology aims for even higher integration density and improved cost efficiency compared to CoWoS by integrating chips on larger substrates (panels). NVIDIA's adoption of CoPoS for its Feynman platform underscores the critical importance of this new technology for high-end AI accelerators. The commercialization of CoPoS is expected to alleviate current CoWoS constraints, enabling the construction of even larger-scale AI systems.

Background & Context

The rapid evolution of AI has dramatically increased the demand for high-performance computing (HPC) chips and High Bandwidth Memory (HBM). The advanced packaging technologies required to integrate these components have become a significant bottleneck in the semiconductor supply chain. TSMC has continuously invested in and innovated its technology to address this bottleneck. The improved CoWoS supply is expected to partially ease the AI chip shortage, accelerating the deployment of AI infrastructure. However, as AI chip performance requirements continue to escalate, the need for even more advanced packaging technologies like CoPoS grows, indicating that the industry may face new bottlenecks down the line.

Strategic Significance & Outlook

The reduction in TSMC's CoWoS supply gap and the introduction of CoPoS will have a profound impact on the AI chip market. In the short term, improved supply stability will accelerate AI hardware deployment and boost the growth of key players like NVIDIA. In the medium to long term, NVIDIA's early adoption of CoPoS could establish this new technology as an industry standard. The mass production of CoPoS has the potential to further enhance AI chip integration and performance, revolutionizing the design of next-generation AI applications and data centers. However, new challenges, such as establishing the CoPoS supply chain and stabilizing yields, are anticipated, making future developments in this area highly anticipated.

Source: https://www.moomoo.com/news/post/71534056/ai-computing-capacity-bottleneck-easing-report-taiwan-semiconductor-s-cowos

Collected: June 19, 2026 | Automated Research System (Gemini API)

TSMC's CoWoS Capacity, Targeting 125K-130K Wafers/Month by 2026, Still Falls Short as Nvidia Reserves 60% of Output

Published June 17, 2026 INDmoney India

OVERVIEW

TSMC's CoWoS advanced packaging remains a hidden bottleneck in AI chip supply, despite targeting 125,000-130,000 wafers per month capacity by the end of 2026. Demand continues to outstrip supply, with TSMC's CEO stating CoWoS capacity is 'very tight and sold out' through 2026. Nvidia has reserved approximately 60% of TSMC's total CoWoS production for 2026, equating to 800,000-850,000 CoWoS wafers, driving advanced packaging prices up 2-4 times faster than the wafers themselves.

IN DEPTH

Key Findings

TSMC's CoWoS (Chip on Wafer on Substrate) advanced packaging technology continues to be a critical, albeit often hidden, bottleneck in the supply of AI chips. Despite the company's aggressive target to reach approximately 125,000-130,000 wafers per month in production capacity by the end of 2026, this expansion is still falling short of the explosive demand for AI chips. TSMC's CEO has explicitly stated that CoWoS capacity for 2026 is "very tight and sold out," underscoring the severe supply constraints. Notably, Nvidia has already reserved a substantial portion—approximately 60%—of TSMC's total CoWoS production for 2026, translating to 800,000-850,000 CoWoS wafers, which has driven advanced packaging prices to increase 2 to 4 times faster than the wafers themselves.

Technical & Economic Details

CoWoS technology enables the high-density integration of multiple logic dies with High Bandwidth Memory (HBM) stacks on a silicon interposer, dramatically boosting the performance and efficiency of AI processors. This technology is indispensable for achieving the high-speed data transfer and power efficiency required for complex AI computations, making it essential for AI chip leaders like Nvidia. Nvidia's strategy of securing a significant portion of TSMC's CoWoS capacity highlights its market dominance and simultaneously reveals the struggle other AI chip developers face in securing adequate supply. Consequently, the rising cost of advanced packaging is increasingly contributing to the overall manufacturing cost of AI chips, directly leading to higher prices for AI hardware.

Background & Context

The rapid evolution of AI has unleashed an unprecedented wave of demand on the semiconductor industry, while simultaneously creating new bottlenecks that traditional manufacturing processes cannot easily address. Advanced packaging is positioned as a new frontier for enhancing semiconductor performance, especially as Moore's Law faces its physical limits. The supply constraints in TSMC's CoWoS capacity directly impact the pace of AI infrastructure deployment and hold significant strategic implications for global AI competition. This situation also motivates competitors like Intel and Samsung to develop and strengthen their own advanced packaging solutions.

Strategic Significance & Outlook

The projection that TSMC's CoWoS supply constraints will persist through 2026 indicates that the supply-demand balance in the AI chip market remains volatile. Nvidia's continued securing of major CoWoS capacity will likely sustain its AI accelerator product dominance. However, supply limitations and rising costs could also slow down the development and deployment of broader AI applications. In the long term, while TSMC expands CoWoS capacity, the transition to next-generation packaging technologies like CoPoS, along with alternative solutions from Intel and Samsung, could contribute to diversifying and stabilizing the AI chip supply chain. The industry will continue to pursue innovation across all aspects of materials, equipment, and processes to resolve this critical bottleneck.

Source: https://www.indmoney.com/blog/us-stocks/tsmc-cowos-bottleneck-ai-chip-supply-squeeze-explained

Collected: June 19, 2026 | Automated Research System (Gemini API)

ABF Substrates Become AI Accelerator Bottleneck, Nvidia's H100 Requires 12+ Layers; Glass Substrates Emerge as Next-Gen Solution, Commercialization Years Away

Published June 14, 2026 Data Gravity USA

OVERVIEW

Ajinomoto Build-up Film (ABF) substrates are a critical component and growing bottleneck in AI accelerators, HBM, and chiplet-based designs. Nvidia's H100 GPU demands over 12 layers of ABF, with the Blackwell B200 using CoWoS-L as one of the largest packages in production history. Glass substrates are seen as a promising solution to ABF's 'warpage wall,' offering finer via density and superior dielectric properties, though high-volume manufacturing requires new equipment, process qualification, and supply chain infrastructure, still several years away.

IN DEPTH

Key Findings

Ajinomoto Build-up Film (ABF) substrates, essential components in AI accelerators, High Bandwidth Memory (HBM), and chiplet-based designs, have emerged as a new bottleneck in semiconductor packaging. Nvidia's high-performance H100 GPU requires over 12 layers of ABF due to its complex architecture, and the next-generation Blackwell B200, utilizing CoWoS-L, is positioned as one of the largest packages ever produced. A promising next-generation technology to address ABF challenges is glass substrates. Glass substrates are expected to resolve the primary 'warpage wall' issue of ABF, offering finer via density and superior dielectric properties, but mass production is anticipated to be several years away.

Technical & Economic Details

ABF substrates enable multilayer wiring and fine circuit formation, supporting high-density chip integration and high-speed signal transmission. However, warpage and dimensional stability issues during manufacturing are becoming increasingly severe, especially for the larger and more multilayered AI chip packages. State-of-the-art GPUs like Nvidia's H100 and Blackwell B200 require massive transistor counts and HBM integration, necessitating extremely precise and complex ABF substrates. Glass substrates, with their superior mechanical strength and thermal stability, significantly reduce warpage problems compared to traditional organic ABF substrates. They also allow for finer Through-Glass Vias (TGVs) and wiring, along with excellent dielectric properties that reduce electrical signal loss. However, mass production of glass substrates requires dedicated manufacturing equipment development, stringent process qualification, and the establishment of new supply chain infrastructure, all of which demand substantial investment and time.

Background & Context

The explosive growth of AI is imposing unprecedented demands on the semiconductor industry. Specifically, advanced packaging, which tightly integrates HBM and logic chips, has become one of the most critical factors determining the performance of AI accelerators. The supply shortage and technological limitations of ABF substrates are impacting the overall production capacity of AI chips, driving a widespread search for solutions within the industry. Against this backdrop, major semiconductor companies, including Intel, are positioning glass substrate technology as key to next-generation packaging and are actively pursuing R&D and investment. Glass substrates have the potential to further advance chiplet technology and enable the realization of higher-performance heterogeneous integration packages.

Strategic Significance & Outlook

Glass substrate technology holds immense potential to resolve the major bottlenecks posed by ABF substrates and dramatically enhance the performance of AI accelerators and HPC (High-Performance Computing) chips. As companies like Intel invest heavily in glass substrates, technological development and supply chain establishment for mass production will accelerate. However, significant challenges remain on the path to commercialization, including the inherent brittleness of glass, the establishment of new manufacturing processes, and improvements in cost efficiency. How glass substrate technology overcomes these hurdles and establishes itself as a mainstream packaging technology in the coming years will be a crucial factor in shaping the development of the semiconductor industry in the AI era.

Source: https://www.datagravity.dev/p/the-abf-substrate-bottleneck

Collected: June 19, 2026 | Automated Research System (Gemini API)

TSMC Strengthens Glass Substrate Supply Chain for CoWoS, Achieving 16% Warpage Reduction for High-Performance AI GPUs

Published June 16, 2026 Wccftech USA

OVERVIEW

TSMC is expanding its glass substrate supply chain for advanced CoWoS packaging, collaborating with Innolux and Ibiden. Glass substrates demonstrate a 16% reduction in package warpage, along with improved thermal expansion, resistance, and inductance, holding significant potential for high-performance computing chips. While suitable for high-end AI GPUs like NVIDIA's Rubin and Blackwell chips, mass production is still considered to be some time away.

IN DEPTH

Key Findings

TSMC is actively working to strengthen its glass substrate supply chain for advanced versions of its CoWoS (Chip on Wafer on Substrate) packaging technology. The company is collaborating with display giant Innolux and Japanese IC substrate manufacturer Ibiden to develop next-generation packaging solutions optimized for high-performance AI GPUs. Glass substrates have demonstrated superior characteristics, including a 16% reduction in package warpage compared to conventional organic substrates, along with improvements in key electrical and thermal properties such as thermal expansion, electrical resistance, and inductance. While this technology holds immense potential to maximize the performance of high-end AI GPUs like NVIDIA's Rubin and Blackwell chips, full-scale mass production is still considered to be a distant prospect.

Technical & Economic Details

The introduction of glass substrates is poised to dramatically improve 'warpage,' a major challenge in advanced packaging. Package warpage poses significant problems in multi-chip stacking and fine interconnect formation, negatively impacting yield and reliability. The low coefficient of thermal expansion and high rigidity of glass substrates are highly effective in mitigating this warpage issue. Furthermore, glass possesses superior dielectric properties compared to organic materials, capable of reducing electrical resistance and inductance in high-speed signal transmission. This enables faster data transfer between HBM (High Bandwidth Memory) and logic dies, while also enhancing power efficiency. TSMC's partnership with Innolux and Ibiden is a strategic move not only for technology development but also for establishing a stable supply system for glass substrates, expected to push the boundaries of design flexibility and performance for next-generation AI accelerators.

Background & Context

The evolution of AI is imposing unprecedented demands on semiconductor chip design and packaging. Specifically, the training and inference of large-scale AI models require immense computational power and data transfer bandwidth, which traditional packaging technologies are increasingly struggling to support. While TSMC's CoWoS has become a de facto standard for HBM-integrated AI chips, further performance enhancements and larger package sizes necessitate innovation in substrate materials. Glass substrates are attracting industry-wide attention as a promising solution to this challenge, with Intel also intensifying its investments in this technology. This competitive drive is a significant force pushing the limits of semiconductor performance in the AI era.

Strategic Significance & Outlook

TSMC's leadership in strengthening the glass substrate supply chain will have a profound impact on the future of high-performance AI GPUs. The tangible achievement of a 16% reduction in warpage clearly demonstrates the superior advantages of glass substrates over conventional organic alternatives. If NVIDIA's next-generation chips adopt glass substrates, AI accelerator performance is poised to reach new levels. However, significant technical challenges remain for mass production, including glass processing technologies, Through-Glass Via (TGV) formation, and compatibility with existing semiconductor manufacturing equipment. If these challenges are overcome and cost-effective mass production is established, glass substrates could become a mainstream advanced packaging technology, redefining computing performance in the AI era.

Source: https://wccftech.com/tsmc-bets-on-glass-for-cowos-as-silicon-mimicking-thermals-beat-organic-substrates-yet-mass-production-stays-distant/

Collected: June 19, 2026 | Automated Research System (Gemini API)

Henkel Expands Electronics Materials Investment in Korea, Bolstering HBM Packaging Material Development for Surging AI Semiconductor Demand

Published June 17, 2026 The Elec Inc. South Korea

OVERVIEW

German materials giant Henkel is expanding its investment in the electronics materials business in South Korea to meet the escalating demand for AI semiconductors. This includes reinforcing R&D personnel and strengthening technological capabilities. The company is developing packaging materials for next-generation High Bandwidth Memory (HBM), supplying key semiconductor packaging materials such as die attach paste, underfill materials, non-conductive pastes/films, encapsulants, and thermal interface materials (TIMs).

IN DEPTH

Key Findings

Henkel, a leading German chemical company, has announced a significant expansion of its electronics materials business in South Korea, in response to the rapid growth of the AI semiconductor market and the consequent increase in demand for advanced packaging materials. This strategic reinforcement includes boosting research and development (R&D) personnel and further enhancing cutting-edge technological capabilities. Specifically, the company is focusing on developing essential packaging materials for next-generation High Bandwidth Memory (HBM), playing a crucial role in supplying key semiconductor packaging materials such as die attach paste, underfill materials, non-conductive pastes/films, encapsulants, and thermal interface materials (TIMs).

Technical & Economic Details

The performance of AI chips heavily relies on advanced packaging technologies that densely integrate multiple chiplets, including logic dies and HBM stacks. High-performance materials are indispensable for securely connecting these components and efficiently managing the heat generated during operation. Henkel's HBM packaging materials are designed to address the following technical challenges: 1. Die attach pastes provide robust connections between chips and substrates, offering excellent thermal conductivity. 2. Underfill materials mitigate stress caused by thermal expansion coefficient mismatches between the chip and package, enhancing connection reliability. 3. TIMs maximize heat transfer from the chip to the heatsink, preventing AI chip overheating. These materials are critical for ensuring the long-term reliability and performance of chips in HBM's multi-layer stack structures and advanced packaging solutions like CoWoS. Henkel's investment aims to expand the supply capacity of these high-performance materials and maintain technological leadership.

Background & Context

The AI revolution is explosively increasing demand for high-performance servers in data centers and AI inference processing in edge devices. This has made advanced packaging technologies, which integrate advanced memory like HBM with AI processors, a bottleneck in the semiconductor supply chain, leading to a surge in demand for related materials. South Korea, home to major HBM manufacturers like Samsung Electronics and SK Hynix, has become a central hub in the advanced semiconductor supply chain. Henkel's expanded investment in South Korea is a strategic move to address this growing market and deepen collaboration with key customers. In the global semiconductor materials market, the stable supply of high-performance materials is crucial for the overall development of the AI industry.

Strategic Significance & Outlook

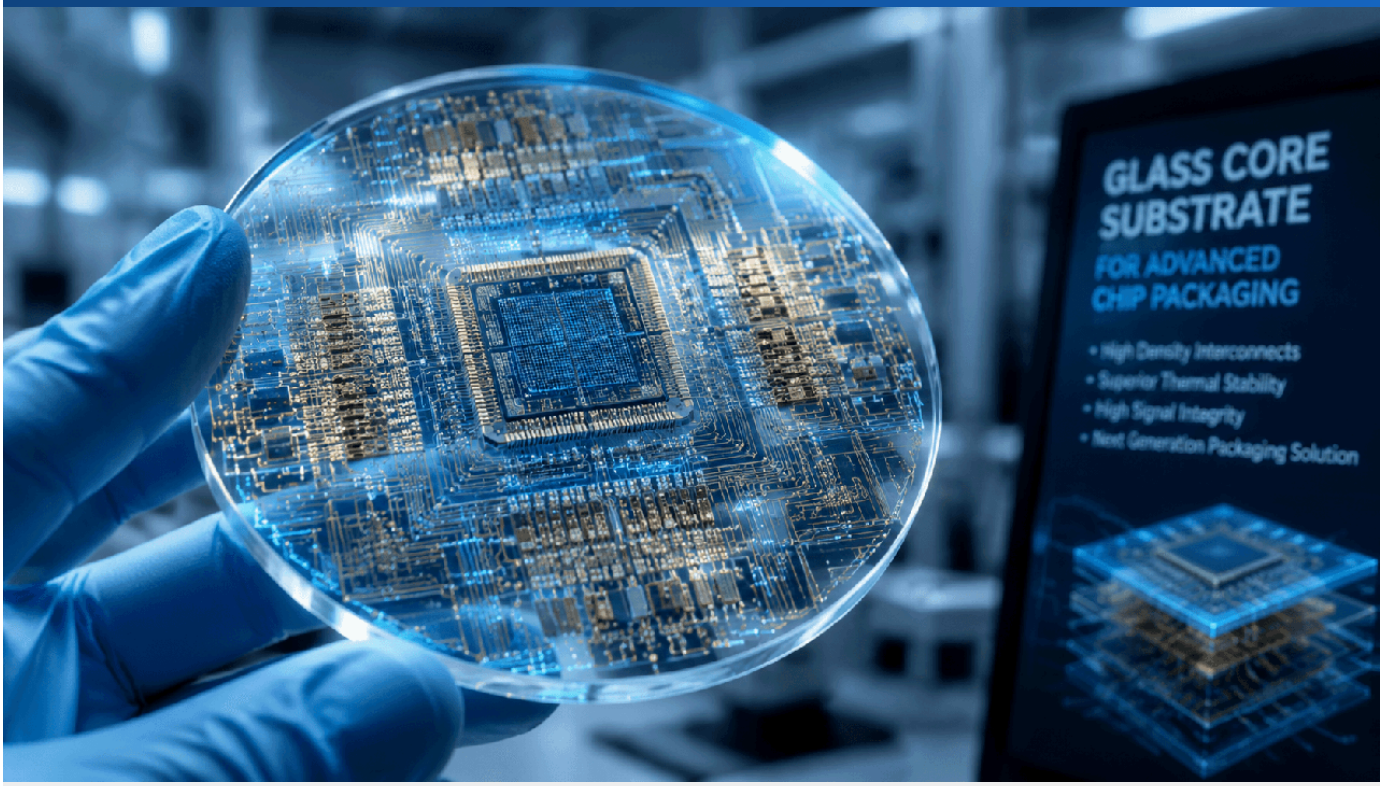
Henkel's expanded investment in its electronics materials business in South Korea will play a significant role in supporting the sustained growth of the AI semiconductor market. Particularly, technological innovation and strengthened supply capabilities for HBM packaging materials will accelerate the development and mass production of next-generation AI accelerators. The company's high-performance materials will directly contribute to improving the reliability, performance, and power efficiency of AI chips, thereby fostering the broader adoption of AI technologies. Moving forward, as AI technology continues to evolve, the demand for even more sophisticated packaging materials is expected to grow, making the role of material manufacturers like Henkel increasingly strategic.

Source: https://www.thelec.net/news/articleView.html?idxno=11397

Collected: June 19, 2026 | Automated Research System (Gemini API)

Glass Core Substrates Emerge as Next-Gen AI/HPC Packaging Technology, Face Commercialization Hurdles in Brittleness and TGV Formation

Published June 14, 2026 Pandaily China



OVERVIEW

Glass core substrates are garnering significant attention in the semiconductor packaging industry, driven by escalating performance demands in AI chips, HPC, and advanced processor packaging. They offer superior dimensional stability, a lower coefficient of thermal expansion, and enhanced electrical performance at finer line widths compared to traditional organic substrates. However, mass production faces several challenges, including glass brittleness, developing scalable Through-Glass Via (TGV) formation processes, and establishing robust supply chain infrastructure.

IN DEPTH

Key Findings

Glass core substrates are emerging as a critically important technology in the semiconductor industry, driven by the surging demand for higher performance in AI chips, High-Performance Computing (HPC), and next-generation advanced processor packaging. This innovative substrate offers distinct advantages over conventional organic substrates, including superior dimensional stability, a significantly lower coefficient of thermal expansion (CTE), and enhanced electrical performance at finer line widths. However, widespread mass production still confronts several technical and manufacturing hurdles, notably the inherent brittleness of glass, the development of scalable Through-Glass Via (TGV) formation processes, and the establishment of the necessary supply chain infrastructure.

Technical & Economic Details

One of the most salient advantages of glass core substrates is their excellent dimensional stability. This is crucial for improving alignment accuracy between chips and substrates in increasingly larger and multi-layered advanced packages, thereby boosting manufacturing yield. Furthermore, glass's CTE closely matches that of silicon, which helps mitigate stress caused by thermal expansion mismatches between the chip and substrate, enhancing package reliability. Glass also exhibits superior dielectric properties, reducing electrical losses in high-frequency signal transmission and enabling finer line widths and via pitches, which is advantageous for improving data transfer rates between HBM (High Bandwidth Memory) and logic dies. However, to fully harness these benefits, it is essential to develop manufacturing processes that address glass brittleness and establish high-throughput, reliable TGV formation technology. TGVs are electrical interconnections passing through the glass substrate, and their miniaturization and reliability improvement are key to mass production.

Background & Context

The evolution of AI and HPC applications demands pushing the integration density and performance of semiconductor chips to their limits. Traditional organic substrates are increasingly struggling to meet these requirements in terms of their thermal, electrical, and mechanical properties. Especially with the proliferation of chiplet technology, there is a strong demand for new substrate materials that can precisely integrate multiple chiplets and efficiently dissipate heat. Glass core substrates are one of the most promising solutions to this challenge, with many companies, including industry giants like Intel, TSMC, and Samsung, accelerating their R&D and investments. This places the semiconductor packaging industry at the cusp of a new materials revolution.

Strategic Significance & Outlook

While glass core substrates hold great potential for the future of semiconductor packaging, their commercialization requires significant technological breakthroughs and large-scale infrastructure investments. Key challenges remain in overcoming glass brittleness, developing technologies to ensure high yield across the entire manufacturing process, and establishing cost-effective TGV formation techniques. If these hurdles are overcome, glass core substrates could become a mainstream technology for packaging AI chips, HPC processors, and next-generation mobile devices, bringing new dimensions to semiconductor performance and functionality. Over the next few years, accelerated progress toward the mass production of glass core substrates is expected through industry-wide collaboration and innovation.

Source: https://pandaily.com/glass-core-substrate-chip-packaging-commercialization-jun2026

Collected: June 19, 2026 | Automated Research System (Gemini API)

ASE Technology Raises 2026 LEAP Revenue Outlook Above $3.5 Billion, Driven by Soaring AI Advanced Packaging Demand

Published June 12, 2026 Zacks USA

OVERVIEW

ASE Technology Holding expressed strong confidence in its Leading Edge Advanced Packaging (LEAP) business trajectory, raising its 2026 LEAP revenue outlook by 10% to over $3.5 billion. This upward revision explicitly reflects higher-than-anticipated demand for advanced packaging and test services linked to AI applications. ASE plans an additional $600 million in CapEx, with a majority allocated to LEAP-related wafer sorting capacity.

IN DEPTH

Key Findings

ASE Technology Holding has announced a significant upward revision to its 2026 Leading Edge Advanced Packaging (LEAP) revenue outlook, now projecting over $3.5 billion, a 10% increase from previous forecasts. This substantial revision underscores the exceptionally strong and growing demand for advanced packaging and test services, which has exceeded initial expectations due to the rapid proliferation of AI applications. To meet this escalating demand, ASE plans to inject an additional $600 million in capital expenditure for machinery and equipment, with the majority of this investment earmarked for strengthening LEAP-related wafer sorting capacity.

Technical & Economic Details

The LEAP business unit provides essential high-density integration packaging technologies, similar to CoWoS (Chip on Wafer on Substrate), and comprehensive test solutions critical for AI accelerators and High-Performance Computing (HPC) chips. These technologies are vital for efficiently integrating multiple logic dies and HBM (High Bandwidth Memory), enabling high-speed data transfer and superior power efficiency. The upward revision in revenue forecasts suggests that the advanced packaging bottleneck in AI chip manufacturing remains severe, and ASE has established itself as a pivotal supplier in this domain. The additional $600 million in capital investment, particularly targeting wafer sorting capacity, aims to enhance efficiency and throughput in the initial stages of the advanced packaging process, thereby boosting overall production capacity and market responsiveness.

Background & Context

The AI revolution is driving structural changes in the semiconductor industry, where traditional scaling technologies are nearing their limits for performance improvement. Consequently, advanced packaging, including chiplet technology and 3D stacking, is emerging as a key enabler for next-generation semiconductor performance. As AI chip designs become more complex and HBM integration increases, the demand for highly precise and reliable packaging and testing grows exponentially. ASE Technology strategically identified this market trend early on, making significant investments to secure its position as an indispensable player in the AI era supply chain. The company's success clearly demonstrates that advanced packaging has become a new growth engine for the semiconductor industry.

Strategic Significance & Outlook

The sustained growth of ASE Technology's LEAP business and its aggressive capital investments are set to strongly support the evolution and proliferation of AI applications. The 2026 revenue forecast exceeding $3.5 billion indicates that the company will further expand its crucial role in the AI chip supply chain. Moving forward, as AI technology permeates diverse industrial sectors, demand for higher-performance and more diverse advanced packaging solutions is expected to intensify. ASE aims to capitalize on this growth opportunity, driving long-term enterprise value through technological innovation and enhanced production capacity. This trend will accelerate AI hardware development and significantly influence global technological competition.

Source: https://www.tradingview.com/news/zacks:283b6e75a094b:0-asx-expects-over-3-5b-in-leap-revenues-in-2026-is-more-growth-ahead/

Collected: June 19, 2026 | Automated Research System (Gemini API)

Park Systems and imec Forge Alliance for Next-Gen 3D Packaging and Logic Metrology

Published Published June 15, 2026　imec Official Press Release　ベルギー

OVERVIEW

Nano-metrology leader Park Systems has launched a two-year Joint Development Program (JDP) with imec, a global semiconductor research powerhouse. The partnership focuses on creating cutting-edge metrology solutions critical for next-generation 3D advanced packaging and logic chip manufacturing. Through imec's 3D System Integration IIAP, Park Systems will access imec's advanced samples, accelerating the development of these vital inspection technologies.

IN DEPTH

Background

The relentless pace of innovation in Artificial Intelligence (AI), High-Performance Computing (HPC), and the Internet of Things (IoT) is driving unprecedented demands for enhanced performance and integration density in semiconductor chips. As conventional two-dimensional scaling approaches encounter fundamental physical and economic limitations, 3D advanced packaging technology has rapidly emerged as a critical new frontier for the semiconductor industry. However, the intricate manufacturing processes of these vertically stacked 3D structures introduce significant complexities, where precise metrology often becomes a critical bottleneck, impeding yield and progress. imec, a global leader in nanoelectronics research, plays a pivotal role in charting the semiconductor industry's future roadmap. This strategic partnership with Park Systems is designed to directly address and overcome these pressing 3D packaging challenges through advanced metrology innovation, ultimately enhancing the efficiency and quality of next-generation semiconductor manufacturing.

Key Findings

Park Systems, a recognized innovator in nano-metrology technology, has initiated a significant two-year Joint Development Program (JDP) with imec, the globally acclaimed semiconductor research and innovation hub. The core objective of this strategic alliance is the collaborative development of highly advanced metrology solutions, which are deemed indispensable for the fabrication of next-generation 3D advanced packaging and logic chips. Critically, as an integral member of imec's Industrial Affiliation Program (IIAP) for 3D System Integration, imec will furnish Park Systems with proprietary samples derived from its cutting-edge 3D packaging and logic roadmaps, providing crucial real-world data to accelerate validation and optimization efforts.

Technical & Economic Details

3D advanced packaging technology represents a paradigm shift, vertically integrating multiple semiconductor dies to achieve superior data transfer speeds, significantly reduce power consumption, and drastically shrink the overall chip footprint. Nevertheless, this inherently intricate multi-layer architecture is exquisitely sensitive to even minute defects and critical dimensional variations introduced during the complex manufacturing sequence. This sensitivity underscores the absolute necessity of high-precision metrology. Park Systems' proprietary Atomic Force Microscopy (AFM) technology, renowned for its capability to measure surface topography with sub-nanometer accuracy, is uniquely positioned to critically evaluate minute die-to-die misalignments, assess inter-die bonding quality, and characterize critical material properties within these complex 3D stacks. The provision of imec's advanced samples will be instrumental, enabling Park Systems to rigorously validate and extensively optimize its metrology platforms under conditions that closely replicate authentic semiconductor manufacturing environments. This synergistic development is anticipated to directly translate into tangible improvements in yield and significantly enhanced reliability for 3D packaging, thereby de-bottlenecking and accelerating the mass production of next-generation semiconductors.

Strategic Significance & Outlook

This joint development program between Park Systems and imec is poised to exert a decisive influence on the future trajectory of metrology technology for next-generation semiconductor manufacturing. The anticipated advanced metrology solutions will be foundational for optimizing the design, manufacturing processes, and stringent quality control protocols essential for 3D advanced packaging and logic chips. Ultimately, this will significantly accelerate the high-volume production of critical components such as AI accelerators, High Bandwidth Memory (HBM), and other performance-driven chips, thereby catalyzing innovation across the broader semiconductor ecosystem. The profound insights and technological breakthroughs emerging from this strategic partnership are expected to underpin advancements across a diverse array of high-impact application areas, including autonomous vehicles, hyperscale data centers, and advanced edge AI devices, solidifying a crucial technological foundation for continued global digital transformation.

Source: https://www.imec-int.com/en/press/park-systems-invests-advanced-metrology-portfolio-3d-packaging-and-logic-research

TSMC's CoWoS Shortage Eases, But Bottleneck Shifts to 'Hyper-Scale Packaging' as Google Reportedly Engages Samsung for TPU Production

Published June 15, 2026 Zhitong Finance APP Hong Kong

OVERVIEW

Reports suggest Google is in discussions with Samsung Electronics regarding the production of specific hardware components for its AI training and inference Tensor Processing Units (TPUs), highlighting persistent tightness in TSMC's advanced process AI chip manufacturing and packaging capacity. While TSMC's CoPoS advanced packaging platform is slated for mass production around 2028, the alleviation of the CoWoS shortage is expected to shift the bottleneck to advanced process technology, hyper-scale packaging, glass core substrates, TGVs, and system-level yield economics.

IN DEPTH

Key Findings

Reports indicating Google's potential discussions with Samsung Electronics for the production of specific hardware components for its AI training and inference Tensor Processing Units (TPUs) underscore the continued, severe tightness in TSMC's advanced process AI chip manufacturing and advanced packaging capacity. Simultaneously, while TSMC's next-generation advanced packaging platform, CoPoS (Chip-on-Panel-on-Substrate), is targeted for mass production around 2028, it is anticipated that even with an easing of the CoWoS shortage, the bottleneck will merely shift to more complex challenges. These include advanced process technology itself, hyper-scale packaging, glass core substrates, Through-Glass Vias (TGVs), and the economics of system-level yield.

Technical & Economic Details

High-density advanced packaging like CoWoS is critical for enhancing AI chip performance, but its supply constraints are a major factor slowing the deployment of AI hardware. The reports of Google approaching Samsung for TPU production can be interpreted as a strategic move by a major tech company to diversify its supply chain and reduce reliance on TSMC. Unlike CoWoS's wafer-based approach, TSMC's CoPoS aims for higher integration density and improved cost efficiency by integrating chips on larger panels. However, even when CoPoS enters full mass production around 2028, the true bottlenecks are expected to shift to the manufacturing yield of the extremely miniaturized advanced process nodes themselves, the complexity of hyper-scale packaging integrating multiple large chiplets, and the commercialization and economics of emerging technologies like glass core substrates and TGVs.

Background & Context

The AI revolution has brought unprecedented demand to the semiconductor industry, placing immense pressure on existing supply chains, particularly in AI chip design, manufacturing, and packaging. The shortage of advanced packaging capacity is a significant barrier to the advancement and widespread adoption of AI technology, a problem exacerbated by leading companies like Nvidia securing the majority of TSMC's CoWoS capacity. Companies like Google exploring multiple suppliers reflect not only a need for supply security but also aspects of geopolitical risk diversification and driving technological innovation. Industry-wide, strengthening and diversifying the AI chip supply chain has become an urgent priority.

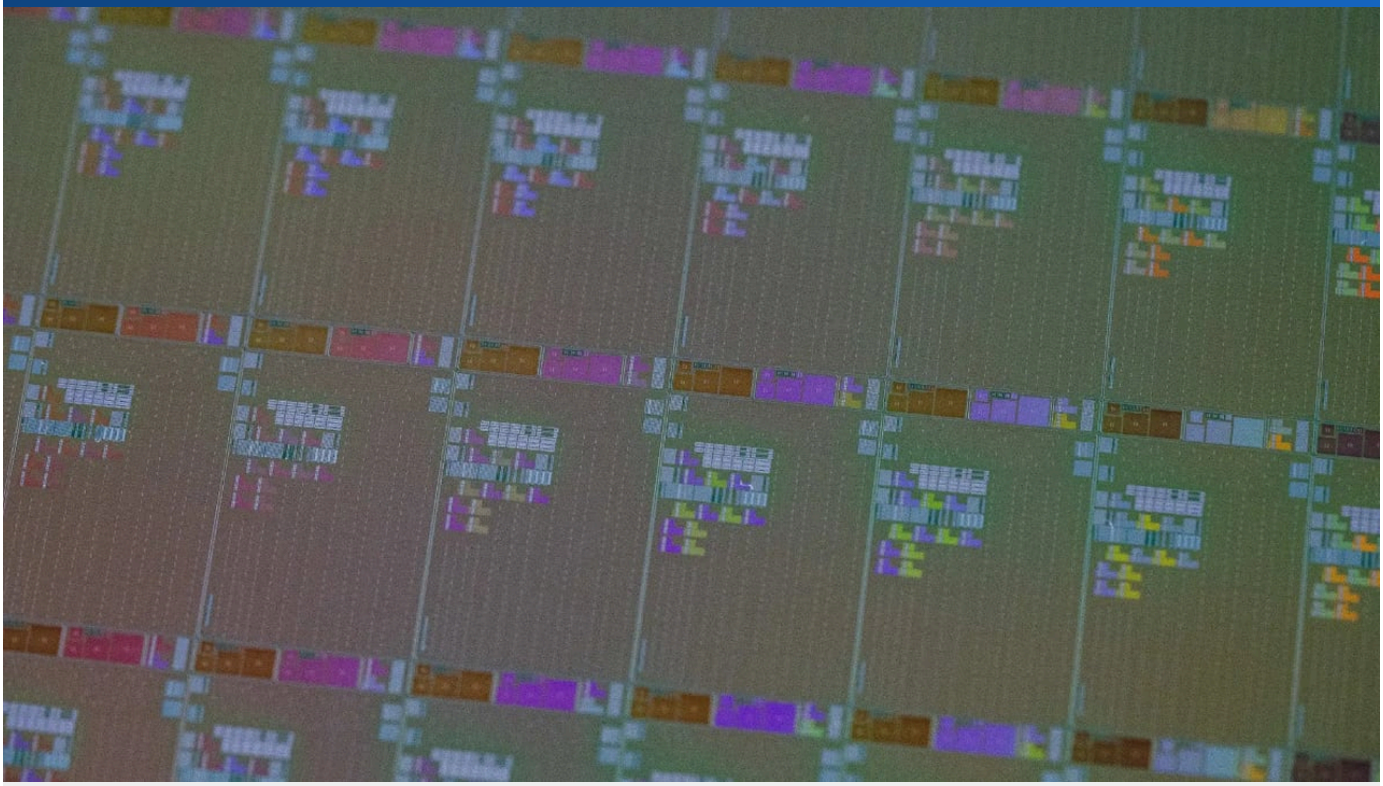
Strategic Significance & Outlook

Even with a partial alleviation of the CoWoS supply shortage, the bottlenecks in AI chip manufacturing are set to transition to more advanced and complex technological challenges. TSMC's CoPoS strategy is a crucial step to meet future AI chip demand and performance requirements, but the maturity of new technologies like glass core substrates and TGVs will take time. The potential collaboration between Google and Samsung could alter the landscape of the AI chip supply chain, potentially shifting the dynamics from a TSMC-dominant situation. Over the next few years, semiconductor manufacturers will be compelled to address a wide range of issues, including improving advanced process technology yields, optimizing hyper-scale packaging, and commercializing new materials and technologies. These challenges will define the new growth trajectory of the semiconductor industry in the AI era.

Source: https://news.futunn.com/en/post/74611332/alleviation-of-the-cowos-shortage-does-not-equate-to-bottleneck

imec Unleashes High-Density MIMCAP RF Interposer for D-Band Millimeter-Wave and Sub-THz Communications, Accelerating III-V Chiplet Integration

Published Published June 15, 2026　imec　ベルギー



OVERVIEW

imec has unveiled a high-density MIMCAP RF interposer specifically engineered for demanding D-band and sub-THz wireless front-ends, alongside hundreds of gigahertz data center links. This innovative platform prioritizes compact passive components, predictable layout behavior, and advanced packaging to seamlessly integrate CMOS, III-V, and photonic dies. The technology is poised to significantly boost performance for next-generation communication systems and high-speed data infrastructure.

IN DEPTH

Key Findings

imec, a global leader in semiconductor research, has unveiled a groundbreaking high-density Metal-Insulator-Metal Capacitor (MIMCAP) RF interposer tailored for advanced high-frequency RF systems. This innovative platform is specifically designed for highly demanding applications such as D-band and above millimeter-wave and sub-terahertz (THz) wireless front-ends, as well as high-speed data center links requiring data transmission at hundreds of gigahertz (GHz). It critically focuses on areas where compact passive components, predictable layout-dependent behavior, and state-of-the-art packaging technology are essential. This enables seamless integration between CMOS, III-V semiconductors, and photonic dies, dramatically boosting the performance of next-generation communication systems.

Technical & Economic Details

The MIMCAP RF interposer facilitates high-density integration while maintaining the integrity of high-frequency signals. MIMCAPs, with their excellent quality factor (Q-factor) and stable capacitance values, are indispensable passive components for impedance matching and filtering in RF circuits. imec's new platform achieves high-density integration of these MIMCAPs on the interposer, significantly reducing the RF system's footprint and improving its power efficiency. For millimeter-wave and sub-THz bands at D-band (110-170 GHz) and beyond, high-precision packaging and interconnect technologies are crucial to minimize signal loss. This interposer has the capability to 'bridge' chiplets fabricated with diverse materials and process technologies—such as CMOS logic, high-performance III-V semiconductors (e.g., GaN, GaAs-based HBTs and HEMTs), and photonic dies for optical signal processing—with high-speed, reliable electrical or optical connections. This allows for extracting optimal performance from each chiplet while reducing overall system complexity.

Background & Context

The realization of next-generation communication systems beyond 5G, particularly 6G and Beyond 5G, critically hinges on the utilization of millimeter-wave and sub-THz bands at D-band and higher. While these frequency bands allow for transmitting vast amounts of data at high speeds, they are characterized by short transmission distances and strong line-of-sight propagation, necessitating high-density, low-loss RF front-ends and antenna technologies. In data centers, the increasing workload from AI and High-Performance Computing (HPC) demands inter-chip communication at hundreds of GHz data rates. Traditional packaging technologies have struggled to effectively integrate multiple heterogeneous chiplets at such ultra-high frequencies. imec's MIMCAP RF interposer offers an innovative solution to these formidable challenges, accelerating the evolution of the communication and data center industries.

Strategic Significance & Outlook

imec's high-density MIMCAP RF interposer technology holds the potential to dramatically enhance the performance of wireless communication systems and high-speed data center links across the D-band millimeter-wave and sub-THz spectrum. The ability to integrate III-V semiconductors with CMOS and photonics will open new avenues for the design of next-generation transceivers, radars, and sensor systems. As this technology advances toward commercialization, it is expected to enable faster, lower-latency wireless communication, leading to revolutionary applications in areas such as autonomous driving, augmented/virtual reality (AR/VR), and terabit-scale data centers. imec's continuous R&D efforts will expedite the market introduction of these technologies, playing a vital role in shaping the future of global digital infrastructure.

Source: https://passive-components.eu/imec-presents-high-density-mimcap-rf-interposer-for-iii-v-chiplets/

Collected: June 19, 2026 | Automated Research System (Gemini API)

TSMC and Amkor Sign 10-Year Advanced Packaging Deal in Arizona, Amkor to Invest $7B for CoWoS Supply Boost and US Ecosystem Build-out

Published June 16, 2026 Bignewsnetwork India

OVERVIEW

TSMC and Amkor have signed a 10-year strategic agreement to expand semiconductor packaging capabilities in Arizona, USA. This partnership focuses on cutting-edge packaging technologies, including TSMC's InFO and CoWoS, critical for demanding applications like AI, HPC, automotive systems, and mobile devices. CoWoS is a major bottleneck in AI chip supply, and Amkor's $7 billion investment in its Peoria, Arizona facility solidifies its position as a key partner in the domestic semiconductor ecosystem.

IN DEPTH

Key Findings

TSMC and Amkor Technology have entered into a landmark 10-year strategic partnership agreement aimed at significantly expanding semiconductor packaging capabilities in Arizona, USA. This long-term contract specifically targets cutting-edge packaging technologies such as TSMC's InFO (Integrated Fan-Out) and CoWoS (Chip on Wafer on Substrate), which are foundational for supporting the most demanding application sectors including AI, High-Performance Computing (HPC), automotive systems, and next-generation mobile devices. Critically, strengthening the supply of CoWoS technology, a primary bottleneck in AI chip supply, is an urgent priority. Amkor's substantial investment of $7 billion in its Peoria, Arizona facility will firmly establish its strategic and indispensable role as a partner within the domestic U.S. semiconductor ecosystem.

Technical & Economic Details

TSMC's InFO and CoWoS technologies are essential for maximizing chip performance and power efficiency by densely integrating multiple logic dies and HBM (High Bandwidth Memory) stacks on a silicon interposer. InFO is a cost-effective, substrate-less fan-out packaging technology widely adopted in mobile devices. CoWoS, on the other hand, offers extremely high integration density and data transfer bandwidth for more complex AI/HPC chips. Amkor's $7 billion investment will build production capabilities for these advanced packaging technologies in Arizona, contributing to the resilience and diversification of the domestic U.S. semiconductor supply chain. This investment is also expected to create thousands of new jobs and significantly boost regional economic development.

Background & Context

The rapid advancement of AI and the increasing demand for supply chain resilience are compelling governments and semiconductor companies worldwide to strengthen domestic manufacturing capabilities, particularly in advanced packaging. The U.S. government, through the 'CHIPS Act,' offers substantial incentives for domestic semiconductor manufacturing, and this partnership between TSMC and Amkor aligns perfectly with these policy objectives. The CoWoS supply shortage is one of the biggest bottlenecks in the current AI chip market, and alleviating this bottleneck is crucial for accelerating AI infrastructure deployment. As a key OSAT partner for TSMC, Amkor's role in U.S. advanced packaging production will bolster America's strategic position in the global semiconductor supply chain.

Strategic Significance & Outlook

The 10-year agreement between TSMC and Amkor will play a decisive role in Arizona's development as a major hub for advanced semiconductor manufacturing and packaging. The expansion of domestic CoWoS production capacity will contribute to stabilizing AI chip supply, accelerating AI technology development and deployment in the U.S. Furthermore, this partnership will foster new technological innovations in advanced packaging and promote the creation of a more resilient and diversified global supply chain. Amkor's role is expected to become even more critical as demand for U.S.-made advanced packaging chips increases in sectors such as automotive, HPC, and defense. This strategic partnership will define the new geopolitics and technological evolution of the semiconductor industry in the AI era.

Source: https://www.bignewsnetwork.com/news/279132343/tsmc-amkor-sign-10-year-deal-to-boost-advanced-chip-packaging-in-us

Collected: June 19, 2026 | Automated Research System (Gemini API)

AI Infrastructure Demand Intensifies Memory Shortage: TSMC CoWoS Constraints and Vietnam Labor Shortages Create Compound Challenges

Published June 15, 2026 Sourceability USA

OVERVIEW

Rising AI infrastructure demand is generating new challenges across the semiconductor supply chain, notably a worsening memory shortage. TSMC's CoWoS packaging limitations are expected to persist with the AI boom. Additionally, labor shortages in Vietnam are cited as a significant impediment to chip investments, highlighting complex issues within the global semiconductor supply chain.

IN DEPTH

Key Findings

The explosive demand for AI infrastructure is imposing widespread new challenges across the entire semiconductor supply chain, with a particularly acute and worsening memory shortage. At the core of this issue lies the persistent constraint in TSMC's CoWoS (Chip on Wafer on Substrate) packaging capacity, which is indispensable for AI chip manufacturing. Furthermore, labor shortages in critical manufacturing hubs like Vietnam are emerging as a significant impediment to new chip investments and production expansion, underscoring the vulnerabilities and complex challenges within the global semiconductor supply network.

Technical & Economic Details

AI chips, particularly Graphics Processing Units (GPUs) and AI accelerators, require High Bandwidth Memory (HBM) and advanced packaging technologies to process vast amounts of data at high speeds. TSMC's CoWoS is essential for efficiently integrating multiple HBM stacks with logic dies, and its limited supply capacity restricts overall AI chip production. As AI models become more complex, the demand for HBM is growing exponentially, making the combination of HBM and CoWoS the current bottleneck for AI chip supply. Additionally, Southeast Asian regions like Vietnam play a crucial role in outsourced semiconductor assembly and test (OSAT), but shortages of skilled labor and infrastructure constraints are hampering new investments and capacity expansions. This indicates that complex challenges arise not only from single technological bottlenecks but also from the interplay of regional labor and infrastructure issues.

Background & Context

The rapid advancement of AI demands unprecedented computational and data processing capabilities across diverse fields, including data centers, edge computing, and autonomous vehicles. While the semiconductor industry is experiencing one of its fastest growth periods in history, it simultaneously faces new bottlenecks across the entire supply chain. Since the COVID-19 pandemic, there has been a strong call for global supply chain resilience and diversification, recognizing the risks of over-reliance on specific technologies or regions. TSMC's CoWoS constraints symbolize this single-point-of-failure risk, and Vietnam's labor shortage exemplifies how geopolitical factors and demographics impact the supply chain.

Strategic Significance & Outlook

The sustained increase in AI demand will continue to exert strong pressure on the semiconductor supply chain. While TSMC is striving to expand CoWoS production capacity, combined with rising demand for advanced memory like HBM, supply constraints are likely to be prolonged. This situation could motivate competitors like Intel and Samsung to develop and strengthen their own advanced packaging solutions, potentially fostering supply chain diversification. Furthermore, labor and infrastructure challenges in regions like Vietnam highlight the necessity for governments and industries to collaborate on accelerating talent development and investment. The AI era's semiconductor supply chain will be tested not only by technological innovation but also by global cooperation and strategic regional investments.

Source: https://sourceability.com/post/ai-demand-consumes-thousands-of-chips-heightening-memory-shortage

Collected: June 19, 2026 | Automated Research System (Gemini API)

Nokia Ramps Up U.S. Advanced Chip Packaging Capacity Tenfold in Pennsylvania to Fuel AI Networks

Published Published June 19, 2026 Cyprus Shipping News キプロス

OVERVIEW

Nokia is significantly expanding its U.S. advanced semiconductor test and packaging operations in Allentown, Pennsylvania, targeting a tenfold increase in domestic production capacity for optical networking technologies critical to AI infrastructure. This strategic investment, part of Nokia's broader $4 billion U.S. R&D and manufacturing commitment, aims to bolster AI-ready networks and address escalating demands from the burgeoning AI era.

IN DEPTH

Background

The explosive growth of Artificial Intelligence (AI) is exerting unprecedented strain on data centers and network infrastructure. Both the training and inference phases of AI models necessitate robust optical networks capable of transmitting massive data volumes at exceptionally high speeds. Concurrently, U.S. policy seeks to reinforce domestic semiconductor production capabilities and reduce reliance on foreign sources for critical technological components. Nokia's investment directly aligns with these strategic national objectives, enhancing its competitiveness in the U.S. market while positioning it as a key domestic manufacturer of critical national security infrastructure.

Key Findings

Nokia has announced a major expansion of its advanced semiconductor test and packaging operations at its Allentown, Pennsylvania facility. This strategic investment aims to bolster AI-ready network infrastructure by increasing domestic production capacity for optical networking technologies, crucial for AI connectivity, by a factor of ten.

Technical and Business Details

- This expansion is a pivotal part of Nokia's multi-year $4 billion investment strategy for U.S. R&D and manufacturing. The Allentown facility will specialize in the advanced testing and packaging of optical networking chips, producing technologies essential for enabling high-speed, low-latency interconnections vital for AI data centers.
- The tenfold increase in production capacity is critical for bolstering U.S. self-sufficiency in infrastructure development, directly addressing the surging AI workloads and data traffic. This initiative is expected to mitigate supply chain risks and accelerate domestic technological innovation.
- Nokia's optical networking technologies are fundamental for efficiently processing the massive data volumes generated by AI systems, which typically rely on AI processors, high-bandwidth memory (HBM), and complex chiplet architectures. Advanced packaging is crucial for miniaturizing and enhancing the performance of these optical modules.

- The investment, estimated to be in the hundreds of millions of dollars, is also projected to create new jobs within Pennsylvania's high-tech sector.

Strategic Significance & Outlook

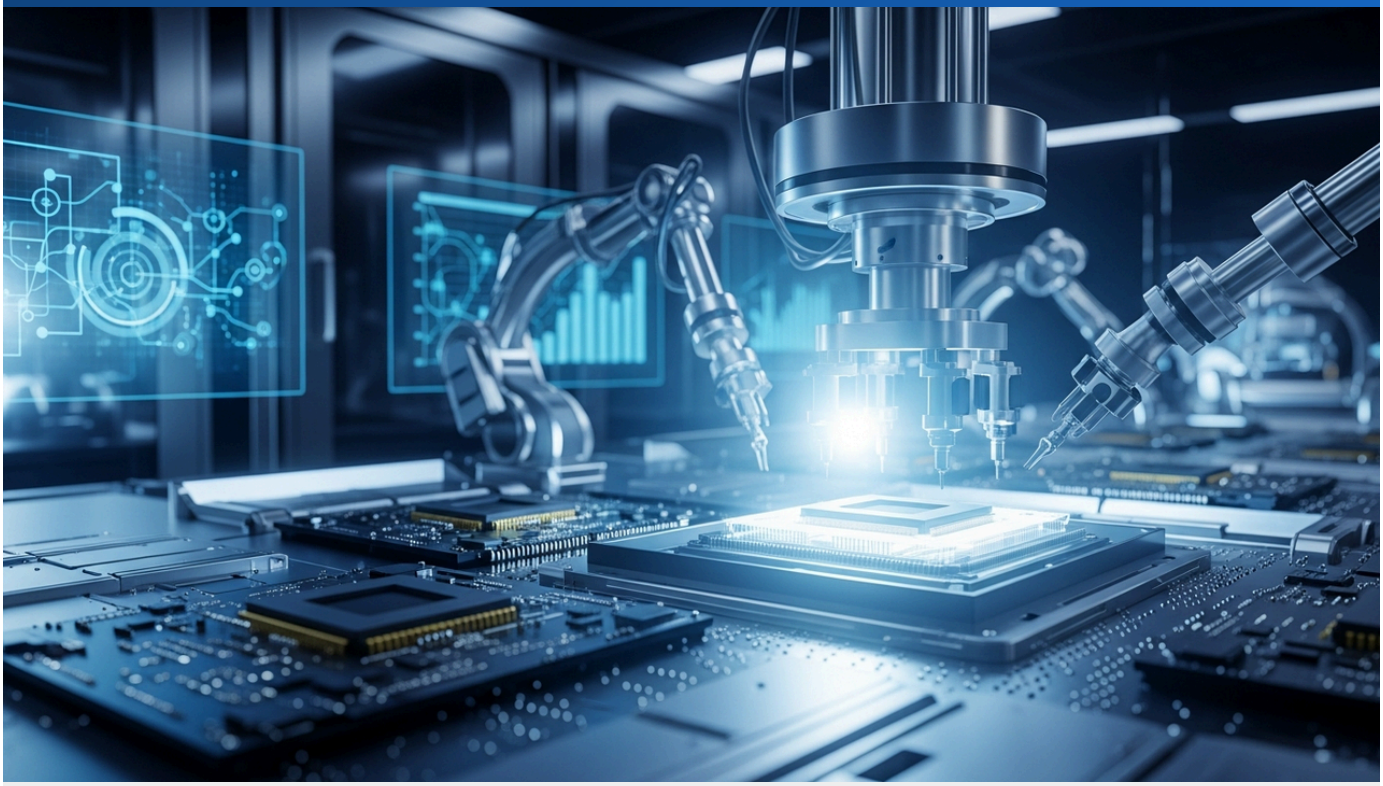
This substantial expansion of the Allentown facility carries significant implications for Nokia's strategy to solidify its leadership in network connectivity for the AI era. The investment will be instrumental in building the requisite infrastructure to support next-generation AI applications and services, thereby accelerating the growth of the U.S. digital economy. Moreover, such significant domestic investments could catalyze similar strategic moves by other telecommunications equipment manufacturers and semiconductor companies.

Source: https://cyprusshippingnews.com/2026/06/19/nokia-announces-major-expansion-of-us-semiconductor-advanced-test-and-packaging-in-pennsylvania-to-bolster-ai-growth/

Collected: June 19, 2026 | Automated Research System (Gemini API)

Malaysia Commits RM185M to Advanced Packaging Consortium, Targeting High-Value AI and HPC Semiconductors

Published Published June 15, 2026　不明　Malaysia



OVERVIEW

Malaysia has initiated the "Malaysia Advanced Packaging Consortium (MAPC)" with a substantial RM185 million (~$39.5M USD) investment, aiming to strategically pivot its semiconductor industry towards higher-value activities. This collaborative effort, involving five key local companies, will accelerate advanced packaging technology development, specifically addressing the escalating demand for AI and high-performance computing (HPC) chips. The consortium is backed by a balanced funding model, combining a RM92 million government R&D grant with RM93 million in industry contributions.

IN DEPTH

Background & Context

The global semiconductor industry is experiencing unprecedented growth, propelled by technological advancements in AI, 5G, and IoT. The explosive increase in demand for AI chips, in particular, has dramatically heightened the need for high-performance, high-density packaging solutions. For many years, Malaysia has been a vital hub for semiconductor back-end processes (assembly, test, and packaging) in the global supply chain. However, a strategic shift towards higher-value segments is imperative for continued growth and enhanced international competitiveness, moving beyond traditional manufacturing to advanced innovation.

The Malaysia Advanced Packaging Consortium (MAPC)

Addressing this strategic necessity, Malaysia has launched the groundbreaking "Malaysia Advanced Packaging Consortium (MAPC)" with a substantial total investment of RM185 million (approximately $39.5 million USD). This initiative aims to pivot the nation's semiconductor industry towards higher-value activities and establish a stronger foothold in advanced manufacturing. The consortium's funding model includes a RM92 million R&D grant from the government and RM93 million in industry contributions.

Technical & Business Details

- The MAPC is formed through the collaborative efforts of five key local companies: Skyechip, FusionAP, Inari, Pentamaster, and NSW Automation. Their collective objective is to accelerate research, development, and adoption of cutting-edge advanced packaging technologies within the country.
- Advanced packaging is a crucial enabling technology for modern high-end semiconductors, including sophisticated AI accelerators and high-performance computing (HPC) chips, offering significant improvements in performance, power efficiency, and chip integration density.
- The government grant has been approved for a 24-month period, during which the consortium is expected to achieve significant technological advancements and drive commercialization in advanced packaging solutions.

Strategic Significance & Outlook

The establishment of MAPC and this substantial investment is anticipated to inject new vitality into Malaysia's technology sector. By spearheading the development and commercialization of advanced packaging technologies, the country is poised to attract greater foreign direct investment and generate high-skilled technical jobs. This initiative represents a crucial step for Malaysia to evolve from a prominent "manufacturing hub" to a leading "technological innovation hub" within the dynamic global semiconductor ecosystem, playing a more significant role in the advanced semiconductor supply chain.

Source: #

TSMC to Halve AI Chip Supply Gap from 20% to 10% by End-2026 with CoWoS Capacity Boost; Next-Gen CoPoS on Track

Published June 15, 2026 TrendForce Taiwan

OVERVIEW

TSMC is projected to halve the AI chip supply-demand gap from approximately 20% to 10% by the end of 2026 through aggressive expansion of its CoWoS advanced packaging capacity. The company's monthly CoWoS production capacity is expected to reach 120,000-140,000 chips by 2026, approaching 200,000 chips including OSAT partners. Furthermore, TSMC is developing its next-generation CoPoS platform to overcome current chip size limitations, with NVIDIA's Feynman platform slated as the first customer for mass production in 2028-2029.

IN DEPTH

Key Findings

TSMC is projected to significantly narrow the AI chip supply-demand gap, reducing it from approximately 20% to around 10% by the end of 2026, through aggressive expansion of its CoWoS advanced packaging capacity. This strategic scaling is vital for meeting the explosive growth in the AI market and alleviating critical bottlenecks in the semiconductor supply chain.

Technical and Business Details

- According to a TrendForce report, TSMC's monthly CoWoS production capacity is anticipated to reach 120,000-140,000 chips by 2026. Including additional capacity from Outsourced Semiconductor Assembly and Test (OSAT) partners, the total monthly capacity is expected to approach 200,000 chips.
- CoWoS (Chip-on-Wafer-on-Substrate) is a 2.5D packaging technology that integrates multiple chips (e.g., GPUs and HBM) on a silicon interposer, indispensable for high-performance AI accelerators. This technology delivers high bandwidth, low latency, and superior power efficiency.
- To overcome current chip size limitations (up to 60x60mm), TSMC is also actively developing its next-generation packaging platform, CoPoS (Chip-on-Package-on-Substrate). CoPoS will enable the integration of larger chips or multiple chiplets, enhancing design flexibility for future AI chips.
- NVIDIA's next-generation AI platform, Feynman, is slated to be the first customer for CoPoS, with full-scale mass production planned for 2028-2029, signaling further leaps in AI chip performance and integration density.
- This capacity expansion creates substantial business opportunities for advanced semiconductor equipment manufacturers (such as Lam Research, Applied Materials, and KLA) and material suppliers (including ABF substrates and glass substrates).

Background & Context

The rapid evolution of AI applications has created unprecedented demand for AI chips, with major AI chip design companies like NVIDIA heavily relying on advanced packaging capabilities such as TSMC's CoWoS. However, demand has significantly outstripped supply, creating a severe bottleneck. TSMC's proactive investments and CoWoS capacity ramp-up are crucial steps to address this supply-demand imbalance and accelerate the growth of the entire AI industry. The development of new technologies like CoPoS demonstrates TSMC's foresight in pushing the boundaries of future AI hardware.

Strategic Significance & Outlook

TSMC's CoWoS capacity expansion and CoPoS development will further accelerate the AI chip market's growth and usher in a new era of high-performance computing. The narrowing supply-demand gap will contribute to greater stability in AI chip supply, meaning AI developers will have more accessible powerful hardware. This is expected to further advance the commercialization and application of AI technologies. Moreover, the mass production of CoPoS will dramatically boost the performance of next-generation AI accelerators, enabling the realization of even more complex and larger-scale AI models.

Source: https://www.trendforce.com/news/2026/06/15/news-tsmc-cowos-supply-demand-gap-reportedly-seen-narrowing-from-20-to-10-by-end-2026-as-capacity-expands/

Collected: June 19, 2026 | Automated Research System (Gemini API)

Semiconductor Engineering June 2026 Report Highlights On-Chip Photonics, Hybrid Bonding, and GaN for AI/HPC

Published June 18, 2026 Semiconductor Engineering USA

OVERVIEW

Semiconductor Engineering's June 2026 issue features on-chip photonics for AI systems, enhanced connectivity via hybrid bonding, new GaN power device designs, and managing manufacturing variations at advanced nodes. Intel Foundry's Lori Scott underscored the role of packaging in redefining AI and HPC scalability, citing advancements in EMIB-T, co-packaged optics, and glass substrates at ECTC 2026. These technologies are crucial for overcoming performance and power bottlenecks in next-gen computing.

IN DEPTH

Key Findings

Semiconductor Engineering's June 2026 edition delivered a comprehensive feature on the latest trends and technical challenges across semiconductor manufacturing, packaging, and materials. The report provided detailed insights into the manufacturability of on-chip photonics for AI systems, the enhancement of connection density through hybrid bonding, novel design approaches for Gallium Nitride (GaN) power devices, and strategies for addressing manufacturing variations at advanced nodes.

Technical Details

- **On-chip Photonics**: Investigates the manufacturing feasibility of integrating optical circuits directly onto chips to alleviate data transmission bottlenecks in AI systems. This technology promises faster and more power-efficient data transfer than traditional electrical signaling.
- **Hybrid Bonding**: Highlighted as a key technology for dramatically increasing die-to-die connection density, crucial for 3D stacked structures and chiplet integration. It enables finer bonding pitches and higher reliability, indispensable for next-generation HPC and AI chips.
- **GaN Power Devices**: Gallium Nitride (GaN)-based power devices are seeing expanded adoption in power management and EV applications due to their high efficiency and compact size. The feature presented new design approaches to further optimize these devices.
- **Addressing Manufacturing Variations**: As scaling progresses to advanced nodes, manufacturing process variability has a growing impact on product yield and performance. The report discussed advanced metrology and process control strategies to counter these effects.
- **Insights from ECTC 2026**: Lori Scott of Intel Foundry, speaking at the Electronic Components and Technology Conference (ECTC) 2026, elaborated on advancements in Intel's EMIB-T (Embedded Multi-die Interconnect Bridge-Tile), Co-packaged optics, and glass substrate technologies. These innovations point towards next-generation packaging solutions set to redefine the limits of scalability for AI and HPC applications.

Background & Context

The explosive growth of AI continuously pushes the performance limits of semiconductor chips. Challenges in data processing, transmission, and power consumption are becoming increasingly evident, and conventional technologies are struggling to keep pace. In this scenario, packaging technology has emerged as a pillar of innovation, possessing importance equal to, if not greater than, transistor scaling. The industry as a whole is striving to overcome these challenges by leveraging heterogeneous integration and novel material science.

Strategic Significance & Outlook

The technologies discussed in this feature are indispensable for enabling next-generation AI and HPC systems. On-chip photonics will dramatically improve communication bandwidth within data centers, and hybrid bonding will unlock the performance potential of 3D-stacked AI accelerators. GaN devices will enable more efficient power management, reducing overall system power consumption. The continuous advancement and integration of these technologies will be key to solving the most complex challenges facing the semiconductor industry and accelerating innovation in the AI era.

Source: https://semiengineering.com/newsletter/manufacturing-packaging-materials-june-2026/

Collected: June 19, 2026 | Automated Research System (Gemini API)

AT&S Commits €2 Billion to Malaysian Expansion, Supercharging AI IC Substrate Capacity for AMD and Key Tech Partners

Published Published June 15, 2026 EQS News オーストリア

OVERVIEW

Austrian IC substrate manufacturer AT&S is undertaking a significant €1.5-2 billion expansion of its Kulim, Malaysia plant to dramatically increase high-end IC substrate production for AI and high-performance computing (HPC) applications. This strategic move, driven by long-term agreements with key customers like AMD, is fully financed by customer contracts, mitigating AT&S's financial risk while addressing unprecedented demand from global AI infrastructure build-out. The investment is projected to contribute tens of millions of euros to AT&S's EBIT by fiscal year 2026/27.

IN DEPTH

Background

The ongoing artificial intelligence (AI) revolution is profoundly reshaping the semiconductor industry, creating an exponential demand for advanced packaging solutions and high-performance substrates. Amidst intensifying global competition to develop advanced data centers and AI accelerators, securing reliable and scalable IC substrate suppliers has become a critical imperative for leading chip design companies such as AMD. Leveraging its deep technological expertise and established manufacturing capabilities, AT&S is strategically strengthening its position within the advanced semiconductor supply chain by directly addressing this burgeoning demand. Furthermore, Malaysia, with its robust and established ecosystem for semiconductor back-end processes, continues to be an attractive strategic location for such substantial manufacturing investments.

Key Findings

AT&S, an Austrian manufacturer renowned for its advanced IC substrates and PCBs, has announced a significant expansion of its Kulim manufacturing site in Malaysia. This strategic move is anchored by long-term agreements with key customers, including AMD and another leading technology company, and aims to substantially boost high-end IC substrate production capacity specifically for artificial intelligence (AI) and high-performance computing (HPC) infrastructure.

This expansion plan represents a substantial investment, estimated between €1.5 billion and €2 billion. Critically, this investment is fully financed through long-term customer agreements, including those with AMD, significantly mitigating AT&S's financial risk. The project encompasses both the enhancement of existing production capacity at Plant 1 and the renovation of the currently unused Plant 2 building, coupled with the construction of entirely new manufacturing facilities for IC substrate cores and advanced PCBs. This comprehensive upgrade positions AT&S to address the evolving demands of advanced packaging, which require higher integration density, larger substrate form factors, and increased layer counts.

AT&S projects a positive impact on its Earnings Before Interest and Taxes (EBIT) of tens of millions of euros in fiscal year 2026/27, underscoring the company's commitment to long-term revenue growth. The escalating requirements of AI chips and HPC processors necessitate increasingly complex and higher-performance substrates to facilitate enhanced data processing capabilities and optimized power efficiency. AT&S's advanced IC substrates are engineered to be critical components in meeting these demanding specifications.

The Kulim plant expansion represents a pivotal strategic maneuver by AT&S, designed to capitalize on significant long-term growth opportunities within the AI and HPC markets. This substantial investment is projected to not only significantly enhance the company's production capacity but also to deepen its relationships with critical customers and strengthen technological partnerships. As global AI infrastructure continues its rapid evolution, the demand for high-value, high-performance IC substrates is anticipated to rise unabated, and AT&S is proactively positioning itself to meet this sustained trend. Moreover, this initiative is expected to further elevate Malaysia's standing as an advanced semiconductor manufacturing hub within the global supply chain.

Source: https://www.eqs-news.com/news/corporate/ats-expands-kulim-site-to-support-long-term-customer-demand-and-deepen-strategic-technology-partnerships/c5a2b864-597b-4fc6-9a59-f1717706125d_en

KAIST Develops Breakthrough Liquid Cooling Technology to Shatter AI Semiconductor Thermal Bottleneck

Published June 16, 2026 Mirage News South Korea

OVERVIEW

KAIST researchers have developed an innovative liquid cooling technology that breaks through the severe thermal management bottleneck in AI semiconductors and advanced electronic packaging. This breakthrough could be implemented in existing semiconductor fabs without major additional investment, promising to solve thermal challenges across a wide range of high heat flux electronic systems, including AI accelerators, HPC, 3D semiconductor packaging, and power electronics.

IN DEPTH

Key Findings

Researchers at the Korea Advanced Institute of Science and Technology (KAIST) have developed a groundbreaking liquid cooling technology poised to overcome one of the most critical challenges facing AI semiconductors and advanced electronic packaging: thermal management bottlenecks. This breakthrough holds the potential to significantly enhance the performance and reliability of next-generation AI hardware.

Technical Details

- The liquid cooling technology developed by KAIST offers a significant advantage: it can be integrated into existing semiconductor manufacturing processes and fab infrastructure without requiring large-scale additional capital expenditure. This drastically reduces the cost and risk associated with adopting the new technology.
- This technology is specifically designed to address thermal management issues across a broad spectrum of high heat flux electronic systems, including heat-intensive AI accelerators, high-performance computing (HPC) systems, 3D semiconductor packaging, and power electronics.
- The precise cooling mechanism likely utilizes optimized microfluidic channels or phase-change cooling elements to efficiently remove heat directly from the chip. This enables far higher heat transfer efficiency compared to conventional air cooling or indirect liquid cooling solutions.
- The research team states that this technology will contribute to maintaining AI semiconductors at safe operating temperatures while simultaneously allowing for increased clock frequencies and maximizing processing capabilities. This is expected to shorten AI model training times and improve real-time inference performance.

Background & Context

The relentless pursuit of higher performance in AI chips inevitably leads to increased power consumption and heat generation. Particularly, 3D-stacked high-bandwidth memory (HBM) and large AI processors generate extremely high heat fluxes, which have become a primary bottleneck limiting overall system performance and reliability. Existing cooling solutions are increasingly struggling to meet these demands, prompting the semiconductor industry to urgently seek innovative thermal management technologies. KAIST's breakthrough offers a direct solution to this pressing challenge.

Strategic Significance & Outlook

The introduction of KAIST's liquid cooling technology will provide new design freedom in AI semiconductor development, accelerating the creation of more powerful and power-efficient AI hardware. Its easy integration into existing fabs suggests a rapid industrial adoption, potentially becoming a standard thermal management solution in AI, HPC, and data center applications. In the future, this technology could also enable the adoption of high-performance AI chips in constrained environments like smartphones and edge devices, further catalyzing the widespread deployment of AI.

Source: https://www.miragenews.com/kaist-shatters-ai-bottleneck-with-advanced-1692935/

Collected: June 19, 2026 | Automated Research System (Gemini API)

Samsung's Advanced Packaging Lag Clouds AI Chip Comeback, Falling Behind TSMC and Intel

Published June 12, 2026 digitimes Taiwan

OVERVIEW

Despite efforts in HBM and foundry services, Samsung Electronics' lagging advanced packaging capabilities remain a significant weakness in the AI chip supply chain. Industry sources and Korean media reports indicate Samsung lags behind TSMC and Intel in this critical area, impacting its ability to secure a larger share of the burgeoning AI chip market. The increasing importance of advanced packaging for AI chip performance exacerbates this challenge.

IN DEPTH

Key Findings

Samsung Electronics, while striving to rebound in high-bandwidth memory (HBM) and foundry services, faces a major hurdle: its lag in advanced packaging capabilities within the AI chip supply chain. Reports from industry insiders and Korean media highlight that Samsung trails TSMC and Intel in this crucial area.

Technical and Business Details

- The performance of AI chips relies heavily not only on advanced process nodes but also on advanced packaging technologies that integrate multiple chips (e.g., GPUs, HBM, interposers) in high density. While Samsung boasts strengths in HBM, its supply capacity and technological maturity in 2.5D/3D packaging solutions like CoWoS are perceived as inferior to competitors.
- Analysts at DigiTimes Research suggest that Samsung's advanced packaging capacity may not be adequately meeting the demands of major AI chip customers such as NVIDIA. This potentially places Samsung at a disadvantage when offering comprehensive solutions that combine its HBM products with its foundry services.
- Intel is aggressively advancing its proprietary packaging technologies like Foveros and EMIB, while TSMC dominates the market with CoWoS. In contrast, Samsung requires further investment and time to build its own robust ecosystem and mass production capabilities in advanced packaging.
- Although HBM supply capacity is crucial in the AI chip market, it is essential that the packaging technology integrating HBM does not become a bottleneck, allowing HBM performance to be fully realized.

Background & Context

The AI revolution is shifting the focal point of competition in the semiconductor industry. Where traditional foundry competition centered on fine process nodes, advanced packaging has become the new battleground, dictating AI chip performance and time-to-market. Samsung, a global leader in DRAM and NAND flash memory and with a foundry business, finds its strategic position in the AI chip market threatened by this relative delay in advanced packaging. This represents a critical challenge for the company to assert leadership in the AI era.

Strategic Significance & Outlook

Samsung recognizes strengthening its advanced packaging capabilities as a top priority and is expected to accelerate massive investments and technological development. This will likely include R&D for new packaging technologies, expansion of production facilities, and establishment of supply chain partnerships. If Samsung successfully bridges this gap and stands alongside TSMC and Intel, competition in the AI chip market will further intensify, fostering accelerated innovation. However, for now, this disparity in packaging capabilities is likely to cloud Samsung's growth prospects in the AI chip market.

Source: https://www.digitimes.com/news/a20260611VL219/samsung-packaging-tsmc-intel-hbm.html

Lam Research Forecasts Over 50% Growth in Advanced Packaging Revenue by 2026, Emerging as a Key AI "Picks and Shovels" Provider

Published June 11, 2026 XTB.com USA

OVERVIEW

Lam Research, a leading semiconductor equipment manufacturer, predicts over 50% growth in its advanced packaging related revenue by 2026, driven by soaring demand for AI accelerators, HBM, and chiplet-based architectures. The company's management identifies advanced packaging as one of its fastest-growing business segments, solidifying its role as a "picks and shovels" provider in the AI era. Lam Research recorded Q3'26 revenue of $5.84 billion, a 24% year-over-year increase, reflecting strong AI-driven demand for its etching and deposition tools.

IN DEPTH

Key Findings

Lam Research, a global leader in semiconductor manufacturing equipment, has issued an assertive forecast, projecting over 50% growth in its advanced packaging-related revenue by 2026. This surge is attributed to the explosive demand for AI accelerators, high-bandwidth memory (HBM), and chiplet-based architectures. Company management emphasizes advanced packaging as one of the fastest-growing segments within Lam Research's operations.

Business and Technical Details

- While Lam Research is a leader in front-end semiconductor manufacturing processes (e.g., etching and deposition), it is also actively expanding its technology portfolio in advanced packaging. Advanced packaging is becoming increasingly crucial for enhancing performance and bandwidth in next-generation computing systems.
- Specifically, advanced packaging technologies such as CoWoS (Chip-on-Wafer-on-Substrate) and hybrid bonding are indispensable for boosting the performance, bandwidth, and power efficiency of AI chips. Lam Research provides precise etching and deposition tools that enable these critical technologies.
- In Q3 2026, Lam Research reported revenue of $5.84 billion, a 24% year-over-year increase. This robust performance indicates that AI chip demand is a strong driver for the company's etching and deposition equipment.
- The company is positioned as a "picks and shovels" provider for the AI era—analogous to selling shovels during a gold rush. Instead of directly manufacturing AI chips, Lam Research captures growth opportunities by supplying the foundational technologies that underpin AI hardware.

Background & Context

The rapid advancement of AI is redefining the semiconductor industry's technology roadmap. With limits approaching for transistor scaling, heterogeneous integration and advanced packaging have emerged as primary means to enhance the performance of next-generation AI chips. Equipment manufacturers like Lam Research directly benefit from this paradigm shift, with the growth of the advanced packaging market becoming a new engine for the company's expansion.

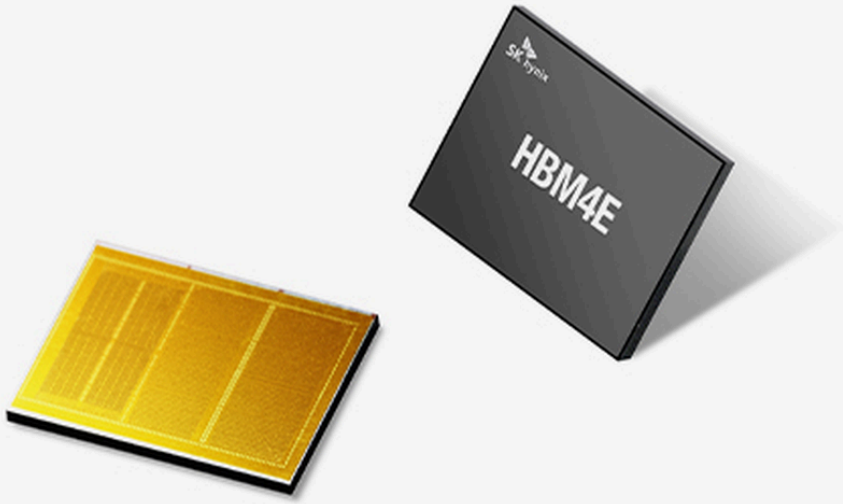
Strategic Significance & Outlook

Lam Research's optimistic forecast for its advanced packaging segment underscores the profound impact of AI chip demand on the broader semiconductor equipment market. The company will likely continue to invest in R&D, developing tools that cater to evolving packaging technologies such as CoWoS, CoPoS, hybrid bonding, and chiplet integration to maintain its market leadership. This growth could serve as a "hidden catalyst" for Lam Research's stock, making it imperative for investors to closely monitor the company's advanced packaging strategy.

Source: https://www.xtb.com/en/market-analysis/stock-of-the-week-lam-research-the-quiet-seller-of-ai-picks-and-shovels

SK Hynix Begins Shipping 12-Layer Next-Gen 'HBM4E' Samples for AI, Delivering Significant Performance and Power Efficiency Gains Amidst NVIDIA CEO's Endorsement

Published June 18, 2026 SK hynix Inc. South Korea



OVERVIEW

SK Hynix has commenced shipping samples of its 12-layer 'HBM4E,' a next-generation DRAM for AI, to key customers. This HBM4E features data processing speeds of up to 16Gbps per pin and over 20% improved power efficiency compared to existing models, representing more than a 30% speed increase over HBM4's 11.7Gbps. The company utilized Advanced MR-MUF technology to achieve 48GB capacity and a 17% reduction in thermal resistance. NVIDIA CEO Jensen Huang visited SK Hynix's Computex 2026 booth, signaling high industry anticipation.

IN DEPTH

Key Findings

SK Hynix has announced the commencement of sample shipments for its 12-layer 'HBM4E,' a next-generation high-performance memory designed for AI accelerators, to its key customers. This innovative memory promises to significantly boost data processing speed and power efficiency compared to previous HBM4 generations, further pushing the performance boundaries of AI chips.

Technical and Business Details

- The HBM4E shipped boasts a data processing speed of up to 16Gbps per pin, which is over 30% faster than HBM4's 11.7Gbps. This high bandwidth is crucial for efficiently meeting the massive data processing requirements in AI model training and inference.
- Power efficiency has also been substantially improved, with over a 20% gain compared to existing models. Reducing power consumption in AI data centers is a pressing challenge, and this efficiency enhancement will significantly contribute to lower operational costs and environmental impact.
- SK Hynix employs its proprietary Advanced MR-MUF (Mass Reflow-Molded Underfill) technology in this HBM4E product. This technology is vital for achieving high stacking layers while enhancing structural stability and heat dissipation. It enabled the realization of a large capacity of 48GB and a 17% reduction in thermal resistance compared to HBM4. The reduced thermal resistance contributes to the stable operation of memory chips in high-heat-generating AI chip environments.
- According to reports from TradingKey, SK Hynix has initiated sample shipments earlier than its initially planned "second half of the year" schedule, with shipments expected as early as this month or next.
- During Computex 2026, NVIDIA CEO Jensen Huang visited SK Hynix's booth, leaving a message, "Produce more," indicating the high level of industry anticipation for HBM4E.
- This HBM4E is manufactured using 10-nanometer class 6th generation (1c) DRAM, characterized by the fusion of cutting-edge process and packaging technologies.

Background & Context

The evolution of AI has dramatically escalated the demand for high-performance semiconductor chips and memory capable of processing vast amounts of data at high speeds. High-Bandwidth Memory (HBM) is an indispensable component for maximizing the performance of AI accelerators (such as GPUs), and technological leadership in HBM is paramount in the AI era. SK Hynix has been a long-standing pioneer in the HBM market, and this HBM4E sample shipment further solidifies its leadership.

Strategic Significance & Outlook

SK Hynix's HBM4E is poised to dramatically enhance the performance of next-generation AI accelerators, enabling the training and inference of larger and more complex AI models. The initiation of sample shipments indicates that AI chip manufacturers are preparing to integrate HBM4E into their product roadmaps, and it is expected to significantly contribute to AI infrastructure performance improvements over the next few years. SK Hynix's technological edge will be crucial in maintaining its dominant position in the HBM market and accelerating the growth of the overall AI semiconductor market.

Source: https://news.skhynix.com/12-layer-hbm4e-sample/

Collected: June 19, 2026 | Automated Research System (Gemini API)

SK Hynix Holds U.S. Talks on HBM Supply and Investment Plans, Bolstering Domestic Semiconductor Supply Chain

Published June 19, 2026 digitimes Taiwan

OVERVIEW

SK Hynix reportedly held private discussions with U.S. Deputy Assistant Secretary Alison Hooker regarding high-bandwidth memory (HBM) supply to key U.S. tech firms and potential semiconductor investment plans in the U.S. This engagement signals SK Hynix's strategic moves to contribute to strengthening the domestic semiconductor supply chain within the United States.

IN DEPTH

Key Findings

SK Hynix reportedly engaged in private discussions with senior U.S. State Department officials concerning the expansion of high-bandwidth memory (HBM) supply and potential new semiconductor investment plans in the United States. This meeting aligns with the broader objective of strengthening the resilience and security of the domestic semiconductor supply chain within the U.S.

Business and Technical Details

- According to a DigiTimes report, SK Hynix met with U.S. Deputy Assistant Secretary Alison Hooker to discuss the potential for expanding HBM supply to major U.S. technology companies. HBM is an indispensable component for maximizing the performance of AI accelerators, directly contributing to the growth of the U.S. AI industry.
- Discussions also focused on SK Hynix's potential investment plans for semiconductor manufacturing or packaging facilities in the U.S. This suggests the company's intent to leverage U.S. government incentives, such as the CHIPS Act, to establish domestic production capabilities.
- HBM utilizes 3D stacking technology to vertically stack DRAM dies, connected to CPUs or GPUs via an interposer, achieving dramatically higher bandwidth compared to conventional DRAM. Domestic production of such advanced technology holds significant implications for national security.
- While specific investment amounts, locations, and timelines have not been publicly disclosed, this meeting clearly demonstrates SK Hynix's intention to deepen its commitment to the U.S. market and strengthen relationships with key customers.

Background & Context

In recent years, the U.S. has strongly advocated policies to reduce reliance on foreign semiconductor supply chains and bolster domestic production capabilities. Securing secure and reliable domestic supply sources is a top priority, especially in strategic technology sectors like AI and HPC. SK Hynix is one of the global leaders in the HBM market, and its potential HBM supply and investment in the U.S. hold significant meaning for the growth of the American AI industry and national security.

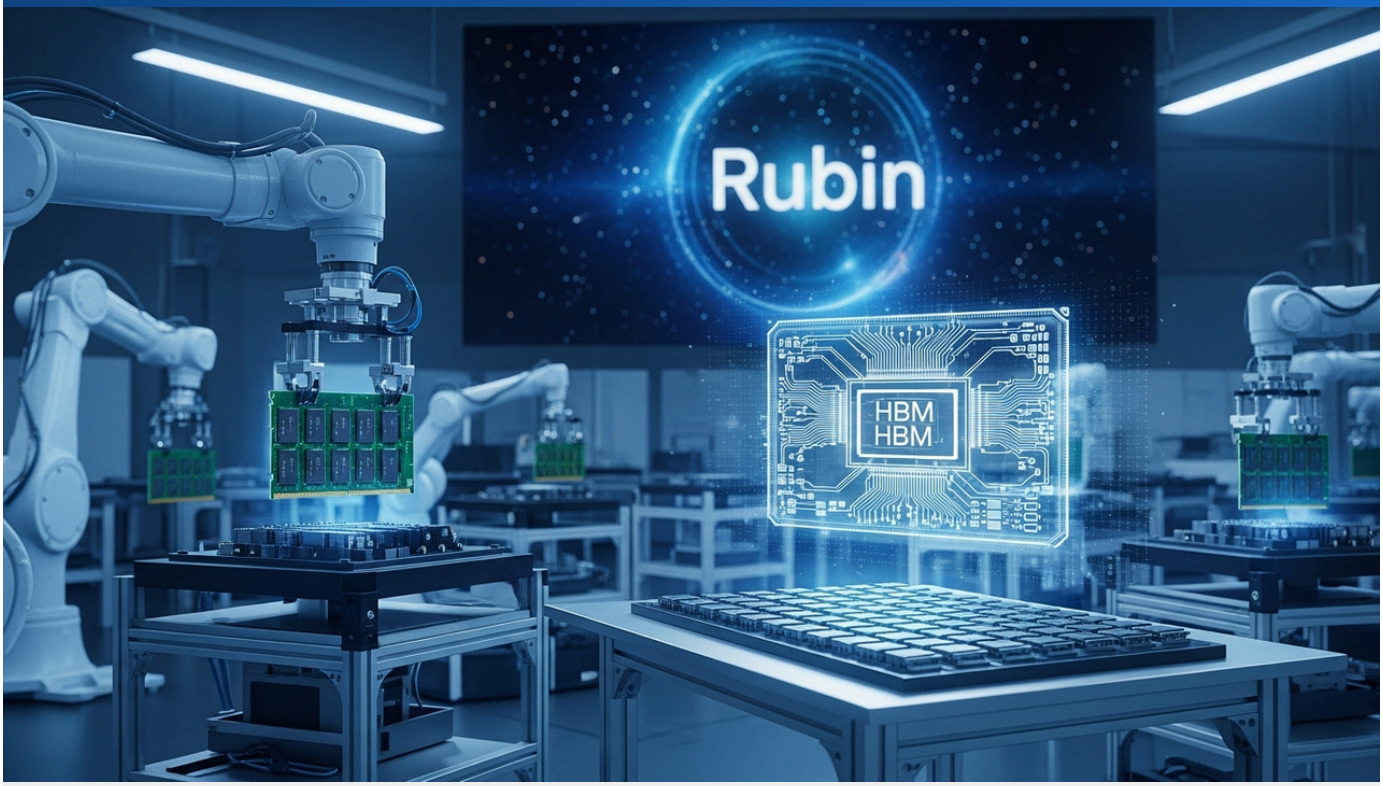
Strategic Significance & Outlook

SK Hynix and U.S. government officials' discussions signal the potential for substantial future investments and partnerships. Should SK Hynix establish HBM-related manufacturing or packaging facilities in the U.S., it would represent a major contribution to the U.S. semiconductor ecosystem, accelerating domestic technological innovation and job creation. Furthermore, this would lead to a more diversified global HBM supply chain, enhancing its resilience against geopolitical risks.

Source: https://www.digitimes.com/news/a20260618PD233/sk-hynix-hbm-investment-shipments-supply-chain.html

Micron's HBM Capacity Sold Out Through 2026, Securing Position in NVIDIA's Next-Gen AI Platform "Vera Rubin"

Published June 15, 2026 Investing.com USA



OVERVIEW

Micron Technology has announced that its high-bandwidth memory (HBM) production capacity is completely sold out through 2026, with long-term contracts secured, reflecting overwhelming demand for AI-driven HBM. Notably, NVIDIA has qualified Micron as an HBM4 supplier for its next-generation "Vera Rubin" AI platform, integrating Micron deeply into its top-tier AI memory roadmap. This underscores Micron's strong market position and the critical role of HBM in advanced AI systems.

IN DEPTH

Key Findings

Micron Technology has declared its high-bandwidth memory (HBM) production capacity fully sold out through 2026, securing long-term contracts with major customers. This announcement vividly demonstrates the unprecedented strength of demand for HBM tailored for AI and high-performance computing (HPC) applications. Crucially, NVIDIA has qualified Micron as an HBM4 supplier for its next-generation "Vera Rubin" AI platform, deeply integrating Micron into its top-tier AI memory roadmap.

Business and Technical Details

- The complete sale of Micron's HBM capacity indicates that AI chip design companies are entering early, long-term contracts to secure HBM supply. HBM, directly connected to AI accelerator GPUs, dramatically enhances the performance of AI model training and inference by supplying massive amounts of data at high speeds.
- NVIDIA's qualification of Micron as an HBM4 supplier is strong evidence of Micron's HBM technology possessing industry-leading performance and reliability. HBM4 is the next-generation HBM standard, offering further improvements in bandwidth and power efficiency compared to HBM3E.
- Micron leverages its strengths in DRAM stacking technology, requiring precise manufacturing capabilities for Through Silicon Via (TSV) and microbumps in HBM production. Each generation of HBM relies on complex packaging technologies to achieve higher bandwidth, larger capacity, and superior power efficiency.
- Micron is currently constructing a new HBM advanced packaging facility in Singapore, which is expected to play a crucial role in future HBM capacity expansion and meeting customer demand.

Background & Context

The explosive growth of AI has brought unprecedented benefits to the semiconductor industry, particularly the HBM market. AI chip giants like NVIDIA require the highest-performance HBM to maximize their GPU capabilities. This forges fierce competition over technology and production capacity among leading HBM suppliers such as Micron, SK Hynix, and Samsung. Micron's sold-out HBM capacity signifies its strong position in this competitive landscape.

Strategic Significance & Outlook

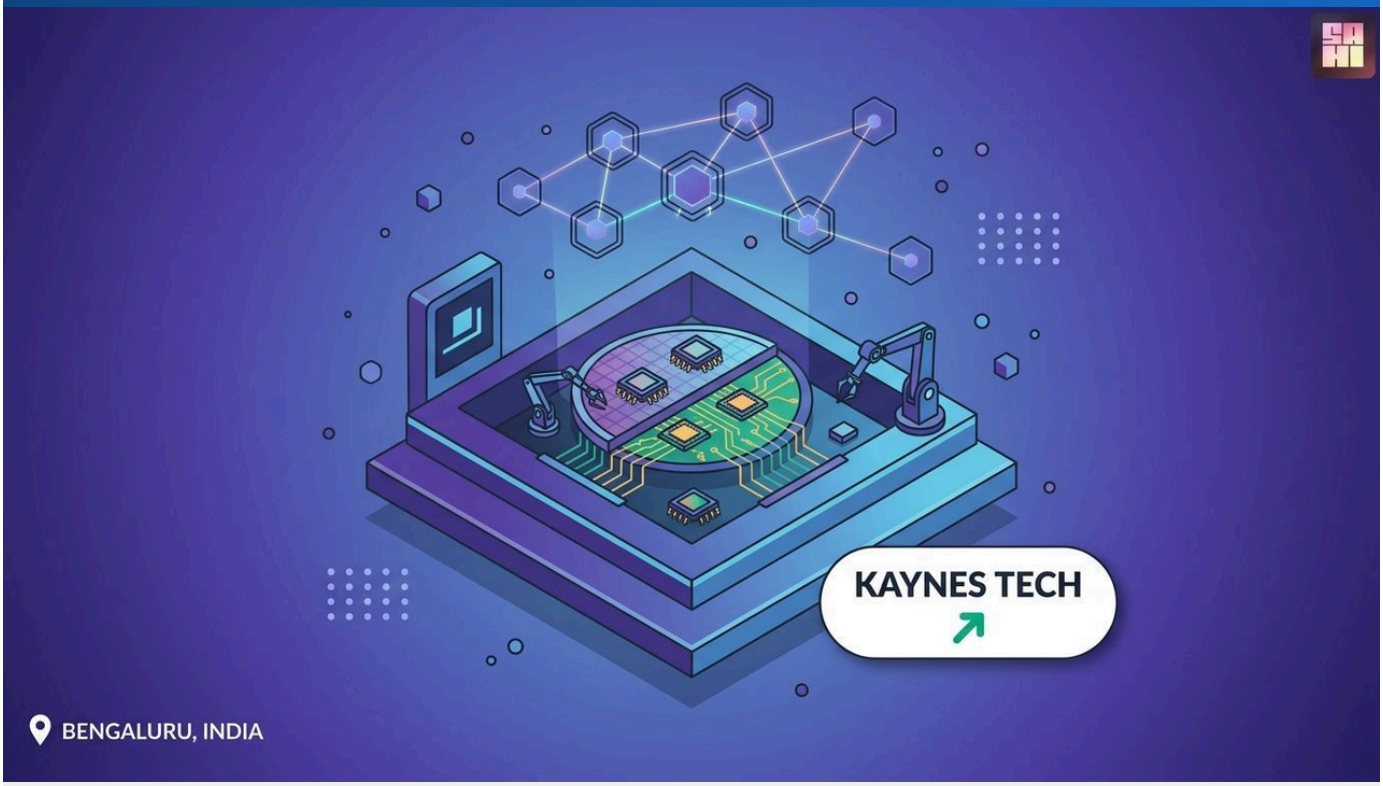
Micron's HBM production capacity and qualification by NVIDIA will serve as a significant catalyst for its future growth. HBM demand is expected to continue accelerating with the evolution of AI applications, and Micron has established a strong foundation for securing long-term revenue and market share. This success will encourage further investment in HBM technology, contributing to accelerated innovation in next-generation AI hardware.

Source: https://www.investing.com/analysis/microns-soldout-hbm-capacity-makes-june-24-a-makeorbreak-catalyst-200682176

Collected: June 19, 2026 | Automated Research System (Gemini API)

Kaynes Technology Partners with Japan's AOI Electronics to Build ₹3,307 Cr OSAT Plant in India, Boosting Semiconductor Back-End Capabilities

Published June 16, 2026 Sahi India



OVERVIEW

Kaynes Technology's subsidiary has formally partnered with Japanese OSAT leader AOI Electronics for a ₹3,307 crore (approx. $395 million USD) Sanand OSAT facility, slated for commercial operation in H2 2026. This collaboration integrates advanced back-end processes into India's semiconductor ecosystem. Combined with a materials supply chain tie-up with Mitsui & Co., this partnership completes the trifecta of technology, raw materials, and manufacturing essential for scheduled commercial launch.

IN DEPTH

Key Findings

Kaynes Semicon, a subsidiary of Indian Electronics Manufacturing Services (EMS) giant Kaynes Technology, has formally inked a pivotal technology partnership with AOI Electronics, a leading Japanese Outsourced Semiconductor Assembly and Test (OSAT) firm. This collaboration paves the way for the ₹3,307 crore (approximately $395 million USD) Sanand OSAT facility to commence commercial operations in the second half of 2026, integrating advanced back-end process capabilities into India's burgeoning semiconductor ecosystem.

Business and Technical Details

- This substantial investment is approved under the Indian government's "Semiconductor India Programme," aligning with the national strategy to establish an indigenous semiconductor supply chain.
- The technology tie-up with AOI Electronics grants Kaynes Semicon access to advanced packaging and testing technologies. This will enable the assembly and testing of complex semiconductor chips for smartphones, automotive applications, IoT, and AI devices.
- Concurrently, Kaynes Semicon is strengthening its materials supply chain partnership with Mitsui & Co. This ensures a stable supply of high-quality raw materials essential for OSAT factory operations.
- This tripartite alliance—"Technology (AOI Electronics), Raw Materials (Mitsui & Co.), and Manufacturing (Kaynes Semicon)"—completes the necessary synergy for the Sanand plant's scheduled commercial launch in H2 2026.
- The facility is expected to offer a wide range of packaging services, including flip-chip, wire bonding, and advanced testing solutions, catering specifically to the back-end processing of high-value chips.

Background & Context

Amidst global semiconductor supply chain restructuring and efforts to bolster domestic manufacturing capabilities, India is actively striving to establish itself as a semiconductor manufacturing hub. Particularly with the proliferation of AI and IoT devices, semiconductor back-end processes (OSAT) have become critical factors determining chip performance and cost-efficiency. The partnership between Kaynes Technology and AOI Electronics represents a significant step for India to evolve from merely a semiconductor consumer to a nation with advanced manufacturing capabilities.

Strategic Significance & Outlook

The commercial operation of the Sanand OSAT facility will be a landmark event for India's semiconductor industry. It is expected to strengthen the domestic semiconductor manufacturing ecosystem, attract foreign direct investment, and create high-skilled technical jobs. Moreover, the collaboration with Japan's AOI Electronics and Mitsui & Co. deepens economic cooperation between India and Japan, bringing strategic benefits to both nations. Kaynes Technology will leverage this new capability to enhance its competitiveness in both domestic and international markets, addressing the semiconductor demand of the AI era.

Source: https://www.sahi.com/news/kaynes-tech-secures-japan-s-aoi-electronics-tech-for-3-307-cr-semiconductor-osat-unit-5226-PE1_COR

Collected: June 19, 2026 | Automated Research System (Gemini API)

TSMC and Amkor Forge 10-Year Strategic Partnership to Boost U.S. Advanced Packaging Capabilities

Published June 18, 2026 Focus Taiwan Taiwan

OVERVIEW

TSMC and Amkor Technology have entered a 10-year strategic agreement to bolster advanced semiconductor packaging in the United States. Under this pact, TSMC will procure advanced packaging and test services from Amkor, accelerating its Arizona investments to establish a robust, integrated supply chain for escalating AI and HPC demands. This collaboration marks a significant step towards a complete domestic silicon supply chain, from manufacturing to packaged devices, enhancing U.S. technological sovereignty and resilience.

IN DEPTH

Key Findings

TSMC, the world's largest contract chipmaker, and Amkor Technology, a leading outsourced semiconductor assembly and test (OSAT) provider, have announced a landmark 10-year strategic partnership to significantly enhance advanced semiconductor packaging capabilities within the United States. This agreement ensures TSMC's procurement of advanced packaging and test services from Amkor, accelerating its investments in Arizona and aiming to build an integrated, resilient supply chain crucial for the surging demands of artificial intelligence (AI) and high-performance computing (HPC) applications.

Technical / Clinical Details

At the core of this partnership is TSMC's strategic sourcing of advanced packaging and test services from Amkor. This collaboration is designed to synergize TSMC's leading-edge wafer fabrication with Amkor's specialized back-end capabilities, ensuring efficient delivery of finished semiconductor devices. The exponential growth in demand for AI and HPC chips necessitates sophisticated packaging technologies, including 2.5D/3D integration and chiplet architectures. Amkor plans to meet these requirements by expanding its existing campus in Peoria, Arizona, with the goal of becoming the first high-volume advanced packaging OSAT facility in the U.S. This expansion will enable the provision of high-performance packaging solutions essential for satisfying the complex design specifications of advanced AI chips.

Background & Context

In response to rising geopolitical risks and the imperative for supply chain diversification, major nations are actively pursuing the reshoring of semiconductor manufacturing capabilities. The U.S., bolstered by initiatives like the CHIPS Act, is aggressively pushing for a domestic semiconductor industry resurgence. The TSMC-Amkor alliance aligns perfectly with this strategic objective, further solidifying the semiconductor ecosystem in Arizona. This collaboration represents a crucial stride towards a "complete supply chain" in the U.S., encompassing everything from wafer fabrication to packaging and testing. Such integration is expected to reinforce America's technological leadership and economic security in strategic sectors like AI and HPC.

Strategic Significance & Outlook

Amkor's CEO emphasized that this partnership is a pivotal step toward providing a comprehensive domestic supply chain in the U.S., from advanced silicon manufacturing to tested packaged devices. The decade-long agreement is poised to contribute significantly to the sustained growth and innovation within the U.S. semiconductor industry, while also serving as a model for enhancing global semiconductor supply chain resilience. As the evolution of AI and HPC accelerates, such strategic alliances will only grow in importance, forming the fundamental pillars for future technological advancements.

Source: https://focustaiwan.tw/business/202606180011

Collected: June 19, 2026 | Automated Research System (Gemini API)

AT&S Commits €2 Billion to Accelerate AI/HPC Chip Substrate Production in Asia, Bolstered by AMD Partnership

Published Published June 15, 2026　TNW　オーストリア

OVERVIEW

Austrian IC substrate manufacturer AT&S is investing €1.5-2 billion to significantly expand high-end IC substrate capacity at its Kulim, Malaysia, and Chongqing, China, facilities. This strategic move, driven by soaring global demand for AI and HPC chips and secured by multi-year agreements with key customers including AMD, aims to alleviate critical supply bottlenecks. The expansion will solidify AT&S's position as a crucial supplier for next-generation AI infrastructure, enhancing its competitive edge in a rapidly evolving market.

IN DEPTH

Background & Context

The explosive growth of artificial intelligence (AI) has created unprecedented demand for high-performance semiconductor devices, leading to concerns that the supply capacity of critical components like chip substrates and advanced packaging solutions could become a significant bottleneck. Austrian-based AT&S, a global leader in printed circuit boards (PCBs) and IC substrates, is directly addressing this market imperative. By strategically investing in expanded capacity, the company aims to ensure a stable supply of high-performance substrates, especially as major semiconductor manufacturers like AMD accelerate their development of next-generation AI chips. Asia, particularly Malaysia and China, remains a crucial hub for the semiconductor manufacturing supply chain, making investments in these regions essential for supporting global AI infrastructure development.

Key Investment & Strategic Focus

AT&S has announced a substantial investment of €1.5 to €2 billion into its facilities in Kulim, Malaysia, and Chongqing, China. This funding is earmarked to significantly expand its production capacity for high-end IC substrates, which are critical for the functionality and performance of AI and high-performance computing (HPC) chips. This massive investment is anchored by multi-year supply agreements with key customers, including AMD and another undisclosed technology company, reflecting the sustained strong demand for AI infrastructure and validating AT&S's strategic direction.

Technological Deep Dive

The high-end IC substrates produced by AT&S are crucial for unlocking the maximum performance of AI accelerators and HPC processors. These substrates are designed to synergize with advanced packaging technologies such as CoWoS (Chip-on-Wafer-on-Substrate) and InFO (Integrated Fan-Out), enabling higher integration and efficiency. Key features include high-density wiring, excellent signal integrity, and efficient thermal management capabilities, all vital for powerful AI chips. The announced investment will bolster production lines for advanced packaging substrates, including those utilizing ABF (Ajinomoto Build-up Film) technology. Specifically, the Kulim facility in Malaysia will focus on state-of-the-art IC substrate manufacturing, while the Chongqing plant in China will enhance its capacity for high-growth markets. These expansions will involve the adoption of new technologies to support higher-layer count substrates, finer line-and-space geometries, and advanced via structures, contributing directly to improved power efficiency and processing power for next-generation AI chips.

Market Impact & Outlook

This investment is crucial for AT&S to solidify its position as a leading supplier in the burgeoning AI and HPC markets. By substantially expanding its production capacity, AT&S will be better equipped to flexibly respond to fluctuations in customer demand and accelerate new product development cycles. This strategic move is expected to further intensify investment competition across the semiconductor packaging and substrate industry, as other players vie for market share. More broadly, AT&S's expansion will serve as a vital factor in accelerating the performance improvement and widespread adoption of AI chips across various sectors. In the long term, this investment is anticipated to underpin the continued evolution of AI technology and enable new industrial applications, pushing the boundaries of what AI can achieve.

Source: https://thenextweb.com/news/ats-malaysia-china-ai-chip-boom-investment

Collected: June 19, 2026 | Automated Research System (Gemini API)

Amkor Supercharges U.S. Chip Packaging with 67-Acre Arizona Expansion, Aiming for First High-Volume Advanced OSAT

Published Published June 16, 2026 StocksToTrade USA

OVERVIEW

Amkor Technology has significantly expanded its U.S. presence by acquiring an additional 67 acres at its advanced packaging and test campus in Peoria, Arizona. This strategic move targets establishing the nation's first high-volume advanced packaging OSAT facility, crucial for meeting surging demand from AI, HPC, automotive, and communications markets. Despite recent stock fluctuations, Amkor's long-term strategic positioning is robust, pivotal for strengthening the U.S. semiconductor supply chain.

IN DEPTH

Background

The reshoring of semiconductor manufacturing is accelerating, driven by policy incentives such as the U.S. CHIPS Act. Advanced packaging has emerged as a critical new frontier for enhancing chip performance and reducing costs, especially as traditional Moore's Law scaling approaches its physical limits. Amkor's significant investment directly aligns with the national strategy to bolster domestic advanced packaging capabilities and mitigate reliance on overseas production. Securing domestic production capacity is paramount for ensuring supply chain resilience and economic security amidst strong demand from high-growth markets like AI, HPC, and automotive.

Key Findings

Amkor Technology has announced a substantial expansion of its U.S. operations, acquiring an additional 67 acres at its advanced packaging and test campus in Peoria, Arizona. This strategic acquisition is poised to establish Amkor as the first high-volume advanced packaging Outsourced Semiconductor Assembly and Test (OSAT) facility in the United States, directly addressing surging demand across AI, high-performance computing (HPC), automotive, and communications sectors. This move significantly bolsters Amkor's pivotal role within the domestic semiconductor supply chain.

Amkor's advanced packaging facilities are already equipped with cutting-edge technologies including flip-chip, fan-out wafer-level packaging (FOWLP), system-in-package (SiP), and 2.5D/3D packaging. These capabilities are indispensable for next-generation AI processors and HPC chips, facilitating the integration of more transistors into smaller, higher-density footprints, while simultaneously enhancing data transfer speeds and optimizing power consumption. The newly acquired 67 acres will provide substantial room for new cleanrooms, advanced testing equipment, and highly automated assembly lines. This expansion will significantly augment Amkor's capacity to tackle critical challenges in semiconductor back-end processing, such as extreme miniaturization, complex heterogeneous integration, and advanced thermal management, paving the way for the mass production of future high-performance chips.

This expansion in Arizona forms a critical foundation for the U.S. to sustain its leadership in AI and advanced semiconductor technologies. While Amkor's stock saw a temporary dip following 2028 revenue and EPS targets that fell below analyst expectations, the company's long-term strategic positioning remains overwhelmingly bullish. This optimism stems from the sustained, robust demand for AI chips and the broader vision for a resilient domestic manufacturing ecosystem within the U.S. By enhancing its capabilities, Amkor will deliver a faster and more secure supply chain to its key customers, solidifying its role as an indispensable enabler of future technological innovation.

Source: https://stockstotrade.com/amkr-stock-jumps-as-arizona-expansion-fuels-ai-packaging-push/

Collected: June 19, 2026 | Automated Research System (Gemini API)

Intel Appoints Former SK hynix CEO Lee Seok-hee as Senior VP of Advanced Packaging to Bolster AI Systems

Published June 19, 2026 The Korea Herald South Korea

OVERVIEW

Intel has appointed Lee Seok-hee, former CEO of SK hynix and SK On, as Senior Vice President of Intel Foundry. Lee will lead advanced packaging, system integration, back-end technology development, and back-end manufacturing, reporting directly to the CEO. This appointment underscores Intel's firm commitment to establishing advanced packaging as a core competency and drastically enhancing its manufacturing and packaging capabilities for next-generation AI systems.

IN DEPTH

Key Findings

Intel has brought on Lee Seok-hee, the former CEO of SK hynix and SK On, as a Senior Vice President for Intel Foundry. Lee will oversee advanced packaging, system integration, back-end technology development, and back-end manufacturing, reporting directly to the CEO. This high-profile appointment clearly signals Intel's strong intent to position advanced packaging as a core strategic pillar and to fundamentally strengthen its manufacturing and packaging capabilities, especially for next-generation AI systems.

Technical / Clinical Details

Lee Seok-hee's expertise, honed in the DRAM and NAND flash memory sectors, particularly his experience in packaging and integrating advanced memory like High Bandwidth Memory (HBM), will be critical for Intel's AI strategy. Advanced packaging is key to improving chip performance and power efficiency as the physical limits of Moore's Law are approached. Intel has developed proprietary 2.5D/3D packaging technologies such as EMIB (Embedded Multi-die Interconnect Bridge) and Foveros, and Lee's leadership is expected to accelerate their maturation and volume production. His role will focus on developing and implementing innovative back-end solutions for efficiently integrating diverse chiplets, ultimately maximizing the performance of AI accelerators and CPUs.

Background & Context

In the semiconductor industry, while the race for finer process nodes intensifies, packaging technology has emerged as a new battleground for system-level performance enhancements. For AI chips in particular, tight integration with HBM and efficient chiplet-to-chiplet connectivity within a package are essential. SK hynix is a leader in the HBM market, and Lee's extensive experience there makes him an invaluable asset for Intel to catch up and surpass competitors in developing heterogeneous integration solutions, including HBM. This appointment suggests Intel's ambitious goal of revitalizing its foundry business and closing the gap with competitors like TSMC and Samsung by acquiring top-tier talent and technology.

Strategic Significance & Outlook

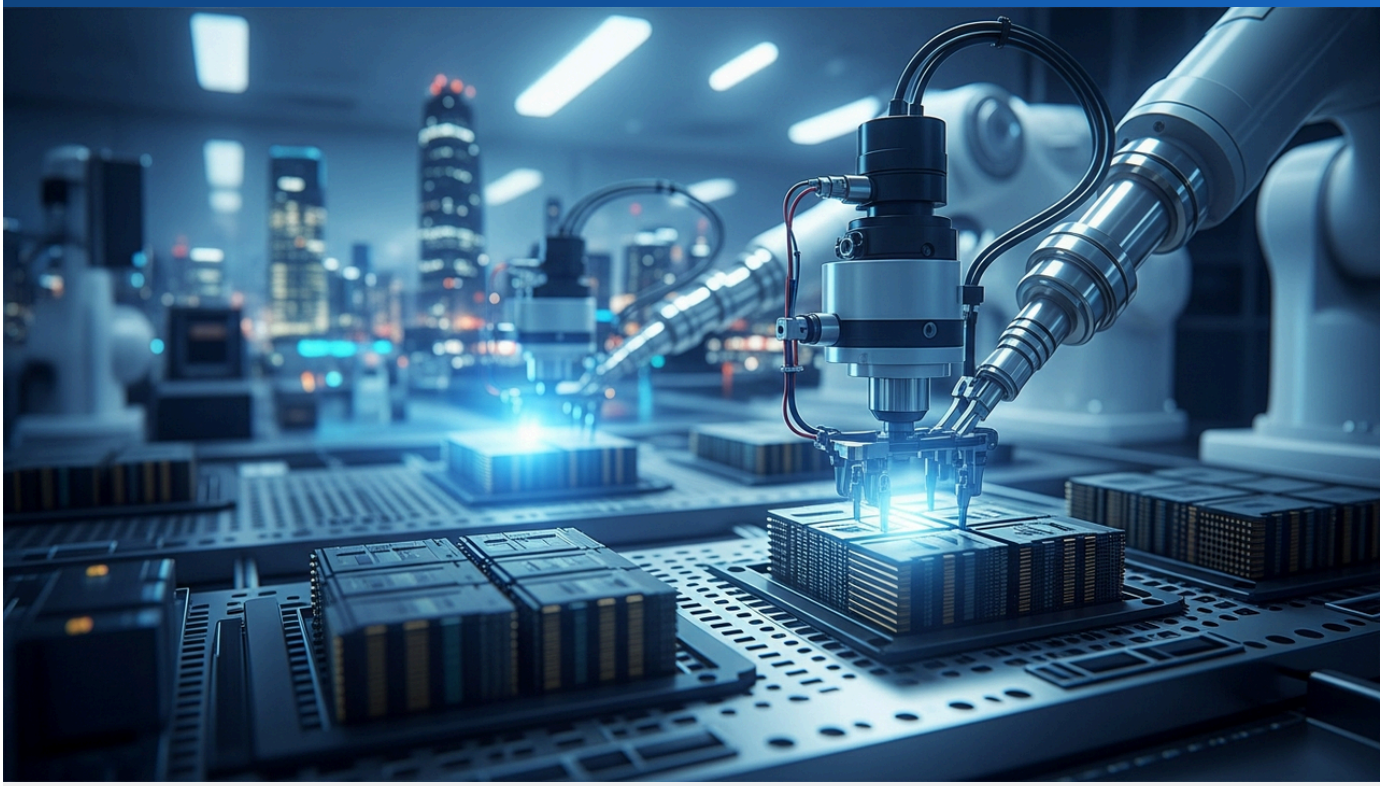
Lee Seok-hee's arrival at Intel is expected to significantly boost the company's advanced packaging strategy. Under his leadership, Intel will likely accelerate the market introduction of more sophisticated packaging solutions and, in particular, strengthen its competitiveness in the AI chip sector. This means Intel will be better positioned to offer comprehensive, turnkey solutions to its foundry customers. In the long term, this strategic talent acquisition is poised to further solidify Intel's vertical integration model in semiconductor manufacturing and lay the groundwork for accelerating innovation in next-generation AI, HPC, and data center technologies.

Source: https://www.koreaherald.com/view.php?ud=20260619000539

Collected: June 19, 2026 | Automated Research System (Gemini API)

Samsung Considers New HBM-Focused Advanced Semiconductor Packaging Plant in South Korea's Honam Region to Meet AI Server Demand

Published June 14, 2026 SamMobile South Korea



OVERVIEW

Samsung Electronics is exploring the construction of a new advanced semiconductor packaging facility in South Korea's Honam region, with Gwangju emerging as a prime candidate. This project aims to bolster Samsung's AI chip supply chain capabilities, specifically focusing on High Bandwidth Memory (HBM) chips for AI servers. This strategic move is part of Samsung's broader expansion to meet surging AI infrastructure demand and is expected to enhance its competitiveness in the critical HBM market.

IN DEPTH

Key Findings

Samsung Electronics is actively exploring the construction of a new advanced semiconductor packaging facility in South Korea's southwestern Honam region, with Gwangju city emerging as a leading candidate. This significant project aims to dramatically enhance Samsung's capabilities within the artificial intelligence (AI) chip supply chain, specifically focusing on the packaging of High Bandwidth Memory (HBM) chips, which are crucial for AI servers. This investment is part of the company's broader strategic expansion of manufacturing facilities to meet the globally surging demand for AI infrastructure.

Technical / Clinical Details

The new packaging facility is expected to incorporate state-of-the-art technologies dedicated to HBM chip manufacturing. HBM is a 3D packaging technology that vertically stacks multiple DRAM dies, connecting them to a logic chip via a high-speed interposer. This architecture delivers significantly higher data bandwidth and power efficiency compared to conventional DRAM, enabling AI processors to achieve maximum performance. Samsung has been focusing on developing its proprietary advanced packaging techniques, such as Thermal Compression Non-Conductive Film (TC NCF) bonding, which are likely to be implemented in the new plant. This will strengthen the mass production capability for next-generation HBM products, such as HBM4E, and contribute to improved yield rates and reliability.

Background & Context

The evolution of AI, requiring massive data processing and parallel computation, has led to an explosive increase in demand for HBM chips. High-performance accelerators, exemplified by NVIDIA's AI GPUs, rely on HBM as an essential component, making HBM supply capacity a key bottleneck influencing the growth of the entire AI ecosystem. Samsung is a major player in the HBM market, alongside SK hynix, and competition in this segment is intense. The construction of a new plant in the Honam region represents a strategic move by Samsung to expand its HBM market share and solidify its leadership in the AI era. This initiative also aligns with the South Korean government's plans to strengthen the domestic semiconductor ecosystem and is expected to contribute to regional economic revitalization.

Strategic Significance & Outlook

If the packaging plant in the Honam region materializes, Samsung will significantly expand its HBM chip supply capacity, enabling it to respond more quickly and stably to demand from major AI chip manufacturers. This will enhance the profitability of the company's AI semiconductor business and strengthen its competitive edge in the HBM market. In the long term, this investment is expected to lay the foundation for Samsung to drive innovation in AI, high-performance computing, and data center sectors, marking a critical milestone in leading next-generation technological advancements.

Source: https://www.sammobile.com/news/samsung-considering-new-semiconductor-packaging-plant-honam-south-korea/

Collected: June 19, 2026 | Automated Research System (Gemini API)

SK hynix Begins Shipping Next-Gen HBM4E AI Memory Chips with 12-Layer Stack, 48GB Capacity, 16Gbps per Pin, and Over 20% Power Efficiency Boost

Published June 18, 2026 Bisinfotech South Korea

OVERVIEW

SK hynix has commenced shipments of its next-generation HBM4E AI memory chips, featuring a 12-layer stack with 48GB capacity, ultra-fast data transfer rates of up to 16Gbps per pin, and over 20% improved power efficiency. The company utilizes its proprietary Advanced MR-MUF packaging technology, applying a specialized material between layers for enhanced protection. This launch solidifies SK hynix's leadership in the AI server and high-performance computing markets, meeting critical demands for next-generation AI applications.

IN DEPTH

Key Findings

SK hynix has initiated shipments of its next-generation High Bandwidth Memory (HBM), the HBM4E AI memory chips. This groundbreaking product achieves a substantial capacity of 48GB in a 12-layer stack and boasts ultra-high-speed data transfer rates of up to 16Gbps per pin. Furthermore, it delivers over 20% improvement in power efficiency compared to previous generations, promising a dramatic enhancement in the performance and efficiency of AI accelerators and high-performance computing (HPC) applications.

Technical / Clinical Details

The HBM4E's capabilities are realized through a combination of SK hynix's state-of-the-art 3D stacking technology and its proprietary Advanced MR-MUF (Mass Reflow-Molded Underfill) chip packaging technique. In this Advanced MR-MUF process, multiple DRAM dies are stacked vertically, and a specialized molded underfill material is applied between these layers. This method significantly improves the chip's thermal management, enhances mechanical strength, and boosts overall reliability. Specifically, this technology optimizes heat dissipation within the chip, enabling stable operation in high-density integration environments. The 12-layer stack structure provides maximum memory capacity within a limited footprint, while the 16Gbps per pin data transfer rate substantially alleviates data bottlenecks in AI model training and inference.

Background & Context

As AI models grow in scale and complexity, AI accelerators require increasingly higher capacity and faster memory. HBM has become a critical component for AI GPUs and HPC processors due to its significantly higher bandwidth and lower power consumption compared to conventional DRAM. SK hynix has established itself as a pioneer and leader in the HBM market, and by rapidly bringing HBM4E to market after HBM3E, it aims to further cement its competitive advantage. The commencement of HBM4E shipments is an essential factor for major AI chip manufacturers like NVIDIA in developing their next-generation products, marking a significant milestone that will accelerate the growth of the overall AI semiconductor market.

Strategic Significance & Outlook

The launch of SK hynix's HBM4E memory chips is set to profoundly impact the evolution of AI technology. The provision of faster, higher-capacity, and more power-efficient memory will enable more complex and larger AI models, thereby enhancing the performance of various AI applications, including autonomous driving, drug discovery, and large language models. The over 20% improvement in power efficiency is particularly significant, contributing to reduced operational costs for data centers and a lower environmental footprint. Through this, SK hynix is expected to solidify its leadership in the HBM market and play a central role in the design and implementation of next-generation AI systems.

Source: https://www.bisinfotech.com/sk-hynix-hbm4e-ai-memory-chips/

Collected: June 19, 2026 | Automated Research System (Gemini API)

TSMC Accelerates CoPoS Packaging Development, Standardizing 310x310mm Panel Format; Introduces Glass Core Substrate for CoWoS Towards Late 2028 Mass Production

Published June 17, 2026 TrendForce Taiwan

OVERVIEW

TSMC is accelerating the development of its CoPoS (Chip-on-Panel-on-Substrate) packaging architecture, standardizing a 310x310mm panel format, with pilot production targeted for 2027 and mass production in late 2028. Additionally, TSMC plans to integrate glass core substrates into advanced CoWoS versions, collaborating with Innolux and Ibiden. These initiatives aim to establish next-generation packaging solutions for AI and HPC, maintaining TSMC's technological leadership.

IN DEPTH

Key Findings

TSMC, a world-leading research and innovation hub in nanoelectronics and digital technologies, has announced a breakthrough in system-level III-V chiplet integration on a 300mm RF silicon interposer platform. This achievement significantly boosts capacitance density by 10 to 100 times compared to previous technologies and demonstrates an exceptionally high alignment precision of less than 600nm. This milestone unlocks new integration possibilities for RF and power applications within heterogeneous chiplet architectures, promising profound impacts on next-generation electronics systems.

Technical / Clinical Details

The RF silicon interposer platform developed by imec enables the co-integration of high-Q integrated passives with III-V semiconductor chiplets on a silicon-based platform. III-V semiconductors offer high-frequency performance and superior power efficiency that are challenging to achieve with SiGe (silicon-germanium) based technologies, but direct integration with silicon has presented significant technical hurdles. This success was achieved by optimizing high-density wiring layers and micro-bump technologies, realizing an alignment precision of less than 600nm. This precision maximizes electrical and thermal coupling between III-V chiplets and the silicon interposer. The 10-100x increase in capacitance density means the realization of smaller, higher-performance modules for circuits like RF transceivers and power amplifiers. Furthermore, imec has expanded its Automotive Chiplet Program into the Autonomous Edge Chiplet Program, pushing the application of this technology towards edge AI applications that demand high reliability and real-time processing, such as robotics, industrial automation, security, and intelligent infrastructure.

Background & Context

Demand for high-performance RF systems is exploding, driven by the proliferation of 5G/6G communications, radar systems, satellite communications, and edge AI devices. These systems require operation at high frequencies, wide bandwidths, low power consumption, and miniaturization. However, traditional monolithic (single-chip) design methods have difficulty optimizing RF components with different material properties and digital logic. The chiplet architecture addresses this challenge by integrating specialized chips manufactured through different processes. Imec's success, particularly in the RF domain, paves the way for combining the cost benefits of silicon platforms with the high performance of III-V semiconductors, marking a critical step toward accelerating the widespread adoption of heterogeneous integration technology.

Strategic Significance & Outlook

The successful III-V chiplet integration on imec's RF silicon interposer platform holds the potential to revolutionize the design of next-generation wireless communication systems and edge AI devices. Improvements in capacitance density and alignment precision will enable higher-performance, smaller, and more power-efficient RF modules, opening new possibilities for 5G Advanced and 6G communication infrastructure, high-precision radar for autonomous vehicles, and real-time sensing for industrial robots. The expansion into the Autonomous Edge Chiplet Program indicates that this technology is not merely a research outcome but is being pursued for practical applications across diverse industries, acting as a catalyst for innovation across the entire semiconductor industry.

Source: https://www.trendforce.com/news/2026/06/17/tsmc-accelerates-copos-development-taiwan-panel-makers-and-local-materials-and-equipment-suppliers-leverage-foplp-for-glass-core-substrate-opportunity-says-trendforce/

Nokia Announces Major Expansion of U.S. Advanced Semiconductor Test and Packaging Operations in Pennsylvania, Doubling Workforce to Over 500, to Bolster AI Infrastructure

Published June 16, 2026 GlobeNewswire USA

OVERVIEW

Nokia has unveiled a major expansion of its Advanced Test and Packaging (ATP) operations in Allentown, Pennsylvania. This investment aims to enhance domestic production capacity for optical networking technologies vital for scalable AI infrastructure connections, with plans to double the Pennsylvania workforce to over 500 employees. The expansion is part of Nokia's $4 billion U.S. R&D and manufacturing investment plan for AI-ready network connectivity, strengthening the semiconductor supply chain in the U.S.

IN DEPTH

Key Findings

Nokia has announced a significant expansion of its Advanced Test and Packaging (ATP) operations located in Allentown, Pennsylvania, USA. This crucial investment is designed to dramatically improve the domestic production capacity for optical networking technologies, which are essential for scalable artificial intelligence (AI) infrastructure connectivity. The plan includes doubling the workforce in Pennsylvania to over 500 employees, thereby making a substantial contribution to strengthening the U.S.'s AI-related technology development and manufacturing base.

Technical / Clinical Details

This expansion will specifically bolster the development, testing, and packaging capabilities for semiconductors dedicated to optical networking technologies. The focus will be on producing ultra-high-speed, low-latency optical communication chips, which are indispensable for efficiently processing AI and machine learning workloads. Nokia's ATP facility will be capable of handling these chips comprehensively, from initial design through final testing and advanced packaging. The expanded facility will incorporate more advanced automation, precise testing equipment, and environmental control systems, leading to improved manufacturing process efficiency and yield rates. This ensures the supply of highly reliable and high-performance optical components necessary to handle the enormous data traffic between AI data centers.

Background & Context

The widespread adoption of AI and the ensuing surge in demand for inter-data center connectivity and cloud infrastructure are placing immense strain on existing network infrastructure. To address this challenge, optical networking technologies, particularly high-bandwidth optical transceivers and optical switch chips, have become increasingly critical. The U.S. government, through initiatives like the CHIPS Act, is promoting the domestic production of semiconductors. Nokia's investment is part of its $4 billion U.S. R&D and manufacturing investment plan for AI-ready network connectivity. This represents a strategic move for the U.S. to maintain competitiveness in the AI-driven digital infrastructure era and ensure supply chain resilience.

Strategic Significance & Outlook

Nokia's expansion of its ATP operations in Pennsylvania will play a pivotal role in solidifying the company's position as a key infrastructure provider in the AI era. Strengthening domestic production capacity for optical networking technologies will enhance the security and reliability of U.S. communication infrastructure, while also accelerating the deployment of high-speed networks that underpin AI advancements. The doubling of the workforce will contribute to regional job creation and the development of skilled technical talent. In the long term, this is expected to foster the growth of the broader U.S. technology ecosystem. This investment is poised to become an indispensable foundation for the realization of next-generation AI applications.

Source: https://www.globenewswire.com/news-release/2026/06/16/3295066/0/en/Nokia-announces-major-expansion-of-U-S-semiconductor-advanced-test-and-packaging-in-Pennsylvania-to-bolster-AI-growth.html

Collected: June 19, 2026 | Automated Research System (Gemini API)

Amkor Technology Shifts SiP Production to Vietnam to Enhance High-Value Programs, Driven by Strong Demand for Advanced Packaging in Premium Smartphones

Published June 17, 2026 TradingView USA

OVERVIEW

Amkor Technology continues to benefit from robust demand for advanced packaging solutions like flip-chip and System-in-Package (SiP), fueled by increased semiconductor content in premium smartphones. The company is strategically expanding advanced packaging capacity in South Korea and Taiwan while relocating some SiP production to Vietnam to free up space for higher-value programs. This strategy aims to sustain Amkor's growth momentum by aligning resources with evolving smartphone market demands and focusing on profitable segments.

IN DEPTH

Key Findings

Amkor Technology continues to significantly benefit from robust demand for advanced packaging solutions such as flip-chip and System-in-Package (SiP). This demand is driven by the architectural shift towards premium smartphones and the associated increase in semiconductor content per handset. To sustain this growth momentum, Amkor is strategically expanding its advanced packaging capacity in South Korea and Taiwan while concurrently relocating some SiP production to Vietnam. This move aims to free up production space for higher-value programs, showcasing Amkor's proactive strategy to adapt to market changes and optimize resource allocation.

Technical / Clinical Details

Flip-chip packaging is a technology that directly connects a semiconductor die to a substrate, offering superior electrical performance and thermal characteristics compared to traditional wire bonding. System-in-Package (SiP), on the other hand, is an advanced packaging solution that integrates multiple semiconductor dies and passive components within a single package, enabling space savings and improved system performance. In premium smartphones, SiP is widely adopted for components such as camera modules, RF front-end modules, and power management ICs. Amkor possesses strong capabilities in these advanced technologies. While reinforcing capacity at existing facilities in South Korea and Taiwan, the company is advancing the transfer of SiP production to Vietnam. The Vietnamese facility will leverage cost-effective labor and efficient cost structures to handle standard SiP production, allowing the South Korean and Taiwanese sites to specialize in high-value, complex advanced packaging.

Background & Context

Although the smartphone market is reaching maturity, the premium segment continues to drive demand for more complex and sophisticated chipsets, propelled by the integration of AI features, enhanced camera performance, and 5G connectivity. This trend increases the semiconductor content per handset, leading to higher demand for advanced packaging solutions like SiP and flip-chip. Amkor's strategy is to capitalize on this market trend by focusing investments on high-growth areas. The relocation of production to Vietnam also aligns with the broader semiconductor industry trend of diversifying global manufacturing bases and enhancing supply chain resilience, allowing the company to mitigate geopolitical risks and secure cost competitiveness.

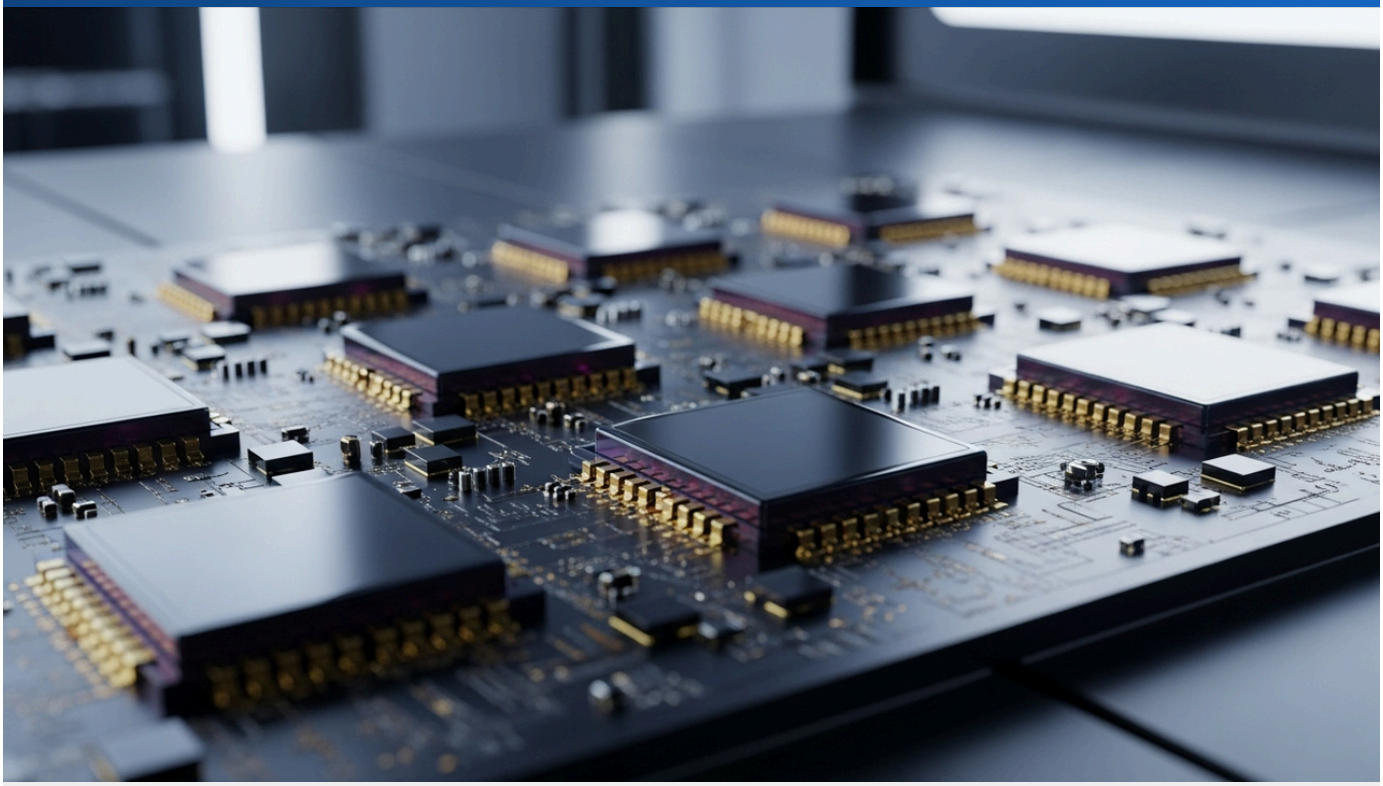
Strategic Significance & Outlook

Amkor Technology's strategic reorganization of its production footprint and capacity enhancement is a crucial step for the company to effectively respond to changing semiconductor market demands and achieve sustained growth. As long as the premium smartphone market continues to grow and AI technology proliferates, demand for advanced packaging solutions like flip-chip and SiP is expected to remain strong. Amkor is, through its focus on high-value programs and the establishment of an efficient global production system, poised to maintain its competitive advantage and further strengthen its position as a major player in the semiconductor packaging market. For investors, this strategy is noteworthy as a factor in sustaining the company's stock momentum.

Source: https://www.tradingview.com/news/zacks:9c1a329d8d1e8:0/can-strong-smartphone-demand-sustain-amkrs-growth-momentum/

imec Breaks New Ground: III-V Chiplets on RF Silicon Interposer Achieve 100x Capacitance Density Boost and Sub-600nm Precision

Published Published June 15, 2026 OriginBrief ベルギー



OVERVIEW

imec has announced a significant breakthrough in heterogeneous integration, successfully integrating III-V chiplets onto a 300mm RF silicon interposer platform. This achievement delivers a 10-100x increase in capacitance density and sub-600nm alignment precision, unlocking new possibilities for high-performance RF and power applications. The technology promises to accelerate advancements in next-generation wireless communications and edge AI, with imec expanding its focus to autonomous edge applications like robotics and intelligent infrastructure.

IN DEPTH

Background

The escalating demand for high-performance RF systems, fueled by the proliferation of 5G/6G communications, advanced radar, satellite systems, and burgeoning edge AI devices, necessitates operation at increasingly high frequencies with wide bandwidths, low power consumption, and compact form factors. Traditional monolithic (single-chip) design approaches struggle to concurrently optimize RF components, which often require diverse material properties, alongside digital logic on a single die. The chiplet architecture emerges as a compelling solution to this challenge, enabling the integration of specialized chips fabricated through optimized, disparate processes. imec's latest achievement, particularly in the RF domain, represents a pivotal stride towards leveraging the cost-effectiveness and maturity of silicon platforms in conjunction with the superior performance characteristics of III-V semiconductors, thereby accelerating the widespread adoption of heterogeneous integration technology.

Key Findings

imec, a global leader in nanoelectronics and digital technologies, has announced a groundbreaking achievement in system-level III-V chiplet integration. Leveraging a 300mm RF silicon interposer platform, imec engineers successfully integrated III-V semiconductor chiplets, demonstrating a significant 10 to 100-fold increase in capacitance density compared to prior technologies. This breakthrough also showcases an exceptionally high alignment precision of less than 600 nanometers. These advancements are set to unlock unprecedented integration possibilities for high-performance RF and power applications within heterogeneous chiplet architectures, promising to profoundly impact the development of next-generation electronic systems by enabling smaller, higher-performance modules for critical components such as RF transceivers and power amplifiers.

Technical Details

The core of this innovation lies in imec's specialized RF silicon interposer platform, which facilitates the co-integration of high-quality (high-Q) integrated passives alongside advanced III-V semiconductor chiplets on a robust silicon substrate. While III-V semiconductors are renowned for their superior high-frequency performance and power efficiency—attributes difficult to match with conventional SiGe-based technologies—their direct integration with silicon has historically posed substantial technical challenges. imec overcame these hurdles through meticulous optimization of high-density wiring layers and advanced micro-bump interconnection technologies. This optimization was crucial in achieving the sub-600nm alignment precision, which is critical for maximizing both electrical and thermal coupling between the high-performing III-V chiplets and the silicon interposer, ensuring optimal system performance and reliability.

Strategic Significance and Outlook

This successful integration of III-V chiplets on imec's RF silicon interposer platform carries profound strategic significance, poised to revolutionize the design paradigms for next-generation wireless communication systems and sophisticated edge AI devices. The enhanced capacitance density and unprecedented alignment precision will be instrumental in creating higher-performance, significantly smaller, and more power-efficient RF modules. This opens vast new possibilities for critical applications such as 5G Advanced and future 6G communication infrastructure, high-resolution radar systems essential for autonomous vehicles, and real-time sensing capabilities crucial for industrial robotics. Moreover, imec's strategic expansion of its Automotive Chiplet Program into the broader Autonomous Edge Chiplet Program underscores a clear commitment to accelerating the practical application of this technology. This initiative focuses on edge AI applications that demand exceptional reliability and real-time processing, encompassing robotics, industrial automation, security, and intelligent infrastructure. By serving as a catalyst for innovation across diverse industries, imec's work is set to drive significant advancements throughout the entire semiconductor industry.

Source: https://www.originbrief.com/semiconductor-chip-industry-weekly-report-june-15-2026/