Semiconductor Packaging

Weekly Intelligence Report

2026-06-07 | 27 articles | 9 countries

troy-technical.jp

This Week's Keyword

AI Packaging Bottleneck

Capacity, 3D Integration & CPO Drive Innovation

27	9	$1.3-1.4B	120K
articles	countries	USD	wafers/month
Total Articles Analyzed	Source Countries/Regions	KLA FY26 Pkg Revenue	TSMC CoWoS Capacity Target

All 27 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	ASMPT Adv. Pkg Council	Corp Strategy	●●○○○	●●●●○	●●●○○	●●○○○	●●●●○	ASMPT forms advisory council to guide R&D; roadmap for AI-era advanced packaging, including HBM, CoWoS.
#02	KLA Pkg Biz Soars	Market Report	●●○○○	●●●●●	●●●●○	●●●○○	●●●●●	KLA projects $1.3B+ revenue in FY2026 for advanced packaging, driven by AI inspection demand.
#03	TSMC CoWoS Bottleneck	Supply Chain	●○○○○	●●●●●	●●●●○	●●●○○	●●●●●	TSMC's CoWoS capacity, despite quadrupling to 120K wafers/month by late 2026, still bottlenecks AI chip supply.
#04	Imec/EVG Hybrid Bond	Research	●●●●●	●●○○○	●●●●○	●●●●●	●●●●●	Imec & EVG achieve world-record <40nm overlay accuracy in 200nm pitch W2W hybrid bonding for 3D ICs.
#05	Samsung HBM4E Samples	New Product	●●●●○	●●●●○	●●●●●	●●●●○	●●●●○	Samsung ships first 12-layer HBM4E samples, improving energy efficiency 16% and thermal resistance 14%.
#06	Intel India Glass Sub	Investment	●●●○○	●●●○○	●●●●○	●●●○○	●●●●●	Intel invests $3.3B in India for glass core substrate manufacturing, bolstering advanced packaging supply.
#07	CEA-Leti D2W Hybrid	Research	●●●●○	●●○○○	●●●●○	●●●●●	●●●●●	CEA-Leti demonstrates functional 1µm pitch D2W hybrid bonding, addressing AI hardware bottlenecks.
#08	AMD Taiwan Investment	Investment	●●○○○	●●●●○	●●●●○	●●●○○	●●●●●	AMD invests $10B+ in Taiwan for AI infrastructure and advanced packaging, including EFB tech.
#09	AMAT Record Revenue	Market Report	●●○○○	●●●●●	●●●●○	●●●○○	●●●●●	Applied Materials reports record Q2 2026 revenue, with advanced packaging sales to accelerate 50%+ for AI.
#10	Amkor US Expansion	Investment	●●○○○	●●●●○	●●●●○	●●●○○	●●●●●	Amkor expands Arizona campus to become first high-volume US advanced packaging OSAT facility.
#11	Dow AI Thermal Mgmt	Tech Showcase	●●●○○	●●●●○	●●●○○	●●○○○	●●●●●	Dow showcases next-gen thermal management for AI servers and 400G+ optical transceivers.
#12	Hiwin/Qualcomm PLP AI	Collaboration	●●●○○	●●●○○	●●●○○	●●○○○	●●●●○	Hiwin & Qualcomm integrate Edge AI into PLP equipment for enhanced accuracy and throughput.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#13	GF Malta Fab Expand	Investment	●○○○	●●●●	●●●●	●●●○	●●●●	GlobalFoundries triples Malta fab capacity with $16B CHIPS Act investment, targeting 1.5M wafers/year.
#14	Intel Pkg Push	Corp Strategy	●●●○	●●●●	●●●●	●●●○	●●●●	Intel expands EMIB/Foveros capacity to revive foundry business, attracting Google/Amazon.
#15	Hybrid Bonding 3D IC	Trend Analysis	●●●○	●●●○	●●●●	●●○○	●●●●	Hybrid bonding drives 3D integration for AI accelerators and chiplets, reducing parasitics.
#16	Samsung Vietnam Test	Investment	●○○○	●●●●	●●●○	●●●○	●●●○	Samsung invests $1.5B in Vietnam for memory chip testing, strengthening global supply chain.
#17	Marvell 102.4Tbps Switch	New Product	●●●●	●●●●	●●●●	●●●●	●●●●	Marvell unveils industry's first 102.4 Tbps AI switch, doubling bandwidth with CPO for data centers.
#18	Credo Acquires DustPho	M&A;	●●●○	●●●●	●●●●	●●●○	●●●●	Credo acquires DustPhotonics, bolstering Co-Packaged Optics (CPO) solutions for AI data centers.
#19	SK Group AI Alliances	Partnership	●●●○	●●●●	●●●●	●●●○	●●●●	SK Group deepens alliances with Nvidia & TSMC for next-gen HBM and advanced packaging collaboration.
#20	Fraunhofer Chiplet Sys	Research	●●●●	●●○○	●●●●	●●●●	●●●●	Fraunhofer IPMS develops high-density wafer-level chiplet systems for AI/HPC integration.
#21	Samsung AI Chiplet	Product Roadmap	●●●○	●●●○	●●●●	●●○○	●●●●	Samsung reportedly launching physical AI chiplet platform next year for AI inference/infrastructure.
#22	Synopsys EDA for AI	EDA Solution	●●●○	●●●●	●●●●	●●●○	●●●●	Synopsys enhances EDA for AI/multi-die designs on Samsung Foundry processes, boosting power/performance.
#23	Cadence/Samsung 3D-IC	EDA Solution	●●●○	●●●●	●●●●	●●●○	●●●●	Cadence & Samsung deepen 2nm/3D-IC collaboration for AI infrastructure, enhancing chip performance.
#24	ECTC 2026 Pkg Highlights	Conference Summary	●●●○	●●○○	●●●●	●●●○	●●●●	ECTC 2026 highlights glass core substrates, EMIB-T, and 3D integration for AI/HPC scalability.
#25	Singapore Test Market	Market Report	●○○○	●●●●	●●○○	●●●○	●●○○	Singapore semiconductor testing equipment market projected to reach $310M by 2033 (7.8% CAGR).
#26	Tsinghua Huawei 3D Tool	Research	●●●○	●●○○	●●●●	●●●○	●●●○	Tsinghua develops 3D chip design tool for Huawei's 'LogicFolding' architecture, boosting China's ecosystem.
#27	ECTC 2026 Research	Conference Summary	●●●○	●●○○	●●●●	●●●○	●●●●	ECTC 2026 program reveals latest research in 3D integration, hybrid bonding, new substrates, thermal mgmt.

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI chip supply chain exposed to CoWoS bottlenecks?

TSMC's CoWoS capacity remains a critical bottleneck for AI chip growth, with demand projected to outstrip supply even after quadrupling capacity by late 2026. US/EU AI chip developers must assess their reliance on CoWoS and explore alternative advanced packaging solutions like Intel's EMIB/Foveros or OSAT partnerships to mitigate supply risks.

❷ Are you ready for hybrid bonding's impact on 3D IC design?

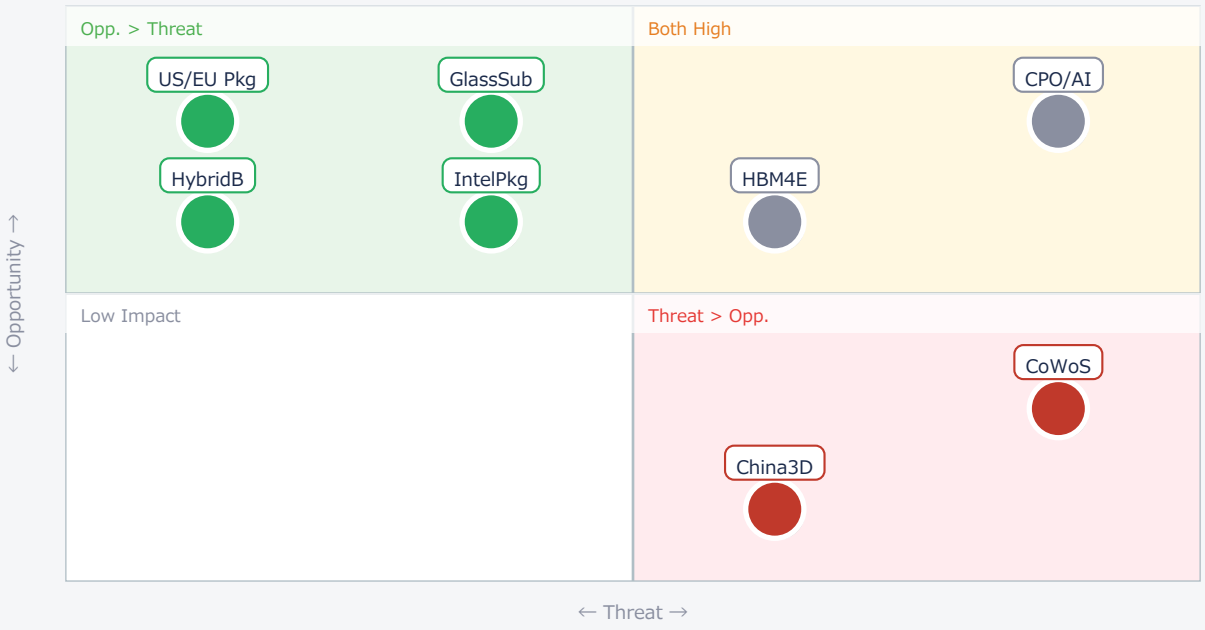
Breakthroughs from Imec/EVG (200nm pitch, <40nm overlay) and CEA-Leti (1µm D2W) demonstrate hybrid bonding's potential for ultra-high-density 3D integration. This technology is fundamental for next-gen AI accelerators and chiplets. US/EU R&D; and design teams must integrate hybrid bonding capabilities into their roadmaps to stay competitive.

❸ How will CPO and advanced thermal management redefine AI data centers?

Marvell's 102.4 Tbps AI switch with CPO and Credo's acquisition of DustPhotonics highlight the shift to optical-electronic integration for AI data center networks. Dow's new thermal materials are also critical. US/EU data center operators and component suppliers must rapidly adopt these technologies to meet escalating bandwidth and power efficiency demands.

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
CoWoS	Threat	Alt pkg demand	AI chip supply crunch
HybridB	Opp.	Next-gen 3D ICs	Obsolete legacy pkg
HBM4E	Critical	AI memory perf	SK/Samsung lead
GlassSub	Opp.	New pkg platform	Organic sub comp

CPO/AI	Critical	AI network scale	Legacy network obs
US/EU Pkg	Opp.	Resilient supply	Asia dominance
IntelPkg	Opp.	Foundry alt pkg	TSMC/OSAT comp
China3D	Threat	—	China tech indep

Deep Dive ① — Hybrid Bonding Breakthrough for 3D ICs

#04 | 2026/05/28 | PR Newswire | Tech Novelty●●●●● Proximity●●○○○ Market Impact●●●●○ Data Reliability●●●●● US/EU Relevance●●●●●

Imec and EV Group achieved a world-record post-bond overlay accuracy of less than 40 nanometers across a 300mm wafer for 200nm copper interconnect pad pitch wafer-to-wafer hybrid bonding. This breakthrough, demonstrated at IEEE ECTC 2026, utilized SiCN as a dielectric and optimized chemical mechanical polishing.

This ultra-high precision is crucial for future logic-on-logic and memory-on-logic tier stacking, enabling extremely high interconnect densities essential for CMOS 2.0 scaling paradigms in AI and HPC. Hybrid bonding eliminates solder/microbumps, reducing parasitic capacitance and inductance for faster, more efficient data transfer.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: This is a fundamental technical breakthrough, pushing the limits of 3D integration. The published numbers are highly reliable, coming from a peer-reviewed conference. Technical barriers remain in scaling this precision to high-volume manufacturing and ensuring long-term reliability across diverse materials. [Opportunity] for US/EU materials & equipment suppliers to develop compatible processes and tools. [Threat] for OEMs relying on traditional packaging, as this technology could enable vastly superior AI/HPC chips. Next actions: [R&D;] Evaluate hybrid bonding readiness and roadmap by Q4 2026; [Business Dev] Explore partnerships with Imec/EVG by end of Q3 2026.

Deep Dive ② — Samsung Ships First 12-Layer HBM4E Samples

#05 | 2026/05/28 | Samsung Electronics | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●○

Samsung Electronics has begun shipping industry-first 12-layer HBM4E samples, delivering up to 3.6TB/s bandwidth per stack. This HBM4E improves energy efficiency by 16% and thermal resistance by over 14% compared to HBM4, leveraging Samsung's 1c DRAM process and a 4nm foundry logic base die.

The advanced logic base die and 2.xD Cube Packaging enable system-level co-optimization for high bandwidth and energy efficiency, crucial for next-generation AI and HPC systems. Samsung plans to ramp HBM4E production to customer schedules, intensifying competition in the high-bandwidth memory market.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: Samsung's HBM4E samples are a significant product announcement, directly impacting the AI memory market. The performance numbers (16% efficiency, 14% thermal resistance) are credible for a new generation, though real-world application performance will vary. Technical barriers include yield scaling for 12-layer stacks and integration with diverse AI accelerators. [Opportunity] for US/EU AI chip designers to leverage this advanced memory for higher performance. [Threat] for US/EU memory competitors (e.g., Micron) and packaging firms, as Samsung strengthens its integrated memory-packaging offering. Next actions: [R&D;] Benchmark HBM4E against competitor roadmaps by Q3 2026; [Procurement] Engage Samsung for sample evaluation and supply chain planning by Q3 2026.

Deep Dive ③ — Marvell Unveils 102.4 Tbps AI Switch with CPO

#17 | 2026/06/03 | Advanced Packaging News | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●●

Marvell announced the industry's first 102.4 Tbps AI switch, doubling bandwidth compared to current top-performing switches. This breakthrough is achieved through advanced semiconductor packaging and Co-Packaged Optics (CPO) solutions, integrating optical and electronic components within the same package.

This innovation dramatically improves data transfer capabilities for high-performance computing environments, addressing critical data movement bottlenecks in large-scale AI model training and inference. It enables ultra-high-speed, low-latency data transfer by reducing signal loss and power consumption associated with traditional electrical signaling.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: Marvell's AI switch is a major product announcement, setting a new benchmark for AI data center networking. The 102.4 Tbps figure is a clear, impactful metric. The primary technical barrier is the maturity and cost-effectiveness of CPO technology for mass deployment, as well as ecosystem development. [Opportunity] for US/EU data center operators to significantly scale AI infrastructure and for component suppliers (e.g., photonics, thermal management) to integrate with CPO solutions. [Threat] for traditional network equipment providers and those not rapidly adopting CPO, as their offerings risk obsolescence. Next actions: [R&D;] Evaluate CPO integration strategies for future products by Q4 2026; [Procurement] Assess Marvell's switch and CPO ecosystem partners for AI infrastructure upgrades by Q3 2026.

Other Notable Articles

TSMC CoWoS Capacity Becomes Major AI Chip Growth Bottleneck (backplane)
TN●○○○○ P●●●●● MI●●●●●

TSMC's CoWoS capacity remains the critical bottleneck for AI chip supply, impacting all major AI developers.

CEA-Leti Demonstrates 1µm Pitch Die-to-Wafer Hybrid Bonding (Chiplet Marketplace)
TN●●●●○ P●●○○○ MI●●●●○

CEA-Leti's 1µm pitch D2W hybrid bonding is a key EU research advance for high-density 3D AI integration.

Intel Commits to Massive Advanced Packaging Push for Foundry Revival (BusinessKorea)
TN●●●○○ P●●●●○ MI●●●●●

Intel's aggressive expansion of EMIB/Foveros is a strategic move to challenge TSMC and attract AI customers.

Fraunhofer IPMS Develops High-Density Chiplet Systems at Wafer Level (Design And Reuse)
TN●●●●○ P●●○○○ MI●●●●○

Fraunhofer's wafer-level chiplet systems advance EU leadership in high-density integration for AI/HPC.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Assess current and projected exposure to TSMC CoWoS capacity bottlenecks for all AI-related projects. Identify alternative packaging options.
- [R&D;] Review internal roadmaps for hybrid bonding and 3D integration to ensure alignment with latest breakthroughs from Imec/EVG and CEA-Leti.

Short-term (1 month)

- [Strategy] Evaluate Intel's EMIB/Foveros and US/EU OSAT capabilities (e.g., Amkor) as potential alternative advanced packaging suppliers to diversify supply chains.
- [R&D;] Initiate feasibility studies on Co-Packaged Optics (CPO) and advanced thermal management solutions for next-generation AI hardware and data center designs.
- [Business Dev] Engage with Samsung to understand HBM4E sample availability, performance benchmarks, and future mass production schedules.

Medium-long term (quarter+)

- [Executive] Develop a comprehensive strategy for advanced packaging supply chain resilience, including regional manufacturing investments (US/EU CHIPS Act opportunities).
- [Legal/IP] Monitor the development of China's indigenous 3D chip design tools (e.g., Tsinghua/Huawei) for potential competitive threats and IP implications.
- [R&D;] Establish cross-functional teams to integrate advanced materials (e.g., glass core substrates) and EDA tools (Synopsys/Cadence) into future AI chip designs.

Semiconductor_BackEnd — Selected Articles

Date: 2026-06-07

Articles: 27

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#06 Intel to Build $3.3 Billion Glass Core Substrate Manufacturing Facility in India to Bolster Advanced Packaging Supply

#07 CEA-Leti Demonstrates 1μm Pitch Die-to-Wafer Hybrid Bonding, Addressing AI Hardware Bottlenecks

#08 AMD Announces Over $10 Billion Taiwan Ecosystem Investment to Bolster AI Infrastructure and Advanced Packaging Manufacturing

#09 Applied Materials Achieves Record $7.91 Billion Revenue in Q2 2026, Advanced Packaging Business to Accelerate Over 50% for AI

#10 Amkor Technology Acquires 67 Additional Acres in Arizona, Expanding U.S. Advanced Packaging Footprint

#11 Dow Showcases Next-Gen AI Thermal Management Technologies at COMPUTEX Taipei 2026, Supporting 400G+ Optical Transceivers

#12 Hiwin and Qualcomm Integrate Edge AI into Panel-Level Semiconductor Packaging to Enhance Production Accuracy and Throughput

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#21 Samsung Reportedly to Launch Physical AI Chiplet Platform Next Year, Accelerating AI Inference and Infrastructure

#22 Synopsys Enhances Power and Performance for AI and Multi-Die Designs on Latest Samsung Foundry Processes

#23 Cadence and Samsung Foundry Deepen 2nm and 3D-IC Collaboration to Meet Surging AI Infrastructure Demand

#24 IEEE ECTC 2026 Highlights Packaging Technologies Redefining AI and HPC Scalability Limits

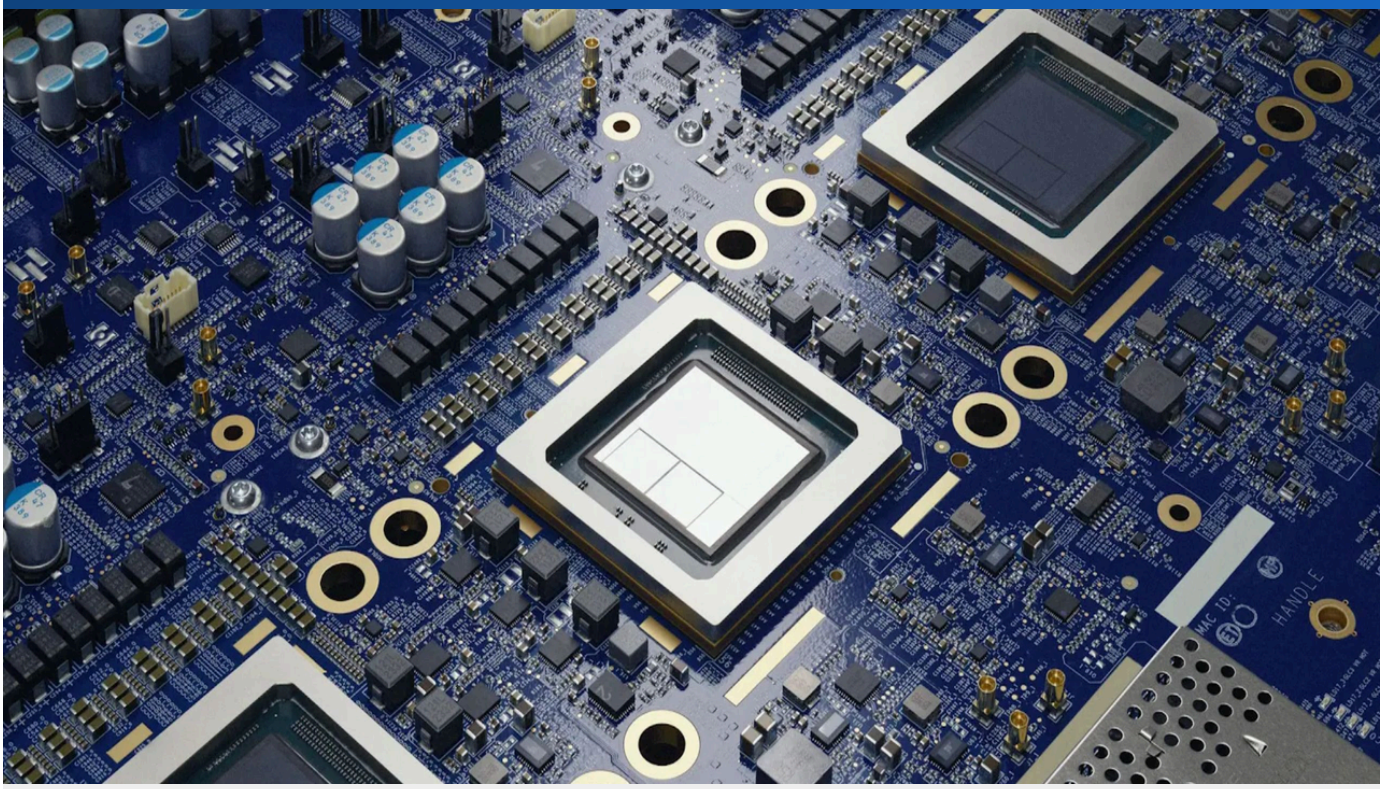
#25 Singapore Semiconductor Testing Equipment Market Projected to Reach $310 Million by 2033, Growing at 7.8% CAGR

#26 Tsinghua University Develops 3D Chip Design Tool Tailored for Huawei's 'LogicFolding' Architecture

#27 IEEE ECTC 2026 Program Reveals Latest Research in Advanced Packaging, Including 3D Integration, Hybrid Bonding, and New Substrate Materials

ASMPT Establishes Advanced Packaging Technology Advisory Council to Accelerate AI-Era Innovation

Published May 28, 2026 ASMPT Singapore



OVERVIEW

ASMPT has established an Advanced Packaging Technology Advisory Council (TAC) to address the growing importance of advanced packaging for next-generation computing and AI components. The TAC will focus on a broad range of emerging packaging formats, including HBM, CoWoS, EMIB-T, photonics, and 2.5D/3D/3.5D heterogeneous integration, to provide strategic guidance for ASMPT's R&D roadmap. This initiative aims to accelerate innovation within the AI ecosystem and overcome technical bottlenecks in advanced packaging.

IN DEPTH

Key Findings

ASMPT has formed an Advanced Packaging Technology Advisory Council (TAC) to respond to the escalating importance of advanced packaging in enabling next-generation computing and artificial intelligence (AI) components. This strategic move underscores ASMPT's commitment to leading semiconductor innovation in the AI era.

Technical Details

The TAC will concentrate on a comprehensive array of next-generation packaging formats and emerging trends. These include advanced memory (High-Bandwidth Memory (HBM) & HBM Fabric (HBF)), Chip-on-Wafer-on-Substrate (CoWoS) & Embedded Multi-die Interconnect Bridge (EMIB-T), integrated photonics, and 2.5D/3D/3.5D heterogeneous integration ecosystems. The council aims to address the complexities of advanced packaging technologies and provide strategic guidance for ASMPT's R&D roadmap, thereby overcoming critical technical bottlenecks in the industry. Furthermore, ASMPT has introduced Active Oxide Removal (AOR) TCB™ technology to tackle key challenges in HBM manufacturing. This fluxless thermocompression bonding approach ensures clean, residue-free interconnects, improves bonding uniformity, and eliminates contamination risks, leading to reduced defects, accelerated yields, and lower overall cost per bit for next-generation HBM production.

Background and Context

Taiwan, a global hub for the semiconductor and electronics supply chain, demands highly specialized processes, stringent quality requirements, and rapid production cycles. Headquartered in Singapore, ASMPT provides hardware and software solutions for the semiconductor assembly, packaging, and SMT industries, spanning from wafer deposition to assembly and packaging. The advent of AI has led to a surge in demand for high-density, high-performance, and low-power packaging solutions, making advanced packaging technology evolution crucial for enhancing AI chip performance and accelerating time-to-market.

Strategic Significance and Outlook

The establishment of the TAC highlights ASMPT's dedication to strengthening its leadership in advanced packaging and proactively addressing the technical challenges of the AI era. By providing strategic direction for its R&D roadmap, ASMPT will be better equipped to rapidly develop innovative solutions that meet the demands of future AI and HPC applications. Combined with technological advancements like AOR TCB™, ASMPT is expected to boost the efficiency and reliability of HBM and other advanced packaging manufacturing, thereby supporting the growth of the entire AI ecosystem.

Source: https://www.asmpt.com/en/newsroom/press-releases/2026/asmpt-forms-technical-advisory-council-to-accelerate-ai-era-innovation/

KLA's Advanced Packaging Business Soars, Projecting Over $1.3B Revenue in FY2026 Driven by AI Inspection Demand

Published May 31, 2026 Bitget USA

OVERVIEW

KLA Corporation, a global leader in semiconductor process control and yield management, is experiencing rapid growth in its advanced packaging business, driven by the increasing complexity of AI chips. Revenue from this segment is projected to reach $1.3-1.4 billion in fiscal year 2026, marking approximately 57% year-over-year growth from an estimated $925 million in 2025. This surge is fueled by demand for high-end inspection systems in HBM memory stacking, CoWoS/SoIC substrate inspection for AI accelerator packaging, and fan-out wafer-level packaging for mobile SoCs.

IN DEPTH

Key Findings

KLA Corporation has announced remarkable growth in its advanced packaging business, solidifying its position as a global leader in semiconductor process control and yield management. Revenue from its advanced packaging division is projected to reach between $1.3 billion and $1.4 billion in fiscal year 2026, representing an impressive year-over-year growth of approximately 57% from an estimated $925 million in 2025. This growth is robustly driven by the escalating demand for advanced inspection and measurement systems in AI chip manufacturing.

Technical Details

KLA's expansion is propelled by the continuous scaling of AI infrastructure. The increasing demand for GPUs, high-bandwidth memory (HBM), and advanced semiconductor packaging exacerbates the complexity of the entire wafer manufacturing process. KLA has established a leading position in HBM memory stacking inspection (with SK Hynix and Micron as key customers), CoWoS/SoIC substrate inspection for AI accelerator packaging at TSMC, and fan-out wafer-level packaging for mobile SoCs. KLA's high-end inspection systems are crucial for defect detection and yield optimization, addressing the intricate challenges posed by the proliferation of chip stacking and hybrid bonding. The adoption of EUV lithography further amplifies the need for sophisticated inspection systems.

Background and Context

The increasing complexity of AI semiconductor manufacturing necessitates unprecedented precision and control at every stage of the production process. The industry's shift towards chiplet architectures and 3D stacking technologies intensifies packaging challenges, thereby increasing reliance on advanced process control solutions. KLA leverages its comprehensive portfolio of defect review, critical dimension (CD), and overlay measurement solutions to maintain its market leadership. While competitors like Applied Materials also anticipate rapid growth in their advanced packaging businesses for AI accelerators, KLA continues to hold a strong competitive edge in specific inspection and measurement domains.

Strategic Significance and Outlook

The sustained growth of KLA's advanced packaging business underscores the critical importance of process control in AI-era semiconductor manufacturing. With this portfolio expected to reach over $1 billion in 2026, KLA is positioned as an indispensable player in the evolution of AI infrastructure. The company's technologies are central to ensuring the reliability of HBM, the performance of AI accelerators, and the yield of next-generation mobile SoCs, and are expected to continue contributing to overall innovation and efficiency improvements across the semiconductor industry.

Source: https://www.bitget.com/stock/nasdaq-klac/what-is

Collected: June 05, 2026 | Automated Research System (Gemini API)

TSMC CoWoS Capacity Becomes Major AI Chip Growth Bottleneck: Ramping to 120K Wafers/Month by late 2026 Still Falls Short of Demand

Published June 02, 2026 backplane Taiwan

OVERVIEW

TSMC's CoWoS packaging capacity is identified as the most critical bottleneck hindering AI chip evolution. While TSMC plans to quadruple its CoWoS production capacity from approximately 35,000 wafers/month in late 2024 to 120,000–140,000 wafers/month by late 2026, demand from next-generation architectures like Nvidia's Blackwell (CoWoS-L) and AMD's Instinct MI325X is expected to continue outstripping supply. This bottleneck is primarily linked to plasma processing and thin-film deposition, specifically deep reactive ion etching for TSV formation and PVD seed layer deposition/sputtering for RDL, posing a significant supply chain constraint for the AI industry.

IN DEPTH

Key Findings

TSMC's Chip-on-Wafer-on-Substrate (CoWoS) packaging capacity has emerged as the most critical bottleneck for the production of high-end AI accelerators, effectively slowing down the evolution and market deployment of AI chips. Despite TSMC's ambitious plans to quadruple its production capacity from approximately 35,000 wafers per month in late 2024 to an estimated 120,000–140,000 wafers per month by the end of 2026, demand from next-generation architectures like Nvidia's Blackwell (utilizing CoWoS-L) and AMD's Instinct MI325X is projected to continuously outstrip the available supply.

Technical Details

CoWoS is an indispensable technology for Nvidia's AI accelerators, which integrate GPU logic dies and HBM (High-Bandwidth Memory) stacks side-by-side on a silicon interposer. The bottlenecks in this packaging process are multifaceted, with plasma processing and thin-film deposition steps being particularly critical. Specifically, deep reactive ion etching (DRIE) for Through-Silicon Via (TSV) formation, and physical vapor deposition (PVD) seed layer deposition and sputtering processes for Redistribution Layer (RDL) creation, are identified as primary contributors to the supply constraints. These processes require advanced technology and extended processing times, thereby limiting the rapid scalability of production capacity.

Background and Context

The explosive growth in demand for high-performance AI chips is intrinsically linked to the rapid expansion of AI infrastructure. However, relying solely on miniaturization, as per traditional Moore's Law, is increasingly insufficient for achieving desired chip performance gains. Consequently, advanced packaging technologies such as CoWoS, which enable chiplet and 3D integration, have become more crucial differentiators. Nvidia CEO Jensen Huang's visit to TSMC to secure CoWoS capacity for the Vera Rubin platform underscores the severity of this bottleneck. While TSMC is establishing geographically diversified manufacturing sites in Arizona, Kumamoto (JASM), and Dresden, Germany (ESMC), equipment lead times and process qualification present significant hurdles to rapid capacity expansion.

Strategic Significance and Outlook

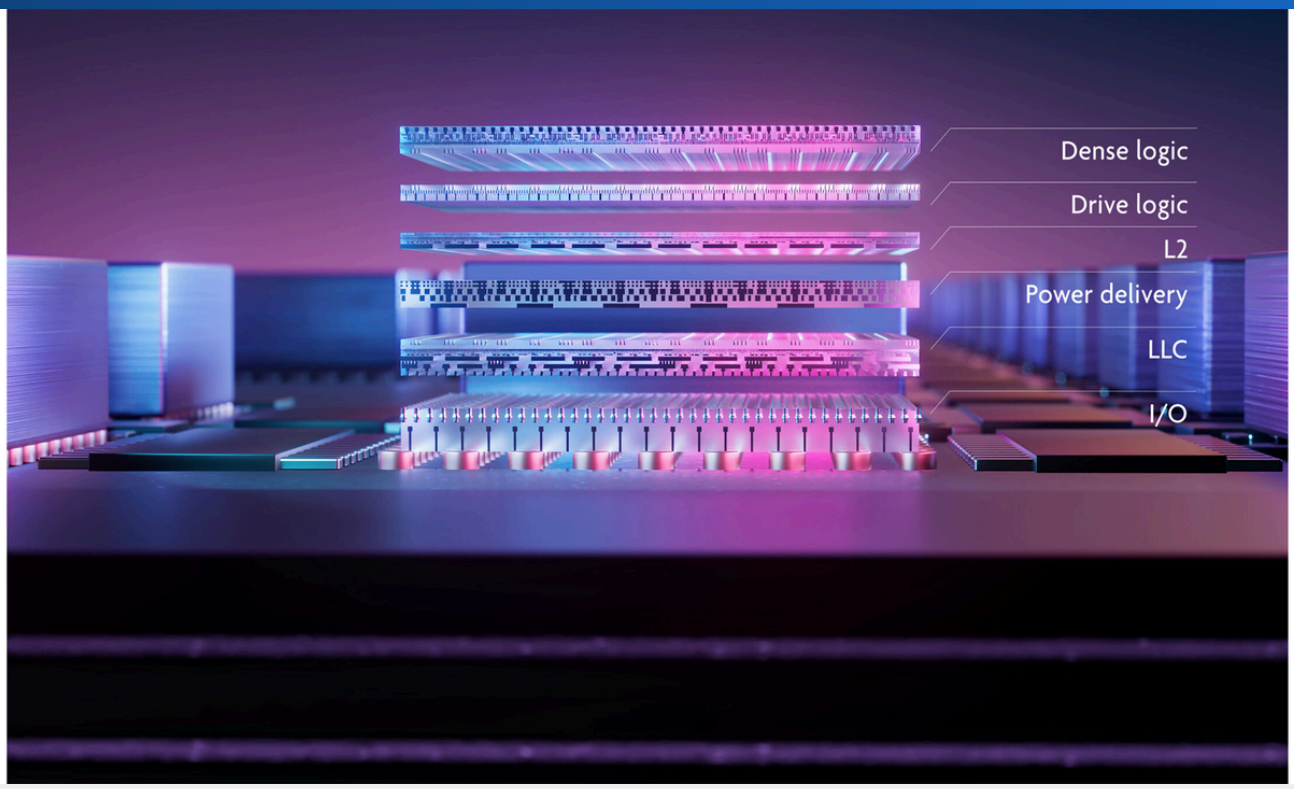
The CoWoS capacity shortage is expected to persist, with demand outstripping supply through 2025 and into 2026, a forecast reinforced by predictions at Computex 2026 that AI memory shortages will extend until 2030. This situation has prompted massive capital expenditures across the industry, such as AMD's commitment of over $10 billion to Taiwan's ecosystem for AI infrastructure and advanced packaging manufacturing. While TSMC anticipates CoWoS capacity to grow at an 80% annual rate through 2027, hyperscaler demand is still projected to exceed this expansion, indicating that the pace of AI industry growth will remain highly dependent on the timely scaling of CoWoS supply.

Source: https://www.backplane.gg/bottlenecks/cowos

Collected: June 05, 2026 | Automated Research System (Gemini API)

Imec and EV Group Set New World Record for 3D Chip Stacking Precision with Sub-40nm Wafer Bond Overlay

Published Published May 28, 2026 PR Newswire ベルギー



OVERVIEW

Imec and EV Group have achieved a world-record post-bond overlay accuracy of less than 40 nanometers across a 300mm wafer for 200nm pitch hybrid bonding, a crucial advancement for next-generation 3D ICs. Demonstrated at ECTC 2026, this robust, high-yield process on routable test vehicles enables ultra-high-density logic-on-logic and memory-on-logic stacking, critical for the CMOS 2.0 scaling paradigm and future AI accelerators. The breakthrough leverages optimized SiCN dielectric and chemical mechanical polishing.

IN DEPTH

Background

As conventional CMOS scaling approaches its fundamental physical limits, three-dimensional (3D) integration has emerged as a critical pathway to continue enhancing semiconductor performance and functionality. This approach is particularly vital for demanding applications such as AI accelerators and advanced chiplet platforms, which necessitate ultra-high-density interconnects and significantly increased bandwidth. However, a persistent challenge in vertically stacking chips has been ensuring precise alignment accuracy and robust connection reliability between tiers. Imec and EV Group's latest achievement provides a decisive solution to this long-standing hurdle, accelerating the realization of future systems—including AI, High-Performance Computing (HPC), and advanced smart vision systems—that require the extremely high interconnect densities envisioned by the CMOS 2.0 scaling paradigm.

Key Findings

Imec, a world-leading semiconductor research institute, in collaboration with EV Group (EVG), a prominent supplier of wafer processing equipment, recently showcased a robust, high-yield wafer-to-wafer hybrid bonding technology at the 2026 IEEE Electronic Components and Technology Conference (ECTC). This groundbreaking demonstration featured a 200-nanometer (nm) copper interconnect pad pitch, achieving a new world-record accuracy: a post-bond overlay vector of less than 40 nm across a full 300mm wafer. This precision represents a significant leap forward, critically enabling the realization of next-generation 3D integrated circuits (ICs).

Technical Details

The demonstrated hybrid bonding technology masterfully integrates both metal-to-metal (primarily copper-to-copper, or Cu-Cu) and dielectric-to-dielectric (oxide-to-oxide) bonding processes within a single interface. This innovative approach ensures both electrical continuity and robust mechanical integrity without the need for traditional solder or microbumps. The research utilized a sophisticated test vehicle incorporating routable interconnects, specifically designed to demonstrate the feasibility of high-density logic-on-logic and memory-on-logic tier stacking. The exceptional overlay accuracy and impressive yield were critically achieved through two key optimizations: the specific use of silicon carbon nitride (SiCN) as the dielectric material, and the meticulous optimization of the chemical mechanical polishing (CMP) step performed immediately prior to bonding. This combined technique facilitates simultaneous Cu-to-Cu and oxide-to-oxide bonding at aggressive sub-micron pitches, dramatically enabling finer interconnects and substantially reducing parasitic capacitance and inductance compared to conventional packaging methods.

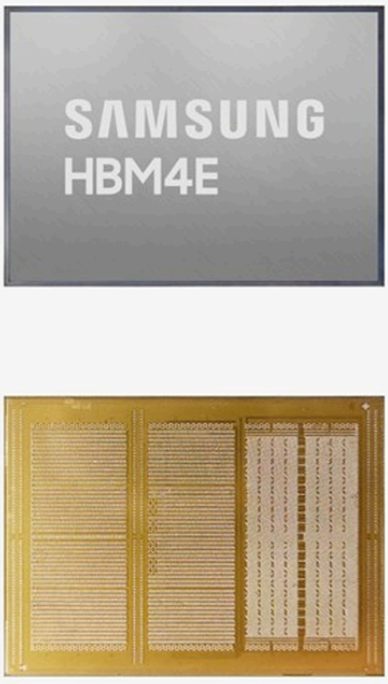
Strategic Significance and Outlook

The realization of this record-breaking hybrid bonding technology marks a profound advancement in the evolution of 3D IC stacking, unlocking new paradigms for the design of high-performance AI accelerators and other advanced chiplet-based system architectures. By dramatically reducing interconnect path lengths, this technology promises significantly improved data transfer speeds and substantial reductions in power consumption. This capability has the potential to revolutionize the performance and energy efficiency of next-generation AI hardware and High-Performance Computing (HPC) systems. The ongoing collaboration between Imec and EVG is poised to continue pushing the technical boundaries of fine-pitch interconnection, thereby fostering widespread innovation across the entire semiconductor industry.

Source: https://www.prnewswire.com/news-releases/imec-and-ev-group-demonstrate-wafer-to-wafer-hybrid-bonding-with-200nm-interconnect-pitch-and-record-high-overlay-accuracy-302783981.html

Samsung Electronics Begins Shipment of Industry's First 12-Layer HBM4E Samples, Improving Energy Efficiency by 16% and Thermal Resistance by 14% Over HBM4

Published May 28, 2026 Samsung Electronics South Korea



OVERVIEW

Samsung Electronics has commenced shipments of industry-first 12-layer HBM4E samples to key global customers. This HBM4E improves energy efficiency by 16% and thermal resistance by over 14% compared to HBM4, while delivering memory bandwidth of up to 3.6TB/s per stack. Following HBM4 mass production, Samsung plans to ramp HBM4E production to customer schedules, strengthening its leadership in the high-bandwidth memory market crucial for advancing AI chipset performance.

IN DEPTH

Key Findings

Samsung Electronics has announced the commencement of sample shipments for its 12-layer HBM4E, the industry's first such high-bandwidth memory, to leading global customers. This latest generation of HBM significantly improves energy efficiency by 16% and thermal resistance by over 14% compared to its predecessor, HBM4. It delivers an astounding memory bandwidth of up to 3.6 terabytes per second (TB/s) per stack, poised to profoundly impact the market as an essential memory solution for enhancing AI chipset performance.

Technical Details

Samsung's 12-layer HBM4E is manufactured using the company's innovative 1c DRAM process and a 4nm foundry logic base die. This combination results in a speed improvement of over 20% compared to HBM4, achieving the ultra-fast data processing capabilities required by state-of-the-art AI applications. By leveraging advanced logic nodes in the base die, power efficiency is enhanced, and data throughput is substantially increased. As I/O density continues to scale, optimizing the base die becomes a critical factor in improving overall system efficiency. Samsung Foundry integrates advanced logic, memory, and packaging within a unified development framework, enabling system-level co-optimization to deliver the high bandwidth and energy efficiency essential for next-generation AI and HPC systems.

Background and Context

The rapid evolution of AI computing and high-performance computing (HPC) has driven demand for high-bandwidth memory to unprecedented levels. HBM is a core component of AI accelerators, and its supply has become one of the primary bottlenecks for AI server capacity. With SK Hynix having gained an early lead in HBM3E market share, Samsung's HBM4E sample shipments intensify competition in the HBM market and represent a crucial effort by the company to reclaim leadership in the advanced memory sector. Samsung Foundry's 2.xD Cube Packaging demonstrates its capability to handle the increasing complexity of AI systems through heterogeneous integration of multiple chips.

Strategic Significance and Outlook

Samsung plans to begin mass production of HBM4E in line with customer schedules, following the successful mass production of HBM4. The introduction of HBM4E is expected to further boost the processing power of AI applications, providing faster and more energy-efficient solutions, particularly for training and inference of large-scale AI models. Market analysts predict that HBM supply and AI server capacity will continue to be a major bottleneck for chip manufacturers. Samsung's latest innovation is therefore crucial in alleviating this bottleneck and supporting the continued growth of the AI industry.

Source: https://news.samsung.com/global/samsung-electronics-begins-shipment-of-industry-first-hbm4e-samples

Intel to Build $3.3 Billion Glass Core Substrate Manufacturing Facility in India to Bolster Advanced Packaging Supply

Published June 01, 2026 TrendForce USA

OVERVIEW

Intel, in collaboration with 3D Glass Solutions (3DGS), is progressing with plans to invest approximately $3.3 billion in an advanced packaging glass core substrate manufacturing facility in Odisha, India. The plant, scheduled for a 5-6 year buildout, will focus on high-density interconnect substrates and related semiconductor technologies. This investment aims to enhance the supply capacity for next-generation packaging vital for AI and HPC applications, supporting Intel's goal of integrating one trillion transistors in a single package by 2030.

IN DEPTH

Key Findings

Intel, in collaboration with 3D Glass Solutions (3DGS), is moving forward with plans to invest approximately $3.3 billion in a state-of-the-art manufacturing facility for advanced packaging glass core substrates in Odisha, eastern India. This substantial investment marks a crucial step for Intel to strengthen its supply capabilities for next-generation packaging technologies, essential for artificial intelligence (AI) and high-performance computing (HPC) applications, and to achieve its ambitious goal of integrating one trillion transistors within a single package by 2030.

Technical Details

The planned facility will focus on advanced packaging glass core substrates, high-density interconnect (HDI) substrates, and related semiconductor technologies. Glass core substrates offer superior electrical, thermal, and dimensional stability compared to traditional organic substrates. These properties enable larger package sizes, finer interconnect pitches, and lower warpage, thereby resolving critical scalability bottlenecks in heterogeneous integration for AI and HPC. Intel's advanced packaging roadmap encompasses multiple technology platforms, including EMIB (Embedded Multi-die Interconnect Bridge), Foveros, and Foveros Direct, with Foveros Direct leveraging hybrid bonding to further enhance interconnect density and energy efficiency. Furthermore, Intel has successfully applied its 18A process for the first time in data center processors, the Xeon 6+, which combines Foveros Direct and EMIB technologies to achieve high-density packages with up to 288 energy-efficient cores.

Background and Context

The rise of AI has dramatically increased the importance of advanced packaging technologies for enhancing performance and optimizing power efficiency in the semiconductor industry. Amidst the industry-wide bottleneck caused by TSMC's CoWoS capacity limitations, Intel is positioning its proprietary advanced packaging technologies like EMIB and Foveros as key drivers for its foundry business revival. Absolics, a subsidiary of SKC, is expected to commence commercial production of the world's first glass substrates by the end of 2026, and Samsung Electro-Mechanics has also activated its pilot lines. Intel's investment in India aligns with the rapid growth forecast for the glass core substrate market and also with the broader trend of diversifying geopolitical supply chains and strengthening regional manufacturing capabilities.

Strategic Significance and Outlook

The new manufacturing facility in India, slated for construction over five to six years, will significantly expand Intel's global manufacturing footprint and enhance its strategic autonomy, particularly in the supply of advanced packaging materials. This initiative positions Intel to boost its competitiveness as a major foundry in the AI era, potentially gaining earlier recognition from external customers. The commercialization of glass core substrates is expected to redefine the performance limits of AI and HPC systems, and enable the integration of next-generation technologies such as co-packaged optics (CPO), thus driving innovation across the entire semiconductor industry.

Source: https://www.trendforce.com/news/2026/06/01/news-intel-advances-glass-substrate-push-with-3dgs-us3-3-billion-india-plant-set-for-five-to-six-year-buildout/

Collected: June 05, 2026 | Automated Research System (Gemini API)

CEA-Leti Demonstrates 1µm Pitch Die-to-Wafer Hybrid Bonding, Addressing AI Hardware Bottlenecks

Published May 29, 2026 Chiplet Marketplace France

OVERVIEW

CEA-Leti announced a significant advancement at ECTC 2026, demonstrating functional test vehicles utilizing die-to-wafer (D2W) hybrid bonding down to 1µm pitch, poised to resolve critical AI hardware bottlenecks. This D2W technology shortens interconnect paths, significantly boosts data transfer rates, and reduces power consumption by vertically stacking device layers at ultra-fine pitches. Successful electrical testing of structures up to 100,000 links confirms the technology's applicability for high-density interconnects, advancing 3D integration for high-density computing, smart vision, and AI.

IN DEPTH

Key Findings

CEA-Leti announced a significant breakthrough at the 2026 IEEE Electronic Components and Technology Conference (ECTC) by demonstrating functional test vehicles utilizing die-to-wafer (D2W) hybrid bonding down to a 1-micrometer (µm) pitch. This advancement addresses critical performance bottlenecks in artificial intelligence (AI) hardware and represents a major milestone in the evolution of 3D integration for high-density computing, advanced smart vision systems, and AI applications.

Technical Details

The D2W technology enables ultra-fine-pitch, high-density inter-die connections by vertically stacking device layers. This approach dramatically shortens interconnect paths between chips, resulting in significantly increased data transfer speeds and reduced power consumption. CEA-Leti successfully conducted electrical tests on structures with up to 100,000 links, confirming the technology's applicability for complex AI accelerator designs that require high-density interconnects. Hybrid bonding combines both metal-to-metal (primarily copper-copper) and dielectric-to-dielectric (oxide-to-oxide) bonding in a single interface, providing both electrical continuity and mechanical integrity without the need for solder or microbumps. This achieves dramatically finer interconnect pitches and reduces parasitic capacitance and inductance compared to traditional packaging.

Background and Context

With the explosive growth of AI, AI chips demand ever-greater data processing capabilities and higher energy efficiency. In conventional 2D architectures, data movement bottlenecks and associated power consumption increases have become severe challenges. 3D integration, particularly D2W hybrid bonding, is one of the most promising solutions to address these issues. The miniaturization of interconnects tackles critical bottlenecks in interconnect density and bandwidth for AI accelerator designs, drastically improving data transmission efficiency. This technological advancement strengthens the foundation for integrating advanced memories like HBM (High-Bandwidth Memory), chiplet-based systems, and ultimately, cutting-edge 3D packaging solutions such as Intel's Foveros Direct and TSMC's SoIC.

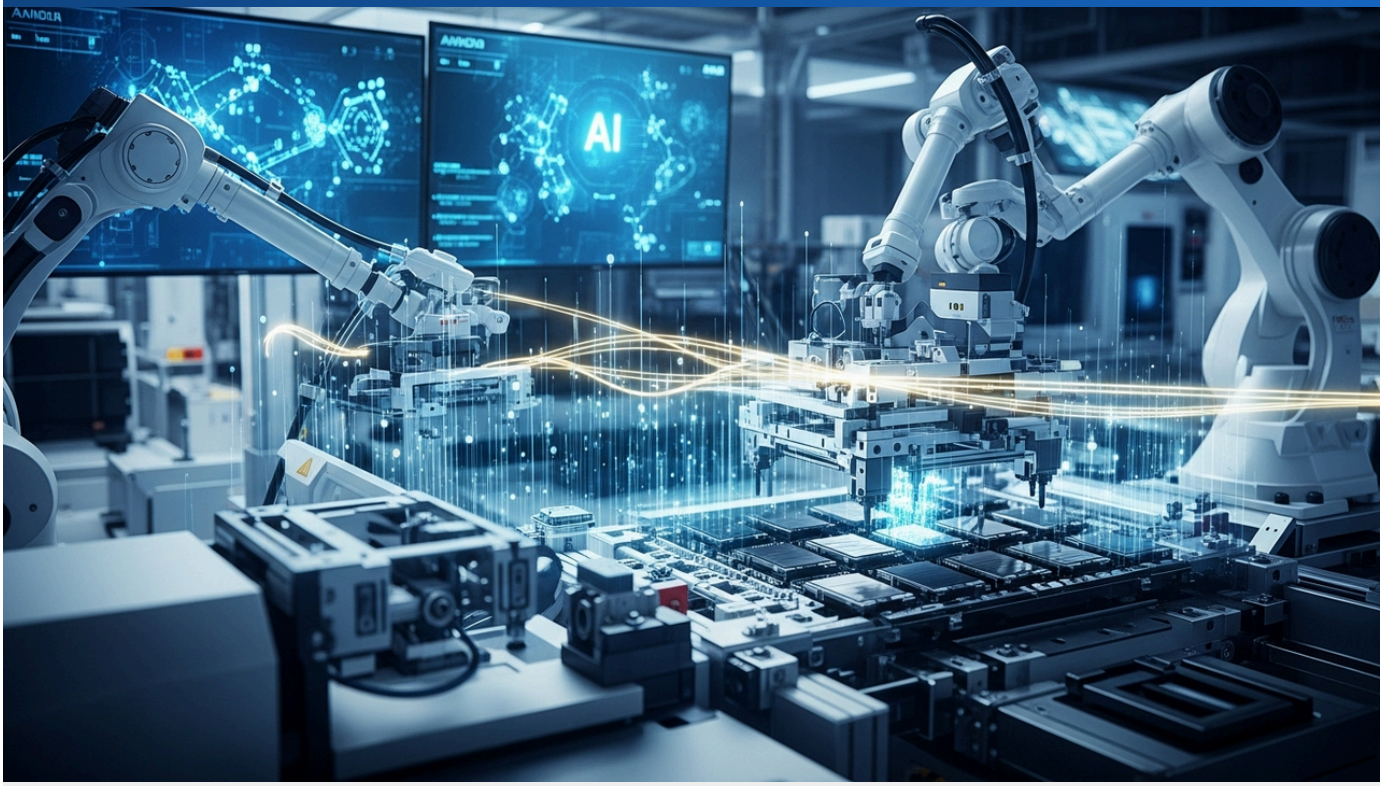
Strategic Significance and Outlook

The D2W hybrid bonding technology demonstrated by CEA-Leti holds the potential to significantly enhance the scalability and performance of AI hardware. If commercialized, this technology could lead to smaller, faster, and more energy-efficient AI chips, revolutionizing a wide range of AI applications, from edge AI to large-scale data centers. This achievement paves the way for high-performance, energy-efficient, next-generation semiconductor designs that are crucial for shaping the future of AI computing.

Source: https://chiplet-marketplace.com/insights/news/

AMD Announces Over $10 Billion Taiwan Ecosystem Investment to Bolster AI Infrastructure and Advanced Packaging Manufacturing

Published May 28, 2026 Electronics Engineering Herald - EEHerald USA



OVERVIEW

AMD announced an investment exceeding $10 billion in Taiwan's ecosystem to expand its AI infrastructure and advanced packaging manufacturing capabilities. This significant capital injection will bolster AMD's chiplet architecture, high-bandwidth memory integration, 3D hybrid bonding, and rack-scale system design, supporting the development of advanced silicon and manufacturing technologies. Critically, AMD will collaborate with partners like ASE and SPIL in Taiwan to develop and qualify Elevated Fanout Bridge (EFB), a next-generation wafer-based 2.5D bridge interconnect technology, aiming to alleviate AI semiconductor supply bottlenecks.

IN DEPTH

Key Findings

AMD has announced an investment exceeding $10 billion in Taiwan's semiconductor ecosystem to significantly expand its AI infrastructure and advanced packaging manufacturing capabilities. This substantial capital commitment aims to resolve performance bottlenecks in AI chipsets and accelerate the development of next-generation AI and high-performance computing (HPC) solutions.

Technical Details

This investment will fortify AMD's key technological domains. Firstly, it will advance its chiplet architecture, enhancing the ability to integrate diverse functional chips into a single, high-performance processor. Secondly, it will strengthen its high-bandwidth memory (HBM) integration capabilities, crucial for achieving the high-speed data access required by demanding AI workloads. Furthermore, the investment will drive the development of 3D hybrid bonding technology, aiming for denser chip stacking and improved power efficiency. Finally, it will optimize rack-scale system design, thereby boosting the overall efficiency and scalability of AI data centers. AMD is actively collaborating with leading Taiwanese OSAT (Outsourced Semiconductor Assembly and Test) providers, including ASE Technology Holding and its subsidiary Siliconware Precision Industries Co. (SPIL), to develop and qualify Elevated Fanout Bridge (EFB), a next-generation wafer-based 2.5D bridge interconnect technology.

Background and Context

The rapid advancement of AI has led to AI chip manufacturing, especially advanced packaging technologies like TSMC's CoWoS, becoming a critical industry-wide bottleneck. AMD's investment directly addresses the supply constraints arising from the surging demand for AI infrastructure. Taiwan, as the global hub for the semiconductor supply chain, is indispensable for AMD to secure strategic supply chains and accelerate technological innovation. Nvidia has also announced plans to invest $150 billion annually in Taiwan, highlighting the pivotal role of the region's semiconductor industry for major AI chip manufacturers.

Strategic Significance and Outlook

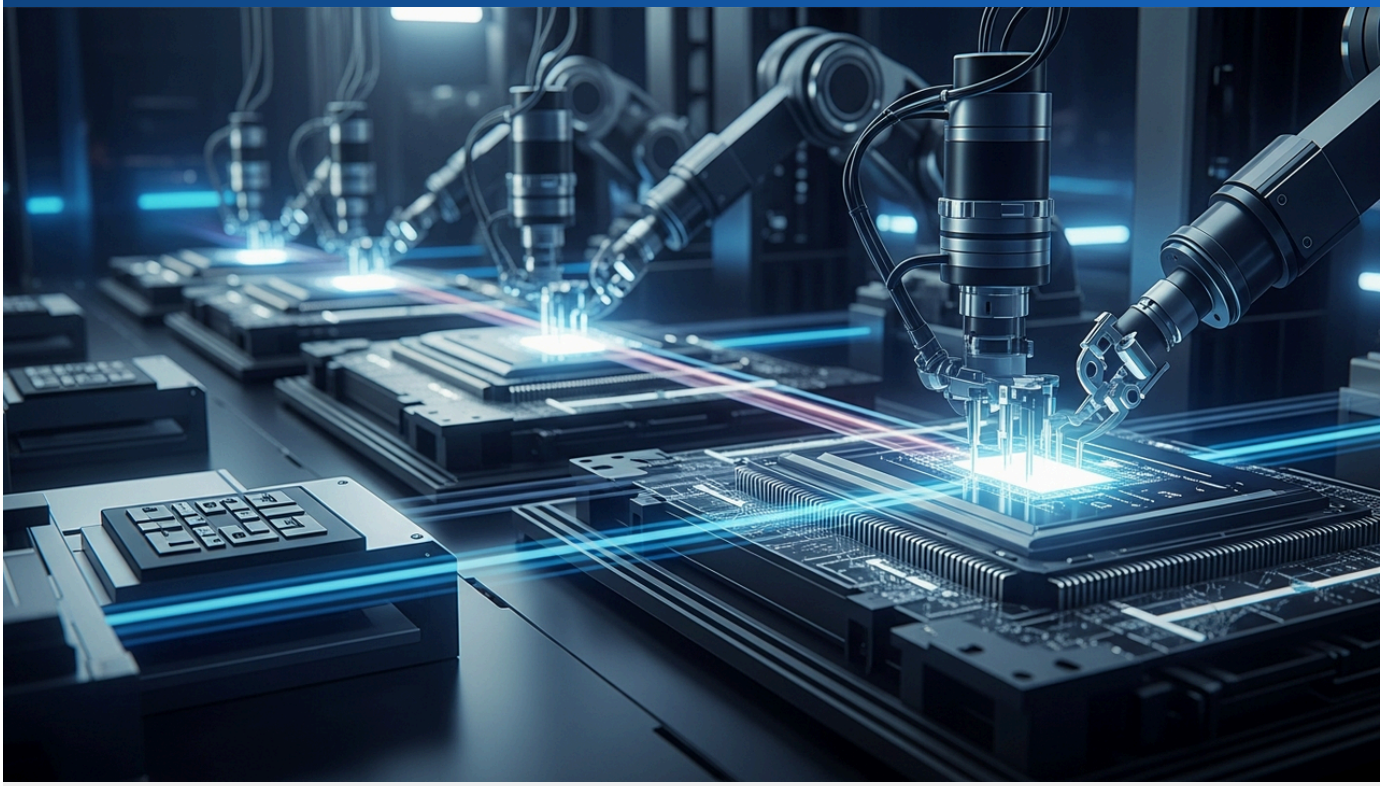
AMD's investment of over $10 billion into the Taiwanese ecosystem is expected to significantly enhance its competitiveness in the AI semiconductor market. The development and qualification of EFB technology, in particular, will establish new standards for 2.5D packaging and contribute to the realization of higher-performance, more cost-effective AI accelerators. This investment is anticipated to further strengthen Taiwan's semiconductor industry and foster stability and innovation within the global AI supply chain. In the long term, it could alleviate AI chip shortages and accelerate the broader adoption and evolution of AI technologies.

Source: https://www.eeherald.com/section/news/p20260526nwamd.html

Collected: June 05, 2026 | Automated Research System (Gemini API)

Applied Materials Achieves Record $7.91 Billion Revenue in Q2 2026, Advanced Packaging Business to Accelerate Over 50% for AI

Published May 28, 2026 MLQ.ai USA



OVERVIEW

Applied Materials reported record revenue of $7.91 billion in Q2 2026, marking a 13% sequential and 11% year-over-year increase, with non-GAAP gross margin reaching 50%, an 80 basis point improvement. The company anticipates its advanced packaging sales, driven by AI computing advancements, to accelerate over 50% in 2026 and continue strong growth beyond 2027. Applied Materials is also partnering with Broadcom to develop advanced chip packaging technologies for AI systems.

IN DEPTH

Key Findings

Applied Materials reported a record revenue of $7.91 billion in the second quarter of 2026, showcasing robust growth in the semiconductor equipment market and strong momentum in the AI computing sector. This revenue represents a 13% increase quarter-over-quarter and an 11% increase year-over-year. The company's non-GAAP gross margin also reached 50%, an 80 basis point improvement from the previous year. Applied Materials forecasts that the advancement of AI computing will propel advanced packaging demand, with sales accelerating over 50% in 2026 and sustaining strong growth beyond 2027.

Technical Details

AI systems, characterized by highly integrated packages with multiple components, necessitate sophisticated packaging technologies such as 3D stacking and chiplet integration. Applied Materials is expanding its portfolio for scaling AI-driven chip packaging, notably by acquiring ASMPT's NEXX business to strengthen its position in panel-level advanced semiconductor packaging equipment. The company has also partnered with Broadcom to focus on developing advanced chip packaging technologies specifically for AI systems. This collaboration aims to enhance interconnect density and bandwidth in semiconductor systems, which is critical for pushing the performance boundaries of AI infrastructure.

Background and Context

The semiconductor industry is experiencing a surge in investments in advanced packaging technologies due to the explosive growth in AI chip demand. AI semiconductors require higher performance, lower power consumption, and smaller form factors, which cannot be achieved solely through traditional 2D scaling. As a leading player in the wafer manufacturing equipment market, Applied Materials anticipates significant growth in wafer manufacturing equipment for AI logic and memory fabs in 2026 and 2027, which has led its stock price to hit an all-time high of $485.96. The company is recognized as a vital entity in the AI ecosystem, poised to benefit regardless of which specific chips dominate the AI market.

Strategic Significance and Outlook

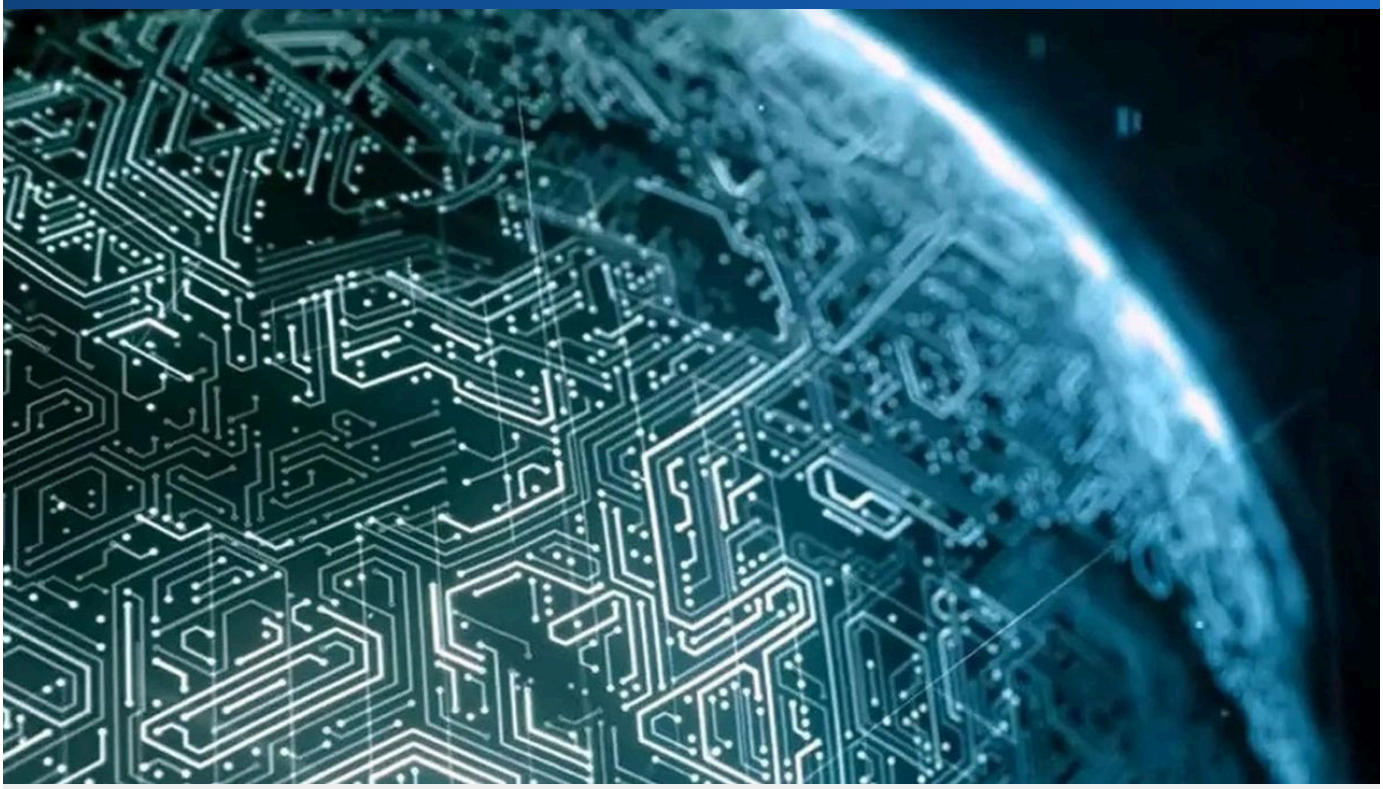
The rapid growth of Applied Materials' advanced packaging business and its strategic partnerships clearly demonstrate its pivotal role in AI-era semiconductor manufacturing. The collaboration with Broadcom will accelerate the development of next-generation packaging solutions for AI systems, establishing new benchmarks for interconnect density and bandwidth. The company's continuous investments and technological innovations are indispensable for supporting the performance improvement and widespread adoption of AI chips, while enhancing the overall efficiency and scalability of the semiconductor supply chain.

Source: https://mlq.ai/stocks/AMAT/q2-2026-earnings/

Collected: June 05, 2026 | Automated Research System (Gemini API)

Amkor Technology Acquires 67 Additional Acres in Arizona, Expanding U.S. Advanced Packaging Footprint

Published May 29, 2026 Dataquest Bureau USA



OVERVIEW

Amkor Technology has secured an additional 67 acres adjacent to its existing campus in Peoria, Arizona, to significantly expand its U.S. advanced semiconductor packaging and test capabilities. This strategic move aims to support large-scale, cutting-edge operations for the AI, high-performance computing, automotive, and communications markets. The expansion is anticipated to become the first high-volume advanced packaging OSAT facility in the U.S., directly addressing the domestic chip production trend and surging demand for AI-centric semiconductor services.

IN DEPTH

Key Findings

Amkor Technology has bolstered its commitment to expanding advanced semiconductor packaging and test capabilities in the United States by securing an additional 67 acres of land adjacent to its existing manufacturing campus in Peoria, Arizona. This strategic expansion is designed to address the surging demand from the artificial intelligence (AI), high-performance computing (HPC), automotive, and communications markets, as well as to align with U.S. policies aimed at strengthening domestic semiconductor manufacturing.

Technical Details

The land acquisition provides Amkor with strategic flexibility for future expansions of its advanced packaging and test facilities in Arizona. The company's Peoria plant already offers a comprehensive range of packaging solutions, including wafer bump, wafer test, flip chip, and System-in-Package (SiP) technologies. This expansion will enable Amkor to further increase its production capacity for high-density, power-efficient advanced packaging technologies, which are essential for AI chips and HPC processors. This is crucial for enabling more complex heterogeneous integration and chiplet-based designs.

Background and Context

The explosive growth of AI demand is accelerating investments in advanced semiconductor packaging worldwide. In the U.S., in particular, policies such as the CHIPS Act are driving the reinforcement of domestic manufacturing capabilities. Amkor's investment aligns with the broader trend of U.S.-based companies seeking to build more resilient semiconductor supply chains and mitigate geopolitical risks. This facility is expected to become the first high-volume advanced packaging OSAT (Outsourced Semiconductor Assembly and Test) facility in the U.S., playing a critical role in strengthening the domestic chip production ecosystem.

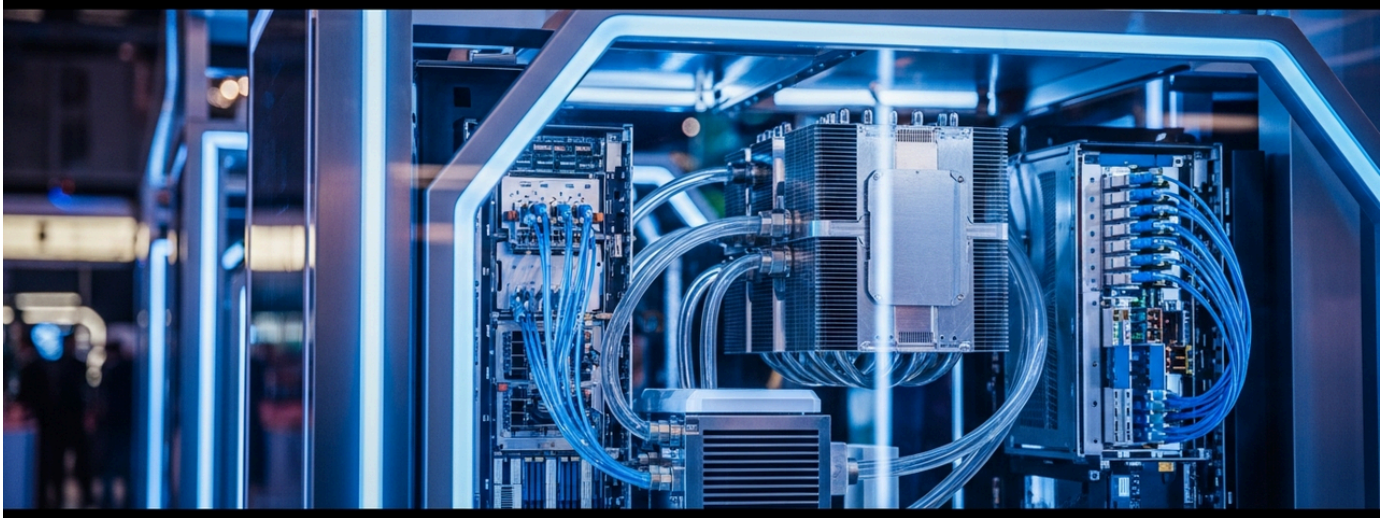
Strategic Significance and Outlook

Amkor's Arizona expansion is vital for alleviating advanced packaging bottlenecks within the U.S. semiconductor supply chain and stabilizing the domestic supply of chips for the AI, HPC, and automotive markets. This facility will serve as a core hub to meet the robust demand for advanced packaging, which is projected to continue beyond 2027. It is expected to significantly contribute to strengthening the competitiveness and accelerating innovation within the U.S. semiconductor industry, while also creating new employment opportunities.

Source: https://www.dqindia.com/esdm/amkor-expands-us-advanced-packaging-footprint-with-additional-land-in-arizona-11875728

Dow Showcases Next-Gen AI Thermal Management Technologies at COMPUTEX Taipei 2026, Supporting 400G+ Optical Transceivers

Published June 01, 2026 chemXplore USA



OVERVIEW

Dow showcased next-generation thermal management technologies for AI servers and high-speed optical transceivers at COMPUTEX Taipei 2026. The company presented thermal interface materials (TIMs) and silicone-based materials for advanced semiconductor packaging, designed to support efficient heat dissipation in 400G, 800G, and 1.6T applications. These materials enhance thermal conductivity, adhesion, and compatibility, minimize package warpage, and support large-area molding processes, with a keynote highlighting their role in AI data center cooling.

IN DEPTH

Key Findings

Dow presented its next-generation thermal management technologies for AI servers and high-speed optical transceivers at COMPUTEX Taipei 2026, offering innovative solutions to enhance the performance and reliability of AI-driven computing. The company broadly introduced thermal interface materials (TIMs) and silicone-based materials for advanced semiconductor packaging, designed to support efficient heat dissipation in applications operating at ultra-high speeds such as 400G, 800G, and even 1.6T.

Technical Details

The thermal management materials showcased by Dow are engineered to effectively dissipate heat from high-performance components like AI processors, power modules, and optical transceivers. Specifically, the portfolio includes TIMs, silicone thermal conductive adhesives, encapsulants, and silicone hot melt technologies. These materials provide excellent thermal conductivity, high adhesive strength, and good compatibility with various package materials. The silicone hot melt technology, in particular, is optimized to support large and complex molding processes while minimizing package warpage, playing a critical role in resolving heat-related challenges in AI chipsets. This technology extends chip lifespan and prevents performance degradation due to overheating.

Background and Context

The explosive growth of AI and the expanding demand for data centers have made thermal management one of the most critical challenges in semiconductor packaging. AI servers, GPUs, and HBM (High-Bandwidth Memory) consume vast amounts of power and generate significant heat, making efficient cooling systems indispensable. Traditional thermal management solutions are finding it increasingly difficult to meet the demands of these next-generation components. Dow's solutions, as highlighted in its keynote speech on AI data center cooling, offer an advanced approach to address these new challenges, serving as a vital component for supporting the scalability and sustainability of AI infrastructure.

Strategic Significance and Outlook

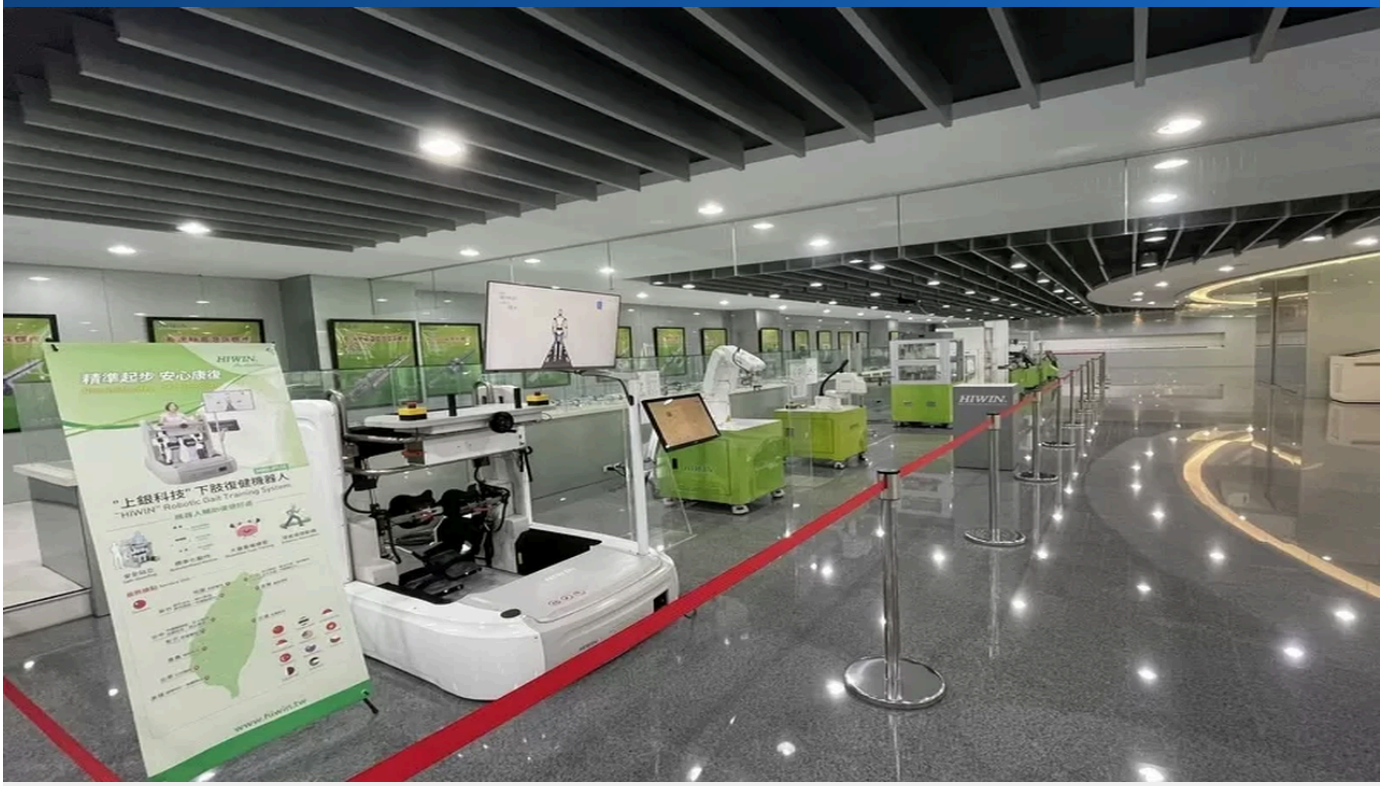
Dow's innovative thermal management materials will play a central role in enhancing the performance and ensuring the reliability of AI and HPC systems. Especially as optical-electronic integration advances in areas like co-packaged optics (CPO), these materials become essential for addressing bandwidth and energy efficiency challenges in data centers. Dow's technology is expected to continue pushing the limits of AI chipsets and contribute to building sustainable AI infrastructure, thereby driving innovation across the entire semiconductor industry.

Source: https://chemxplore.com/news/dow-ai-thermal-materials-computex

Collected: June 05, 2026 | Automated Research System (Gemini API)

Hiwin and Qualcomm Integrate Edge AI into Panel-Level Semiconductor Packaging to Enhance Production Accuracy and Throughput

Published June 01, 2026 Packnode Taiwan



OVERVIEW

Taiwanese motion control specialist Hiwin Technologies is collaborating with Qualcomm to integrate Dragonwing Q6 Edge AI into panel-level semiconductor packaging (PLP) equipment. This partnership combines machine vision, edge computing, and high-precision handling to enhance alignment accuracy and process control in PLP. The initiative aims to improve performance in high-speed semiconductor production environments, addressing the critical need for precise alignment and stable process control as PLP gains traction for its high density, throughput, and cost-efficiency in AI-related semiconductor packaging.

IN DEPTH

Key Findings

Hiwin Technologies, a Taiwanese specialist in motion control, has announced a groundbreaking partnership with Qualcomm to integrate Dragonwing Q6 Edge AI into panel-level semiconductor packaging (PLP) equipment. This collaboration aims to enhance performance in high-speed semiconductor production environments, particularly by improving alignment accuracy and robust process control, through the combination of machine vision, edge computing, and high-precision handling at the wafer load port.

Technical Details

PLP technology is an advanced method that processes semiconductors on large, rectangular panels rather than traditional round wafers, allowing for more chips to be processed at once and improving material utilization and production throughput. However, scaling PLP effectively requires exceptionally high alignment accuracy and stable process control. The partnership between Hiwin and Qualcomm addresses this challenge by merging Qualcomm's Dragonwing Q6 Edge AI processor capabilities with Hiwin's high-precision motion control technology. Integrating edge AI directly into the load port enables real-time defect detection, positional adjustments, and process optimization, allowing for adjustments in milliseconds without human intervention. This contributes to improved packaging yield and reduced cost per bit.

Background and Context

As demand for AI and high-performance computing (HPC) rapidly increases, semiconductor packaging is becoming increasingly complex and a major bottleneck for performance improvement. PLP is gaining significant attention in AI-related semiconductor packaging for its potential to deliver higher density, greater throughput, and improved cost efficiency. However, the commercialization of this technology necessitates advanced automation and intelligence to ensure manufacturing process precision and stability. The integration of AI and edge computing is accelerating the development of smart factories in semiconductor manufacturing, setting new standards for quality control and production efficiency.

Strategic Significance and Outlook

The collaboration between Hiwin and Qualcomm is expected to play a crucial role in accelerating the adoption of PLP technology and reducing the manufacturing cost and production time for AI chips. The implementation of edge AI will make manufacturing processes more autonomous and adaptive, enabling them to meet the complex packaging requirements of future AI and HPC systems. This partnership is poised to drive digital transformation in semiconductor manufacturing and enhance the resilience and efficiency of the entire AI ecosystem supply chain.

Source: https://www.packnode.org/en/innovation/hiwin-and-qualcomm-bring-edge-ai-to-panel-level-semiconductor-pa

Collected: June 05, 2026 | Automated Research System (Gemini API)

GlobalFoundries Triples Malta Fab Capacity with $16 Billion US CHIPS Act Investment, Targeting 1.5 Million Wafers/Year by late 2028

Published May 28, 2026 Tom's Hardware USA

OVERVIEW

GlobalFoundries is advancing a $16 billion US investment plan, bolstered by the CHIPS Act, to triple production capacity at its Malta fab. This includes an 11 billion Euro expansion at its Dresden plant, aiming for 1.5 million wafers annually by late 2028. As TSMC and Samsung prioritize advanced nodes and packaging for AI, GlobalFoundries, as a mature node foundry, is benefiting significantly, addressing demand from automotive, industrial, and IoT markets. EXTOLL and Chip Interfaces are also introducing a UCIe IP solution for GlobalFoundries' FDX technology, promoting chiplet connectivity.

IN DEPTH

Key Findings

GlobalFoundries is proceeding with a substantial $16 billion U.S. investment plan, significantly bolstered by funding from the U.S. CHIPS Act. This initiative aims to triple the production capacity at its Malta fabrication facility over the next decade. The plan also encompasses an 11 billion Euro expansion at its Dresden plant, which is already Europe's largest semiconductor factory, with a target of producing 1.5 million wafers annually by the end of 2028.

Technical Details

This massive investment primarily targets strengthening the production capacity of mature node semiconductors for the automotive, industrial, and IoT markets. Amidst accelerating demand for AI chips, leading foundries like TSMC and Samsung are allocating vast resources to cutting-edge nodes and advanced packaging (e.g., 2nm, 3nm). This shift has created a tightening supply in mature nodes, where GlobalFoundries plays a crucial role in bridging this market gap. Furthermore, EXTOLL and Chip Interfaces have announced the industry's first integrated UCIe (Universal Chiplet Interconnect Express) IP solution for GlobalFoundries' FDX (FD-SOI) technology. This solution promotes the standardization of chiplet-to-chiplet connections and facilitates broader chiplet adoption across diverse applications, further strengthening GlobalFoundries' ecosystem.

Background and Context

The global semiconductor supply chain is undergoing a significant restructuring driven by geopolitical risks and AI-led demand. As the U.S., Europe, and Japan strive to restore and strengthen domestic semiconductor manufacturing capabilities, government incentives like the CHIPS Act are playing a pivotal role. TSMC, for instance, is reallocating 40-90nm production capacity for CoWoS advanced packaging and silicon interposer manufacturing for AI accelerators, resulting in a reduction of mature node wafer supply. In this scenario, mature node foundries like GlobalFoundries are significantly benefiting as customers previously using advanced nodes now seek alternative capacity.

Strategic Significance and Outlook

GlobalFoundries' investments in its Malta and Dresden fabs are indispensable for substantially enhancing the resilience of the U.S. and European semiconductor supply chains and increasing geopolitical autonomy. The production target of 1.5 million wafers per year will meet robust demand in growing sectors such as AI, automotive, and industrial, contributing to the stable supply of mature node markets. The integration of the UCIe IP solution is expected to expand GlobalFoundries' role in the chiplet ecosystem and contribute to increased integration density in AI and HPC applications. This is projected to lead to improved profitability and market share for the company in the long term.

Source: https://www.tomshardware.com/tech-industry/semiconductors/the-trailing-edge-foundry-roadmap-examined

Intel Commits to Massive Advanced Packaging Push for Foundry Revival, EMIB Capacity Expansion Key

Published May 29, 2026 BusinessKorea USA

OVERVIEW

Intel is committing to a massive expansion of its advanced semiconductor packaging capabilities to accelerate its foundry business revival, with a core focus on expanding its proprietary EMIB (Embedded Multi-die Interconnect Bridge) technology. This initiative aims to significantly boost production capacity to meet the demands of new foundry customers and secure a robust infrastructure for materials, components, and equipment. EMIB, a potential alternative to TSMC's CoWoS, is attracting interest from customers like Google and Amazon, strengthening Intel's competitiveness in addressing the complexity of AI infrastructure.

IN DEPTH

Key Findings

Intel is committed to a large-scale expansion of its advanced semiconductor packaging capabilities to accelerate the revival of its foundry business. The core of this initiative focuses on expanding the capacity of Intel's proprietary EMIB (Embedded Multi-die Interconnect Bridge) technology. This effort aims to significantly boost production capacity to meet the demands of new foundry customers and to secure a robust infrastructure for materials, components, and equipment.

Technical Details

Intel's advanced packaging roadmap covers multiple technology platforms, including EMIB, Foveros, and Foveros Direct, with the ambitious goal of integrating one trillion transistors within a single package by 2030. EMIB enables high-density interconnects without requiring a large silicon interposer, thereby reducing energy loss in data transmission within the package. Foveros vertically integrates chiplets in 3D stacks, while Foveros Direct employs hybrid bonding technology to further enhance interconnect density and energy efficiency. Intel has successfully applied its 18A process for the first time in data center processors, the Xeon 6+, which combines Foveros Direct 3D packaging technology with EMIB to create high-density packages featuring up to 288 energy-efficient cores. EMIB-T, a variant, enables ultra-large, high-performance chiplet systems, achieving over 12 Gb/s for HBM4e and 64 Gb/s for UCIe interfaces.

Background and Context

The surging demand for AI infrastructure and 'physical AI' has dramatically increased the importance of advanced packaging technologies in the semiconductor industry. With TSMC's CoWoS packaging capacity being one of the most critical bottlenecks in the AI hardware stack, Intel's EMIB is gaining significant attention as a viable alternative, particularly from hyperscalers like Google and Amazon. Intel believes that advanced packaging could gain quicker external customer adoption compared to advanced process technologies, thereby strengthening its competitive position in the foundry market.

Strategic Significance and Outlook

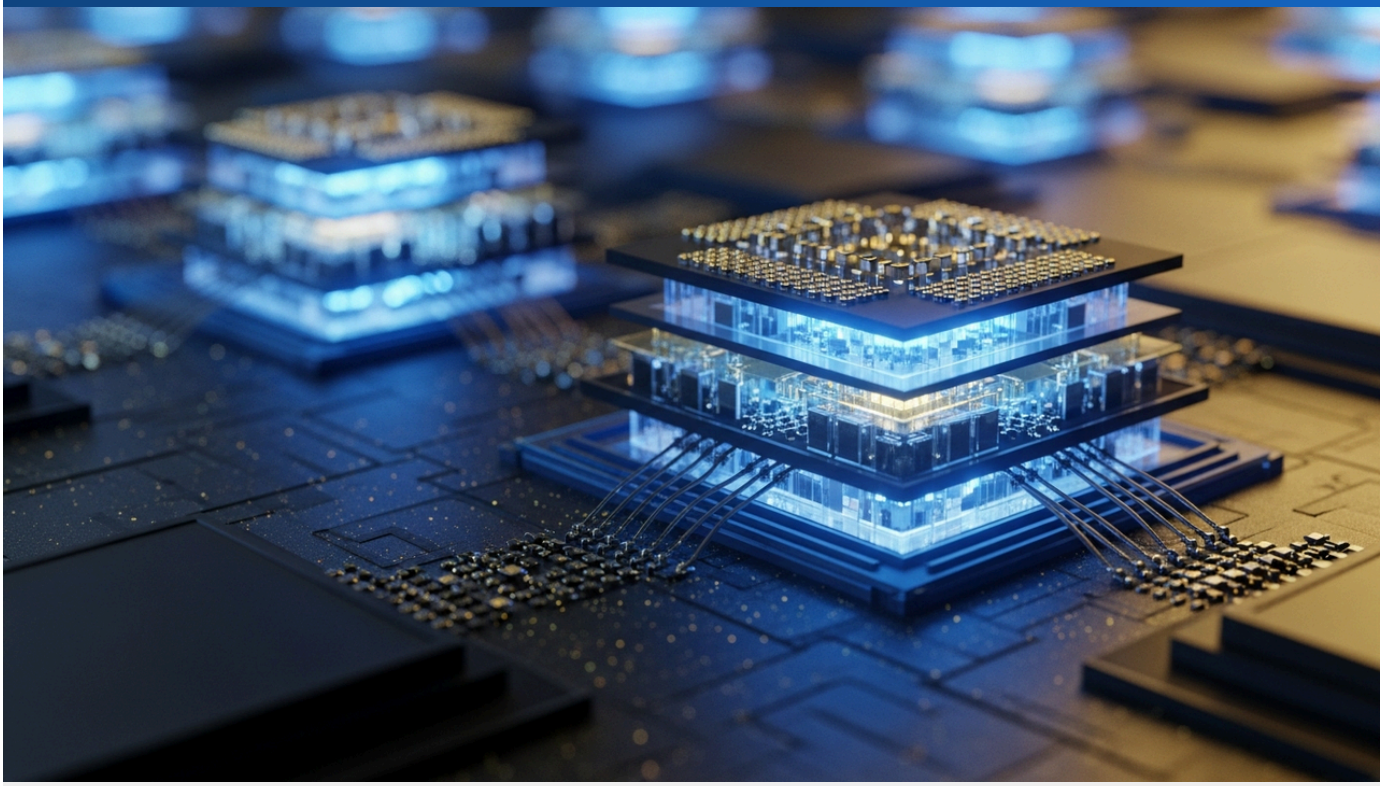
Intel's substantial investment in advanced packaging represents a critical strategic move for the company to regain competitiveness as a leading foundry in the AI era. The capacity expansion of technologies like EMIB, Foveros, and Foveros Direct is set to redefine the scalability limits of AI and HPC, enabling high-performance heterogeneous integration, improved power delivery, and reduced warpage. This initiative will be an indispensable factor in Intel's efforts to attract more external customers and drive resilience and technological innovation across the entire semiconductor supply chain. In the long term, this is expected to stabilize the supply of AI chips and accelerate the broader adoption and evolution of AI technologies.

Source: https://en.etnews.com/20260529200001

Collected: June 05, 2026 | Automated Research System (Gemini API)

Hybrid Bonding Unlocks New Frontiers in 3D Integration, Driving AI Accelerators and Chiplet Designs

Published June 02, 2026 PatSnap UK



OVERVIEW

Hybrid bonding, an innovative 3D integration technology, enables both electrical continuity and mechanical integrity without solder or microbumps by combining metal-to-metal (primarily Cu-Cu) and dielectric-to-dielectric (oxide-to-oxide) bonding in a single interface. This technology allows simultaneous Cu-to-Cu and oxide-to-oxide bonding at sub-micron pitches, drastically reducing interconnect pitch, parasitic capacitance, and inductance compared to conventional packaging. It is driving the evolution of 3D IC stacking for AI accelerators and chiplet platforms, emerging as an essential solution for high-performance and high-efficiency AI.

IN DEPTH

Key Findings

Hybrid bonding is an innovative 3D integration technology in semiconductor packaging that achieves both electrical continuity and mechanical integrity by combining metal-to-metal (primarily Cu-Cu) and dielectric-to-dielectric (oxide-to-oxide) bonding in a single interface. This technology eliminates the need for solder or microbumps and enables simultaneous bonding at ultra-fine pitches, dramatically advancing 3D IC stacking for AI accelerators and chiplet platforms.

Technical Details

The primary advantage of hybrid bonding lies in its ability to perform simultaneous Cu-to-Cu and oxide-to-oxide bonding at sub-micron pitches. This dramatically miniaturizes interconnect pitches and substantially reduces parasitic capacitance and inductance compared to traditional packaging. Consequently, data transfer speeds between chips are enhanced, and power consumption is mitigated. For instance, conventional microbumps in HBM (High-Bandwidth Memory) stacks create parasitic capacitance issues, acting as bottlenecks for speed and performance. A transition to hybrid bonding is considered the only appropriate method to fundamentally resolve this issue. Hybrid bonding also offers potential fundamental solutions for challenges like increased HBM PHY power and thermal management.

Background and Context

With the rapid advancement of AI, AI chips are becoming increasingly complex, demanding high-density and high-speed data processing capabilities. As Moore's Law approaches its limits, 3D integration has emerged as a crucial means to enhance semiconductor performance and optimize power efficiency. Hybrid bonding stands at the forefront of this 3D integration, holding the potential to significantly boost AI hardware performance. Equipment manufacturers like KLA and Applied Materials also anticipate increased demand for high-end inspection systems and manufacturing equipment to address the growing complexity of packaging due to the proliferation of chip stacking and hybrid bonding, accelerating industry-wide investment in this technology.

Strategic Significance and Outlook

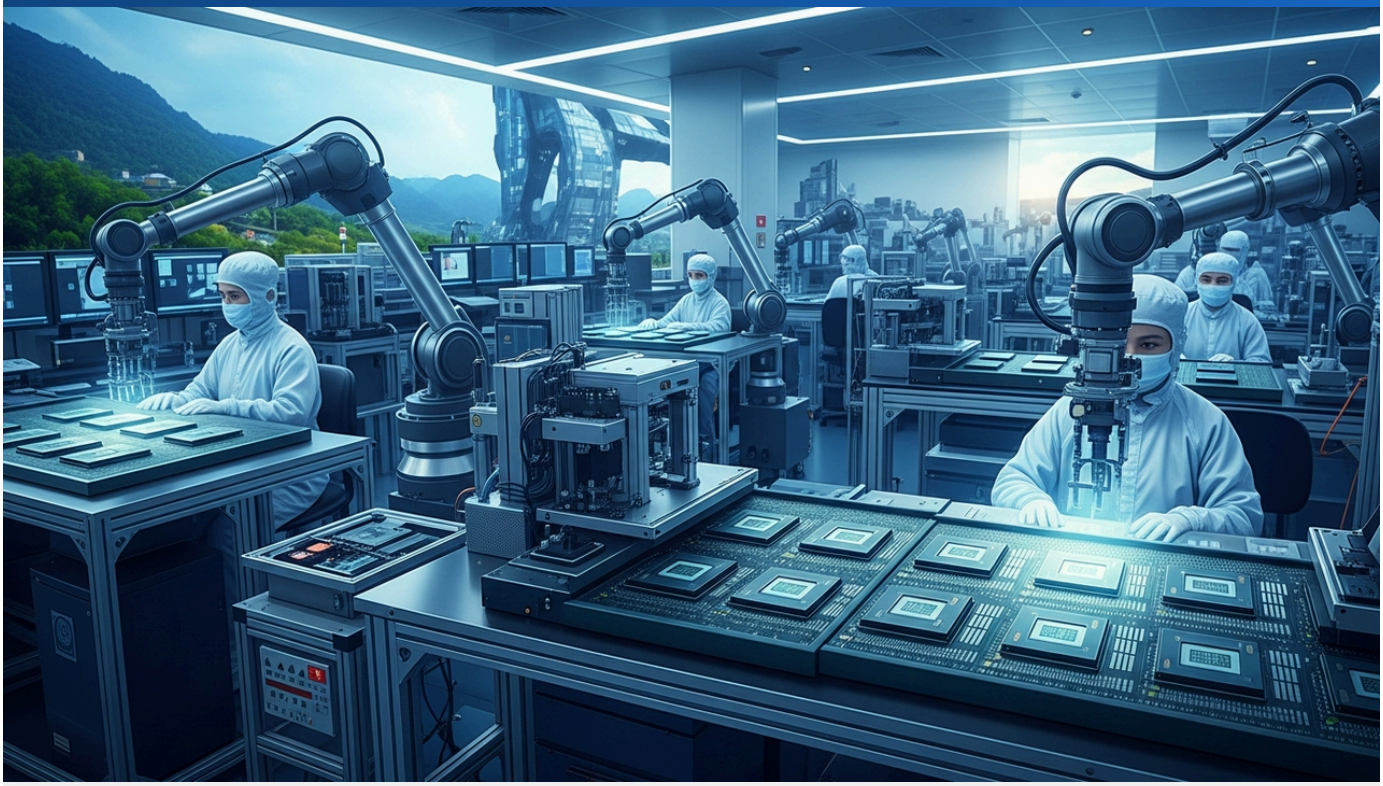
The evolution of hybrid bonding technology will establish new benchmarks for performance and efficiency in AI accelerators, HPC systems, and chiplet-based designs. Enhanced interconnect density and reduced parasitic effects will alleviate data movement bottlenecks, enabling the development of smaller, more powerful AI chips. This technology is key to realizing next-generation 3D packaging solutions such as Intel's Foveros Direct, which achieves over 12 Gb/s for HBM4e and 64 Gb/s for UCIe interfaces, and TSMC's SoIC. Hybrid bonding will continue to be an indispensable technology driving semiconductor innovation in the AI era, pushing the limits of computational capability.

Source: https://www.patsnap.com/resources/blog/rd-blog/hybrid-bonding-3d-integration-technology-landscape-2026/

Collected: June 05, 2026 | Automated Research System (Gemini API)

Samsung Electronics to Invest $1.5 Billion in Vietnam Semiconductor Test Facility Amid Surging AI Chip Demand

Published June 02, 2026 Quintile Reports South Korea



OVERVIEW

Samsung Electronics announced plans to invest approximately $1.5 billion in a semiconductor testing facility in Vietnam to address the memory chip shortage caused by surging AI chip demand. This strategic expansion aims to strengthen its global memory chip supply chain, focusing on DRAM and NAND memory chip testing, with operations scheduled to commence in November 2027. Vietnam is entering a new strategic phase in its semiconductor industry, with FPT also planning a high-end chip testing and packaging facility for IoT, automotive, and edge AI applications by 2027.

IN DEPTH

Key Findings

Samsung Electronics has announced plans to invest approximately $1.5 billion in a semiconductor testing facility in Vietnam. This initiative is a direct response to the memory chip supply shortage exacerbated by the soaring demand for AI chips. This significant investment aims to bolster Samsung's global memory chip supply chain, with the facility slated to commence operations in November 2027, focusing primarily on testing DRAM and NAND memory chips.

Technical Details

The new semiconductor testing facility in Vietnam will specialize in the final testing stages of DRAM and NAND memory chips. The performance of AI chips, particularly High-Bandwidth Memory (HBM), is heavily reliant on the precision of its testing and packaging processes. This facility will incorporate state-of-the-art testing equipment and technologies to optimize the quality, reliability, and yield of memory products, thereby meeting the stringent demands of AI and High-Performance Computing (HPC) applications. It will also play a role in alleviating overall supply chain bottlenecks by enabling faster and more efficient product delivery in conjunction with advanced packaging technologies.

Background and Context

The explosive growth of AI computing has dramatically increased the demand for high-bandwidth memory. The supply of memory chips and AI server capacity continue to be major bottlenecks for chip manufacturers. Samsung's investment is a strategic move to secure the supply capacity of next-generation HBM, such as HBM4E, and to strengthen its market competitiveness. Vietnam is entering a new strategic phase in its semiconductor industry, with milestones such as Viettel breaking ground on the country's first semiconductor manufacturing plant and FPT announcing an advanced testing and packaging facility for high-end chips targeting IoT, automotive, and edge AI applications, scheduled to begin operations in 2027. Samsung's investment will further establish Vietnam as a significant semiconductor hub in Southeast Asia.

Strategic Significance and Outlook

Samsung's $1.5 billion investment in Vietnam will contribute to the geographical diversification and resilience of the global memory chip supply chain, playing a crucial role in addressing the increasing demand for AI chips. The operational launch in November 2027 will significantly increase the memory testing capacity needed to support the continuous growth of the AI industry, which is key for Samsung to maintain and enhance its leadership in the HBM market. This investment is expected to accelerate Vietnam's semiconductor industry and promote the further adoption and evolution of AI technologies.

Source: https://www.quintilereports.com/press-release/samsung-electronics-announces-1-5-billion-semiconductor-testing-facility-in-vietnam-to-strengthen-global-memory-chip-supply-chain/46/

Collected: June 05, 2026 | Automated Research System (Gemini API)

Marvell Unveils Industry's First 102.4 Tbps AI Switch, Doubling Bandwidth for AI Data Center Networks

Published June 03, 2026 Advanced Packaging News USA

OVERVIEW

Marvell announced the industry's first 102.4 Tbps AI switch, setting a new benchmark for network bandwidth in AI data centers. This innovative switch doubles bandwidth compared to current top-performing switches, dramatically improving data transfer capabilities for high-performance computing environments. It addresses data movement bottlenecks in large-scale AI model training and inference, thereby enhancing AI system efficiency and scalability, driven by the explosive growth of AI/ML workloads.

IN DEPTH

Key Findings

Marvell has unveiled the industry's first 102.4 Terabits per second (Tbps) AI switch, establishing a new benchmark for network bandwidth in artificial intelligence (AI) data centers. This groundbreaking product is designed to meet the explosive growth of AI and machine learning (ML) workloads, dramatically improving data transfer capabilities by doubling the bandwidth compared to currently available top-performing switches.

Technical Details

The 102.4 Tbps AI switch is engineered using advanced semiconductor packaging technologies and Co-Packaged Optics (CPO) solutions. CPO integrates optical and electronic components within the same package, directly addressing bandwidth and energy efficiency challenges in data centers. This approach significantly reduces signal loss and power consumption associated with traditional electrical signaling, enabling ultra-high-speed and low-latency data transfer. The switch's architecture facilitates efficient communication among large GPU clusters and AI accelerators equipped with HBM (High-Bandwidth Memory), which is particularly critical for resolving data movement bottlenecks in distributed AI model training.

Background and Context

The evolution of AI places unprecedented demands on data center network infrastructure. Large-scale AI models process vast amounts of data in real time and communicate frequently between GPUs, making network bandwidth a primary bottleneck limiting AI system performance. Existing 100Gbps and 200Gbps Ethernet infrastructures are increasingly struggling to meet the requirements of modern AI workloads. Marvell's 102.4 Tbps switch is a crucial step to bridge this gap, serving as a foundational technology to enable next-generation scalability for AI data centers. The industry is witnessing a broader convergence of optical and electronic communications, exemplified by acquisitions like Credo's of DustPhotonics to strengthen its CPO solutions.

Strategic Significance and Outlook

The introduction of Marvell's 102.4 Tbps AI switch is poised to revolutionize AI data center design and operation. This high-bandwidth solution will shorten training times for large AI models and enhance real-time AI inference capabilities. Furthermore, improved energy efficiency will contribute to reduced data center operating costs and enhanced sustainability. This technology is expected to be a significant milestone, accelerating the further adoption and evolution of AI and driving innovation in semiconductor packaging and optical interconnect technologies.

Source: https://advancedpackaging.news/article/124316/Marvell_unveils_102.4_Tbps_AI_switch

Collected: June 05, 2026 | Automated Research System (Gemini API)

Credo Completes DustPhotonics Acquisition, Bolstering Co-Packaged Optics (CPO) Solutions to Accelerate AI Data Centers

Published June 03, 2026 Advanced Packaging News USA

OVERVIEW

Credo has completed its acquisition of DustPhotonics, significantly strengthening its Co-Packaged Optics (CPO) solutions. This acquisition is poised to advance high-bandwidth, low-power interconnect technologies in AI data centers, accelerating the integration of optical and electronic components crucial for resolving AI infrastructure bottlenecks. The fusion of DustPhotonics' silicon photonics technology with Credo's SerDes and DSP expertise is expected to dramatically enhance the performance and efficiency of next-generation data centers.

IN DEPTH

Key Findings

Credo has announced the completion of its acquisition of DustPhotonics, a specialist in optical interconnect technology. This strategic acquisition is expected to significantly enhance Credo's Co-Packaged Optics (CPO) solutions and accelerate the development of high-bandwidth, low-power interconnect technologies for AI data centers.

Technical Details

DustPhotonics excels in the development of high-performance silicon photonics technology, particularly optical engines and optical transceivers. The integration of Credo's industry-leading SerDes (serializer/deserializer) and DSP (digital signal processor) technologies with DustPhotonics' optical expertise will elevate CPO solutions to a new level. CPO is a technology that tightly integrates switch ASICs (Application-Specific Integrated Circuits) and optical engines within the same package. Compared to traditional electrical connections via PCBs (Printed Circuit Boards), CPO minimizes signal loss and significantly reduces power consumption. This enables scalable and energy-efficient interconnects necessary for next-generation data transmission speeds of 400G, 800G, and even 1.6T.

Background and Context

The explosive growth of AI and high-performance computing (HPC) workloads has placed unprecedented demands on data center network infrastructure. Especially in the training and inference of large-scale AI models, vast amounts of data must move at high speeds between chips, and existing electrical interconnects have become bandwidth and power efficiency bottlenecks. CPO technology is garnering significant attention as one of the most promising solutions to address this challenge, and its adoption is accelerating across the industry. As evidenced by Marvell's announcement of the industry's first 102.4 Tbps AI switch, data center bandwidth requirements are increasing exponentially, and CPO is an indispensable technology for meeting these demands.

Strategic Significance and Outlook

Credo's acquisition of DustPhotonics is expected to further accelerate the growth of the co-packaged optics market in AI data centers. The integrated technology stack will enable the construction of higher-performance and more energy-efficient AI infrastructure, contributing to reduced operating costs and improved sustainability for data centers. This acquisition is a crucial step in shaping the future of data center networking in the AI era and is expected to significantly impact the development of next-generation AI accelerators, switches, and co-packaged optics modules.

Source: https://advancedpackaging.news/article/124317/Credo_completes_DustPhotonics_acquisition

Collected: June 05, 2026 | Automated Research System (Gemini API)

SK Group Chairman Deepens AI Alliances with Nvidia and TSMC, Expanding Next-Gen HBM and Advanced Packaging Collaboration

Published June 04, 2026 The Korea Herald South Korea

OVERVIEW

SK Group Chairman Chey Tae-won has strengthened alliances with leading AI chipmakers, meeting with Nvidia CEO Jensen Huang and later with TSMC Chairman C.C. Wei in Taiwan. Discussions focused on expanding cooperation in next-generation High-Bandwidth Memory (HBM) and advanced packaging. SK hynix aims to reinforce its position in the custom AI memory market by combining TSMC's 12nm base die technology with its own 1b DRAM process for HBM4, seeking to play a pivotal role in the AI-era semiconductor supply chain.

IN DEPTH

Key Findings

SK Group Chairman Chey Tae-won has intensified alliances with the world's most influential AI chipmakers, following a meeting with Nvidia CEO Jensen Huang and subsequently with TSMC Chairman C.C. Wei in Taiwan. These discussions focused on expanding cooperation in next-generation High-Bandwidth Memory (HBM) and advanced packaging, aiming to solidify SK Group's strategic position in the AI-era semiconductor supply chain.

Technical Details

SK hynix is strategically positioning itself to gain a competitive edge in the custom AI memory market by combining TSMC's advanced 12nm base die technology with its own innovative 1b DRAM process for HBM4, the next generation of HBM. HBM4 is designed to deliver higher bandwidth, lower power consumption, and superior thermal management performance, which are indispensable for maximizing the performance of AI accelerators. This technological partnership aims to jointly resolve complex 3D stacking and advanced packaging challenges, thereby enhancing the overall efficiency and performance of AI chipsets. Next-generation HBMs, such as HBM4E, offer significant improvements in energy efficiency and thermal resistance characteristics compared to their predecessors, making them key to meeting the demands of AI data centers.

Background and Context

The explosive growth of AI has dramatically increased demand for high-performance AI chips and the HBM that forms their core. With TSMC's CoWoS packaging capacity being a major bottleneck for AI hardware, the shortage of HBM supply and AI server capacity has become an industry-wide challenge. In this context, close collaboration among leading semiconductor companies is crucial for stabilizing the supply chain and accelerating technological innovation. SK hynix has established a strong leadership position in the HBM sector, and competition is intensifying, with Samsung Electronics also commencing HBM4E sample shipments.

Strategic Significance and Outlook

The deepening collaboration between SK Group, Nvidia, and TSMC will significantly impact future technological development and supply chain dynamics in the AI semiconductor market. The technology partnership for HBM4, in particular, will push the performance limits of AI chips even further, enabling the realization of larger and more complex AI models. This cooperative relationship is expected to be an essential factor in alleviating AI chip supply bottlenecks and supporting the continuous growth and evolution of the AI industry. In the long term, this will likely position South Korea to play an even more central role in the global AI semiconductor ecosystem.

Source: https://www.koreaherald.com/article/10763730

Collected: June 05, 2026 | Automated Research System (Gemini API)

Fraunhofer IPMS Develops High-Density Chiplet Systems at Wafer Level, Advancing Integration for AI and HPC

Published May 28, 2026 Design And Reuse Germany

OVERVIEW

Fraunhofer IPMS has developed high-density chiplet systems at the wafer level, aiming to enhance integration for AI and high-performance computing (HPC) applications. This research contributes to the miniaturization and increased performance of chiplet technology, addressing interconnect density and bandwidth challenges to innovate next-generation AI hardware design. This breakthrough is expected to unlock new possibilities for 3D integration, leading to more complex and efficient AI systems.

IN DEPTH

Key Findings

Fraunhofer IPMS has successfully developed high-density chiplet systems at the wafer level. This innovative approach aims to dramatically increase chip integration density for artificial intelligence (AI) and high-performance computing (HPC) applications, paving new avenues for next-generation AI hardware design.

Technical Details

The high-density chiplet systems developed by Fraunhofer IPMS achieve significantly higher integration density than traditional chip integration methods by combining fine interconnect technology with advanced 3D stacking techniques. Wafer-level integration minimizes the connection distance between chiplets, substantially reducing signal latency and power consumption. This technology proves particularly effective in applications demanding immense data processing capabilities and high-speed communication, such as AI accelerators and large-scale multi-core processors. It also synergizes with hybrid bonding technology, which enables ultra-fine-pitch inter-die connections, maximizing the performance and efficiency of AI chips.

Background and Context

With the deceleration of Moore's Law, the semiconductor industry is increasingly looking beyond miniaturization to advanced packaging and chiplet technologies for performance improvements. The explosive growth of AI has accelerated this trend, creating a strong demand for high-density, high-bandwidth, and low-power solutions. Chiplets offer the potential to increase design flexibility and reduce manufacturing costs by integrating multiple dies with different functionalities, but their realization requires highly precise integration technologies. Fraunhofer IPMS's research strengthens European technological leadership in this field and represents a significant contribution to the global AI supply chain.

Strategic Significance and Outlook

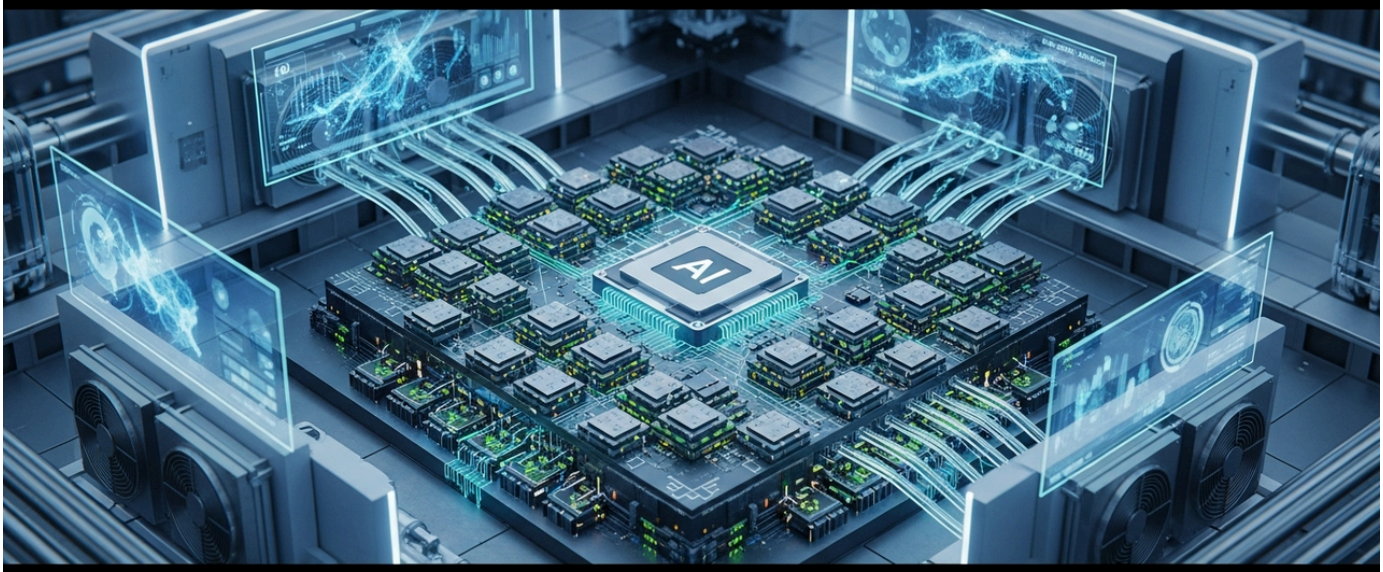
The high-density chiplet systems developed by Fraunhofer IPMS will be indispensable technologies for next-generation AI and HPC systems. Wafer-level integration offers significant advantages in terms of scalability and cost-efficiency, enabling the development of smaller and more powerful AI chips. As this technology progresses towards commercialization, it is expected to enhance the performance and efficiency of a wide range of AI applications, from data centers to edge devices, fostering further adoption and evolution of AI technology. This marks an important achievement that drives a new wave of innovation in the semiconductor industry.

Source: https://www.design-reuse.com/news/list/INTERCONNECT

Collected: June 05, 2026 | Automated Research System (Gemini API)

Samsung Reportedly to Launch Physical AI Chiplet Platform Next Year, Accelerating AI Inference and Infrastructure

Published May 28, 2026 Design And Reuse South Korea



OVERVIEW

Samsung is reportedly planning to launch a physical AI chiplet platform as early as next year, aiming to accelerate next-generation chip development for AI inference and infrastructure. This platform seeks to provide the high bandwidth and energy efficiency critical for meeting the explosive demand of AI. This move is part of Samsung's strategy to achieve system-level co-optimization within an integrated development framework spanning advanced logic, memory, and packaging, thereby strengthening its competitiveness in the AI semiconductor market.

IN DEPTH

Key Findings

Samsung is reportedly poised to launch a physical AI chiplet platform as early as next year. This initiative aims to accelerate the development of next-generation chips specifically designed for AI inference and infrastructure, providing crucial enhancements in high bandwidth and energy efficiency to meet the explosive demand for artificial intelligence (AI).

Technical Details

This physical AI chiplet platform will be central to Samsung's strategy of achieving system-level co-optimization within an integrated development framework that encompasses advanced logic, memory, and packaging. The chiplet architecture aims to enhance design flexibility and surpass performance limitations of monolithic chips by integrating multiple dies with different functionalities. Particularly in next-generation HBM (High-Bandwidth Memory) architectures, leveraging advanced logic nodes in the base die improves power efficiency and boosts data throughput. As I/O density continues to scale, optimizing the base die becomes a critical factor in enhancing overall system efficiency. Samsung Foundry's 2.xD Cube Packaging enables heterogeneous integration of multiple chips, achieving both high-density integration and high bandwidth.

Background and Context

The rapid evolution of AI presents new challenges and opportunities for the semiconductor industry. Training and inference of large-scale AI models require immense computational power and memory bandwidth, which traditional monolithic chip designs are increasingly struggling to meet. Chiplet technology has emerged as a promising solution to this challenge, and its adoption is accelerating across the industry. Electronic Design Automation (EDA) companies like Cadence and Synopsys are also deepening their collaboration with Samsung Foundry, offering solutions to improve power and performance for AI and multi-die designs using 2nm processes and 3D-IC technology, indicating a clear industry-wide shift towards chiplet-based architectures.

Strategic Significance and Outlook

The launch of Samsung's physical AI chiplet platform will significantly bolster its competitiveness in the AI semiconductor market. This platform is expected to provide faster and more energy-efficient solutions, particularly for AI inference, improving the performance of a wide range of applications from edge AI to data centers. Samsung's continued investment in advanced packaging and chiplet technologies is anticipated to be a crucial step in pushing the limits of AI-era computing capabilities and contributing to the construction of sustainable AI infrastructure.

Source: https://www.design-reuse.com/news/list/INTERCONNECT

Synopsys Enhances Power and Performance for AI and Multi-Die Designs on Latest Samsung Foundry Processes

Published May 29, 2026 Chiplet News USA

OVERVIEW

Synopsys announced solutions at SAFE Forum 2026 to enhance power efficiency and performance for AI and multi-die designs, leveraging Samsung Foundry's latest process technologies. This initiative directly addresses the surging demand for AI infrastructure and physical AI, aiming to accelerate high-performance computing solutions for next-generation AI systems. Synopsys' optimized EDA tools and IP contribute to maximizing the capabilities of Samsung's advanced packaging, such as 2.xD Cube Packaging, and chiplet platforms.

IN DEPTH

Key Findings

Synopsys announced at SAFE Forum 2026 its new solutions designed to dramatically improve power efficiency and performance for artificial intelligence (AI) and multi-die designs, utilizing Samsung Foundry’s latest process technologies. This innovative approach directly addresses the surging demand for AI infrastructure and physical AI, aiming to accelerate high-performance computing solutions for next-generation AI systems.

Technical Details

The solutions introduced by Synopsys include optimized Electronic Design Automation (EDA) tools and Intellectual Property (IP) portfolios for Samsung Foundry's advanced processes, particularly for cutting-edge nodes like 2nm. This enables designers to minimize power consumption while maximizing processing speed in logic, memory, and interconnect designs for AI chips and multi-die systems. Specifically, by collaborating with advanced packaging technologies such as Samsung’s 2.xD Cube Packaging, heterogeneous integration of multiple chips can be performed efficiently, leading to significant improvements in overall system bandwidth and energy efficiency. This is a critical factor in AI design, where system-level co-optimization becomes indispensable as I/O density continues to scale.

Background and Context

The explosive growth of AI presents unprecedented design challenges for the semiconductor industry. Traditional monolithic chip designs are finding it difficult to balance the immense computational power, data bandwidth, and low power consumption required by AI workloads. Chiplet and 3D-IC (3-Dimensional Integrated Circuit) technologies have emerged as primary solutions to this challenge, necessitating close collaboration between semiconductor manufacturers and EDA vendors. Cadence is also deepening its collaboration with Samsung Foundry on 2nm and 3D-IC technologies, providing solutions to improve power and performance for AI and multi-die designs, which further indicates the industry-wide acceleration towards building ecosystems for next-generation AI systems.

Strategic Significance and Outlook

The collaboration between Synopsys and Samsung Foundry is crucial for accelerating innovation in the AI and HPC markets. The combination of optimized EDA solutions and advanced process technologies will shorten AI chip design cycles and time-to-market, while enabling the development of higher-performance and more energy-efficient AI processors. This initiative is expected to be an indispensable factor in supporting the continuous evolution of AI infrastructure and shaping a future where physical AI proliferates across autonomous driving, robotics, smart cities, and beyond.

Source: https://chiplet-marketplace.com/insights/news/

Cadence and Samsung Foundry Deepen 2nm and 3D-IC Collaboration to Meet Surging AI Infrastructure Demand

Published May 29, 2026 Chiplet News USA

OVERVIEW

Cadence and Samsung Foundry are deepening their collaboration in 2nm process technology and 3D-IC (3D Stacked Integrated Circuit) technology to address the surging demand for AI infrastructure and physical AI. This partnership aims to accelerate high-performance computing solutions for next-generation AI systems, providing a design environment that maximizes Samsung's advanced packaging and chiplet platform capabilities. The technological integration is expected to enhance AI chip performance and energy efficiency while shortening time-to-market.

IN DEPTH

Key Findings

Cadence and Samsung Foundry are strengthening their collaboration in 2nm process technology and 3D-IC (3-Dimensional Stacked Integrated Circuit) technology to address the rapidly escalating demand for artificial intelligence (AI) infrastructure and physical AI. This strategic partnership aims to accelerate high-performance computing solutions for next-generation AI systems and reduce time-to-market.

Technical Details

Cadence provides optimized Electronic Design Automation (EDA) tools and Intellectual Property (IP) for Samsung Foundry's advanced processes, specifically tackling design challenges at the 2nm process node. This collaboration delivers solutions that manage the complexity of AI chip and multi-die system designs, optimizing power consumption while maximizing performance. 3D-IC technology vertically stacks multiple dies, shortening interconnect distances between chips, improving data transfer speeds, and enhancing power efficiency. The synergy between Samsung Foundry's advanced packaging technologies, such as 2.xD Cube Packaging, and Cadence's EDA toolchain is expected to facilitate seamless heterogeneous integration and dramatically boost the overall performance of AI systems.

Background and Context

The explosive growth of AI presents unprecedented design and manufacturing challenges for the semiconductor industry. As the limits of traditional 2D scaling approach, chiplet technology and 3D stacking are becoming indispensable for achieving the immense computational power, high bandwidth, and low power consumption required by AI workloads. Samsung is striving to achieve system-level co-optimization within an integrated development framework that combines advanced logic, memory, and packaging, with its collaboration with Cadence being a crucial part of this strategy. Synopsys is also partnering with Samsung Foundry to provide solutions that improve power and performance for AI and multi-die designs, indicating that close collaboration between EDA vendors and foundries is essential for resolving industry bottlenecks.

Strategic Significance and Outlook

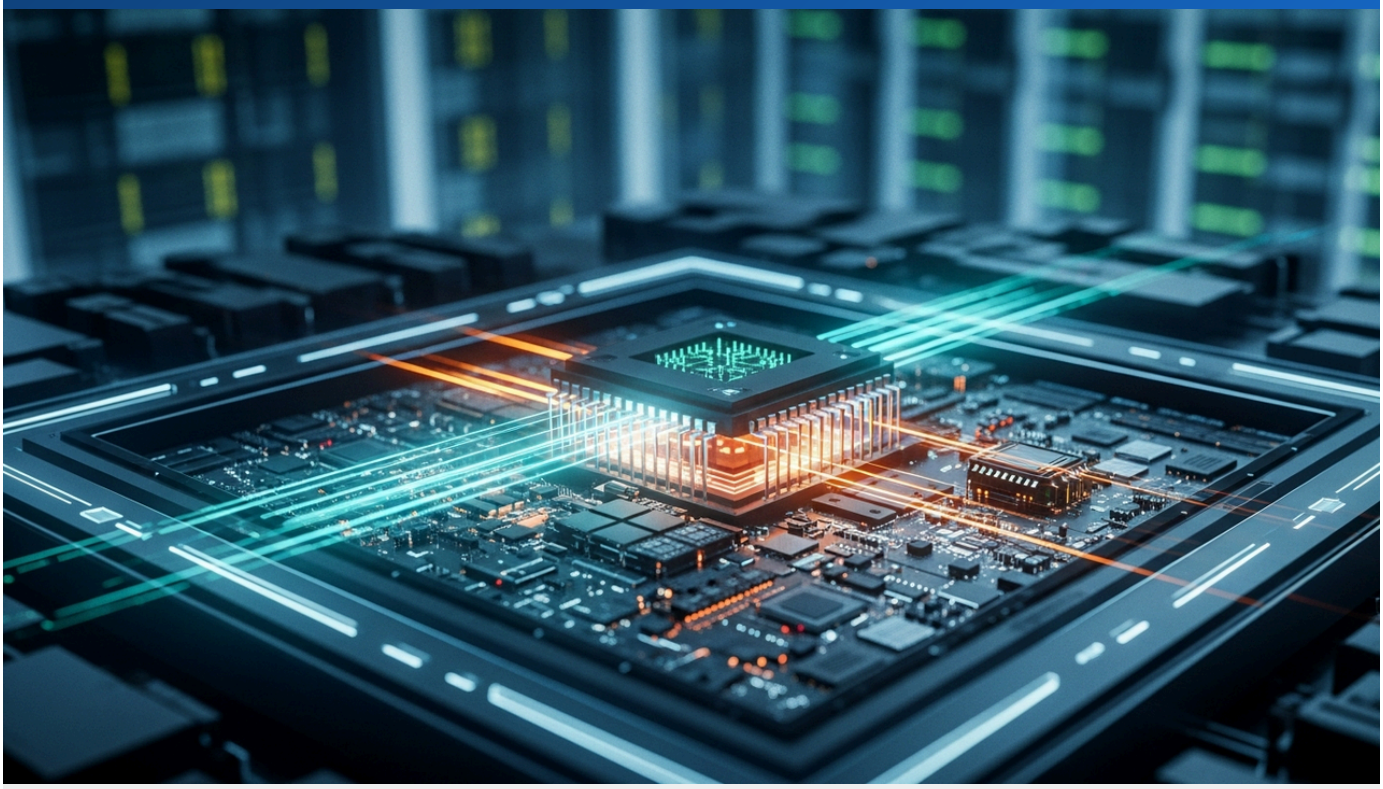
The deepened collaboration between Cadence and Samsung Foundry is critical for accelerating technological innovation in the AI and HPC markets. This partnership streamlines the design and manufacturing processes for AI chips, enabling the rapid development of higher-performance and more energy-efficient AI processors. By strengthening the design ecosystem for next-generation AI systems, both companies are expected to support the continuous evolution of AI infrastructure and play a central role in shaping a future where physical AI becomes pervasive in applications like autonomous driving, robotics, and smart cities.

Source: https://chiplet-marketplace.com/insights/news/

Collected: June 05, 2026 | Automated Research System (Gemini API)

IEEE ECTC 2026 Highlights Packaging Technologies Redefining AI and HPC Scalability Limits

Published May 29, 2026 IEEE Electronic Components and Technology Conference (ECTC) USA



OVERVIEW

The 2026 IEEE Electronic Components and Technology Conference (ECTC) spotlighted packaging technologies redefining AI and HPC scalability limits. Intel Foundry's R&D emphasized glass core substrates as key to enabling high-performance heterogeneous integration, improved power delivery, stability, and low warpage in large AI/HPC packages. Advancements in EMIB-T technology were also presented, achieving over 12 Gb/s for HBM4e and 64 Gb/s for UCIe interfaces, facilitating complex chiplet-based AI systems. The conference showcased diverse research in 3D integration, hybrid bonding, and new substrate materials.

IN DEPTH

Key Findings

The 2026 IEEE Electronic Components and Technology Conference (ECTC) prominently featured advanced packaging technologies that are redefining the scalability limits of artificial intelligence (AI) and high-performance computing (HPC). Notably, Intel Foundry's research and development highlighted glass core substrates as a critical enabler for addressing these challenges, showcasing their potential to achieve high-performance heterogeneous integration, improved power delivery and stability, and reduced warpage in large-scale AI and HPC packages.

Technical Details

The conference presented advancements in through-glass via (TGV) technology for glass core substrates as a next-generation foundational technology enabling electrical and optical integration on a single platform. This is expected to significantly reduce energy loss in data transmission within AI chips and dramatically alleviate data movement bottlenecks. Furthermore, Intel announced progress in its EMIB-T (Embedded Multi-die Interconnect Bridge with Through-Silicon Vias) advanced packaging technology. EMIB-T allows for ultra-large, high-performance chiplet systems that scale beyond the limits of silicon reticles and conventional packaging constraints, achieving over 12 Gb/s for HBM4e and 64 Gb/s for UCIe (Universal Chiplet Interconnect Express) interfaces. This technology delivers high bandwidth and low latency in complex AI systems that integrate multiple chiplets.

Background and Context

The explosive growth of AI is imposing unprecedented demands on semiconductor packaging technologies. As the limitations of traditional 2D scaling become apparent, advanced packaging techniques such as 3D integration, chiplets, hybrid bonding, and novel substrate materials have become indispensable for enhancing chip performance and optimizing power efficiency. With TSMC's CoWoS capacity being a major bottleneck for the AI hardware stack, technologies like glass core substrates and EMIB-T are anticipated as crucial solutions to mitigate this bottleneck and support the continuous evolution of AI infrastructure.

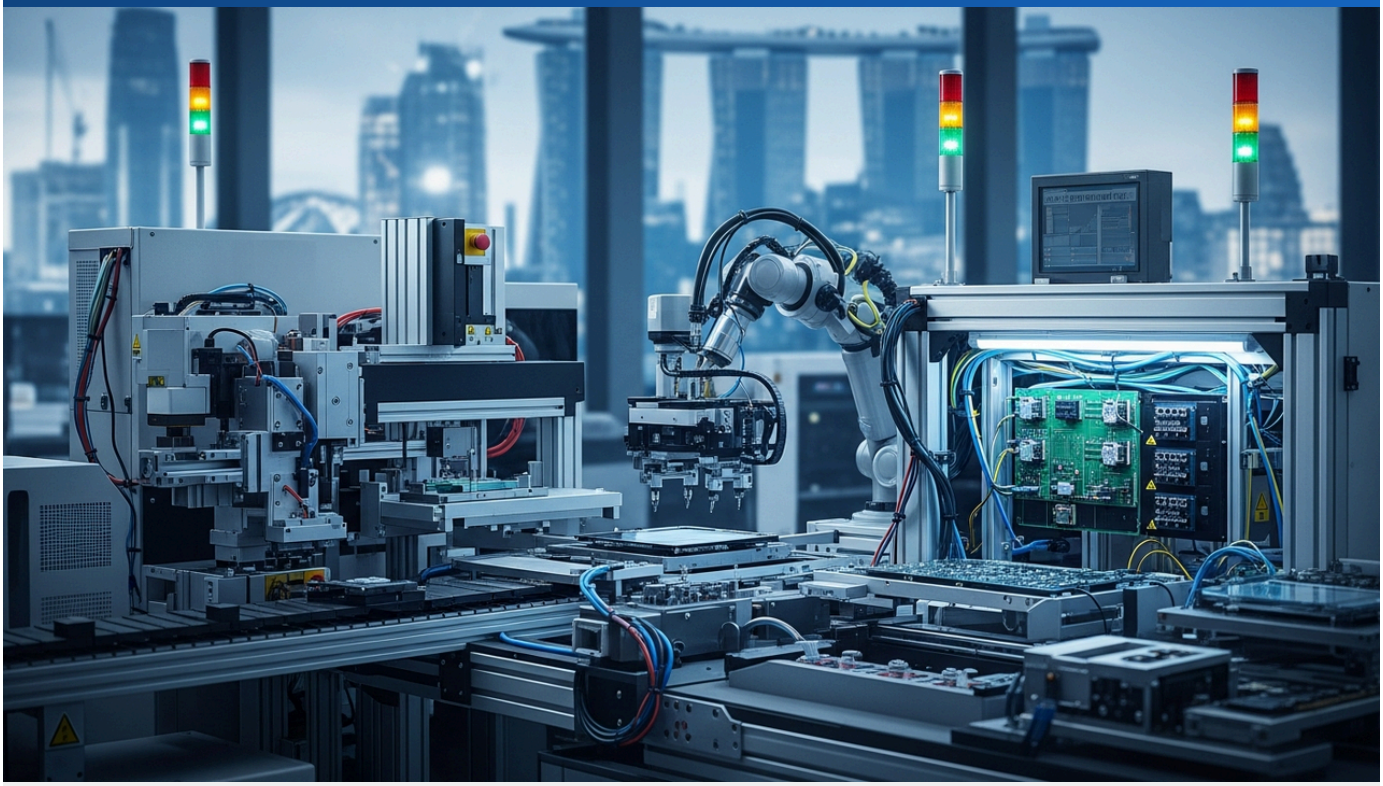
Strategic Significance and Outlook

The research presented at ECTC 2026 holds immense potential for substantially improving the scalability and performance of AI and HPC. The commercialization of glass core substrates and the widespread adoption of advanced packaging technologies like EMIB-T are poised to revolutionize the design and manufacturing of AI chips, enabling the development of higher-performance and more energy-efficient AI processors. These technologies will enhance the performance and efficiency of a wide range of AI applications, from data centers to edge devices, fostering further adoption and evolution of AI technology. ECTC continues to present critical technological trends that shape the future of the semiconductor industry.

Source: https://ectc.net/wp-content/uploads/2023/03/76-ECTCAdvance-Web2.pdf

Singapore Semiconductor Testing Equipment Market Projected to Reach $310 Million by 2033, Growing at 7.8% CAGR

Published May 28, 2026 ABNewswire Singapore



OVERVIEW

This article provides an overview of a market research report on the Singapore semiconductor testing equipment market, distributed by ABNewswire. The report forecasts the market to reach $310 million by 2033, with a CAGR of 7.8% from 2026 to 2033. This growth is driven by Singapore's strategic positioning in advanced packaging, specialized semiconductors, power electronics, and back-end manufacturing.

IN DEPTH

This article provides an overview of the market research report "Singapore Semiconductor Testing Equipment Market Outlook 2026-2034" distributed by ABNewswire.

Report Overview

This report focuses on the current status and future projections of the semiconductor testing equipment market in Singapore. The market covered is the entire Singapore region, and the forecast period spans from 2026 to 2033.

Key Findings

- The Singapore semiconductor testing equipment market is projected to reach $310 million by 2033.
- The market is expected to grow at a Compound Annual Growth Rate (CAGR) of 7.8% during the forecast period from 2026 to 2033.
- This growth is driven by Singapore's unique position in advanced packaging, specialized semiconductors, power electronics, and back-end manufacturing.
- Advantest and Teradyne lead the market in high-end ATE (Automated Test Equipment) systems for AI processors, memory, and high-speed computing applications.
- Cohu holds a strong position with its handlers, inspection platforms, and thermal test solutions.
- ASMPT leverages Singapore's packaging ecosystem to provide integrated assembly and test capabilities.

About the Publisher

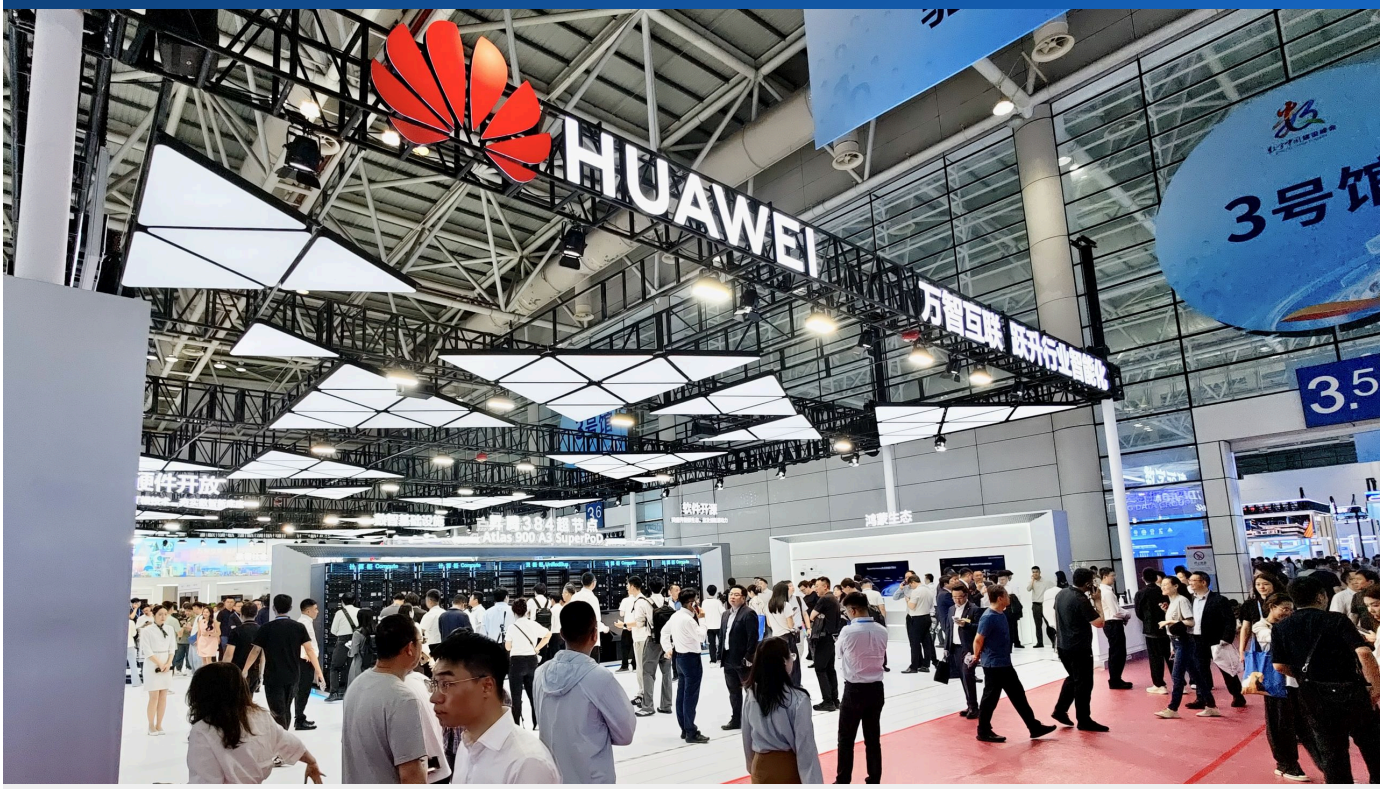
ABNewswire is a press release distribution service, and this report was prepared by a market research firm.

Source: https://www.geraldgrain.com/markets/stocks.php?article=abnewswire-2026-5-28-singapore-semiconductor-testing-equipment-market-set-to-nearly-double-reaching-usd-310-million-by-2033-at-

78-cagr

Tsinghua University Develops 3D Chip Design Tool Tailored for Huawei's 'LogicFolding' Architecture

Published May 28, 2026 Tom's Hardware China



OVERVIEW

Tsinghua University in China has developed a 3D chip design tool specifically tailored for Huawei’s 'LogicFolding' architecture. This tool aims to optimize chip performance and efficiency for AI and HPC applications through advanced 3D integration. Customized to Huawei's technical requirements, the design tool is expected to play a crucial role in overcoming existing advanced packaging challenges and accelerating the establishment of China's indigenous semiconductor ecosystem. This development gains significance amidst slow adoption of Intel's EMIB and Foveros, highlighting the importance of domestic innovation in China.

IN DEPTH

Key Findings

Tsinghua University in China has successfully developed a 3D chip design tool specifically tailored for Huawei's 'LogicFolding' architecture. This specialized tool aims to optimize chip performance and efficiency in artificial intelligence (AI) and high-performance computing (HPC) applications through advanced 3D integration, marking a significant advancement in China's efforts to build its own semiconductor technology ecosystem.

Technical Details

The developed 3D chip design tool streamlines the process of vertically integrating multiple chip dies, thereby reducing design complexity. The 'LogicFolding' architecture aims to achieve shorter interconnect paths and lower power consumption by arranging logic blocks in a folded manner, and this design tool is customized to those specific needs. It addresses challenges such as alignment precision, thermal management, and signal integrity in 3D stacking, ultimately enhancing overall system performance. While advanced packaging technologies like Intel's EMIB (Embedded Multi-die Interconnect Bridge) and Foveros theoretically offer superior performance, their adoption has been slower and more selective thus far. This is attributed to factors such as cost, ecosystem inertia, and limited use cases, and Tsinghua University's initiative seeks to overcome the limitations of existing technologies and provide more practical solutions.

Background and Context

Amidst intensifying technological competition between the U.S. and China, China is strongly promoting self-sufficiency and technological independence in its semiconductor industry. Sanctions against Huawei have spurred the company to build its own semiconductor design and manufacturing ecosystem, with domestic research institutions like Tsinghua University playing a central role in this endeavor. 3D integration technology is a crucial frontier for improving chip performance as the physical limits of Moore's Law approach, and China's investment in this area is essential for securing its competitiveness in future AI and HPC markets.

Strategic Significance and Outlook

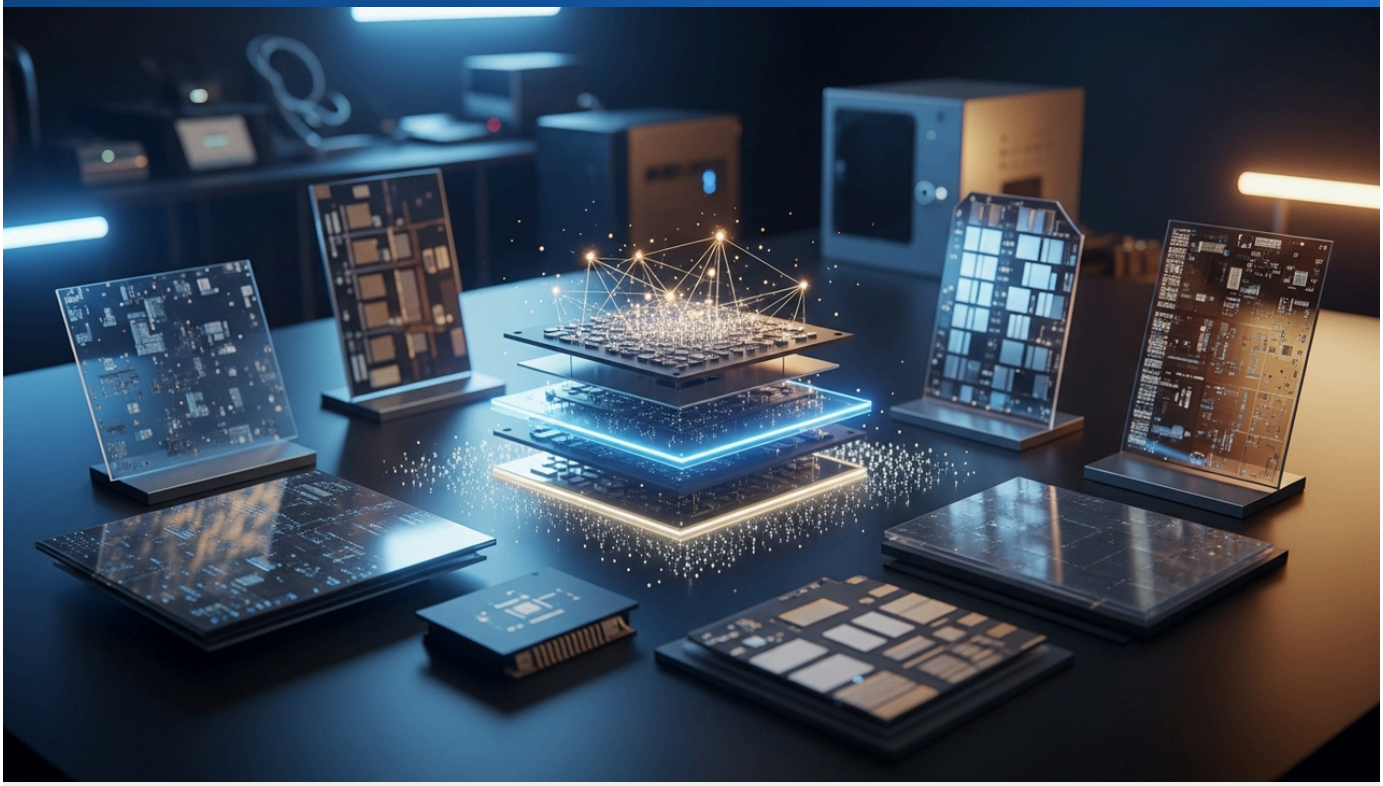
The 3D chip design tool developed by Tsinghua University for Huawei will play a vital role in China's efforts to establish its own technology in the AI and HPC sectors. The success of this tool will not only enhance China's design capabilities in the semiconductor industry but also accelerate the development of a domestic chiplet and 3D integration ecosystem. This is expected to enable Huawei to develop higher-performance and more energy-efficient AI chips, thereby increasing its resilience against global technological constraints.

Source: https://www.tomshardware.com/tech-industry/semiconductors/peking-university-builds-3d-chip-design-tool-tailored-to-huaweis-logicfolding-architecture

Collected: June 05, 2026 | Automated Research System (Gemini API)

IEEE ECTC 2026 Program Reveals Latest Research in Advanced Packaging, Including 3D Integration, Hybrid Bonding, and New Substrate Materials

Published May 29, 2026 IEEE Electronic Components and Technology Conference (ECTC) USA



OVERVIEW

The program for the 76th IEEE Electronic Components and Technology Conference (ECTC) unveiled a wide array of cutting-edge research in advanced packaging, focusing on 3D integration, 2.5D architectures, bridge and chiplet integration, hybrid bonding, and wafer-to-wafer/chip-to-wafer bonding. The conference also covered diverse topics such as new substrate materials, high-density RDL, next-generation interconnects, large panel warpage management, large package manufacturing, AI/ML, and thermal management, indicating key future directions for back-end semiconductor technology.

IN DEPTH

Key Findings

The advance program for the 76th IEEE Electronic Components and Technology Conference (ECTC) has been released, showcasing a wide range of cutting-edge research and innovations at the forefront of back-end semiconductor technology. The conference particularly highlighted advancements in advanced packaging technologies, including 3D integration, 2.5D architectures, bridge and chiplet integration, hybrid bonding, and wafer-to-wafer and chip-to-wafer bonding.

Technical Details

ECTC 2026 featured research presentations across diverse technological topics:

- **3D and 2.5D Architectures:** Technologies for vertically or horizontally integrating multiple dies to enhance performance and density.
- **Bridge and Chiplet Integration:** Methods for integrating smaller chips with different functionalities (chiplets) to improve system flexibility and cost-efficiency.
- **Hybrid Bonding:** A technology achieving ultra-fine-pitch interconnects through direct metal-to-metal (Cu-Cu) and dielectric-to-dielectric (oxide-to-oxide) bonding. Imec and EV Group reported a world-record overlay accuracy of less than 40nm at 200nm pitch.
- **Wafer-to-Wafer and Chip-to-Wafer Bonding:** High-precision bonding techniques for entire wafers or individual dies to substrates or other wafers.
- **New Substrate Materials:** Next-generation materials like glass core substrates, offering superior electrical and thermal properties compared to conventional organic substrates. Intel Foundry emphasized the potential of glass core substrates for AI and HPC.
- **High-Density RDL (Redistribution Layer) and Next-Generation Interconnects:** Fine-pitch wiring technologies to improve signal transmission efficiency between chips.
- **Large Panel Warpage Management and Large Package Manufacturing:** Challenges and solutions for manufacturing increasingly large packages.

- **AI/ML and Thermal Management:** New cooling materials and techniques to address increased heat generation from AI workloads. Dow showcased next-generation thermal management technologies at COMPUTEX Taipei 2026.

Background and Context

The semiconductor industry is facing the physical limits of Moore's Law and is increasingly relying on advanced packaging technologies, rather than solely miniaturization, for chip performance improvements. The explosive growth in demand across AI, HPC, and edge computing is accelerating the urgent need for high-density, high-bandwidth, and low-power packaging solutions. ECTC serves as a premier forum where experts from academia and industry converge to address these challenges and define the direction of next-generation semiconductor technologies.

Strategic Significance and Outlook

The research presented at ECTC 2026 illuminates the path for semiconductor innovation in the AI era. The continuous evolution of 3D integration and advanced packaging technologies is indispensable for enhancing the performance, energy efficiency, and scalability of AI chips. These technologies are expected to accelerate the adoption and advancement of AI across a wide range of application areas, including data centers, automotive, and IoT devices, while also contributing to the resilience and technological independence of the entire semiconductor supply chain.

Source: https://ectc.net/wp-content/uploads/2023/03/76-ECTCAdvance-Web2.pdf