Semiconductor packaging

Weekly Intelligence Report

2026-06-13 | 15 articles | 7 countries

troy-technical.jp

This Week's Keyword

AI Packaging Bottleneck

Capacity & tech race for AI chips intensifies

15 articles	7 countries	130K wafers/month	>$7B USD
Total Articles Analyzed	Source Countries	TSMC CoWoS Capacity '26	Amkor US Fab Investment

All 15 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	TSMC CoWoS/CoPoS Boost	Corporate Strategy	●●●●○	●●●●○	●●●●●	●●●●○	●●●●●	TSMC expands CoWoS tenfold to 130K/month by late 2026, accelerates glass-substrate CoPoS for AI chips.
#02	SK Hynix TC Bonder	New Product/Capacity	●●○○○	●●●●○	●●●●○	●●●●○	●●●●○	SK Hynix orders Hanmi TC Bonders for HBM4 production, boosting capacity at Cheongju M15X fab.
#03	Samsung HBM Hybrid Bond	Corporate Strategy	●●●●○	●●●○○	●●●●○	●●●○○	●●●●○	Samsung plans new advanced packaging fab in Gwangju, shifting HBM bonding to HCB by 2029.
#04	Silicon Box Funding	Corporate Strategy	●●●○○	●●●●●	●●●○○	●●●●○	●●●○○	Silicon Box secures $77.5M debt financing to expand advanced packaging and chiplet integration.
#05	ASE Packaging Price Hike	Market Report	●○○○○	●●●●●	●●●●○	●●●○○	●●●●●	ASE to raise advanced packaging prices by 5-20% in 2026 due to surging AI demand and capacity constraints.
#06	Amkor Arizona Fab	Corporate Strategy	●●●○○	●●●○○	●●●●●	●●●●○	●●●●●	Amkor invests over $7B in Arizona for advanced packaging, strengthening US semiconductor ecosystem.
#07	NVIDIA HBM Contracts	Corporate Strategy	●○○○○	●●●●●	●●●●●	●●●○○	●●●●●	NVIDIA signs multi-year HBM supply deals with SK Hynix and others, anticipating shortages through 2028+.
#08	Europe AP Investment	Research/Policy	●●●○○	●●○○○	●●●○○	●●○○○	●●●●●	Europe boosts investment in advanced packaging and chiplet integration, with imec launching FAMES pilot line.
#09	Ibiden/Unimicron ABF	Corporate Strategy	●●○○○	●●●○○	●●●●○	●●●○○	●●●●○	Ibiden and Unimicron invest over $5B to boost ABF substrate capacity for AI servers, addressing shortage.
#10	Glass Substrates Race	Technology Analysis	●●●●○	●●●○○	●●●●○	●●●○○	●●●●●	Glass substrates emerge as AI packaging game-changer, accelerating global race for mass production by 2026-2029.
#11	Low-Distortion Bonding	Research	●●●●●	●○○○○	●●●○○	●●●●●	●●●●●	New pneumatic-curved wafer fusion bonding achieves sub-10nm residual distortion for next-gen BSPDN.
#12	AP Tech Evolution	Technology Analysis	●○○○○	●●●●●	●●●●○	●●●○○	●●●●●	Advanced packaging evolves with 2.5D/3D, chiplets, and hybrid bonding driving AI/HPC, with glass core emerging.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#13	Intel-Tesla AI Packaging	Corporate Strategy	●●●○○	●●●○○	●●●●○	●●○○○	●●●●●	Intel and Tesla partner for AI6 data center chips, leveraging Intel's EMIB/Foveros advanced packaging at Terafab.
#14	Apple M5 Ultra SoIC-mH	New Product	●●●●○	●●●●○	●●●●○	●●●○○	●●●●●	Apple's M5 Ultra chip likely to use TSMC's N3P process and SoIC-mH high-density packaging for Mac Studio.
#15	TSMC COUPE CPO	New Product	●●●●○	●●●○○	●●●●○	●●●○○	●●●●○	TSMC to mass produce COUPE (CPO) in 2026, integrating Micro LED for AI clusters, targeting lower latency.

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI chip supply chain exposed to packaging bottlenecks?

TSMC's CoWoS capacity is expanding tenfold but still can't meet demand. HBM supply is projected to remain short through 2028-2029. Are your procurement strategies robust enough to secure critical advanced packaging and HBM components?

❷ How will glass substrates disrupt your packaging roadmap?

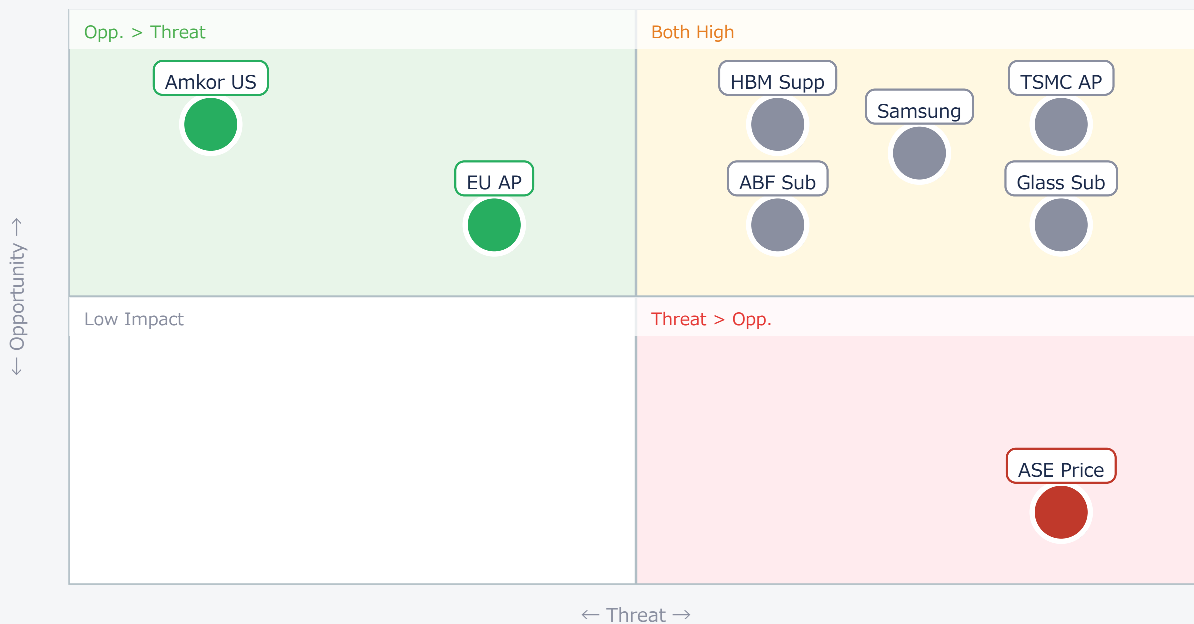
Intel, TSMC, Samsung, and SK Absolics are racing to commercialize glass substrates by 2026-2029. This technology promises superior performance for AI/HPC. Does your R&D; have a strategy to integrate or compete with this shift?

❸ Are US/EU regional packaging efforts sufficient for resilience?

Amkor's $7B US investment and Europe's imec FAMES pilot line aim to localize advanced packaging. Are these initiatives creating a resilient enough supply chain for your US/EU operations, or will reliance on Asia persist?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
● TSMC AP	Critical	Access advanced AP	Capacity bottleneck
● HBM Supp	Critical	Secure long-term deals	Chronic shortages
● ASE Price	Threat	—	Increased packaging cost
● Amkor US	Opp.	US supply resilience	—
● Glass Sub	Critical	Next-gen performance	Tech transition risk
● ABF Sub	Critical	Invest in materials	Critical material lack
● Samsung	Critical	HCB tech access	Competitive pressure

● EU AP	Opp.	EU R&D;, local sourcing	—

Deep Dive ① — TSMC's Aggressive AI Packaging Expansion

#01 | 2026/06/10 | Tom's Hardware | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●●

TSMC is dramatically scaling CoWoS capacity tenfold to 130,000 wafers/month by late 2026 to meet surging AI demand, though supply will still lag. The AP7 site becomes its largest SoIC campus for next-gen GPUs.

Concurrently, TSMC accelerates CoPoS development, a panel-level packaging technology using glass substrates, targeting mass production by 2028-2029. Glass offers superior dimensional stability, lower CTE, and finer interconnects for future AI chips.

> ▶ Strategic Analyst's Perspective
>
> Strategic Analyst's Perspective: TSMC's capacity expansion is realistic given the AI boom, but demand outstripping supply is a persistent challenge. The shift to glass substrates (CoPoS) is a critical technical barrier, requiring new materials and process flows, but promises significant performance gains. [Opportunity] for US/EU materials & equipment suppliers to partner on glass substrate tech; for OEMs to gain access to higher-performance packaging. [Threat] for US/EU OEMs if they cannot secure sufficient CoWoS/CoPoS capacity, risking market share. [Action] Procurement & Strategy teams must engage TSMC and its ecosystem partners (HBM, substrate vendors) immediately to understand future capacity allocation and technology roadmaps by Q3 2026.

Deep Dive ② — Amkor's $7B US Advanced Packaging Investment

#06 | 2026/06/05 | Amkor | Tech Novelty●●●○○ Proximity●●●○○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●●

Amkor Technology is expanding its Arizona advanced packaging and test facility investment to over $7 billion, up from $2 billion. This aims to bolster the US semiconductor ecosystem for AI, HPC, mobile, and automotive sectors.

The facility, supported by the US CHIPS Act, will focus on high-density chiplet integration, 2.5D/3D packaging, and advanced test services. It will create over 1,300 jobs and collaborate with TSMC and Intel to build an integrated domestic ecosystem.

> ▶ Strategic Analyst's Perspective
>
> Strategic Analyst's Perspective: Amkor's substantial investment is a credible move to localize advanced packaging in the US, driven by the CHIPS Act. While the technology itself isn't novel, the strategic placement and scale are significant. Technical barriers include workforce development and establishing a robust local supply chain for materials. [Opportunity] for US/EU OEMs to diversify their packaging supply chain away from Asia, reducing geopolitical risk; for US/EU materials & equipment suppliers to serve a growing domestic market. [Threat] for Asian OSATs facing increased competition in the US market. [Action] Procurement and Strategy teams should evaluate Amkor's capabilities and timeline for US-based advanced packaging services by Q4 2026 to assess supply chain diversification options.

Deep Dive ③ — Glass Substrates: The Next AI Packaging Frontier

#10 | 2026/06/11 | The Economy | Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○ Data Reliability●●●○○ US/EU Relevance●●●●●

Glass substrates are emerging as a game-changer for AI chip advanced packaging, offering superior dimensional stability, thermal properties, and finer interconnects over organic or silicon interposers.

Intel has invested over $1B, showcasing EMIB+glass samples. TSMC (CoPoS), Samsung, and SK Absolics (US fab targeting 2026 mass production) are also accelerating glass substrate solutions, with mass production aimed for 2026-2029.

> ▶ Strategic Analyst's Perspective
>
> Strategic Analyst's Perspective: The global race for glass substrates is real and critical. The published targets for mass production by 2026-2029 are ambitious but plausible given the industry's investment. Technical barriers include developing robust manufacturing processes for large-panel glass, managing warpage, and ensuring cost-effectiveness. [Opportunity] for US/EU materials suppliers (e.g., specialized glass, bonding materials) and equipment manufacturers to become key enablers; for OEMs to gain significant performance advantages in AI/HPC. [Threat] for US/EU companies reliant on traditional organic substrates if they fail to adapt quickly; for those without access to this next-gen technology. [Action] R&D; and Business Development teams should initiate partnerships with glass substrate developers and evaluate integration pathways into future product designs within the next 6 months.

Other Notable Articles

Samsung HBM Hybrid Bonding (TrendForce)
Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○

Samsung plans new advanced packaging fab and full transition to Hybrid Copper Bonding (HCB) for HBM by 2029.

ASE, AI demand drives 2026 advanced packaging price hike (AXTEK)
Tech Novelty●○○○○ Proximity●●●●● Market Impact●●●●○

World's largest OSAT, ASE, to increase advanced packaging prices by 5-20% in 2026 due to AI-driven demand.

NVIDIA secures HBM supply through 2028+ (gagadget.com)
Tech Novelty●○○○○ Proximity●●●●● Market Impact●●●●●

NVIDIA signs multi-year HBM supply contracts with SK Hynix and others, anticipating shortages to persist.

Ibiden & Unimicron invest >$5B in ABF substrates for AI (Next Financial)
Tech Novelty●●○○○ Proximity●●●○○ Market Impact●●●●○

Major Japanese and Taiwanese suppliers are investing heavily to address the critical ABF substrate shortage for AI servers.

Apple M5 Ultra to use TSMC N3P & SoIC-mH (TrendForce)
Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●○

Apple's next-gen M5 Ultra chip is expected to leverage TSMC's N3P process and advanced SoIC-mH packaging for high-density integration.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Conduct an urgent audit of HBM, advanced packaging (CoWoS/SoIC), and ABF substrate supply contracts and projected allocations through 2028.
- [Strategy] Assess the immediate impact of ASE's 5-20% price hike on 2026 product margins and adjust pricing/cost models accordingly.
- [Executive] Review current AI chip procurement strategies in light of NVIDIA's long-term HBM deals; identify potential competitive disadvantages.

Short-term (1 month)

- [R&D;] Initiate a technical feasibility study on integrating glass substrates into next-generation packaging designs, focusing on thermal and electrical performance.
- [Business Dev] Engage with Amkor's US operations to understand capabilities and timelines for domestic advanced packaging services for potential supply chain diversification.
- [Procurement] Explore alternative or second-source suppliers for critical ABF substrates and HBM, even if at a premium, to mitigate single-point-of-failure risks.

Medium-long term (quarter+)

- [R&D;] Establish internal R&D; programs or external partnerships focused on hybrid bonding and advanced 3D stacking techniques (e.g., SoIC-mH, CoPoS) to stay competitive.
- [Strategy] Develop a long-term strategy for regionalizing advanced packaging and testing capabilities, leveraging US/EU government incentives (e.g., CHIPS Act, EU Chips Act).
- [Legal/IP] Monitor IP developments around glass substrates and hybrid bonding to identify licensing opportunities or potential infringement risks.

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Semiconductor_BackEnd — Selected Articles

Date: 2026-06-13

Articles: 15

Table of Contents

#01 TSMC to Boost CoWoS Capacity Tenfold to 130K Wafers/Month by Late 2026, Accelerates Glass-Substrate CoPoS for AI Chips

#02 SK Hynix、HBM4生産拡大に向けHanmi Semiconductorから442億ウォンのTC Bonderを受注、清州M15X工場に設置へ

#03 Samsung、光州に先端パッケージング工場建設検討とHBMハイブリッドボンディング能力を2029年までに全面移行へ

#04 Silicon Box、7750万米ドルの融資を獲得し先端パッケージングとチップレット統合事業を拡大

#05 ASE、AI需要急増を背景に2026年の先端パッケージング価格を5～20%引き上げへ

#06 Amkor、アリゾナ州に先端パッケージング工場を建設、米国半導体エコシステム強化へ70億ドル超を投資

#07 NVIDIA、2028年以降も続くHBM供給不足を見越してSK Hynixを含む主要メーカーと複数年契約を締結

#08 欧州、先端パッケージングとチップレット統合へ投資強化、imecはFAMESパイロットライン稼働で地域サプライチェーンリスク軽減へ

#09 IbidenとUnimicron、AIサーバー向けABF基板生産能力を大幅増強へ合計8000億円超を投資

#10 AIパッケージングの新たなゲームチェンジャー：ガラス基板が量産に向けた世界的な競争を加速

#11 ArXiv論文：空圧で湾曲させたウェーハを用いた低歪みフュージョンボンディングでサブ10nmの残存歪みを達成

#12 先端パッケージング技術の進化：2.5D/3D統合、チップレット、ハイブリッドボンディングがAI・HPCを牽引

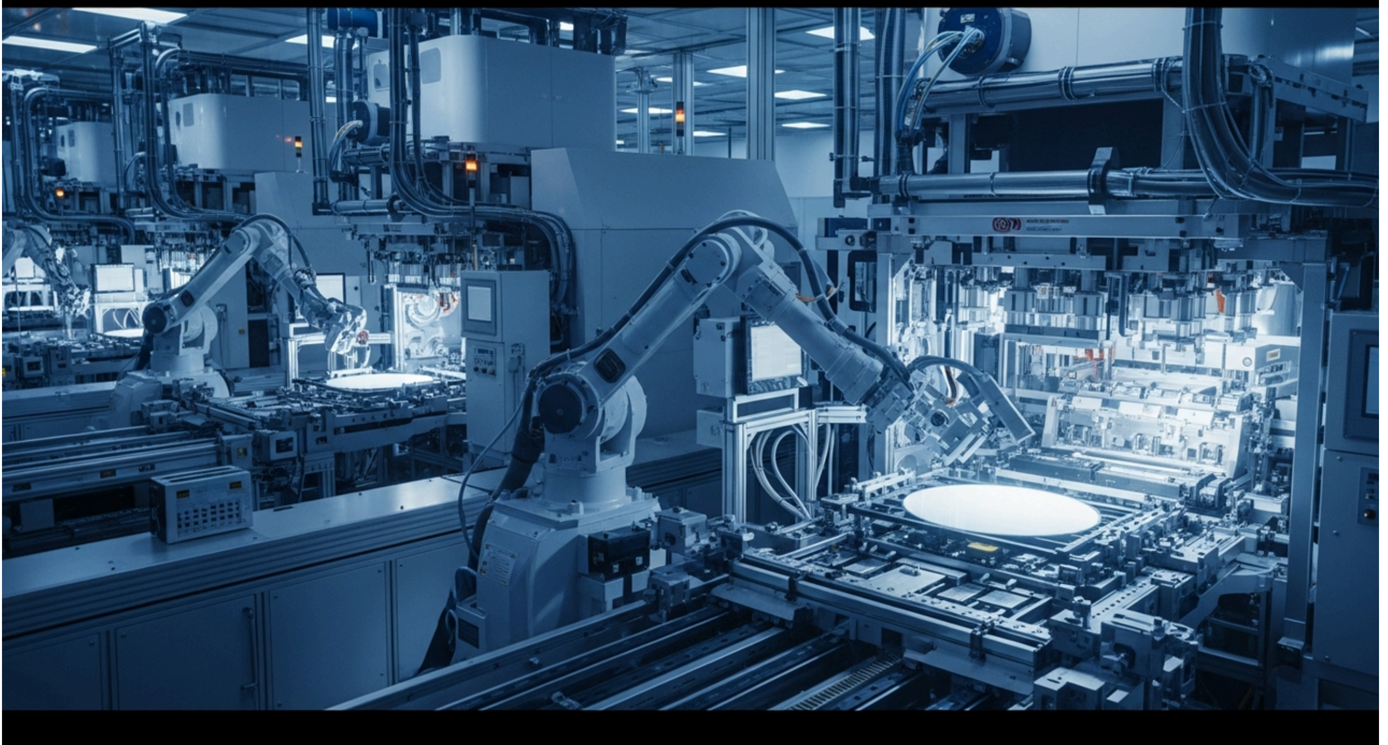
#13 IntelとTeslaがAI6データセンター向けに先進パッケージングで提携、オースティンの「Terafab」で生産

#14 Apple次世代M5 Ultraチップ、TSMCのN3Pプロセスと高密度パッケージング技術SoIC-mHを採用か

#15 TSMC、コパッケージドオプティクス向け「COUPE」を2026年量産開始、Micro LED統合でAIクラスター性能向上へ

TSMC to Boost CoWoS Capacity Tenfold to 130K Wafers/Month by Late 2026, Accelerates Glass-Substrate CoPoS for AI Chips

Published June 10, 2026 Tom's Hardware USA



OVERVIEW

TSMC is aggressively expanding its advanced packaging capacity, projecting a tenfold increase in CoWoS production to over 130,000 wafers per month by the end of 2026 to meet surging AI demand. Despite this, demand is still expected to outpace supply, with the AP7 site becoming its largest SoIC campus for Nvidia's next-gen GPUs. The company is also accelerating the development of CoPoS, a panel-level packaging technology using glass substrates, targeting mass production by 2028-2029 to enhance performance and reduce costs for future AI chips.

IN DEPTH

Key Findings

TSMC is dramatically scaling up its advanced packaging capabilities, specifically for CoWoS (Chip-on-Wafer-on-Substrate) and SoIC (System-on-Integrated-Chips) technologies, to address the insatiable demand for AI accelerators. The company plans to boost CoWoS production capacity to more than 120,000-130,000 wafers per month by the end of 2026, a more than tenfold increase from late 2023 levels. However, this aggressive expansion is still anticipated to be outstripped by the explosive growth in AI chip demand. Concurrently, TSMC is accelerating the development of CoPoS, a panel-level packaging technology utilizing glass substrates, aiming for mass production between 2028 and 2029.

Technical Details

TSMC's strategy centers on its 2.5D and 3D packaging solutions. CoWoS integrates logic chips and High Bandwidth Memory (HBM) onto a silicon interposer, significantly enhancing data transfer speeds and power efficiency, critical for modern AI workloads. Variations such as CoWoS-S, CoWoS-R, and CoWoS-L are tailored for leading customers like AMD, NVIDIA, and Apple. SoIC, a more advanced 3D stacking technique, enables direct die-to-die bonding at the wafer level, creating ultra-high-density interconnects. The AP7 site in Chiayi is being developed as TSMC's largest advanced packaging campus, primarily leveraging SoIC for NVIDIA's next-generation GPUs, while AP8 is expected to exceed 40,000 CoWoS wafers per month by late 2026.

Furthermore, TSMC's investment in glass-core substrates for its CoPoS technology represents a significant leap forward. Glass substrates offer superior dimensional stability, lower coefficient of thermal expansion (CTE), and finer interconnect capabilities compared to traditional organic substrates. This allows for higher-density chip integration, improved thermal management, and enhanced signal integrity, ultimately boosting AI chip performance and potentially reducing manufacturing costs. This transition is crucial for overcoming the physical limitations of current organic interposers and meeting future performance requirements.

Background and Context

The proliferation of AI applications has made advanced packaging a critical bottleneck in the semiconductor supply chain, with memory and packaging now accounting for 60-70% of AI chip costs. NVIDIA, a dominant player in the AI accelerator market, reportedly secures approximately 60% of TSMC's CoWoS capacity, creating supply constraints for other companies and slowing the overall deployment of AI infrastructure. This ongoing shortage underscores the strategic importance of packaging capacity. TSMC's roadmap involves tight collaboration with HBM suppliers, substrate vendors, OSAT partners, and toolmakers to ensure a robust and integrated ecosystem capable of sustaining AI's rapid growth.

Strategic Significance and Outlook

The aggressive capacity expansion by TSMC, combined with its innovation in technologies like CoPoS, is pivotal for unlocking future advancements in AI and high-performance computing. While immediate supply relief remains challenging due to persistently high demand, these investments are foundational for the long-term growth of the AI industry. The shift towards glass-core substrates and panel-level packaging promises to deliver significant improvements in power efficiency, bandwidth, and cost-effectiveness, paving the way for even more powerful and complex AI systems. TSMC's leadership in this domain will continue to dictate the pace of innovation across the broader semiconductor landscape, influencing everything from data centers to edge AI applications.

Source: https://www.tomshardware.com/tech-industry/semiconductors/analyzing-tsmcs-fab-expansion-roadmap-multi-fab-n2-ramp-cowos-soic-and-uncorking-bottlenecks

Collected: June 12, 2026 | Automated Research System (Gemini API)

SK Hynix Boosts HBM4 Production with Major TC Bonder Order from Hanmi Semiconductor

Published Published June 08, 2026 The Korea Herald South Korea

OVERVIEW

SK Hynix has made a significant investment, ordering ₩44.2 billion (approx. $28.7 million USD) worth of advanced 'TC Bonder 4.5 Griffin' thermo-compression bonders from Hanmi Semiconductor. This strategic move aims to fortify its HBM4 production capabilities at the new Cheongju M15X factory by September 2026, directly addressing the escalating demand for AI chips and reinforcing its position as a key HBM4 supplier for customers like NVIDIA.

IN DEPTH

Background

The rapid advancement of artificial intelligence (AI) has ignited an unprecedented demand for high-performance memory, particularly High Bandwidth Memory (HBM). This surge has led to significant HBM supply shortages, which are fast becoming a critical bottleneck for the entire AI chip market. Industry analysts, such as Bernstein, project that while TSMC's CoWoS packaging capacity is expected to reach 125,000 wafers per month by the end of 2026, HBM demand is forecast to outpace this supply increase.

NVIDIA stands as a primary customer for next-generation AI accelerators featuring HBM4. Although SK Hynix, Samsung, and Micron are all certified HBM4 suppliers, SK Hynix is widely anticipated to secure the majority of HBM4 supply for NVIDIA's Vera Rubin platform. Responding to this immense AI-driven demand, SK Hynix has already sold out its HBM supply for 2026 and plans substantial capacity expansions, including an investment of approximately $200 billion for an advanced HBM packaging plant in Indiana slated for operation by late 2028. The current equipment procurement from Hanmi Semiconductor represents a strategic, pre-emptive investment by SK Hynix aimed at bolstering HBM4 mass production and solidifying its leadership in this crucial memory segment.

Key Announcement

SK Hynix has placed a substantial order totaling ₩44.2 billion (approximately $28.7 million USD) with Hanmi Semiconductor for its state-of-the-art “TC Bonder 4.5 Griffin” equipment. This strategic capital expenditure is designed to significantly enhance SK Hynix's cutting-edge HBM4 production capabilities. The acquired equipment is scheduled for installation at SK Hynix’s new M15X factory in Cheongju by early September 2026, positioning the company for an early ramp-up of HBM4 mass production to meet the explosive growth in AI chip demand and establish a stable supply system for this next-generation memory.

Technical Specifications and Strategic Advantage

Thermo-compression bonders (TC Bonders) are a cornerstone of the HBM manufacturing process, representing one of the most critical post-packaging stages. These sophisticated machines are essential for precisely stacking multiple DRAM chips vertically to form a multi-layer HBM module. Hanmi Semiconductor's “TC Bonder 4.5 Griffin” is specifically engineered to deliver high precision, rapid processing speeds, and superior yield, particularly for high-layer-count memories like HBM4.

This advanced bonding technology is paramount for enabling fine-pitch copper-to-copper bonding and other sophisticated interconnection techniques, which critically determine the overall performance, thermal dissipation, and reliability of the entire HBM stack. By integrating these state-of-the-art bonders into its new M15X factory currently under construction in Cheongju, SK Hynix aims to dramatically expand its DRAM and HBM production capacities, specifically establishing a robust mass production system for HBM4. Furthermore, SK Hynix is recognized as a key supplier of HBM4 for NVIDIA's Vera Rubin platform, leveraging proprietary technologies such as Mass Reflow Molded Underfill (MR-MUF) in conjunction with these new bonders to secure a significant competitive advantage.

Future Outlook and Strategic Implications

SK Hynix’s procurement of TC Bonders from Hanmi Semiconductor marks a pivotal milestone in its strategy to establish a robust mass production system for HBM4. This significant investment is underpinned by persistent industry forecasts predicting continuous growth in HBM demand within the AI market through 2030. SK Hynix plans to fully outsource HBM4 base die production to TSMC’s 12nm process and integrate MR-MUF technology with the new TC Bonders in the packaging stage to achieve both high yields and superior performance.

Looking ahead, the company is committed to continuous investment in the development of even higher-density HBM stacks, including future generations like HBM4E and HBM5. By leading the evolution of HBM technology, SK Hynix aims to maintain its dominant position in the AI-driven memory market. These proactive capital expenditures and technological advancements are expected to play a crucial role in alleviating current HBM supply shortages, thereby fostering further development and expansion of the overall AI infrastructure.

Source: https://www.koreaherald.com/article/10766606

Collected: June 12, 2026 | Automated Research System (Gemini API)

Samsung to Establish Gwangju Advanced Packaging Facility, Eyes Full HBM Hybrid Bonding Transition by 2029

Published Published June 10, 2026 TrendForce South Korea

OVERVIEW

Samsung Electronics is reportedly considering a new advanced semiconductor packaging plant in Gwangju, South Korea, with investment plans potentially announced by June 2026. This strategic facility will focus on advanced packaging, especially for High Bandwidth Memory (HBM) production. Concurrently, Samsung aims to significantly expand HBM post-processing capacity at its Cheonan plant by late 2026 and plans a complete migration from Thermo-Compression Bonding (TCB) to Hybrid Copper Bonding (HCB) for HBM stacking by 2029, a move crucial for next-generation AI and HPC applications.

IN DEPTH

Background

The burgeoning proliferation of artificial intelligence (AI) has ignited an unprecedented demand for high-performance High Bandwidth Memory (HBM), transforming HBM supply assurance and advanced packaging technology into a critical competitive frontier within the semiconductor industry. Samsung, alongside rivals SK Hynix and Micron, has been designated a key supplier for HBM4, destined for NVIDIA's next-generation "Vera Rubin" AI accelerator platform, intensifying the technological race. NVIDIA CEO Jensen Huang has engaged in ongoing discussions with Samsung regarding future HBM solutions, encompassing HBM4, HBM4E, and HBM5, underscoring the strategic importance of this memory segment.

Beyond core technological advancements, global supply chain diversification and enhanced regional production capabilities are increasingly prioritized imperatives. In response, Samsung is expanding its international footprint, including a substantial $1.5 billion investment in a semiconductor test facility in Vietnam. The broader industry is also witnessing accelerated investments in advanced packaging from other key players, such as Amkor Technology, with a new facility in Arizona, and integrated device manufacturers like TSMC and Intel, all collectively striving to alleviate bottlenecks in HBM and AI chip production.

Key Findings

To decisively bolster its leadership in the HBM market, Samsung Electronics is reportedly exploring the construction of a new advanced semiconductor packaging plant in Gwangju, South Korea. This substantial investment, which could be formally announced as early as June 2026, is a cornerstone of Samsung's strategy to significantly expand its HBM production capacity and accelerate a complete transition to Hybrid Copper Bonding (HCB), a pivotal next-generation HBM technology.

Samsung is aggressively enhancing its HBM post-processing capabilities at its existing Cheonan facility. By the close of 2026, the company targets a monthly capacity of 231,000 units for conventional Thermo-Compression Bonding (TCB), alongside a robust expansion to 19,500 units for the more advanced HCB. HCB represents a significant leap from traditional micro-bump bonding, enabling direct copper-to-copper interconnects. This innovation facilitates a connection pitch of less than 10 micrometers between stacked DRAM chips, resulting in a substantial reduction in HBM stack height, enhanced data transmission bandwidth, a thermal resistance reduction exceeding 20%, and improved power efficiency.

Samsung has positioned HCB technology as the core enabler for its HBM4 and future HBM5 generations, charting a complete migration from TCB to HCB across its HBM stacking roadmap by 2029. At NVIDIA GTC 2026, Samsung showcased the capability of HCB technology to enable HBM stacks of 16 layers or more, projecting that next-generation HBM4E will achieve a formidable 16 Gbps/pin and a bandwidth of 4.0 TB/s. Furthermore, by integrating advanced 4nm process technology for the HBM4 base die, strategically bypassing the traditional 12nm process, Samsung has demonstrated significant improvements in energy efficiency and achieved over 40% yield during test production.

Samsung's proposed Gwangju facility and the pervasive adoption of HCB technology are set to decisively sharpen its competitive edge in the HBM market. HCB is a critical innovation that will unlock further memory chip stacking density and performance, pushing the computational limits for AI and High-Performance Computing (HPC) applications. Leveraging its inherent advantages as an Integrated Device Manufacturer (IDM), Samsung aims to differentiate itself by optimizing the entire semiconductor value chain, from DRAM manufacturing to advanced packaging. This integrated strategy is expected to play an indispensable role in powering the evolution of AI chips and realizing next-generation computing, while simultaneously reinforcing the resilience of the global semiconductor supply chain.

Source: https://www.trendforce.com/news/2026/06/10/news-samsung-may-announce-new-gwangju-

advanced-packaging-base-by-end-june-as-capacity-expansion-continues/

Collected: June 12, 2026 | Automated Research System (Gemini API)

Silicon Box Secures $77.5M to Scale Advanced Packaging and Chiplet Integration

Published Published June 09, 2026 DealStreetAsia Singapore

OVERVIEW

Singapore-based semiconductor packaging and chiplet integration startup, Silicon Box, has secured S$100 million (approximately US$77.5 million) in debt financing from a global consortium of institutional investors. This funding will significantly expand its manufacturing capabilities to meet the escalating global demand for advanced semiconductor packaging solutions, especially for AI and High-Performance Computing (HPC). Since commencing mass production in 2025, the company has demonstrated rapid growth, having shipped over 250 million semiconductor units from its Singapore facility by Q1 2026.

IN DEPTH

Background

In recent years, the semiconductor industry has confronted the physical limits of Moore's Law, prompting a shift towards chiplets and advanced packaging as crucial enablers for enhancing next-generation semiconductor performance and reducing costs. For demanding applications like AI accelerators and data center chips, the seamless integration of High Bandwidth Memory (HBM) with high-performance logic chiplets has become indispensable. This necessitates sophisticated advanced packaging technologies such as TSMC's CoWoS and Intel's Foveros, which play a pivotal role in overcoming traditional integration hurdles.

Key Findings

Silicon Box, an innovative startup specializing in semiconductor packaging and chiplet integration, has successfully secured S$100 million (approximately US$77.5 million) in debt financing from a global consortium of institutional investors. This significant capital injection is primarily earmarked for a substantial expansion of the company's manufacturing capacity, directly addressing the soaring global demand for advanced semiconductor packaging solutions, particularly in rapidly growing sectors like Artificial Intelligence (AI) and High-Performance Computing (HPC). Furthermore, since initiating mass production in 2025, Silicon Box has achieved remarkable growth, shipping over 250 million semiconductor units from its state-of-the-art Singapore manufacturing facility by the first quarter of 2026.

Technical Deep Dive

Silicon Box distinguishes itself by specializing in chiplet architecture and proprietary advanced packaging technology. The company's innovative approach involves densely integrating multiple functional blocks, known as chiplets, within a single package. This methodology offers superior design flexibility, enhanced performance, and greater cost-efficiency compared to conventional monolithic chip designs. Crucially, it allows for the combination of chiplets manufactured using disparate process nodes, fundamentally transforming the paradigm of semiconductor design and manufacturing. This capability is vital for optimizing performance and cost in an era of increasingly complex and specialized silicon.

Industry Context

Against the backdrop of the semiconductor industry's evolution, chiplet integration solutions provided by specialized entities like Silicon Box are becoming increasingly vital. These solutions contribute significantly to diversifying and strengthening the overall resilience of the semiconductor supply chain. At a time when nations globally are striving to bolster domestic semiconductor manufacturing capabilities, the emergence and growth of advanced technology companies in strategic locations like Singapore hold profound implications for the robustness and innovation within the broader Asian semiconductor ecosystem.

Future Outlook

This US$77.5 million debt financing is poised to serve as a powerful catalyst for Silicon Box, enabling it to further solidify its leadership position within the burgeoning chiplet market. The company is strategically positioned to leverage this capital to expand its manufacturing infrastructure and broaden its customer base, specifically targeting the next generation of AI and HPC chips. As advanced packaging technology remains one of the most critical frontiers for continuous enhancements in semiconductor performance, Silicon Box's trajectory of growth is expected to contribute substantially to overall technological innovation and market expansion across the entire semiconductor industry. With the ongoing efforts towards standardization within the chiplet ecosystem, exemplified by initiatives like the UCIe consortium, the prominence and strategic importance of independent packaging providers such as Silicon Box are anticipated to grow even more significantly.

Source: https://www.dealstreetasia.com/stories/silicon-box-secures-debt-financing-484910

ASE to Raise Advanced Packaging Prices by Up to 20% by 2026 Amid Soaring AI Demand

Published Published June 07, 2026 AXTEK Technology Company Limited Taiwan

OVERVIEW

ASE Technology Holding, the world's largest OSAT provider, plans to increase its backend wafer packaging prices by 5-20% in 2026, driven by a surge in AI-powered semiconductor demand. With advanced packaging capacity utilization projected to reach approximately 90% by 2025 and limited room for expansion in existing facilities, ASE holds strong leverage in upcoming price negotiations. Its LEAP advanced packaging platform is forecast to generate over $3.5 billion in revenue by 2026, as the company prioritizes high-margin AI clients and accelerates the deployment of its proprietary FoCoS (Fan-Out Chip on Substrate) technology.

IN DEPTH

Background

The evolution of artificial intelligence is profoundly impacting the entire semiconductor supply chain, from front-end wafer fabrication to back-end packaging and testing. AI chips, in particular, necessitate the integration of multiple logic dies and High Bandwidth Memory (HBM) into a single package, making advanced technologies like TSMC's CoWoS critically important. However, advanced packaging capacities, including CoWoS, are facing chronic shortages, creating a significant bottleneck for the broader AI chip market. ASE's impending price hike directly reflects this supply-demand imbalance, underscoring the substantially elevated strategic value of packaging within the semiconductor industry. The company's strategy to prioritize high-margin AI-related customers further signals its intent to fully capitalize on the growth opportunities presented by the AI market.

Key Findings

ASE Technology Holding (ASE) has announced its intention to raise prices for its advanced packaging services by 5% to up to 20% in 2026, driven by an explosive surge in AI chip demand. This price adjustment reflects both the current market situation where supply cannot keep pace with demand, and the increasing technical complexity inherent in advanced packaging technologies.

Technical Details

As a leading company in the OSAT industry, ASE offers sophisticated packaging solutions including 2.5D and 3D packaging, chiplet integration, and High Bandwidth Memory (HBM) integration. Its "LEAP (Large-area advanced Packaging)" service platform is specifically designed for high-performance applications such as AI accelerators, High Performance Computing (HPC), and autonomous vehicles, encompassing a broad technological portfolio that includes flip-chip, fan-out, Wafer Level Package (WLP), and System-in-Package (SiP). Through its proprietary FoCoS (Fan-Out Chip on Substrate) technology, ASE achieves high-density interconnects and superior thermal management, meeting customers' stringent performance demands. With utilization rates for advanced packaging already reaching approximately 90% by 2025, expanding new advanced packaging capacity is not straightforward, making supply constraints a primary driver of the price increases.

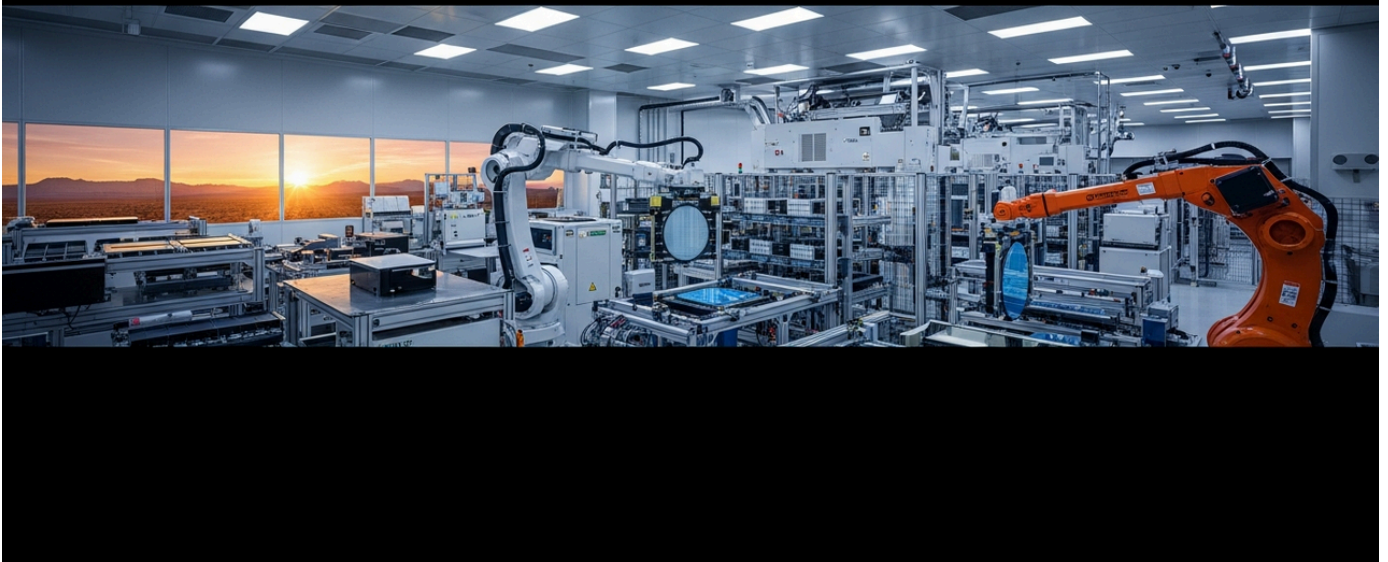
Outlook

ASE's increase in advanced packaging prices is expected to significantly boost the company's revenue and profit margins in 2026. The target of over $3.5 billion in revenue for its LEAP services further underscores that AI-related business is driving ASE's growth. ASE is expanding its factory construction programs not only in Taiwan but also in other regions such as Vietnam, aiming to strengthen its global production capacity to meet long-term market demand. Through price adjustments and capacity expansion, ASE is poised to reinforce its position within the semiconductor value chain in the AI era and to drive further innovation in advanced packaging technologies. Ultimately, these efforts will contribute to enhanced performance and accelerated market deployment of AI chips, thereby supporting the sustainable growth of the entire semiconductor industry.

Source: https://www.axtekic.com/news/ase-2026-price-increase:-ai+driven-advanced-packaging.html

Amkor Bolsters U.S. Semiconductor Ecosystem with Over $7 Billion Investment in Arizona Advanced Packaging Facility

Published Published June 05, 2026 Amkor USA



OVERVIEW

Amkor Technology is dramatically escalating its commitment to a new advanced packaging and test facility in Peoria, Arizona, increasing its investment from an initial $2 billion to over $7 billion. This strategic expansion is set to fortify the U.S. semiconductor supply chain by providing crucial domestic capacity for AI, HPC, and other next-generation technologies, directly supporting the objectives of the CHIPS Act. Concurrently, Amkor has also inaugurated its largest global facility in Vietnam, expanding SiP and memory packaging capabilities to enhance overall global manufacturing resilience.

IN DEPTH

Introduction & Background

Amkor Technology has announced a monumental expansion of its investment in a new state-of-the-art packaging and test facility in Peoria, Arizona, elevating its financial commitment from an initial $2 billion to over $7 billion. This strategic move is poised to play a pivotal role in strengthening the U.S. semiconductor ecosystem, particularly as global supply chain vulnerabilities and geopolitical tensions highlight the urgent need for domestic manufacturing capabilities.

Key Investment & Strategic Expansion

This substantial investment is specifically targeted at supporting the escalating demand for next-generation semiconductor devices across critical growth sectors, including Artificial Intelligence (AI), High-Performance Computing (HPC), mobile communications, automotive, and industrial applications. The Arizona facility is designed to dramatically enhance the resilience and capacity of the U.S. semiconductor supply chain, aligning directly with the objectives of the U.S. CHIPS and Science Act, which provides significant incentives for domestic semiconductor research, development, and manufacturing.

Advanced Packaging Capabilities in Arizona

The new Amkor facility in Peoria, Arizona, is being developed on an expansive site, specifically engineered to specialize in advanced packaging technologies. These capabilities will encompass high-density chiplet integration, 2.5D, and 3D packaging, which are crucial for pushing the boundaries of chip performance. The facility will offer cutting-edge flip-chip packaging, System-in-Package (SiP) solutions, and comprehensive advanced test services, essential for the production of high-performance chips such as AI accelerators and data center GPUs. Upon completion of Phase 1, the facility is projected to employ over 1,300 highly skilled professionals, a critical step in solidifying the U.S.'s position as a semiconductor manufacturing stronghold. Amkor aims to foster a collaborative environment with leading foundry companies like Taiwan Semiconductor Manufacturing Company (TSMC) and Intel, working towards an integrated domestic ecosystem spanning chip manufacturing, packaging, and testing.

Global Manufacturing Footprint: The Vietnam Facility

In parallel with its U.S. expansion, Amkor has also inaugurated Amkor Technology Vietnam (ATV), a state-of-the-art factory located on a 57-acre site within the Yen Phong 2C Industrial Park. This facility stands as Amkor's largest to date, boasting over 200,000 square meters of cleanroom space. It is designed to deliver a broad spectrum of advanced packaging form factors, including SiP and memory packaging, significantly bolstering Amkor's global supply capacity. The initial investment in the Vietnam factory totals $1.6 billion over two phases, underscoring Amkor's dual strategy of enhancing global manufacturing capabilities while boosting U.S. supply chain resilience.

Industry Context & Strategic Significance

The explosive growth in demand for AI chips has made advanced packaging an indispensable element for extending chip performance beyond the traditional limits of Moore's Law. With advanced technologies like TSMC's CoWoS and Intel's Foveros facing capacity constraints for AI accelerators, the role of Outsourced Semiconductor Assembly and Test (OSAT) providers like Amkor is becoming increasingly vital. Amkor's investment directly addresses these bottlenecks, reinforcing the domestic supply chain and reducing reliance on overseas manufacturing for critical components. This move is a direct response to global imperatives for semiconductor manufacturing diversification and security.

Future Outlook & Impact

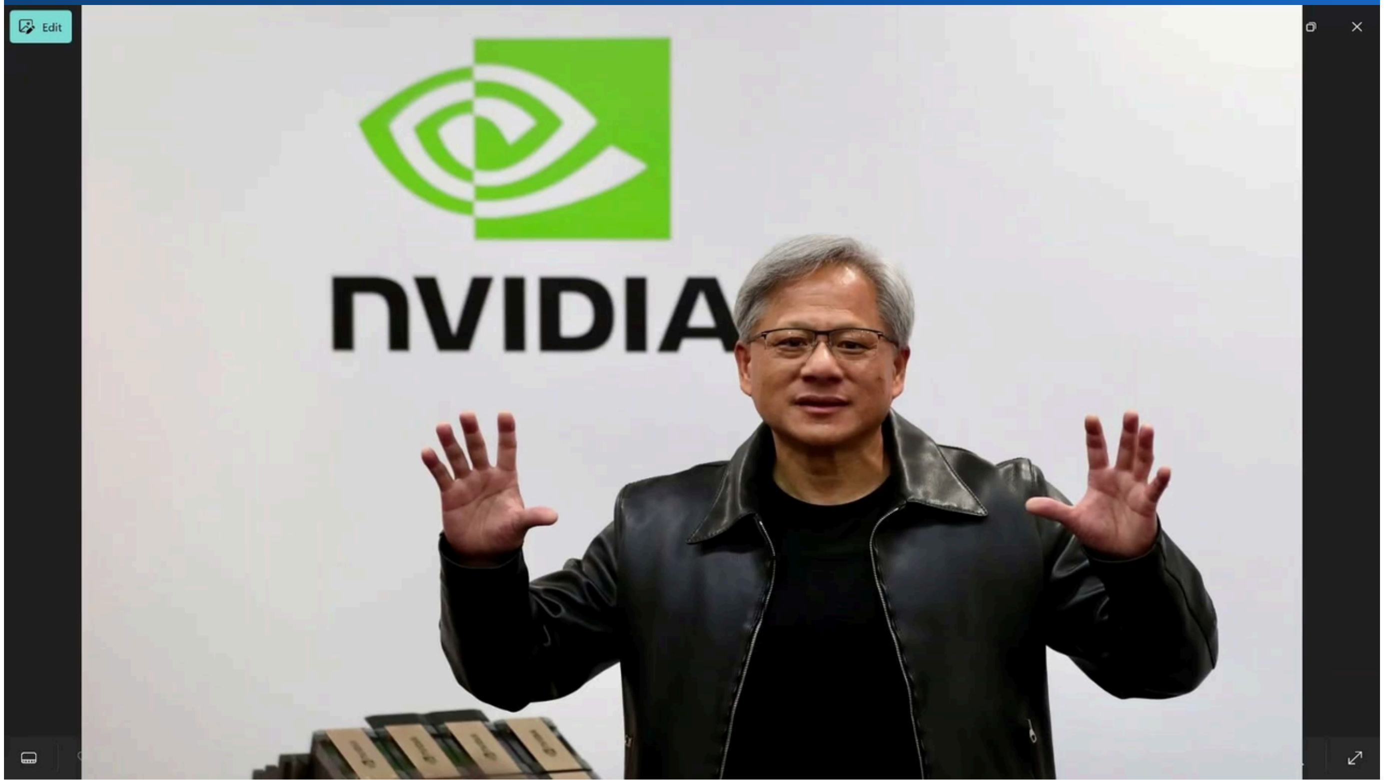
Amkor's extensive investment in its Arizona facility is poised to profoundly impact the revitalization of U.S. semiconductor manufacturing and foster the creation of high-tech domestic employment opportunities. By providing cutting-edge semiconductor packaging services within the U.S., this facility will mitigate geopolitical risks and enhance the resilience of the global supply chain. Amkor is strengthening its global competitiveness by offering advanced solutions from geographically diversified manufacturing locations to customers in burgeoning markets such as AI, HPC, and automotive. This substantial expansion is anticipated to accelerate industry-wide technological innovation and lay a crucial foundation for the development of next-generation AI-driven applications.

Source: https://amkor.com/blog/amkor-ectc-2026-advanced-packaging/

Collected: June 12, 2026 | Automated Research System (Gemini API)

NVIDIA Locks Down Multi-Year HBM Supply Deals, Anticipating Persistent Shortages Beyond 2028

Published Published June 08, 2026 gagadget.com USA



OVERVIEW

NVIDIA CEO Jensen Huang recently visited South Korea, securing multi-year agreements with key partners including SK Hynix, SK Telecom, Naver, and Doosan Group for High Bandwidth Memory (HBM) supply, AI cloud infrastructure, and energy systems. These strategic deals aim to lock in long-term HBM access for NVIDIA, addressing an anticipated supply deficit projected to persist beyond 2028. With HBM demand surging by 80-100% annually against a 50-60% supply growth, analysts forecast shortages until 2028-2029, making SK Hynix a crucial, priority supplier for NVIDIA.

IN DEPTH

Background

The current AI chip market is heavily reliant on advanced packaging technologies like TSMC's CoWoS and the availability of High Bandwidth Memory (HBM), both of which represent significant bottlenecks in AI infrastructure development. CoWoS capacity, for instance, is reportedly fully booked through 2026, and HBM supply is similarly reserved until 2026. HBM demand is surging by an astounding 80-100% annually, while supply growth lags significantly at 50-60%. This widening gap is projected by analysts to sustain supply shortages until 2028-2029, creating a critical constraint on the overall growth of the AI industry. This scarcity has prompted major players like Broadcom to secure HBM allocations for 2026 and 2027, with discussions already underway for contracts extending beyond 2028. NVIDIA's recent multi-year agreement with SK Hynix underscores the exceptionally high strategic value of HBM in the market, demonstrating that robust relationships with key suppliers are increasingly critical for maintaining a competitive edge.

Key Findings

In a strategic move to secure long-term supply stability amidst industry forecasts of persistent HBM shortages extending from 2028 to 2029, NVIDIA CEO Jensen Huang visited South Korea in early June 2026. During his visit, Huang finalized multi-year agreements with key Korean conglomerates including SK Hynix, SK Telecom, Naver, and Doosan Group. These comprehensive deals encompass High Bandwidth Memory (HBM) supply, the establishment of AI cloud infrastructure, and collaboration on related energy systems.

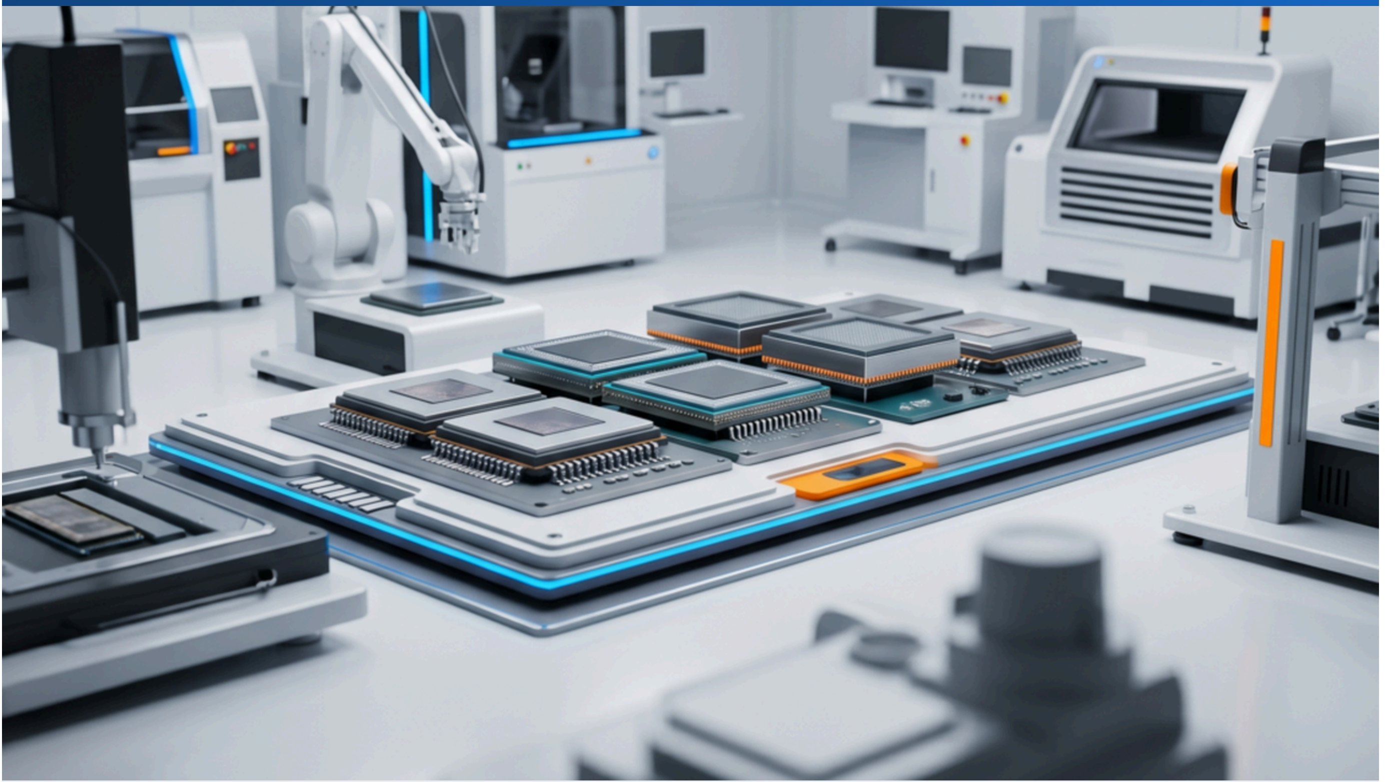
HBM, an essential stacked memory solution featuring ultra-high bandwidth, is critical for maximizing the performance of AI accelerators. As AI chips process increasingly vast datasets, HBM demand has soared at an astounding annual rate of 80-100%. However, supply growth has lagged significantly, expanding by only 50-60% per year, establishing this supply-demand gap as a major bottleneck for the entire AI industry. NVIDIA has committed to adopting HBM4 for its next-generation AI accelerator, the 'Vera Rubin' platform, with all three major memory manufacturers – SK Hynix, Samsung Electronics, and Micron Technology – qualified as HBM4 suppliers. SK Hynix, in particular, demonstrates strong competitiveness in HBM manufacturing through advanced packaging techniques such as Mass Reflow Molded Underfill (MR-MUF), and is anticipated to supply the majority of HBM4 for NVIDIA's Vera Rubin. Beyond securing HBM supply, Huang's visit also included the announcement of plans to establish an AI R&D center in Seoul, leveraging South Korea's robust semiconductor manufacturing capabilities and burgeoning AI technology. This initiative underscores NVIDIA's emphasis on South Korea's role in the fields of physical AI and robotics.

By securing these long-term HBM supply agreements, NVIDIA has fortified its capacity to ensure the stable market introduction of its next-generation AI accelerators. This move is crucial for solidifying NVIDIA's leadership in the AI chip market and maintaining its competitive advantage. Despite these efforts, the overall HBM market tightness remains severe. Major suppliers like SK Hynix (with its Indiana plant scheduled to commence operations in late 2028), Samsung (accelerating its transition to hybrid bonding technology), and Micron are rapidly expanding production capacity through multi-trillion-yen investments. The strengthened partnership between NVIDIA and SK Hynix is expected to accelerate the development of AI technologies, facilitating the realization of diverse AI applications in data centers, robotics, autonomous driving, and beyond. As the resolution of the HBM supply shortage is still anticipated to take several years, this strategic supply assurance will be a pivotal factor in NVIDIA's sustained growth.

Source: https://gagadget.com/en/714099-nvidia-locks-down-korean-memory-deals-as-hbm-shortage-runs-through-2028/

Europe Boosts Investment in Advanced Packaging and Chiplet Integration; imec's FAMES Pilot Line Aims to Mitigate Regional Supply Chain Risks

Published Published June 10, 2026 Astute Group UK



OVERVIEW

Europe is significantly increasing investment in advanced packaging and chiplet integration technologies to diversify its semiconductor supply chain and reduce regional procurement risks, shifting focus from pure wafer fabrication to high-value back-end processes. This strategic move is exemplified by imec's launch of its FAMES pilot line, dedicated to chiplet-based systems for automotive, robotics, and AI, alongside new co-funding opportunities up to €650,000 in Denmark for research and startups in advanced and heterogeneous packaging.

IN DEPTH

Background

The semiconductor industry faces a confluence of challenges, including escalating geopolitical risks, supply chain disruptions exacerbated by pandemics, and surging demand driven by new technologies such as AI. In response, major regions including the U.S. (via the CHIPS Act), Japan, Taiwan, and South Korea are aggressively pursuing the reshoring and diversification of semiconductor manufacturing capabilities. Europe is similarly strengthening its regional semiconductor ecosystem under the European Chips Act, channeling increased funding into packaging infrastructure, prototype production, and workforce development. Advanced packaging, which is becoming an increasingly critical avenue for enhancing chip performance as Moore's Law approaches its physical limits, is central to Europe's strategy to reinforce its competitive and strategic position in the global semiconductor landscape.

Key Findings

Europe is strategically accelerating investments in advanced packaging and chiplet integration to bolster the autonomy and resilience of its semiconductor supply chain. This marks a pivotal shift from a historical focus on wafer fabrication towards higher-value, back-end processes, aiming to mitigate regional procurement risks and secure technological leadership. A significant development is the launch of imec's FAMES (Flexible Assembly & Manufacturing of advanced Electronic Systems) pilot line in Belgium. This state-of-the-art facility is dedicated to advanced process development for efficient, high-performance integration of diverse chiplets, encompassing cutting-edge technologies like 2.5D and 3D stacking, heterogeneous integration, and ultra-fine pitch connections. FAMES targets critical applications in automotive semiconductors, robotics, and AI, while simultaneously supporting in-region prototype manufacturing and fostering a skilled workforce within Europe.

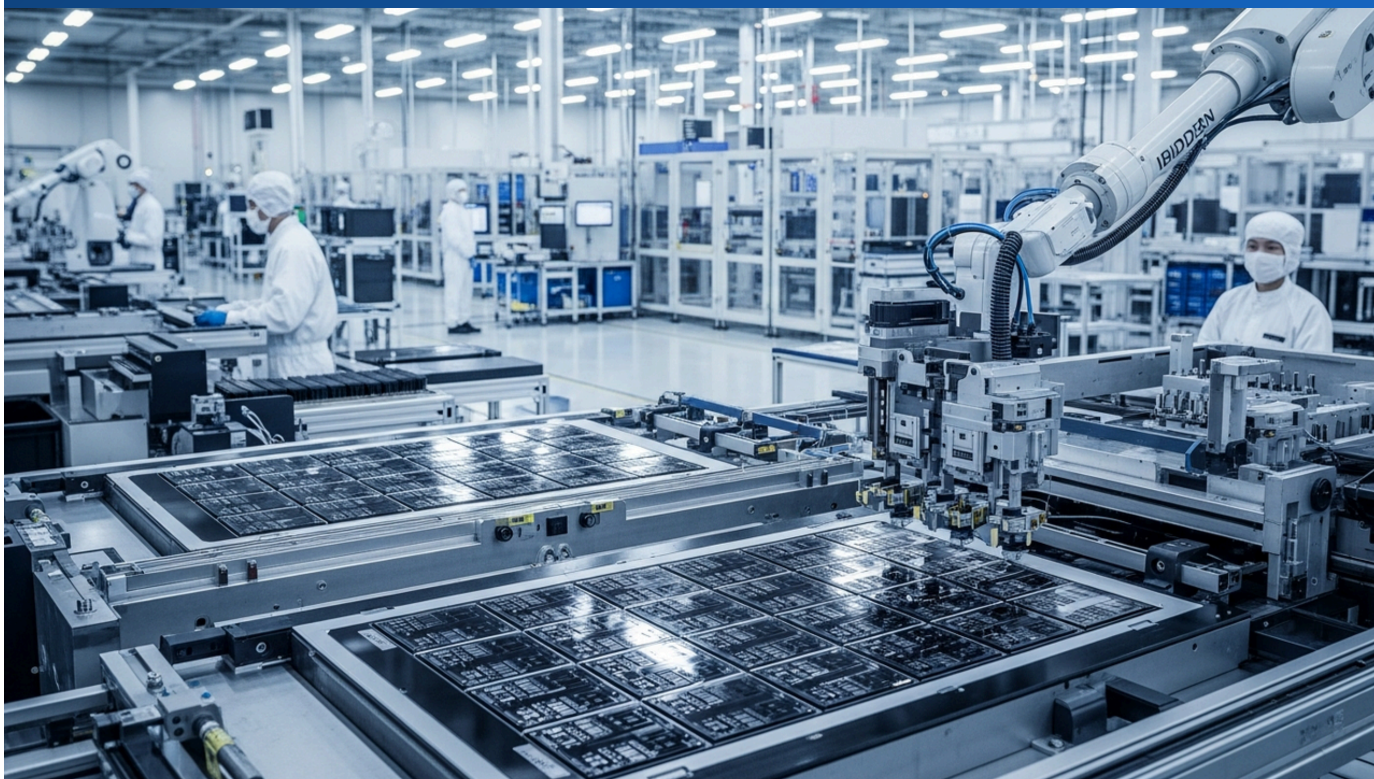
Complementing these efforts, Denmark's "Lab-to-Fab Accelerators" program, established in June 2026, offers new co-funding opportunities—up to €650,000 per project—for researchers, startups, and innovators in advanced packaging and heterogeneous integration, further stimulating region-wide innovation. These initiatives are poised to significantly enhance Europe's long-term semiconductor supply chain resilience and competitiveness. By strengthening crucial research infrastructure like FAMES and promoting vibrant startup ecosystems, Europe aims to catalyze new technological advancements, positioning itself to lead in next-generation fields such as AI, autonomous driving, and the Internet of Things (IoT). These concerted efforts hold the potential to transform Europe from predominantly a semiconductor consuming region into a dynamic, technology-driven innovation hub.

Source: https://www.astutegroup.com/news/general/advanced-packaging-investments-aim-to-reduce-semiconductor-sourcing-risk/

Collected: June 12, 2026 | Automated Research System (Gemini API)

Ibiden and Unimicron Unveil Over $5 Billion Investment to Dramatically Expand AI Server ABF Substrate Production

Published Published June 11, 2026 Next Financial Japan



OVERVIEW

Japanese Ibiden and Taiwanese Unimicron are jointly investing over ¥800 billion (approximately $5 billion USD) to significantly increase production capacity for high-performance ABF (Ajinomoto Build-up Film) substrates. This massive expansion aims to alleviate critical supply shortages of these essential components for AI servers, thereby removing a significant bottleneck in the rapidly expanding AI infrastructure.

IN DEPTH

Background & Industry Context

ABF (Ajinomoto Build-up Film) substrates are indispensable packaging materials for high-performance AI chips and High-Performance Computing (HPC) processors, enabling the high-density integration of multiple chiplets and High Bandwidth Memory (HBM). Their fine wiring patterns, superior electrical characteristics, and thermal stability make them critical for advanced packaging technologies like CoWoS (Chip-on-Wafer-on-Substrate).

The construction of AI infrastructure faces bottlenecks across the entire supply chain, extending beyond the chips themselves to packaging, substrates, materials, and power supply. A particularly severe constraint is the supply of high-grade ABF substrates.

Adding to the challenge, the low-CTE (Coefficient of Thermal Expansion) T-glass cloth, essential for these high-performance ABF substrates, is effectively supplied solely by Nittobo. Projections indicate a 10-20% T-glass shortage in 2026, potentially widening to 20% by 2027. This scarcity of glass fiber is a significant impediment to expanding ABF substrate production capacity.

Driven by insatiable AI chip demand, the ABF substrate market is in a structural growth cycle, with products from major suppliers like Unimicron, Kinsus, and Nan Ya PCB already completely sold out. This situation underscores that ABF substrate supply is now a strategic bottleneck for AI players.

Major Investment Announcement

In response to these escalating supply pressures and the explosive demand for AI chips, Japan's Ibiden and Taiwan's Unimicron have announced plans for a combined investment exceeding ¥800 billion (approximately $5 billion USD) to substantially boost their high-performance ABF substrate production capabilities. This monumental investment aims to address one of the primary bottlenecks in the semiconductor supply chain and meet the surging requirements for AI server components.

Detailed Expansion Plans & Technical Insights

Ibiden is intensifying its AI server substrate production at its Ohno Plant in Gifu Prefecture. While construction is currently only halfway complete, the company will invest approximately ¥500 billion (over $3 billion USD) between fiscal years 2026 and 2028 to further expand capacity. Production at the Ohno facility for AI server substrates initially commenced in October 2025. This investment prioritizes the manufacturing of substrates featuring advanced multi-layer structures and ultra-fine wiring pitches.

Concurrently, Unimicron, a leading Taiwanese ABF substrate manufacturer, has set its capital expenditure for 2026 at over NT$25 billion (approximately $770 million USD) to meet the growing demand for AI substrates. The company plans to increase the supply of high-grade ABF substrates through both optimizing existing production lines and introducing new manufacturing equipment.

It's worth noting that the specialized ABF film, crucial for manufacturing these substrates, is exclusively supplied by Ajinomoto Fine-Techno. The complex manufacturing processes involved and stringent yield requirements for ABF substrates are key contributors to the current supply bottleneck.

Future Outlook & Implications

These substantial investments by Ibiden and Unimicron are critical for long-term improvements in ABF substrate supply capacity, which underpins the burgeoning demand for AI chips. This production ramp-up, coupled with new T-glass production capacity expected to come online from 2027 onwards, should gradually alleviate the ABF substrate shortage and contribute to the stable supply of AI chips.

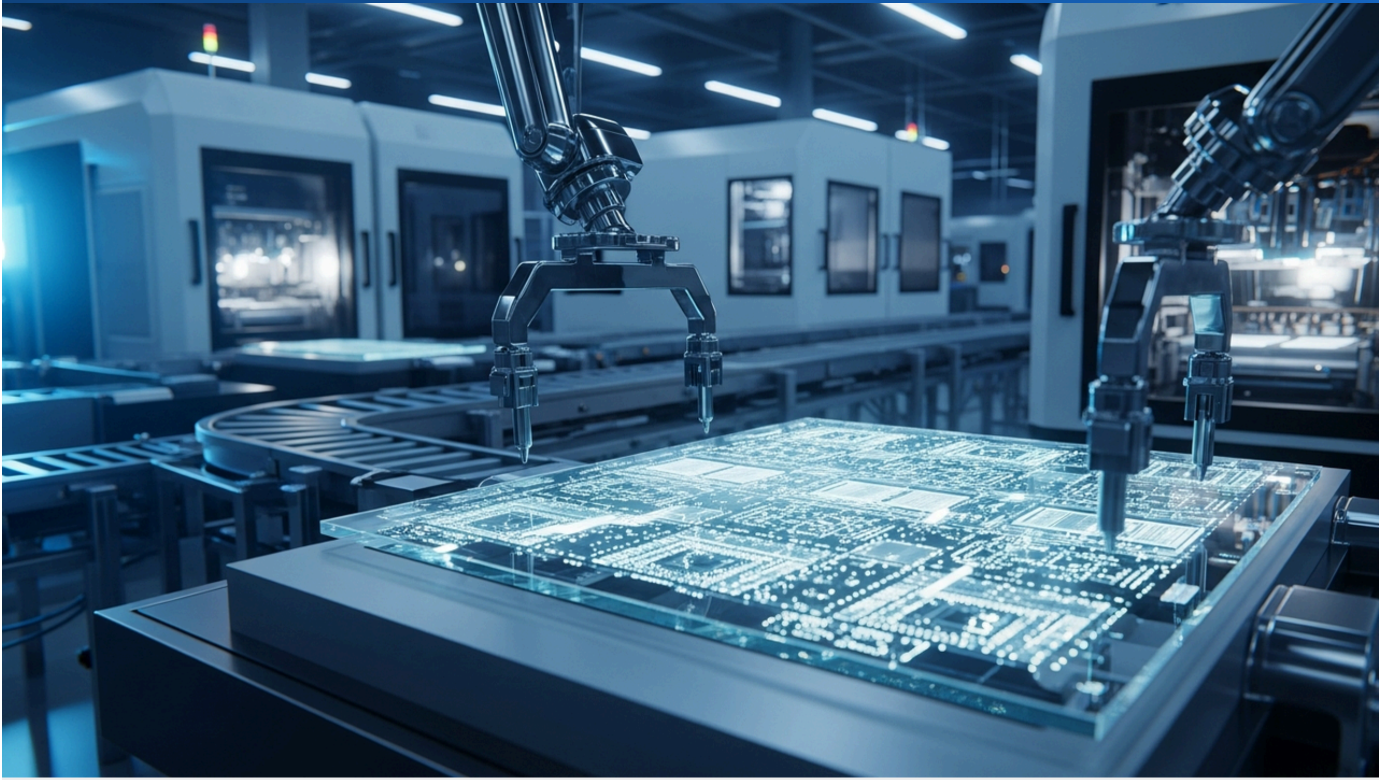
However, as long as demand continues to outpace supply growth, ABF substrates are likely to remain a critical path for AI infrastructure development. These strategic investments are expected to accelerate advancements in semiconductor packaging technology, strengthening the foundation for the design and mass production of next-generation AI chips, and are drawing significant attention across the industry.

Source: https://nextfinancial.substack.com/p/nvidias-single-point-of-failure-is

Collected: June 12, 2026 | Automated Research System (Gemini API)

Glass Substrates: The Next Frontier in AI Packaging and the Race to Mass Production

Published Published June 11, 2026 The Economy South Korea



OVERVIEW

Glass substrates are rapidly emerging as a transformative technology in advanced AI chip packaging, poised to replace conventional organic substrates and silicon interposers by offering superior dimensional stability, thermal characteristics, and ultra-fine wiring for higher-density integration. A global race to mass production is underway, with industry giants like Intel investing over $1 billion and revealing initial samples, while TSMC, Samsung, Rapidus, and SK Absolics target commercialization and high-volume manufacturing within the next few years.

IN DEPTH

The Next Frontier in AI Packaging: Glass Substrates

In advanced packaging technologies designed to push the limits of AI chip performance, glass substrates are emerging as the next-generation key material, accelerating an international development race towards their mass production. Glass overcomes the limitations of conventional organic substrates and silicon interposers, enabling higher-density and higher-performance chip integration, thus becoming an indispensable element for the evolution of AI and High Performance Computing (HPC) applications.

Unlocking Performance: Technical Advantages of Glass

Glass substrates surpass traditional materials in several critical aspects. Firstly, their **exceptional dimensional stability** enables extremely fine wiring pitches (sub-micron level) and high-density interconnections. This is essential for precisely integrating numerous chiplets and High Bandwidth Memory (HBM) within a single package. Secondly, an **excellent Coefficient of Thermal Expansion (CTE)** reduces thermal mismatch with the chips, thereby improving overall package reliability and thermal management performance. Furthermore, glass offers **superior high-frequency characteristics**, ensuring signal integrity crucial for the high-speed data transmission required by AI chips.

Global Race to Mass Production: Key Players and Investments

Intel has already invested over $1 billion in glass substrate research and development, unveiling its first samples combining Embedded Multi-die Interconnect Bridge (EMIB) packaging with glass core substrates at NEPCON Japan in January 2026. TSMC is also developing its CoPoS (Chip-on-Substrate-on-Package) technology, which utilizes glass core substrates and interposers, aiming for mass production in 2028-2029. Samsung is similarly advancing glass substrate technology as part of its vertical integration strategy, while SK Absolics, supported by the U.S. CHIPS Act, is constructing a dedicated factory in Georgia, targeting the start of glass substrate mass production by 2026. Chinese firms are also entering the fray; Visionox is leveraging its expertise in ultra-thin glass (UTG) and display panel manufacturing know-how to apply it to semiconductor-grade glass substrates. PCB manufacturer AKM Meadville established a pilot production line for glass substrates in January 2026 and has begun process verification.

Industry Context and Overcoming Current Limitations

As AI chip designs grow increasingly complex, with chiplet architectures and 3D/2.5D integration becoming mainstream, the importance of packaging has escalated dramatically. Conventional organic substrates have faced limitations in miniaturization, warpage, and thermal management. While silicon interposers offer high performance, they are constrained by cost and size. Glass substrates are positioned as an 'intermediate solution' between these two, considered essential for enhancing the performance of next-generation HBM stacks, AI accelerators, and Co-Packaged Optics (CPO). Shortages of specific glass materials, such as low-CTE T-glass cloth, are exacerbating existing bottlenecks in the ABF (Ajinomoto Build-up Film) substrate market, making the securing of in-house production capabilities and supply chains for glass substrates an urgent priority for companies.

Outlook: Redefining Semiconductor Manufacturing

The global competition toward mass production of glass substrates will redefine the future of semiconductor packaging technology. As this technology matures, it promises significant improvements in AI chip performance, power efficiency, and cost-effectiveness, accelerating the realization of next-generation AI-driven devices and data centers. The substantial investments by leading semiconductor companies and specialized material manufacturers clearly indicate that glass substrates are not merely a research-phase technology but are poised to become mainstream in semiconductor manufacturing within a few years. This is expected to usher the semiconductor industry into a new phase of growth, strengthening the foundation for further innovation in AI technology.

Source: https://economy.ac/news/2026/06/202606289308

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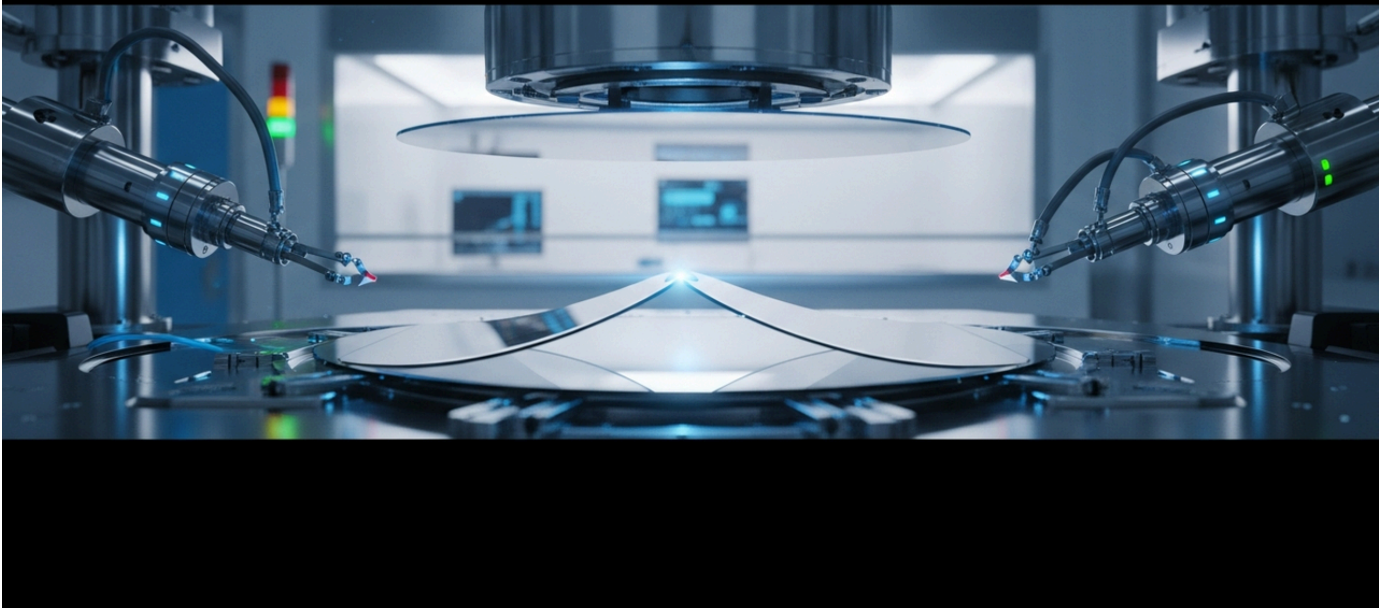
Sub-10nm Residual Distortion Achieved in Low-Distortion Fusion Bonding with Pneumatically Curved Wafers for Advanced Semiconductors

Published Published June 04, 2026 arXiv USA



OVERVIEW

A recent arXiv publication reports the development of a novel low-distortion fusion bonding technique that employs pneumatically curved wafers to achieve an exceptionally low residual grid distortion of less than 10 nanometers. This innovation is specifically engineered for next-generation Backside Power Delivery Networks (BSPDN), effectively mitigating shape deformation and localized stress that could compromise subsequent lithography processes. The research is slated for inclusion in the IEEE ECTC 2026 proceedings.

IN DEPTH

Background

Semiconductor technology is confronting the physical limits of Moore's Law, shifting focus from traditional miniaturization strategies to advanced packaging techniques like 3D stacking and heterogeneous integration. Fusion bonding is a foundational technology for directly connecting different wafers or dies in the formation of chiplets and 3D ICs, with its precision directly correlating to final product performance and yield. Particularly in innovative architectures such as Backside Power Delivery Networks (BSPDN), ultra-high-precision bonding is required between the device layer and the power delivery layer. Conventional bonding techniques face challenges where minor distortions introduced during bonding can compromise the exposure accuracy in subsequent lithography, leading to reduced yield and increased manufacturing costs. The current research provides an effective solution to these challenges, accelerating the mass production of next-generation semiconductors.

Key Findings

In recent research, an innovative method has been developed to significantly suppress distortion during the fusion bonding process by precisely curving wafers pneumatically. This technique achieves an exceptionally low residual grid distortion of less than 10 nanometers in bonded wafers, holding the potential to dramatically improve the precision and yield of next-generation semiconductor manufacturing processes.

Technical Details

This novel fusion bonding approach precisely imparts curvature to wafers within a pneumatic chamber *before* direct bonding, effectively distributing and mitigating stress concentrations during the joining process. Traditional fusion bonding often leads to shape deformation and localized stress due to subtle wafer misalignments and thermal history, which can cause alignment errors and circuit defects in subsequent lithography steps. By contrast, this pneumatic curving technique achieves uniform bonding across the entire wafer, resulting in low distortion that does not adversely affect downstream processes. A residual grid distortion of less than 10 nanometers signifies near-atomic layer precision, a critical achievement for advanced structures like Backside Power Delivery Networks (BSPDN) which incorporate high-density wiring layers on the wafer's backside.

BSPDN is gaining significant attention as a technology that drastically improves the power efficiency and performance of high-performance computing (HPC) and AI accelerators by enhancing power delivery efficiency and reducing signal noise in semiconductor chips. For BSPDN, where fine power delivery layers are formed on the wafer's backside, even slight distortion in the bonding layer can severely degrade the accuracy of subsequent lithography (patterning), directly impacting yield. The results of this study represent a groundbreaking advance in ensuring the reliability and scalability of fusion bonding for ultra-precise manufacturing processes such as BSPDN. This research is scheduled to appear in the proceedings of the IEEE ECTC 2026 (Electronic Components and Technology Conference), where it is anticipated to draw considerable interest from the semiconductor packaging community.

Implications & Outlook

This low-distortion fusion bonding technology is poised to significantly advance the practical implementation of Backside Power Delivery Networks (BSPDN), playing a crucial role in enhancing the power efficiency and performance of AI and HPC chips. Sub-10nm distortion control will enable the sustained accuracy of lithography in future, even finer nodes and multi-layered 3D IC structures, thereby increasing the robustness of manufacturing processes. Widespread adoption of this technology within the semiconductor industry is expected to contribute to improved yields and cost reduction in advanced packaging, accelerating the proliferation of high-performance semiconductors. Furthermore, this achievement will foster the continued development of precise stress management techniques in wafer-level manufacturing, strengthening the foundation for next-generation semiconductor fabrication as a whole.

Source: https://arxiv.org/abs/2606.04625

Advanced Packaging's Evolution: 2.5D/3D Integration, Chiplets, and Hybrid Bonding Propel AI and HPC

Published Published June 12, 2026 Springer Professional Germany

OVERVIEW

Semiconductor packaging technology has dramatically evolved from 2D to 2.5D and 3D IC integration, a transformation accelerated by the explosive demand from AI and High-Performance Computing (HPC). Innovations such as TSMC's CoWoS, FOWLP, and chiplet designs, alongside the rapid adoption of HBM and hybrid bonding, are elevating packaging into a critical system-level engineering discipline that tackles performance, power, and cost challenges.

IN DEPTH

Background and Industry Context

The semiconductor industry is confronting the physical limits of Moore's Law, making performance improvements solely through miniaturization increasingly challenging. In response, advanced packaging has emerged as a new frontier for enhancing chip performance. The explosive demand from AI and HPC, requiring faster data processing, higher bandwidth, and superior power efficiency, has spurred radical innovation in packaging technology. Packaging is no longer merely a backend process; it is now recognized as a core engineering discipline that determines system-level design and performance. However, this evolution also brings new challenges related to manufacturing scalability, process stability, high-density interconnections, and ultimately, product reliability.

Key Developments

Semiconductor packaging has evolved from a simple protective function to a strategic technology dictating performance, power efficiency, and cost. Beginning with 2D integration, 2.5D and 3D IC integration are now mainstream, driving the explosive growth of AI and High-Performance Computing (HPC) applications. Innovative technologies such as TSMC's CoWoS, CoPoS, and Fan-Out Wafer Level Packaging (FOWLP), along with chiplet designs, are central to this evolution.

Technological Deep Dive

The evolution of advanced packaging encompasses diverse approaches:

- **2.5D Integration**: The most prominent example is TSMC's CoWoS (Chip-on-Wafer-on-Substrate). This technique horizontally places multiple dies (e.g., logic, HBM) on a silicon interposer, enabling high-density connectivity. Adopted in products by AMD, NVIDIA, and Apple, it delivers significant improvements in data bandwidth and power efficiency. Various CoWoS-S, CoWoS-R, and CoWoS-L variants exist, optimized for specific application requirements.

- **3D IC Integration**: Exemplified by TSMC's SoIC (System-on-Integrated-Chips) and Intel's Foveros, this method vertically stacks multiple dies, allowing for ultra-high-density integration with shorter connection paths. This is achieved through Through-Silicon Via (TSV) technology and, increasingly, microbump-less copper-to-copper hybrid bonding. Hybrid bonding is key to miniaturizing connection pitches between devices to below 10 micrometers, maximizing performance and power efficiency.
- **Chiplet Design**: This approach constructs systems by combining smaller "chiplets," which are functional blocks derived from a monolithic large chip. It enhances design flexibility, allows for the integration of chips from different process nodes, thereby improving cost efficiency and scalability. Intel's Embedded Multi-die Interconnect Bridge (EMIB) is also part of this trend.
- **High Bandwidth Memory (HBM)**: Essential for AI accelerators, HBM provides data bandwidth far exceeding conventional DRAM by vertically stacking multiple DRAM dies. Development of custom HBM (cHBM) is also progressing, offering memory solutions optimized for specific applications.
- **Glass-Core Packaging**: As an emerging technology, glass substrates are gaining attention as next-generation interposer and substrate materials. Glass offers excellent dimensional stability, a low coefficient of thermal expansion, and superior high-frequency characteristics, leading to improved thermal management and signal integrity, opening possibilities for finer wiring and higher-density integration.

Future Outlook

The continuous evolution of advanced packaging technology forms the foundation for the development of all next-generation technologies, including AI, 5G, autonomous driving, and cloud computing. Hybrid bonding and glass-core packaging, in particular, are expected to play crucial roles in future device integration. The industry is poised to overcome manufacturing challenges in these technologies and drive mass production, further enhancing semiconductor chip performance and cost efficiency. Furthermore, advancements in heterogeneous integration techniques will facilitate the development of custom chips with more diverse functionalities, accelerating the provision of solutions optimized for specific applications. Packaging technology is predicted to remain at the forefront of semiconductor innovation.

Source: https://www.springerprofessional.de/en/advanced-packaging/52495696

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Intel and Tesla Partner on AI6 Data Centers, Tapping Advanced Packaging for Production at Austin's 'Terafab'

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OVERVIEW

Tesla has announced a strategic partnership with Intel Foundry Services to scale its AI6 chip-powered data center clusters, extensively utilizing Intel's advanced packaging technologies. The collaboration will deploy Intel's EMIB for proximate High Bandwidth Memory (HBM) integration with AI6 compute dies and Foveros for 3D stacking of multiple AI6 components into dense package nodes. This chiplet-based approach aims to create self-contained, high-density AI processing units, with production slated for Intel's 'Terafab' project in Austin, Texas.

IN DEPTH

Background & Industry Context

The evolution of AI has dramatically escalated the demand for computational and data processing capabilities, rendering conventional monolithic chip designs increasingly insufficient. Consequently, chiplet architectures and advanced packaging technologies are emerging as critical enablers for enhancing performance and cost-efficiency in next-generation AI accelerators. While leaders in the AI semiconductor market, such as NVIDIA, integrate HBM and GPUs at high densities using technologies like TSMC's CoWoS, the supply capacity of advanced packaging has become a significant bottleneck in AI infrastructure development.

Intel has invested extensively in packaging technologies over many years, developing proprietary solutions like EMIB and Foveros. This partnership with Tesla marks a crucial milestone for Intel Foundry Services (IFS) as it fully commits to offering these cutting-edge technologies to external clients. Tesla, which extensively deploys its self-developed AI chips in autonomous driving, robotics, and other AI applications, views this collaboration with Intel as a strategic move to further bolster its AI infrastructure.

Key Findings

Tesla has announced plans to scale its AI6 chip-powered data center clusters through a strategic partnership with Intel Foundry Services (IFS). This collaboration will leverage Intel's advanced packaging technologies, including EMIB (Embedded Multi-die Interconnect Bridge) and Foveros, to achieve optimal placement of High Bandwidth Memory (HBM) modules and 3D stacking of AI6 components. The goal is to construct high-density, high-performance AI processing units. This innovative chiplet strategy is slated for realization at the 'Terafab' project in Austin, Texas.

Technical Details

At the core of this partnership are Intel's advanced packaging technologies. The AI6 chip, designed for high-performance AI workloads, critically relies on maximizing data bandwidth and power efficiency. Intel's EMIB technology enables the connection of multiple dies—such as the AI6 compute die and HBM modules—at extremely close proximity within the same package. This significantly reduces signal latency and boosts data transfer speeds compared to conventional packaging techniques. By positioning HBM modules close to the AI6 compute die, the AI6 can efficiently leverage the necessary memory bandwidth, thereby enhancing its processing capabilities for data-intensive tasks.

Furthermore, Intel's Foveros technology facilitates the vertical 3D stacking of multiple AI6 components. This enables exceptionally high integration density and functionality within a single package node. Foveros allows for direct micro-bump connections between dies, leading to shorter interconnect paths and lower power consumption. This chiplet-based approach allows Tesla to combine multiple instances of the AI6 chip with HBM and other components to construct modular and scalable AI computing units. Production is planned for Intel's 'Terafab,' a large-scale manufacturing site Intel is developing in Austin, Texas, as part of its broader initiative to strengthen its foundry business and expand semiconductor manufacturing capacity within the United States.

Future Outlook

The partnership between Intel and Tesla is poised to further underscore the importance of advanced packaging in AI chip design and manufacturing. This collaboration will not only maximize the performance and efficiency of the AI6 chips but also expand Intel Foundry Services' customer base and accelerate the growth of Intel's foundry business. Production at Austin's 'Terafab' holds strategic significance for strengthening semiconductor manufacturing capabilities within the United States. This chiplet strategy, leveraging advanced packaging technologies, is expected to optimize power consumption and footprint in AI data centers, contributing to the broader adoption and advancement of AI technologies. In the future, such heterogeneous integration and 3D stacking hold the potential to become the standard for AI hardware design.

Source: https://torovictorioso.substack.com/p/the-formula-1-engine-of-ai

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Apple's M5 Ultra Pioneers Integration with TSMC's N3P Process and SoIC-mH Packaging

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OVERVIEW

Reports indicate Apple's upcoming M5 Ultra chip, expected at WWDC, will likely leverage TSMC's N3P process node and its advanced SoIC-mH (System-on-Integrated-Chips – molded horizontal packaging) technology. SoIC-mH combines a molded horizontal architecture with bump-less hybrid bonding, enabling high-density heterogeneous integration of multiple chips at the wafer level. This innovative packaging is poised to dramatically enhance the chip's packaging density, signal transmission efficiency, and thermal performance.

IN DEPTH

Key Findings

Apple's next-generation M5 Ultra chip is reportedly set to achieve unprecedented performance and efficiency by combining TSMC's N3P process technology with the innovative advanced packaging technique, SoIC-mH (System-on-Integrated-Chips – molded horizontal packaging). This technological integration, expected to debut in Mac Studio products unveiled at WWDC, will establish a new benchmark for high-density heterogeneous integration.

Technical Deep Dive

The adoption of TSMC's N3P process (an enhanced version of the 3nm process) for the M5 Ultra chip will bring further advancements in transistor density and power efficiency. N3P offers higher performance and superior yield characteristics compared to N3E, making it an ideal choice for large-scale, high-performance chips. However, the true innovation of the M5 Ultra lies in its packaging technology.

SoIC-mH is a variation of TSMC's advanced 3D stacking technology, SoIC, specifically optimized for high-density heterogeneous integration. Key features of SoIC-mH include:

- **Molded Horizontal Packaging Architecture**: Multiple chips are arranged horizontally and then encapsulated entirely within a molding material, optimizing both robustness and thermal management.
- **Bump-less Hybrid Bonding**: This technique directly bonds chips using copper-to-copper connections at the wafer level, bypassing conventional micro-bumps. This enables connection pitches finer than 10μm, drastically shortening signal transmission paths, and consequently achieving significant reductions in signal delay and improvements in power efficiency.
- **High-Density Integration**: Seamlessly integrates multiple logic dies and other functional chiplets at the wafer level, delivering levels of integration and functionality previously unattainable with conventional packaging.

These technological advancements will enable the M5 Ultra to accommodate more cores and eliminate inter-chip communication bottlenecks, leading to dramatic performance improvements in graphics processing, AI/ML workloads, and High-Performance Computing (HPC) tasks. This will significantly elevate the processing power of professional workstations like the Mac Studio.

Background and Industry Context

Since introducing its custom-designed M-series chips into Mac products, Apple has led the industry in performance and power efficiency. Chiplet architectures and advanced packaging have emerged as primary means to enhance chip performance, especially as Moore's Law confronts its physical limits. TSMC's SoIC is one of the industry's most advanced packaging technologies, notably adopted in NVIDIA's AI accelerators. Apple's embrace of SoIC-mH for the M5 Ultra underscores its aggressive investment not only in chip manufacturing but also in packaging technology to extract peak performance. This move suggests a further convergence of chip design and packaging across the broader semiconductor industry.

Future Outlook

The adoption of TSMC's N3P process and SoIC-mH in the Apple M5 Ultra will undoubtedly set new benchmarks for professional workstation performance. This high-density packaging technology is anticipated to extend to more Apple products in the future, particularly devices requiring significant AI and HPC capabilities. The M5 Ultra's debut will not only bolster the competitiveness of Apple's Mac products in the high-end market but also serve as a crucial example of how advanced packaging technologies like SoIC-mH will shape the future of heterogeneous integration and chiplet design. This is expected to pave the way for further innovation and performance enhancements across the semiconductor industry.

Source: https://www.trendforce.com/news/2026/06/08/news-apple-may-debut-m5-ultra-powered-mac-studio-at-wwdc-boosting-demand-for-tsmc-n3p-and-soic-mh/

TSMC's COUPE Platform for Co-Packaged Optics Targets 2026 Mass Production, Integrating Micro LEDs for AI Cluster Performance Boost

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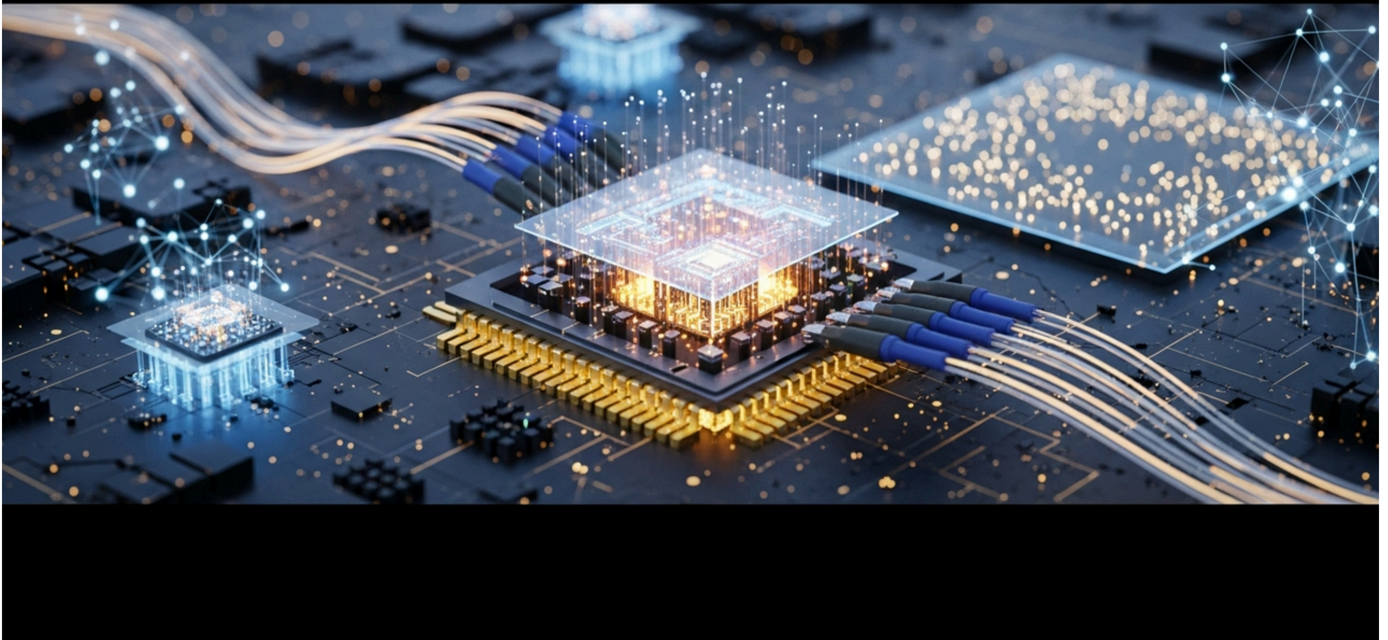

OVERVIEW

TSMC has announced the 2026 mass production launch of "COUPE" (Compact Universal Photonic Engine), an innovative platform for co-packaged optics (CPO) interconnects. Utilizing SoIC bonding to stack photonic and electronic ICs, COUPE aims for a tenfold reduction in latency and significant power efficiency improvements over traditional optical modules. Notably, Micro LED co-packaged optics for NVIDIA's AI clusters are set for commercial debut via TSMC's COUPE process, promising to revolutionize AI data center connectivity despite initial yield challenges.

IN DEPTH

Background

The rapid proliferation of Artificial Intelligence (AI), High-Performance Computing (HPC), and data centers has dramatically escalated the demand for faster and more efficient data transmission across chips, boards, and racks. Traditional copper interconnects are reaching their limits in addressing these demands due to inherent signal attenuation, escalating power consumption, and physical space constraints. Co-packaged optics (CPO) has emerged as an innovative and crucial solution to break this "electrical bottleneck." Major semiconductor industry players, including TSMC, Intel, and Broadcom, are investing significant resources into the development and deployment of CPO technology, anticipating it will form the foundational infrastructure for next-generation data centers.

Key Findings

TSMC has announced the mass production launch of its groundbreaking "COUPE" (Compact Universal Photonic Engine) platform in 2026. This platform is specifically designed for co-packaged optics (CPO), a pivotal next-generation high-speed interconnect technology critical for AI data centers. The COUPE platform leverages TSMC's advanced System-on-Integrated-Chips (SoIC) bonding technology to directly stack photonic ICs and electronic ICs. This approach is engineered to achieve a tenfold reduction in latency and substantial improvements in power efficiency compared to conventional pluggable optical modules. Crucially, CPO solutions integrated with Micro LED technology, specifically developed for NVIDIA's AI clusters, are expected to make their commercial debut through TSMC's COUPE process.

Technical Details

The COUPE platform is built upon TSMC's sophisticated 3D stacking technology, SoIC. SoIC bonding facilitates the direct, high-density stacking of photonic chips (responsible for the generation, modulation, and detection of optical signals) and electronic chips (responsible for processing electrical signals) at the chip level. This integration drastically shortens the physical distance electrical signals must travel before being converted to optical signals and back, yielding several key advantages:

- **Ultra-Low Latency**: By minimizing the physical separation between the chip and the optical module, signal transmission delay is reduced to less than one-tenth of that experienced with conventional methods. This is paramount for AI clusters where thousands of GPUs must operate in tight synchronization for efficient AI/ML model training and inference.
- **Significant Power Efficiency Improvement**: Eliminating the need for signals to traverse lengthy electrical traces substantially reduces the power consumption associated with high-volume data transfer. This directly contributes to lower operational costs and enhanced sustainability for AI data centers.
- **High Bandwidth**: The high-density optical connections enabled by COUPE facilitate ultra-high bandwidths, reaching terabits per second (Tbps) levels, which are exceedingly challenging to achieve with traditional electrical interconnects.

A distinctive feature of the COUPE process is the planned integration of Micro LED technology into its co-packaged optics. Micro LEDs offer compelling advantages over conventional light sources such as VCSELs (Vertical Cavity Surface Emitting Lasers), including superior high-speed modulation capabilities, enhanced miniaturization, higher efficiency, and extended lifespan. These attributes are expected to further elevate CPO performance. The anticipated adoption of this technology by leading AI chip vendors like NVIDIA for their next-generation AI clusters will likely accelerate industry-wide CPO deployment.

Challenges and Outlook

Despite the immense promise, initial CPO technology faces significant manufacturing yield challenges. Industry analyses indicate that TSMC's SoIC manufacturing yield for CPO is currently estimated at approximately 50-60%, with downstream assembly processes showing yields as low as 20-50%. These figures pose a challenge to the short-term supply volume of CPO. However, market projections from firms like Morgan Stanley anticipate explosive growth in the CPO market post-2028, suggesting that these initial yield issues are expected to be resolved as the technology matures and manufacturing processes are optimized.

The 2026 mass production launch of TSMC's COUPE platform with Micro LED co-packaged optics represents a pivotal moment, poised to dramatically enhance the performance and efficiency of AI data centers. While initial yield hurdles exist, CPO technology is strategically positioned to resolve long-term bottlenecks in AI accelerators, thereby enabling the realization of even larger and more powerful AI clusters. The widespread adoption of this electro-photonic integration technology is expected to accommodate the increasing complexity of AI models and data volumes, accelerating the development of AI applications across diverse fields such as autonomous driving, medical diagnostics, and advanced scientific research. As a leader in the foundry space, TSMC is set to continue driving innovation across the semiconductor industry through this critical technological advancement.

Source: https://world.storm.mg/articles/1138532

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