

Semiconductor_BackEnd

Weekly Intelligence Report

2026-06-27 | 30 articles | 9 countries
troy-technical.jp

This Week's Keyword

Advanced Packaging AI

CoWoS capacity eases, HBM4E, new materials

30

articles

Total Articles Analyzed

9

countries

Source Countries

120K-140K

wafers/month

TSMC CoWoS Capacity EOY26

\$8.5B

USD

ASE 2026 Capex

All 30 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	Applied Materials New Systems	New Product	●●●○ ○	●●●● ●	●●●● ●	●●●● ○	●●●● ●	Applied Materials launches new CMP, deposition, and eBeam systems to accelerate 3D chip architectures for AI.
#02	TSMC CoWoS/CoPoS Boost	Corporate Strategy	●●●● ○	●●●● ○	●●●● ●	●●●○ ○	●●●● ○	TSMC expands CoWoS capacity to ease AI chip shortage; CoPoS pilot for NVIDIA 'Feynman' in 2027.
#03	ASE Raises 2026 Capex	Corporate Strategy	●●●○ ○	●●●● ●	●●●● ●	●●●● ○	●●●● ○	ASE raises 2026 Capex to \$8.5B for 15 advanced packaging expansion projects in Taiwan/Malaysia.
#04	Morgan Stanley TSMC AI	Market Analysis	●○○○ ○	●●●● ●	●●●● ●	●●●● ●	●●●● ○	Morgan Stanley forecasts TSMC AI revenue to \$86.3B by 2027, but CoWoS capacity remains a bottleneck.
#05	Malaysia R&D; Investment	Corporate Strategy	●●●○ ○	●●●○ ○	●●●○ ○	●●○○ ○	●●●○ ○	Malaysia invests \$40M in advanced semiconductor R&D; targeting 7% global packaging share with HBM4 test chips.
#06	ATLANT 3D Materials Hub	Research	●●●● ●	●●○○ ○	●●●○ ○	●●○○ ○	●●●● ●	ATLANT 3D, A*STAR, NAMIC launch AI-driven materials hub in Singapore for semiconductors and packaging.
#07	Samsung Hybrid Cu Bonding	Research	●●●● ●	●●●○ ○	●●●○ ○	●●●● ●	●●●● ○	Samsung's Hybrid Copper Bonding shows superior thermal management for HBM4E, reducing hotspot temps and stack thickness.
#08	TSMC CoWoS Bottleneck	Market Analysis	●○○○ ○	●●●● ●	●●●● ●	●●●○ ○	●●●● ○	TSMC's CoWoS capacity remains the bottleneck for HBM4E, despite Korean memory makers shipping samples.
#09	Samsung/SK Hynix HBM	Corporate Strategy	●●○○ ○	●●●● ●	●●●● ●	●●●● ○	●●●● ○	Samsung and SK Hynix announce major HBM capacity expansions, with Samsung allocating half to HBM4.
#10	TSMC CoPoS Glass Substrate	Research	●●●● ○	●●●○ ○	●●●● ○	●●●○ ○	●●●● ○	TSMC accelerates CoPoS with glass core substrates, targeting 30% cost reduction and >90% wafer utilization post-2028.
#11	Resonac HF Gas Production	Corporate Strategy	●●○○ ○	●●●● ●	●●●○ ○	●●●● ○	●●●○ ○	Resonac to start high-purity HF gas production at Tokuyama plant by 2026, strengthening Japan's supply.
#12	Imec Photonics PhD	Research	●●●○ ○	●○○○ ○	●○○○ ○	●○○○ ○	●●●● ●	Imec seeks PhD for microfluidics and photonics packaging research to enhance optical interconnects for AI/HPC.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#13	Imec FeFET for AI	Research	●●●●● ●	●●○○○ ○	●●●○○ ○	●●○○○ ○	●●●●● ●	Imec demonstrates vertically stacked IGZO-based FeFET for AI, improving density and energy efficiency.
#14	Morgan Stanley CoWoS	Market Analysis	●○○○○ ○	●●●●● ●	●●●●● ●	●●●●● ●	●●●●● ○	Morgan Stanley raises CoWoS demand forecast to 2.69M wafers by 2027, driven by CPUs and ASICs.
#15	Imec Chiplet Analysis	Analysis	●○○○○ ○	●○○○○ ○	●●●●● ○	●●●●● ○	●●●●● ●	Imec analyzes the shift to chiplet-based designs for AI/HPC, driven by reticle limits and advanced packaging.
#16	ASML/TSMC/Imec 2D Mat	Research	●●●●● ●	●●○○○ ○	●●○○○ ○	●●●●● ●	●●●●● ●	ASML, TSMC, Imec achieve 300mm integration for 2D-material transistors, bringing industry-ready devices closer.
#17	Hanmi SK hynix TC Bonder	Corporate Strategy	●●○○○ ○	●●●●● ●	●●●●● ○	●●●●● ○	●●●●● ○	Hanmi Semiconductor secures ₩44.2B SK hynix order for HBM4 TC Bonders, signaling strong equipment market.
#18	Startup Funding Diversifies	Market Analysis	●○○○○ ○	●●●●● ●	●●●●● ●	●●●○○ ○	●●●●● ○	Semiconductor startup funding diversifies to interconnects/packaging; TSMC CoWoS capacity to quadruple by EOY 2026.
#19	ASE LEAP Revenue Target	Corporate Strategy	●●○○○ ○	●●●●● ●	●●●●● ●	●●●●● ○	●●●●● ○	ASE expands advanced packaging capacity with 15 new sites, raising 2026 LEAP revenue target to \$3.5B+.
#20	Singapore Exports Soar	Market Overview	●○○○○ ○	●●●●● ●	●○○○○ ○	●●●○○ ○	●●○○○ ○	Singapore's exports hit 22-year high in May 2026, driven by Micron HBM packaging and UMC 22nm production.
#21	SK hynix HBM4E Samples	New Product	●●●●● ○	●●●●● ○	●●●●● ●	●●●●● ○	●●●●● ○	SK hynix ships 12-layer HBM4E samples with Advanced MR-MUF, achieving >20% power efficiency, 17% thermal improvement.
#22	TSMC/Amkor US Alliance	Corporate Strategy	●●○○○ ○	●●●●● ●	●●●●● ●	●●●○○ ○	●●●●● ●	TSMC and Amkor partner for 10 years to expand advanced packaging, including CoWoS, in the US.
#23	OSAT Q1 2026 Growth	Market Overview	●○○○○ ○	●●●●● ●	●●●●● ●	●●●●● ●	●●●●● ○	OSAT vendors (ASE +18%, Amkor +25%) report strong Q1 2026 revenue growth from AI advanced packaging demand.
#24	BESI Raises Targets	Corporate Strategy	●●○○○ ○	●●●●● ●	●●●●● ●	●●●●● ○	●●●●● ●	BESI raises long-term revenue target to €2.2B and margin to 45% due to surging hybrid bonding demand.
#25	TSMC CoWoS Eases NVIDIA	Market Analysis	●○○○○ ○	●●●●● ●	●●●●● ●	●●●○○ ○	●●●●● ○	TSMC's CoWoS capacity expansion eliminates NVIDIA B300 server supply constraint, cutting lead times to 8-16 weeks.
#26	Analog Tech Defense Pack	New Product	●●○○○ ○	●●●●● ●	●●○○○ ○	●●○○○ ○	●●●●● ●	Analog Technologies offers specialized advanced packaging for defense systems, focusing on thermal management and miniaturization.
#27	Applied Materials New Systems	New Product	●●●○○ ○	●●●●● ●	●●●●● ●	●●●●● ○	●●●●● ●	Applied Materials unveils new epitaxy, CMP, and e-beam inspection systems to accelerate AI chip manufacturing.
#28	ATLANT 3D Materials Hub	Research	●●●●● ●	●●○○○ ○	●●●○○ ○	●●○○○ ○	●●●●● ●	ATLANT 3D, A*STAR, NAMIC establish AI-driven materials discovery hub in Singapore for semiconductor innovation.
#29	HBM4E Market Dominance	Market Analysis	●●●●● ○	●●●●● ○	●●●●● ●	●●●○○ ○	●●●●● ○	HBM4E to dominate high-performance memory by late 2026-2027 with 4.0 TB/s bandwidth and 48GB+ capacity.
#30	SK hynix HBM Lead	Corporate Strategy	●○○○○ ○	●●●●● ●	●●●●● ●	●●●○○ ○	●●●●● ○	SK hynix's early HBM investment for AI/NVIDIA demand drives market value lead over Samsung.

●●●●●○ High ●●●○○○ Med-High ●●○○○○ Med ●○○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

1 Is your AI supply chain still bottlenecked by CoWoS capacity?

TSMC's CoWoS capacity is quadrupling by EOY 2026, cutting NVIDIA B300 lead times. However, demand from new drivers like CPUs and ASICs is surging. Assess your specific exposure and alternative OSAT options.

2 Are you investing in next-gen packaging materials and equipment?

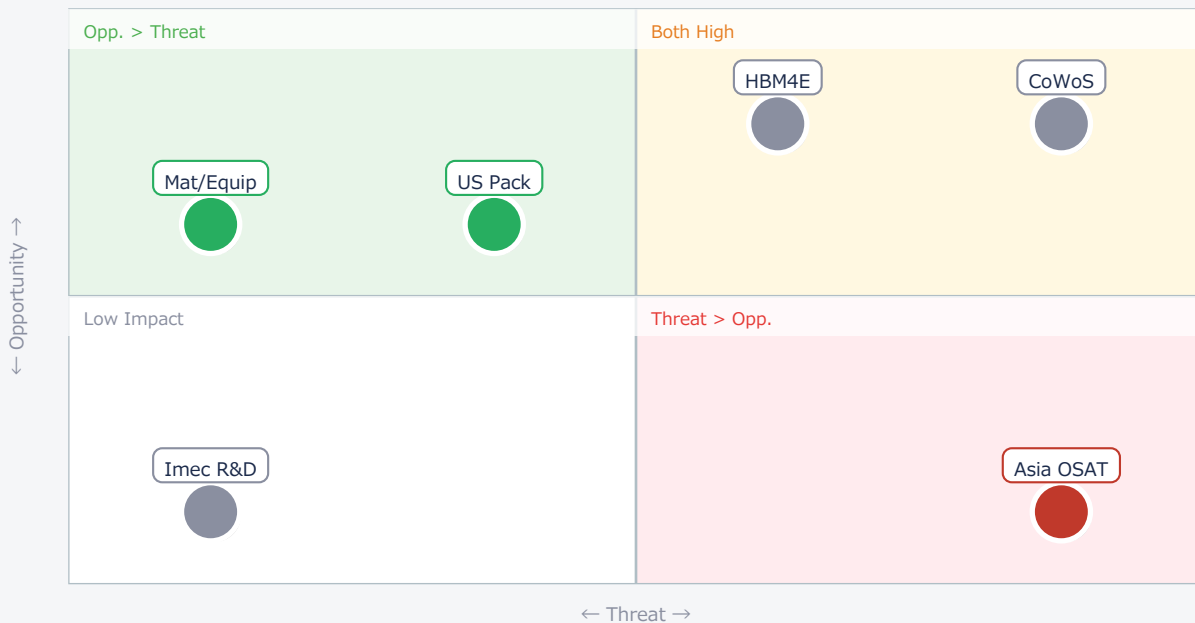
Hybrid bonding (BESI) and glass core substrates (TSMC CoPoS) are critical for future AI/HPC. Evaluate your R&D; and procurement strategies for these foundational technologies to avoid falling behind.

3 How will advanced memory (HBM4E) and novel memory (FeFET) impact your product roadmap?

HBM4E offers 4TB/s bandwidth and 48GB+ capacity by late 2026, while Imec's FeFET promises high-density, low-power AI memory. Are your designs ready for these performance leaps and new architectures?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
● CoWoS	Critical	Faster AI deployment	Supply chain reliance
● HBM4E	Critical	AI performance boost	Thermal/power limits
● Mat/Equip	Opp.	New tech adoption	Lagging R&D;
● US Pack	Opp.	Resilient supply	High cost/scale
● Asia OSAT	Threat	Diversified partners	Regional dominance
● Imec R&D;	Ref.	Future tech base	Long commercialization

Deep Dive ① — Samsung's Hybrid Copper Bonding for HBM4E

#07 | 2026/06/25 | ET News (via IEEE paper) | Tech Novelty ●●●●● Proximity ●●●●○ Market Impact ●●●●○ Data Reliability ●●●●● US/EU Relevance ●●●●○

Samsung's Hybrid Copper Bonding (HCB) significantly improves thermal management for HBM4E, outperforming traditional Thermo-Compression Bonding (TCB). HCB reduces hotspot temperatures, decreases thermal interference, and enables HBM stacks over 15% thinner.

This direct copper-to-copper connection technology is crucial for next-gen HPC systems, especially 16-high HBM stacks, providing higher power budgets and enhanced reliability. It aligns with the industry trend towards hybrid bonding for advanced packaging.

► Strategic Analyst's Perspective

Strategic Analyst's Perspective: Samsung's HCB validation, backed by IEEE data, appears highly realistic and critical for HBM4E's thermal challenges. The technical barrier remains scaling this precision bonding to high-volume manufacturing with consistent yield. [Opportunity] for US/EU materials & equipment suppliers to develop compatible HCB materials and tools. [Threat] for US/EU OEMs if they cannot access HBM4E with superior thermal performance, impacting AI accelerator designs. Next actions: [R&D;] Evaluate HCB compatibility with current and future HBM integration roadmaps by end of Q3. [Procurement] Assess potential HBM4E supplier thermal performance benchmarks by Q4.

Deep Dive ② — TSMC Accelerates CoPoS with Glass Substrates

#10 | 2026/06/20 | Wccftch / CHOSUNBIZ / BigGo Finance | Tech Novelty ●●●●○ Proximity ●●●●○ Market Impact ●●●●○ Data Reliability ●●●●○ US/EU Relevance ●●●●○

TSMC is accelerating CoPoS packaging using glass core substrates, targeting a 30% cost reduction and over 90% wafer utilization for ultra-large AI chips post-2028. This panel-level approach addresses geometric waste and warpage issues of organic substrates.

Glass substrates offer superior co-planarity, lower thermal expansion, and enhanced power integrity, crucial for integrating more chips with higher reliability. Pilot production is slated for 2027, with NVIDIA's 'Feynman' platform as an early adopter.

► Strategic Analyst's Perspective

Strategic Analyst's Perspective: The projected 30% cost reduction and >90% wafer utilization for CoPoS with glass substrates are ambitious but plausible given TSMC's track record and industry partners (Ibiden, Innolux). Technical barriers include developing robust glass substrate manufacturing at scale and integrating new processing steps into existing lines. [Opportunity] for US/EU materials suppliers (e.g., glass, ABF) and equipment manufacturers to co-develop solutions. [Threat] for US/EU foundries and OSATs if they lag in adopting or developing competitive panel-level packaging. Next actions: [R&D;] Initiate feasibility studies on glass core substrates for advanced packaging by Q4. [Strategy] Formulate a long-term roadmap for panel-level packaging, including potential partnerships, within 6 months.

Deep Dive ③ — TSMC CoWoS Capacity Eases NVIDIA B300 Bottleneck

#25 | 2026/06/24 | Contrary Research | Tech Novelty ●○○○○ Proximity ●●●●● Market Impact ●●●●● Data Reliability ●●●○○ US/EU Relevance ●●●●●

TSMC's CoWoS packaging capacity has dramatically expanded, resolving a major GPU procurement constraint for NVIDIA B300 servers. Lead times are now reduced to 8-16 weeks with a 10-20% upfront payment, accelerating AI computing deployment.

This pivotal development removes a significant impediment to AI infrastructure growth, which had persisted for over six months in 2025. The expansion is attributed to new factory construction, line optimization, and enhanced supplier collaboration.

► Strategic Analyst's Perspective

Strategic Analyst's Perspective: The reported reduction in NVIDIA B300 lead times is a critical market signal and appears realistic, reflecting TSMC's aggressive capacity build-out. While a major bottleneck is easing, the underlying demand remains immense, and new drivers like CPUs/ASICs will quickly absorb capacity. [Opportunity] for US/EU cloud providers and AI developers to accelerate their AI infrastructure build-out. [Threat] for smaller AI hardware companies if they cannot secure competitive CoWoS allocations, potentially widening the gap with larger players. Next actions: [Procurement] Re-evaluate AI hardware acquisition strategies and supplier diversification immediately. [Executive] Adjust AI investment and deployment timelines based on improved hardware availability within 1 month.

Other Notable Articles

Applied Materials Unveils New Systems to Accelerate DRAM and Advanced Packaging for AI Chips (Applied Materials, Inc.)
Tech Novelty ●●●○○ Proximity ●●●●● Market Impact ●●●●●

US-based AMAT's new systems for CMP, deposition, and eBeam inspection are vital for next-gen 3D AI chip architectures.

ASML, TSMC, and Imec Achieve Breakthrough 300mm Integration for Industry-Ready 2D-Material Transistors (The cleanroom Portal - Reinraum Online)
Tech Novelty ●●●●● Proximity ●●○○○ Market Impact ●●○○○

Major EU/US/Taiwan collaboration pushing 2D materials from lab to industrial scale for future transistor tech.

SK hynix Ships 12-Layer HBM4E Samples with Advanced MR-MUF Packaging, Achieving Over 20% Power Efficiency and 17% Thermal Resistance Improvement Over HBM4 (Advanced Packaging News)
Tech Novelty ●●●●○ Proximity ●●●●○ Market Impact ●●●●●

SK hynix's HBM4E with advanced MR-MUF sets new benchmarks for AI memory, critical for power and thermal management.

TSMC and Amkor Technology Forge 10-Year Strategic Partnership to Expand Advanced Chip Packaging Capabilities in the US (Focus Taiwan)
Tech Novelty ●●○○○ Proximity ●●●●● Market Impact ●●●●●

Significant move to bolster US domestic advanced packaging capacity, including CoWoS, for AI and HPC.

BE Semiconductor Industries (BESI) Raises Long-Term Revenue Target to €2.2 Billion and Operating Margin Target to 45% Amid Surging Hybrid Bonding Demand (Bits&Chips;)
Tech Novelty ●●○○○ Proximity ●●●●● Market Impact ●●●●●

EU-based BESI's optimistic outlook highlights hybrid bonding as a key enabler for AI, photonics, and CPO.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

■ Immediate (this week)

- [Executive] Review AI chip procurement forecasts against updated CoWoS capacity projections from TSMC and other OSATs.
- [Procurement] Engage with key OSAT partners (ASE, Amkor) to understand their capacity expansion plans and secure future allocations.

■ Short-term (1 month)

- [R&D;] Initiate internal review of hybrid bonding and glass core substrate technologies for integration into next-gen product roadmaps.
- [Strategy] Assess the competitive landscape for HBM4E, evaluating thermal management solutions like Samsung's HCB and SK hynix's MR-MUF.
- [Business Dev] Explore partnerships with advanced materials and equipment suppliers (e.g., BEI, Applied Materials) for future packaging needs.

■ Medium-long term (quarter+)

- [R&D;] Investigate the long-term potential of 2D materials and FeFET memory for fundamental shifts in chip architecture and AI system design.
- [Strategy] Develop a multi-year strategy for diversifying advanced packaging supply chains, including potential US domestic capacity and Asian OSAT partnerships.
- [Legal/IP] Monitor IP developments in advanced packaging (e.g., hybrid bonding, CoPoS) to identify licensing opportunities or potential threats.

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Semiconductor_BackEnd — Selected Articles

Date: 2026-06-27

Articles: 30

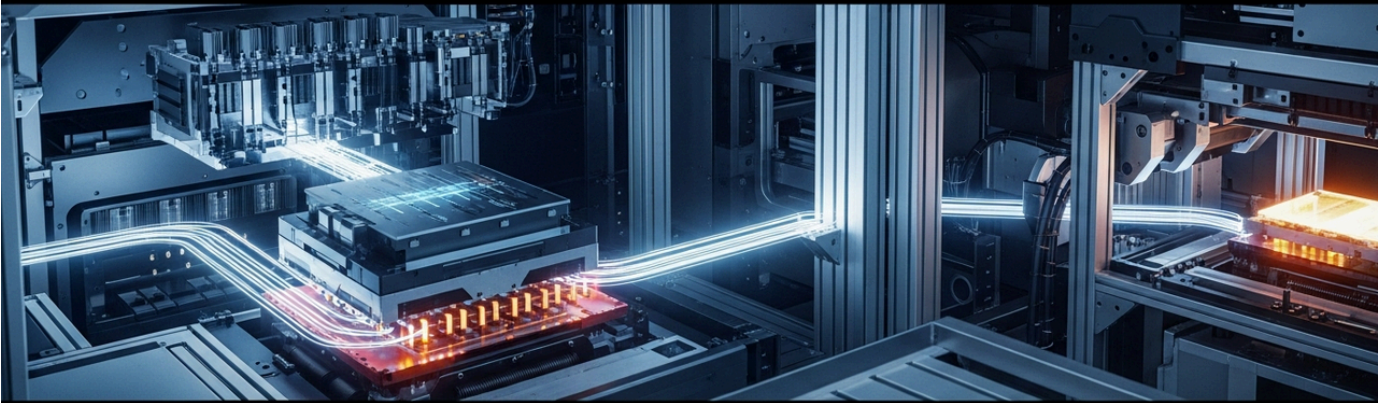
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#01 Applied Materials Unveils New Systems to Accelerate DRAM and Advanced Packaging for AI Chips

Published June 25, 2026 Applied Materials, Inc. USA



OVERVIEW

Applied Materials has introduced a suite of new material engineering systems designed to accelerate the manufacturing of advanced 3D chip architectures crucial for next-generation AI. These innovations, including advanced CMP and deposition systems for HBM and logic chip stacking, and eBeam defect review systems for advanced packaging, promise significant yield improvements and production scalability. This expansion of their materials engineering portfolio directly addresses bottlenecks in DRAM and advanced packaging, vital for the high-performance and power-efficient AI processors of the future.

Key Findings

Applied Materials has unveiled a new lineup of material engineering systems engineered to significantly accelerate the production of advanced 3D chip architectures, which are critical enablers for next-generation artificial intelligence (AI). These systems are specifically designed to enhance yield and performance in critical processes such as High Bandwidth Memory (HBM) and logic chip vertical stacking.

Technical Details

The newly introduced systems incorporate several key technologies:

- **Advanced Chemical Mechanical Planarization (CMP) Systems:** These systems are crucial for achieving ultra-flat surfaces during HBM and logic chip stacking, which dramatically improves the reliability of electrical connections between stacked layers. This precision is paramount for boosting the yield rates of complex 3D stacking processes.
- **High-Performance Deposition Systems:** Capable of forming ultra-thin and highly uniform layers, these systems optimize interconnect performance and minimize signal propagation delays. Their role is particularly vital in the Through-Silicon Via (TSV) processes essential for advanced HBM modules.
- **eBeam Defect Review Systems:** Providing high-speed and high-accuracy detection of minute defects within intricate advanced packaging structures, these systems are key to enhancing product reliability and reducing manufacturing costs in high-volume production environments.

These technological advancements offer foundational solutions for overcoming the limitations of traditional 2D scaling, enabling the practical implementation of 3D integration. As AI applications demand ever-increasing data processing capabilities and lower power consumption, the evolution of HBM and chiplet technologies becomes indispensable, and Applied Materials' new systems directly address these emerging challenges.

Background & Context

The explosive growth of AI has led to an unprecedented demand for computational power in data centers and edge devices. Consequently, advanced packaging technologies that offer high-bandwidth, low-latency memory integration and efficient multi-chip integration have become paramount for the semiconductor industry. Leveraging its extensive expertise in material engineering, Applied Materials aims to solidify its position within the AI semiconductor supply chain by meeting these evolving market requirements.

Strategic Significance & Outlook

Applied Materials anticipates that these new systems will alleviate critical bottlenecks in AI chip design and manufacturing, accelerating the market introduction of more powerful and energy-efficient AI processors. This technological breakthrough is expected to significantly bolster the overall competitiveness of the semiconductor industry in rapidly expanding sectors such as AI, High-Performance Computing (HPC), and data centers.

Source: <https://ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-introduces-new-systems-accelerate-dram-and>

#02 TSMC Boosts CoWoS Capacity, Reducing AI Chip Supply Gap to 10% by Late 2026; Next-Gen CoPoS Pilot Production for NVIDIA's 'Feynman' Slated for 2027

Published June 22, 2026 Futuretech Components / Daily Beirut Taiwan



OVERVIEW

TSMC is rapidly expanding its CoWoS advanced packaging capacity to meet surging demand from AI accelerators and HPC applications, projected to narrow the supply-demand gap from 20% to approximately 10% by the end of 2026. Concurrently, the company is advancing its next-generation CoPoS (Chip-on-Panel-on-Substrate) technology roadmap, with pilot production expected in 2027 and NVIDIA's upcoming 'Feynman' platform poised to be an early adopter. These strategic moves aim to alleviate AI chip shortages and drive future high-performance computing innovation.

IN DEPTH

Key Findings

TSMC is aggressively expanding its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity to address the unprecedented demand emanating from artificial intelligence (AI) accelerators and High-Performance Computing (HPC) applications. This concerted effort is projected to reduce the current 20% supply-demand gap for CoWoS to approximately 10% by the end of 2026, significantly alleviating ongoing AI chip supply constraints.

Technical & Production Details

CoWoS is a leading 2.5D/3D packaging technology that integrates multiple logic dies and HBM (High Bandwidth Memory) on a silicon interposer, which is then connected to a substrate. This architecture dramatically enhances data transfer rates and power efficiency, delivering the performance crucial for complex AI model computations. TSMC's mastery of CoWoS technology positions it as a vital service provider for major AI chip manufacturers.

Furthermore, TSMC is actively developing its next-generation packaging technology, CoPoS (Chip-on-Panel-on-Substrate). CoPoS aims to leverage larger panel substrates to process more chips simultaneously, promising reduced manufacturing costs and increased throughput compared to CoWoS. Pilot production for CoPoS technology is slated for 2027, with NVIDIA's forthcoming AI platform, "Feynman," anticipated to be one of the first products to adopt this innovative technology. The introduction of CoPoS, particularly with the potential integration of glass core substrates, is expected to further cut costs and boost wafer utilization efficiency.

Background & Context

The proliferation of AI has ushered in a new wave of growth for the semiconductor industry, but it also presents novel manufacturing challenges that traditional processes cannot meet. The tight integration of HBM and logic chips is a critical factor determining the performance of AI accelerators. Advanced packaging technologies like CoWoS and CoPoS are key to achieving this integration. TSMC's aggressive investment in these areas is a strategic move to maintain its market leadership and support the burgeoning AI ecosystem.

Strategic Significance & Outlook

The expansion of CoWoS capacity and the introduction of CoPoS will help mitigate AI chip shortages, enabling a greater volume of AI products to enter the market. This, in turn, will accelerate the widespread adoption of AI technologies and foster innovation across various sectors, including autonomous driving, cloud computing, and edge AI. TSMC's ongoing initiatives in advanced packaging are poised to be significant milestones, shaping the future direction of semiconductor manufacturing technology.

Source: <https://www.ftcelectronics.com/news/Electronics-Weekly-News-June-15-21,2026>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#03 ASE Technology Holding Raises 2026 Capex to \$8.5 Billion Driven by Surging AI Advanced Packaging Demand, Launches 15 Expansion Projects in Taiwan & Malaysia

Published June 25, 2026 SemiMedia Taiwan



OVERVIEW

ASE Technology Holding, the world's largest OSAT provider, has significantly increased its 2026 capital expenditure plan from \$7 billion to \$8.5 billion, a 21.4% jump, driven by robust demand from AI servers, HPC, and advanced packaging. The company anticipates its advanced packaging and test businesses to double year-over-year in 2026 and is currently executing 15 capacity expansion projects across Taiwan and Malaysia. This aggressive investment aims to address the rapidly expanding AI chip market and alleviate industry bottlenecks.

Key Findings

ASE Technology Holding, the world's largest outsourced semiconductor assembly and test (OSAT) provider, has announced a substantial upward revision of its 2026 capital expenditure (Capex) plan, increasing it from an initial \$7 billion to \$8.5 billion. This significant 21.4% increase is a direct response to the unprecedented surge in demand for AI servers, High-Performance Computing (HPC), and advanced packaging solutions. The strategic investment aims to resolve advanced packaging bottlenecks in the AI chip supply chain and support the rapid growth of the market.

Business & Investment Details

ASE Technology Holding specializes in semiconductor assembly, testing, and material services, playing a pivotal role in advanced packaging technologies. The company projects a robust doubling of its advanced packaging and test business revenue year-over-year in 2026, necessitating this aggressive Capex strategy.

Specifically, ASE is undertaking 15 capacity expansion projects across its key operational hubs in Taiwan and Malaysia. These projects are designed to boost manufacturing capabilities for cutting-edge advanced packaging technologies, including flip-chip, 2.5D/3D stacking, and chiplet integration. Malaysia, in particular, is cementing its role as a vital hub for the semiconductor back-end industry, playing a central role in ASE's global strategy.

Background & Context

The explosive proliferation of AI has dramatically escalated the demand for more complex and higher-performance semiconductor packaging. AI accelerators, such as NVIDIA's GPUs and AMD's MI series, critically depend on advanced packaging techniques like CoWoS (Chip-on-Wafer-on-Substrate) for integrating multiple dies and HBM (High Bandwidth Memory). In this context, OSAT companies have become indispensable, holding the key to enhancing AI chip performance and optimizing cost efficiency. ASE's increased Capex is a direct response to seize this enormous market opportunity and bolster its competitive edge.

Strategic Significance & Outlook

ASE Technology Holding's \$8.5 billion Capex plan underscores its strong confidence in the sustained growth of the AI semiconductor market. This investment is expected to further solidify the company's leadership in advanced packaging, enabling its fabless and IDM (Integrated Device Manufacturer) clients to rapidly introduce next-generation AI chips to the market. The expansion of production capacities in Taiwan and Malaysia reaffirms the Asia-Pacific region's central role in the global semiconductor supply chain and is poised to be a significant accelerant for technological innovation in the AI era.

Source: <https://www.semimedia.cc/ase-raises-2026-capex-to-8-5-billion-as-ai-drives-advanced-packaging-demand/>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#04 Morgan Stanley Forecasts TSMC AI Revenue to Surge 218% to \$86.3 Billion by 2027, CoWoS Capacity Remains a Critical Bottleneck

Published June 25, 2026 HTX Insights (Morgan Stanleyレポート引用) International



OVERVIEW

A new report from Morgan Stanley forecasts TSMC's AI-related revenue to surge by 218% to \$86.3 billion by 2027, up from \$27.1 billion in 2026. However, this explosive growth is shadowed by a critical bottleneck: CoWoS advanced packaging capacity. Global CoWoS demand is projected to reach 2.694 million units by 2027, significantly outstripping the combined supply from TSMC and other providers, posing a significant challenge to the accelerating AI chip market.

Key Findings

A recent research report by Morgan Stanley illuminates the extraordinary growth potential of TSMC's AI-related business within the semiconductor industry. The report projects TSMC's AI revenue to reach a substantial \$86.3 billion by 2027, marking a staggering 218% increase from \$27.1 billion in 2026. Despite this rapid expansion, the report underscores that production capacity for CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging—essential for high-performance AI chips—remains a critical bottleneck for the market.

Market Projections and Technical Challenges

Morgan Stanley's analysis indicates that the explosive growth of the AI chip market is profoundly transforming TSMC's revenue streams. Demand for AI-related chips is accelerating, driven by the proliferation of data centers, High-Performance Computing (HPC), and edge AI devices, all requiring increasingly sophisticated packaging technologies. CoWoS stands out as one of the most in-demand advanced packaging techniques, critical for maximizing inter-chip data transfer speeds and power efficiency by integrating multiple logic dies with High Bandwidth Memory (HBM).

The report provides a specific forecast, estimating global CoWoS demand to reach 2.694 million units annually by 2027. This projection contrasts sharply with the forecasted supply capacity from TSMC and other OSAT (Outsourced Semiconductor Assembly and Test) providers, which, despite aggressive expansion efforts, is expected to fall considerably short of this demand. Such a persistent supply shortage could directly impede the market introduction schedules for next-generation AI chips and slow the overall deployment pace of AI infrastructure.

Background & Context

In the realm of state-of-the-art semiconductor manufacturing, CoWoS is pivotal for enabling next-generation architectures such as chiplets and 3D stacking. TSMC is a recognized technology leader in this field and an indispensable manufacturing partner for major AI chip design companies, including NVIDIA. However, the inherent complexity of the CoWoS process, coupled with the stringent requirements for highly precise equipment and specialized engineers, renders rapid expansion of production capacity challenging. This bottleneck, therefore, represents a broader systemic challenge for the entire semiconductor supply chain, significantly influencing the adoption rate of advanced AI technologies.

Strategic Significance & Outlook

While CoWoS supply constraints are likely to temper AI chip market growth in the short term, they also serve as a powerful impetus for increased investment across the OSAT industry and the fostering of new technological innovations. TSMC is actively investing in next-generation packaging technologies like CoPoS (Chip-on-Panel-on-Substrate), which are expected to eventually alleviate the current CoWoS bottleneck. Investors and industry stakeholders will need to closely monitor CoWoS supply trends and TSMC's strategic capacity expansion plans to effectively navigate the rapidly evolving AI-era semiconductor market.

Source: <https://www.htx.com/news/report-analysis-tsmcs-ai-revenue-to-double-by-2027-cowos-cap-oSW4K9y0/>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#05 Malaysia Invests RM185 Million (\$40M) in Advanced Semiconductor R&D Initiative, Targeting 7% Global Packaging Market Share with HBM4 Test Chip Development

Published June 26, 2026 Malay Mail / Digital News Asia Malaysia



OVERVIEW

Malaysia's Ministry of Science, Technology and Innovation (Mosti) has launched a RM185 million (approx. \$40 million USD) Research, Development, Innovation, Commercialization, and Economy (RDICE) program to bolster homegrown advanced semiconductor packaging capabilities. This ambitious initiative aims for Malaysia to secure a 7% share of the global advanced packaging market, focusing on the Proof-of-Concept (PoC) development of next-generation HBM4 test chips through collaboration between five local semiconductor firms and academic institutions. The program seeks to elevate Malaysia's strategic position in the AI-era semiconductor supply chain.

Key Findings

Malaysia's Ministry of Science, Technology and Innovation (Mosti) has announced the launch of a substantial Research, Development, Innovation, Commercialization, and Economy (RDICE) program, committing RM185 million (approximately \$40 million USD) to significantly enhance the nation's indigenous capabilities in advanced semiconductor packaging technology. This ambitious initiative sets a clear target for Malaysia to capture a 7% share of the global advanced packaging market, with a primary focus on the Proof-of-Concept (PoC) development of next-generation HBM4 (High Bandwidth Memory 4) test chips.

Program Details and Technical Focus

The RDICE program adopts a multi-faceted approach to invigorate Malaysia's semiconductor ecosystem. Specifically, five leading domestic semiconductor companies will collaborate closely with various universities and research institutions to drive technological innovation and talent development in advanced packaging. Key technical focuses include:

- **HBM4 Test Chip PoC Development:** The development of test chips for HBM4 memory, which is crucial for AI and High-Performance Computing (HPC) systems, represents a vital step for Malaysia to establish leadership in cutting-edge memory packaging technology.
- **Advanced Packaging R&D:** Accelerating research and development in next-generation complex packaging solutions such as flip-chip, 3D stacking, and System-in-Package (SiP).
- **Talent Development and Capacity Building:** Through partnerships with local universities and research institutions, the program will strengthen the cultivation of engineers and researchers skilled in advanced semiconductor packaging technologies.

This investment signifies Malaysia's strategic shift from merely a manufacturing base to a nation that leads research, development, and innovation in advanced technologies.

Background & Context

For decades, Malaysia has established itself as a critical back-end (assembly and test) hub in the global semiconductor supply chain. However, with the exponential rise in demand for advanced packaging driven by AI, Malaysia aims to move into higher value-added technological domains. In an intensifying global semiconductor race, national-level R&D investment is an indispensable element for ensuring technological self-reliance and economic competitiveness. Mosti's program sends a clear message about Malaysia's intention to play a more strategic role in the AI-era semiconductor ecosystem.

Strategic Significance & Outlook

The RM185 million RDICE program is expected to propel Malaysia's semiconductor industry into a new phase of growth, significantly boosting its international competitiveness, particularly in advanced packaging. Success in HBM4 test chip development will strengthen collaborations with major global semiconductor firms, solidifying Malaysia's position as an indispensable partner in the AI chip supply chain. This investment contributes to the diversification of the Malaysian economy and the development of its high-tech industry, with the potential to attract further foreign investment in the future.

Source: <https://www.malaymail.com/amp/news/malaysia/2026/06/26/mosti-launches-rm185m-initiative-to-develop-homegrown-advanced-semiconductor-technology/225235>

#06 ATLANT 3D, A*STAR IMRE, and NAMIC Launch AI-Driven Materials Development Hub in Singapore

Published June 24, 2026 PR Newswire Singapore



OVERVIEW

ATLANT 3D, A*STAR IMRE, and NAMIC have signed an MoU to establish an Advanced Materials Development Hub (A-HUB) in Singapore, leveraging ATLANT 3D's Direct Atomic Layer Processing (DALP®) technology. This collaboration will accelerate the discovery and development of next-generation materials for semiconductor manufacturing, silicon photonics, and advanced packaging applications, combining cutting-edge synthesis with AI-driven discovery to significantly shorten R&D cycles.

Key Findings

ATLANT 3D, the Agency for Science, Technology and Research's (A*STAR) Institute of Materials Research and Engineering (IMRE), and the National Additive Manufacturing Innovation Cluster (NAMIC) announced the signing of a Memorandum of Understanding (MoU) to establish an Advanced Materials Development Hub (A-HUB) in Singapore. The A-HUB aims to accelerate the discovery and development of next-generation materials crucial for semiconductor manufacturing, silicon photonics, and advanced packaging, utilizing AI-driven methodologies.

Technical Details

At the core of the A-HUB's capabilities is ATLANT 3D's proprietary Direct Atomic Layer Processing (DALP®) technology. DALP® enables precise material deposition at the atomic level, delivered with ultra-high throughput. By integrating this technology with A*STAR IMRE's deep expertise in materials science and NAMIC's extensive industry network, the material research and development process will be dramatically streamlined. Applying AI algorithms to materials exploration allows for significantly faster identification and synthesis of new materials meeting specific performance requirements, compared to traditional trial-and-error approaches. This will accelerate the development of new dielectrics, conductors, and protective layers essential for advanced packaging.

Background & Context

The semiconductor industry faces a dual challenge: the slowdown of Moore's Law and the escalating importance of advanced packaging. Next-generation packaging techniques such as chiplet integration, 3D stacking, and photonic integration demand unprecedented high-performance materials and precision processes. Traditional material development is a time-consuming and costly endeavor, often hindering the pace of technological innovation. Singapore has established itself as a global hub for semiconductor manufacturing, and the establishment of the A-HUB represents a strategic step to further strengthen its domestic ecosystem and expand its role in global technological competition. AI-driven materials discovery is seen as a promising approach to overcome these challenges and accelerate innovation across the entire semiconductor industry.

Strategic Significance & Outlook

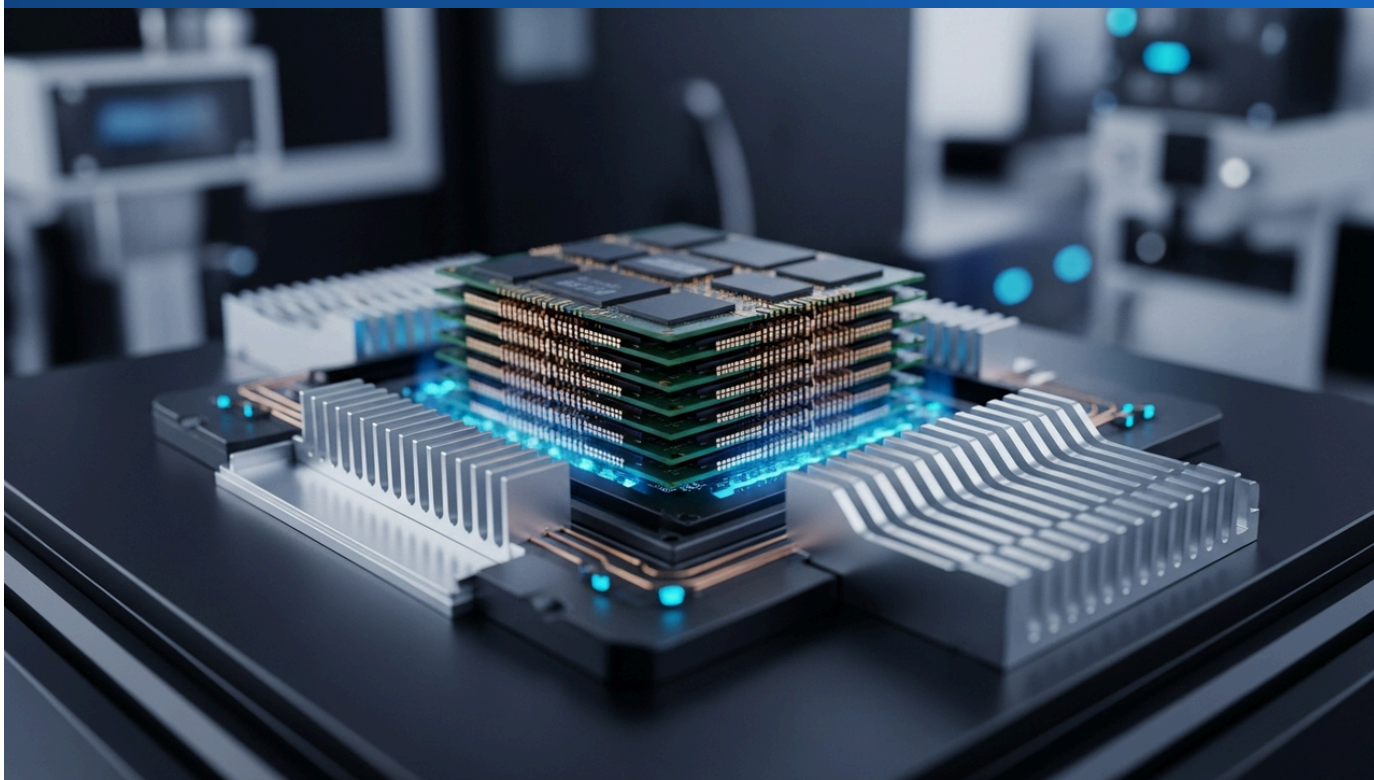
The A-HUB is designed to reduce the lead time for material R&D and expedite the market introduction of advanced semiconductor technologies, solidifying Singapore's position as a center for advanced materials science and AI applications. This initiative has potential applications beyond the semiconductor industry, extending to other fields requiring precision materials, such as aerospace, medical technology, and energy. The MoU serves as a model case for how collaboration between academia, startups, and industry can accelerate technological innovation and enable sustainable growth.

Source: https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQHtFwLOG1icVGGfcVOeKE_RTMC2mJhJj-BtZCDz5dOKwPd4WgaFZZ_GJgd6XevBRxYAQ0omp6cmo8X9xiKViT122a8ms_Lxjs9CHPNZqvipg5b16KmRSybH9E

Collected: June 26, 2026 | Automated Research System (Gemini API)

#07 Samsung Validates Hybrid Copper Bonding's Superior Thermal Management for HBM4E, Outperforming TCB

Published June 25, 2026 ET News (via IEEE paper) South Korea



OVERVIEW

Samsung published research in IEEE demonstrating that its Hybrid Copper Bonding (HCB) offers significant thermal management advantages over conventional Thermo-Compression Bonding (TCB) for HBM4E packaging. HCB reduces hotspot temperatures and thermal interference while enabling HBM stack heights to be over 15% thinner. This validation enhances power budgets and reliability in server environments, solidifying the industry trend towards hybrid bonding for advanced packaging.

Key Findings

Samsung has published research via IEEE demonstrating that its Hybrid Copper Bonding (HCB) technology offers distinct thermal management advantages over traditional Thermo-Compression Bonding (TCB) for HBM4E (High Bandwidth Memory Generation 4 Enhanced) packaging. This breakthrough significantly enhances the performance and reliability of high-density stacked memory solutions.

Technical Details

According to Samsung's research, HCB technology forms direct copper-to-copper connections, which substantially reduces thermal resistance within the HBM stack. This leads to lower hotspot temperatures and decreased thermal interference between adjacent memory layers and logic chips. Specifically, HCB enables a reduction in HBM stack thickness by over 15% compared to TCB, thereby improving cooling efficiency and ameliorating thermal gradients within the stack. This combination of thinning and superior thermal characteristics is critically important for next-generation High-Performance Computing (HPC) systems, especially those incorporating 16-high or higher HBM stacks, providing the foundation for higher power budgets and enhanced long-term reliability.

Background & Context

In fields such as AI, HPC, and data centers, the explosive growth in data processing demands memory with increasingly higher bandwidth and lower power consumption. HBM was developed to meet these requirements, and its ultimate performance is heavily dependent on the underlying packaging technology. Conventional TCB methods have revealed significant thermal design challenges as the number of HBM layers increases. Samsung's demonstration of HCB's superiority underscores the growing importance of hybrid bonding in advanced packaging, particularly for HBM integration. This aligns with the broader semiconductor industry trend of viewing packaging technology as a key frontier for performance improvement, especially as transistor scaling approaches its physical limits.

Strategic Significance & Outlook

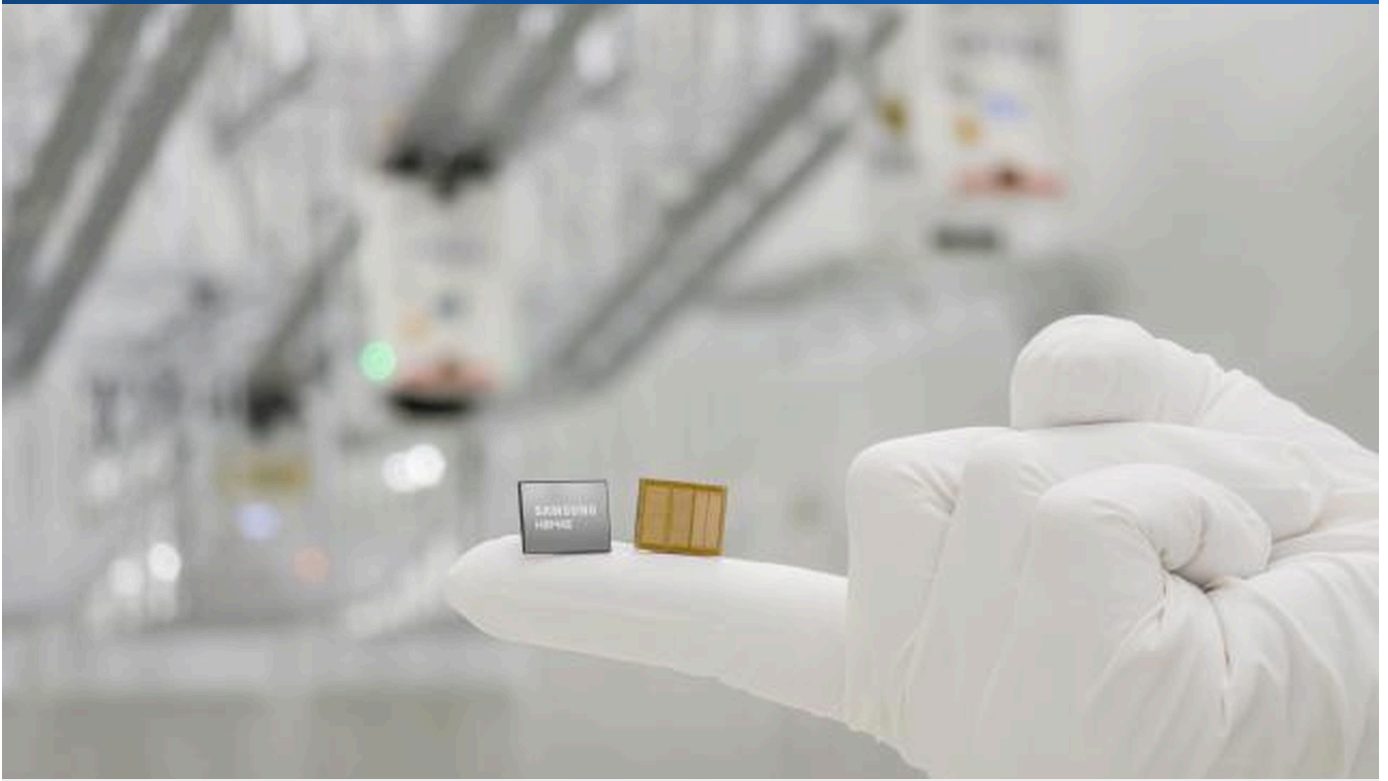
The validation of HCB technology holds substantial implications for Samsung's competitiveness in the HBM market. Leading AI accelerator customers, such as NVIDIA, demand high-performance and highly reliable HBM, where superior thermal management is a critical differentiating factor. Samsung is likely to deploy this technology in HBM4E and subsequent HBM generations, aiming to solidify its leadership in the AI/HPC memory market. The industry at large is expected to accelerate the adoption of hybrid bonding technologies, contributing to enhanced performance and reliability of next-generation high-density semiconductors.

Source: https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQG-PeN9G8tahHemk9f8I7GxAmbuzSb_of0UKGT7BsQ1COOnh4ISGKEE5oH7ely1eUE7mTHCZhyfSUSRpmBsJBLWD2xL_L_Mgo6zrxjGpl0dNWfovYILqd4X4hanFEVQXqcyItB-GWgDh2BuciaZrtbJrR8oSMH3CFvNaoLjdhhl353FzOrbVeVI-5UAKATvFYkitaXq8eY9ElpIIGNWV7qSE=

Collected: June 26, 2026 | Automated Research System (Gemini API)

#08 TSMC's CoWoS Packaging Capacity Identified as Bottleneck in Korea's HBM4E Race, Despite SK hynix and Samsung Shipments

Published June 18, 2026 Aju Press South Korea



OVERVIEW

Despite SK hynix and Samsung Electronics commencing sample shipments of 12-layer HBM4E chips to major customers like Nvidia, TSMC's CoWoS advanced packaging capacity is highlighted as the true bottleneck in the HBM4E era. CoWoS is essential for integrating memory and logic chips into a single system, making packaging a critical differentiator beyond raw memory performance. This means that regardless of how many HBM chips Korean manufacturers produce, the market availability of final products remains constrained by Taiwan's packaging capabilities.

IN DEPTH

Key Findings

While leading Korean memory manufacturers, SK hynix and Samsung Electronics, have begun shipping samples of 12-layer HBM4E chips to key customers including Nvidia, industry analysts indicate that the real bottleneck in the HBM4E era is TSMC's CoWoS advanced packaging capacity. Packaging has emerged as a decisive factor, transcending raw memory performance, in determining the market availability of final products.

Technical Details

HBM4E, the next-generation High Bandwidth Memory designed for AI accelerators, necessitates highly efficient integration with logic chips (GPUs and AI processors) to unlock its full performance potential. TSMC's CoWoS (Chip-on-Wafer-on-Substrate) is the primary advanced packaging technology enabling this tight integration of logic and HBM on a silicon interposer, allowing them to function as a single system. This dramatically boosts data transfer rates and reduces power consumption. For high-stack memories like 12-layer HBM4E, thermal management and signal integrity challenges also intensify, making advanced packaging processes like CoWoS a critical bottleneck.

Background & Context

The increasing complexity and scale of AI models have driven unprecedented demand for advanced memory like HBM. While SK hynix and Samsung lead the world in HBM chip development and mass production, these HBM chips require CoWoS-like advanced packaging to be integrated into AI accelerators for customers such as Nvidia. TSMC holds a dominant share in the CoWoS packaging market, making its production capacity the primary determinant of the overall AI chip supply. This situation underscores a new bottleneck in the semiconductor supply chain: regardless of how many high-performance HBMs Korean manufacturers produce, market supply will be constrained unless TSMC's packaging capacity keeps pace.

Strategic Significance & Outlook

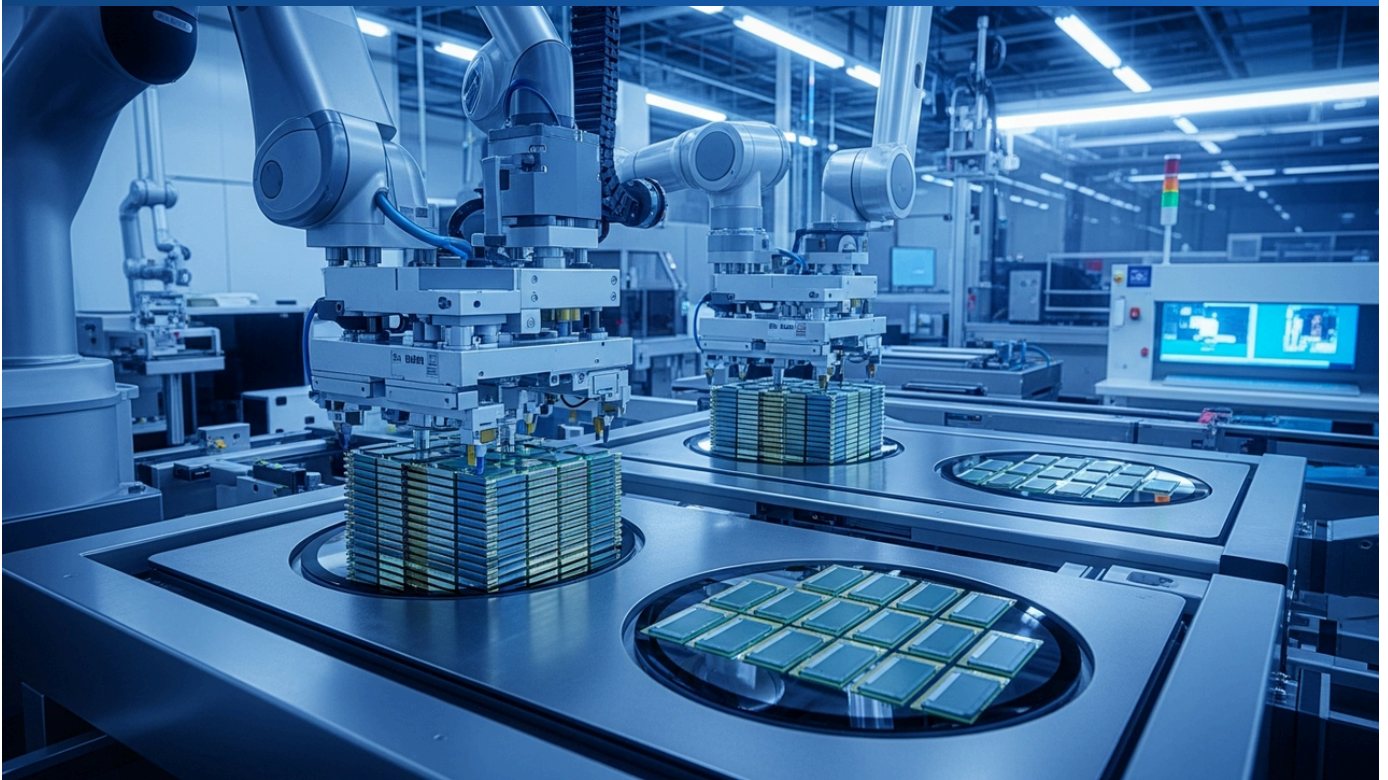
With TSMC's CoWoS capacity holding the key to AI chip market growth, the company plans to expand its capacity by over 80% annually through 2027, aiming to reduce the AI chip supply gap. However, this bottleneck will remain a significant challenge for competitive strategies in the HBM market, particularly for Korean manufacturers, for the foreseeable future. Memory makers will need to focus not only on HBM chip performance but also on strengthening collaborations with packaging partners and exploring cooperation with Outsourced Semiconductor Assembly and Test (OSAT) providers beyond TSMC to alleviate supply constraints. This challenge also presents an opportunity to accelerate diversification and resilience within the broader semiconductor industry supply chain.

Source: <https://www.ajupress.com/view/20260618160856166>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#09 Samsung and SK Hynix Announce Major HBM Capacity Expansions: Samsung Allocates Half to HBM4, Targeting 250K Wafers/Month by EOY 2026

Published June 18, 2026 Industry News / ChosunBiz South Korea



OVERVIEW

Samsung Electronics announced plans to increase its HBM production capacity by approximately 50% from 2025 levels, aiming for 250,000 semiconductor wafers per month by the end of 2026. The company is strategically allocating half of this capacity to the 6th-generation HBM4, having already shipped HBM4 samples in February to accelerate market share recovery. Concurrently, SK hynix is constructing its P&T7 facility in Cheongju, focused on advanced semiconductor packaging and testing, expected to be operational in 2027 to supply next-generation components.

Key Findings

Samsung Electronics announced a substantial increase in its High Bandwidth Memory (HBM) production capacity, targeting approximately 50% growth from 2025 levels to reach 250,000 semiconductor wafers per month by the end of 2026. Simultaneously, SK hynix is developing its P&T7 facility in Cheongju, dedicated to advanced semiconductor packaging and testing, with operations projected to begin in 2027, signaling significant HBM market supply enhancements from both companies.

Technical Details

Samsung has made a strategic decision to dedicate half of its HBM production capacity to the 6th-generation HBM4. This reflects a robust initiative to meet the high demand for HBM4 from Application-Specific Integrated Circuit (ASIC) and cloud companies, aiming to reclaim market share. The company began shipping HBM4 samples in February and is leveraging its integrated foundry and advanced packaging capabilities to optimize base die customization and enhance packaging competitiveness. Concurrently, SK hynix is building its P&T7 facility in Cheongju, Chungcheongbuk-do, focused on state-of-the-art semiconductor back-end processes (packaging and testing). While specific investment figures and detailed production capacities remain undisclosed, the facility is expected to be operational in 2027 to supply next-generation HBM and other high-density integrated components to global customers.

Background & Context

The rapid evolution of AI technology has stimulated unprecedented demand for HBM, with the HBM market projected for substantial growth in the coming years. Samsung and SK hynix, as leading Korean memory manufacturers, are making massive investments through distinct approaches to secure leadership in this expanding market. HBM4 is particularly crucial for future AI accelerators, making both companies' capacity expansions vital for accelerating AI infrastructure development. Samsung, with its in-house foundry and advanced packaging capabilities, is uniquely positioned to optimize base die design. SK hynix's new P&T7 facility aims to cater to a broader range of customer needs by supporting various advanced packaging technologies beyond HBM.

Strategic Significance & Outlook

These large-scale investments and capacity expansions by Samsung and SK hynix are expected to intensify competition in the HBM market while strongly bolstering the development of the entire AI industry. Stabilized supply capacity will enable AI chip design companies to pursue more aggressive product roadmaps, thereby accelerating innovation. The strategic moves by both companies underscore the evolving importance of HBM technology and associated semiconductor back-end processes, making future market dynamics a key area for observation.

Source: https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQFLap996JfQkrbM_ABE4AZaDu0oRDJcl7FiBt6bL3iacaC8mn3tyYsp4JnXUD9-cohoUejCyuh96GKzBXP2tD1hU_pwLs1g2bC06VS3_8asaQVJcwvaeM3L-seuCB5W0r3Hb0gqYmRb4ebKpVZoELn99r1gwMTkSrK6dQo_FOQ-w9uOY5b4uHahccvIhktIVL82NqLay49iqyCkinnuAMPiMMcHtoldEWyE1C4=

Collected: June 26, 2026 | Automated Research System (Gemini API)

#10 TSMC Accelerates CoPoS Packaging with Glass Core Substrates: Targets 30% Cost Reduction, >90% Wafer Utilization Post-2028

Published June 20, 2026 Wccfttech / CHOSUNBIZ / BigGo Finance Taiwan



OVERVIEW

TSMC is accelerating the development of CoPoS packaging, a successor to CoWoS, leveraging glass core substrates co-developed with Ibiden and Innolux. This panel-level packaging approach is projected to reduce costs by 30% and boost wafer utilization from under 70% to over 90% for ultra-large AI chips after 2028, effectively solving geometric waste issues. The glass substrates also offer superior co-planarity, lower thermal expansion, and enhanced power integrity.

IN DEPTH

Key Findings

TSMC is significantly accelerating the development of CoPoS (Chip-on-Panel-on-Substrate) packaging, a next-generation technology intended to eventually supersede CoWoS (Chip-on-Wafer-on-Substrate). This innovative approach centers on glass core substrates, co-developed with Ibiden and Innolux. It aims to achieve a remarkable 30% cost reduction and boost wafer utilization from under 70% to over 90% for ultra-large AI chips post-2028, effectively addressing geometric waste challenges inherent in current processes.

Technical Details

CoPoS packaging differs from traditional wafer-level CoWoS by integrating chips at the panel level. The glass core substrate forms a crucial tri-layer design, sandwiched by Ajinomoto Build-up Film (ABF) material. TSMC's validation metrics for glass substrates reveal significant advantages over organic substrates, including superior co-planarity, a substantially lower coefficient of thermal expansion (CTE), and enhanced power integrity. These improvements are vital for large AI GPU packages, as they drastically reduce issues like warpage and thermal stress, allowing for the integration of more chips with higher reliability. The leap in wafer utilization from below 70% to over 90% will profoundly resolve the problem of geometric waste (e.g., mismatch between circular wafers and square chips) during the manufacturing of ultra-large chips, directly translating to substantial cost reductions.

Background & Context

As AI continues to evolve, the size and complexity of AI chips are steadily increasing. While advanced packaging technologies like CoWoS have become increasingly critical, they have also exposed the physical limitations of organic substrates—particularly warpage and thermal expansion issues at larger scales—and challenges with cost efficiency in wafer-level manufacturing. To overcome these hurdles, TSMC is spearheading the adoption of glass substrates, forging strategic collaborations with leading ABF substrate manufacturer Ibiden of Japan and display panel maker Innolux of Taiwan. This industry shift clearly indicates a move beyond mere transistor scaling towards innovation in back-end processes to pursue both performance and cost efficiency.

Strategic Significance & Outlook

The adoption of CoPoS packaging and glass core substrate technology has the potential to revolutionize the design and manufacturing of next-generation AI chips, especially large-scale AI processors, from 2028 onwards. The projected cost reductions and utilization improvements will accelerate the proliferation of AI hardware, contributing to the realization of a wider array of AI applications. This technology is expected to reshape the competitive landscape of the entire semiconductor industry, creating new business opportunities for material suppliers and packaging equipment manufacturers. TSMC's focus on CoPoS is a critical trend that will significantly influence the future direction of advanced packaging technology and is keenly watched by the industry.

Source: <https://wccftech.com/tsmc-accelerates-copos-packaging-replace-cowos-as-glass-core-substrates-cut-costs-boost-wafer-utilizatio/>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#11 Resonac to Initiate High-Purity HF Gas Production at Tokuyama Plant by 2026, Strengthening Domestic Semiconductor Supply

Published June 25, 2026 Resonac (Official Press Release) / IBTimes JP Japan



OVERVIEW

Resonac announced it will begin producing high-purity hydrogen fluoride (HF) gas for semiconductors at its Tokuyama plant in Shunan City, Yamaguchi Prefecture, within 2026. This establishes a second domestic production base alongside its Kawasaki plant, significantly enhancing the supply stability of HF gas crucial for advanced etching processes. This move is increasingly important for three-dimensional, high-density integrated semiconductor structures driven by AI and data center demand, particularly for cryogenic etching applications.

Key Findings

Resonac announced plans to commence production of high-purity hydrogen fluoride (HF) gas, a crucial material for semiconductor manufacturing, at its Tokuyama Plant in Shunan City, Yamaguchi Prefecture, within 2026. This new production site will establish a second domestic supply base, complementing its existing Kawasaki plant, thereby significantly strengthening the stable supply system for the semiconductor industry.

Technical Details

High-purity HF gas is indispensable in the front-end semiconductor manufacturing process, particularly in etching, where it is used to form intricate patterns on silicon wafers. For high-density, three-dimensional integrated semiconductors targeting AI and data center applications, there is a growing demand for advanced etching technologies, such as cryogenic etching, which enable the creation of deeper and finer structures. Resonac's HF gas provides the ultra-high purity and stability required for these sophisticated etching processes. The commencement of production at the Tokuyama Plant not only boosts production capacity but also diversifies supply risks, contributing to the overall resilience of Japan's semiconductor supply chain.

Background & Context

Semiconductors are the foundational pillars supporting modern digital infrastructure, including AI, 5G, IoT, and data centers, with global demand continuously expanding. Consequently, the stable supply of materials and gases used in semiconductor manufacturing has become an international concern. High-purity gases, in particular, directly impact the quality and yield of manufacturing processes, necessitating highly reliable supply sources. Resonac's increased HF gas production aligns with the Japanese government's policy to strengthen the semiconductor supply chain, aiming to foster an environment where semiconductor manufacturers can operate with greater certainty through enhanced domestic supply capabilities.

Strategic Significance & Outlook

The initiation of high-purity HF gas production at the Tokuyama Plant will further enhance Resonac's competitiveness in the semiconductor materials business. It is expected to contribute to an increased market share, especially in meeting the rising demand for cutting-edge semiconductors used in AI and HPC. Moreover, establishing multiple domestic production bases improves the supply chain's resilience against natural disasters and geopolitical risks, providing a solid foundation for the sustainable growth of Japan's semiconductor industry. This move reaffirms the crucial role that Japan's materials industry plays within the global semiconductor ecosystem.

Source: <https://www.resonac.com/news/2026/06/25/3877.html>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#12 Imec Seeks PhD for Microfluidics and Photonics Packaging in Optical Interconnects for HPC and AI Systems

Published June 23, 2026 ApplyKite (imec) ベルギー



OVERVIEW

Imec is seeking a PhD candidate for groundbreaking research into microfluidics and photonics packaging, crucial for optical interconnects in future AI and High-Performance Computing (HPC) systems. The project will optimize the capillary underfill process, directly addressing challenges like void formation and non-uniform gap heights to significantly enhance the reliability and performance of high-density optical/CMOS packages. This work is pivotal for enabling high-bandwidth, energy-efficient data transfer that will alleviate performance bottlenecks in advanced computing.

Background: The Interconnect Challenge in Next-Gen AI and HPC

The escalating scale of AI models and the increasing processing demands of modern data centers are rapidly exposing the fundamental limits of traditional electrical signaling for chip-to-chip communication. Optical interconnects are emerging as a promising and indispensable solution for next-generation High-Performance Computing (HPC) and AI accelerators, offering high bandwidth, low power consumption, and low latency.

However, achieving efficient and reliably integrated packaging of optical and CMOS devices remains a significant technical hurdle. Specifically, optimizing underfill material properties and process control is critical, as these factors directly impact the long-term reliability and manufacturing yield of these complex packages. Imec, a global leader in semiconductor R&D, is playing a crucial role in pushing the frontiers of this vital field.

Key Research Areas and Strategic Impact

To advance this critical domain, Imec is inviting applications for a PhD candidate to lead research into microfluidics and photonics packaging for optical interconnects, essential for next-generation AI and HPC systems. This project specifically targets the capillary underfill process—a crucial step in packaging integrated optical and CMOS chips—aiming to resolve critical issues that currently limit the reliability and performance of high-density optical/CMOS packages. The successful candidate will focus on overcoming several key technical challenges, including:

- **Void Formation Suppression:** Addressing voids generated during underfill material dispensing and subsequent curing between the chip and substrate, which are a primary cause of reliability degradation.
- **Wetting Behavior and Rheology Optimization:** Precisely controlling the flow and material properties (rheology) of the liquid underfill for uniform filling within the microscopic, confined geometries of advanced packages.
- **Adaptation to Non-Uniform Gap Heights:** Developing robust underfill processes that can reliably accommodate variations in gap height between the chip and substrate, which arise from diversifying package structures.

- **High-Density, Low-Cost, High-Throughput Packaging:** Improving the overall manufacturing efficiency and economic viability of integrating optical and CMOS devices to enable their widespread adoption.

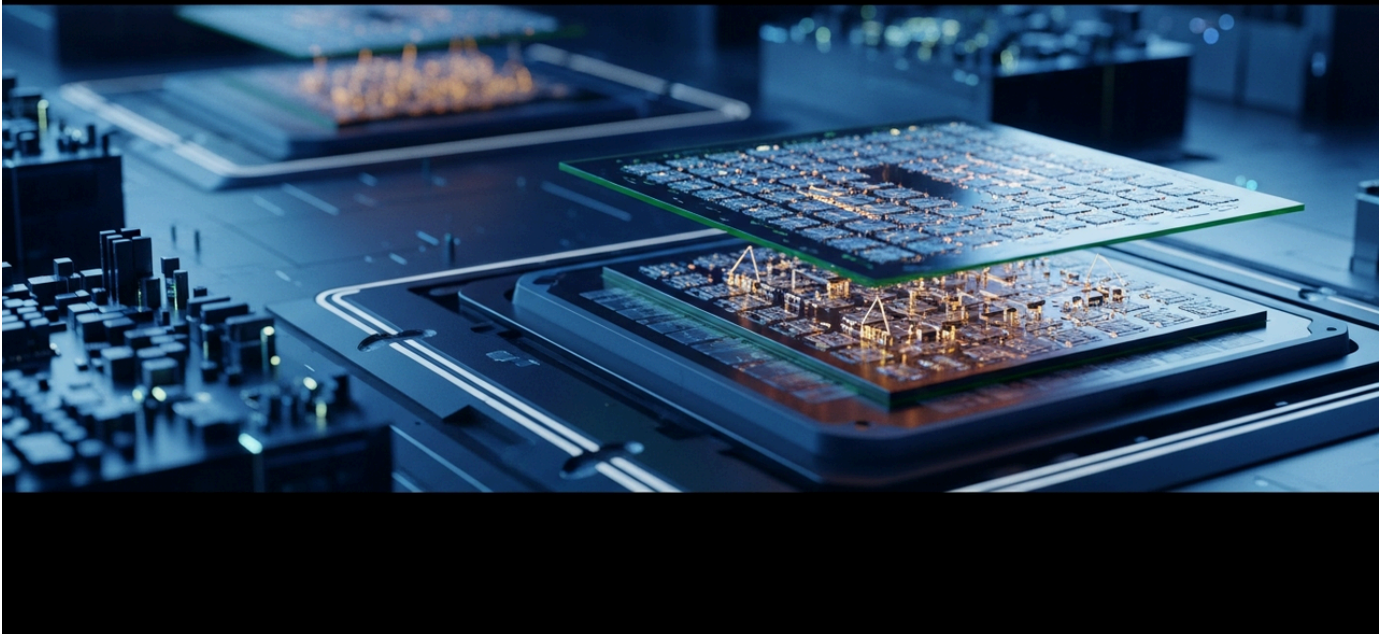
By effectively solving these challenges, this research will significantly enhance the performance, reliability, and manufacturability of optical interconnects, directly contributing to alleviating critical performance bottlenecks in future AI and HPC systems. This work is expected to accelerate the commercialization of optical interconnect technology, contributing to the realization of more powerful and energy-efficient computing platforms. Furthermore, improvements in the capillary underfill process will lead to reduced packaging costs and increased production throughput, fostering broader industrial applications and positioning this research as a vital component in the advanced packaging roadmap for the semiconductor industry.

Source: <https://www.applykite.com/positions/phd-in-microfluidics-and-photonics-packaging-for-optical-interconnects-in-hpc-and-ai-systems-efkh5azus4>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#13 Imec Accelerates Ferroelectric Memory (FeFET) for AI Systems: Demonstrates Vertically Stacked IGZO-Based FeFET Architecture

Published June 22, 2026 IN Electronics & Design ベルギー



OVERVIEW

Imec has achieved a significant breakthrough in ferroelectric memory for AI systems, demonstrating a vertically stacked FeFET architecture utilizing IGZO and successfully reducing ferroelectric capacitor operating voltage. These innovations dramatically enhance storage density and energy efficiency, vital for high-performance AI across all scales. This research is critical for next-generation memory, logic, and packaging roadmaps, solidifying the foundation for advanced AI hardware.

Background: Tackling the AI Memory Wall

The relentless growth of artificial intelligence (AI) is pushing the boundaries of computing, demanding not only immense processing power but also groundbreaking memory solutions capable of efficiently storing and accessing vast amounts of data. Traditional memory technologies like DRAM and NAND flash are struggling to keep pace, presenting challenges in speed and density, respectively. The resulting 'memory wall' – a bottleneck in data movement between processor and memory – has become a critical constraint for high-performance AI systems.

Ferroelectric memory (FeRAM or FeFET), with its unique combination of non-volatility, high speed, and low power, has emerged globally as a highly promising candidate to overcome this 'memory wall' challenge. Research institutions and companies worldwide are actively developing this technology, and Imec's latest achievement significantly boosts the industry's overall efforts toward higher performance and lower power consumption for AI systems.

Key Breakthroughs: Vertical Stacking and Voltage Reduction

Imec has announced a significant breakthrough in ferroelectric memory development specifically tailored for AI systems. Their researchers have successfully demonstrated a vertically stacked FeFET (Ferroelectric Field-Effect Transistor) architecture leveraging Indium Gallium Zinc Oxide (IGZO) as the channel material. Complementing this, they have also achieved a notable reduction in the operating voltage for ferroelectric capacitors. These innovations collectively pave the way for high-density, low-power memory solutions critical for the demanding requirements of next-generation AI applications.

Technical Deep Dive: Enhancing FeFET Performance and Efficiency

The core of Imec's innovation lies in its vertically stacked IGZO-based FeFET architecture. By arranging memory cells in three dimensions, this design dramatically enhances storage density per unit area, a crucial factor for miniaturization and performance scaling in advanced AI hardware. The strategic choice of IGZO as the semiconductor channel material is pivotal, offering both high electron mobility and exceptionally low leakage current. These properties are instrumental in boosting overall FeFET performance, contributing to faster operation and significantly lower standby power consumption.

Furthermore, the successful reduction of operating voltage in the ferroelectric capacitors directly translates to decreased memory power consumption. This profound improvement in energy efficiency impacts a broad spectrum of AI systems, from power-constrained, battery-powered AI edge devices to large-scale data centers. Ferroelectric memory uniquely offers the tantalizing prospect of combining non-volatility with operational speeds approaching SRAM and densities comparable to DRAM. This unique blend holds immense promise for radically enhancing data processing efficiency, especially for emerging paradigms such as AI in-memory computing and highly integrated edge AI applications, addressing the data movement bottleneck head-on.

Strategic Significance & Outlook: Redefining Memory for Next-Gen AI

Imec's significant advancements in ferroelectric memory technology are poised to redefine the very role of memory within AI systems, serving as a catalyst for the development of far more powerful and energy-efficient AI hardware. The combined benefits of enhanced storage density and reduced operating voltage are expected to accelerate the proliferation of sophisticated edge AI devices and enable a more seamless and consistent AI infrastructure extending from cloud data centers to the intelligent edge.

This technology is strategically positioned to be a pivotal player in the fiercely competitive next-generation memory landscape. Anticipated applications include serving as a viable, high-performance alternative to NAND flash memory for persistent storage and as high-density embedded memory directly integrated into logic chips. This innovation is also deeply intertwined with broader semiconductor roadmaps, including advanced memory, logic integration, and advanced packaging techniques such as chiplets and 3D stacking. Through this breakthrough, Imec is expected to make a foundational contribution to the continued evolution of AI technology and its pervasive deployment across a vast array of electronic devices.

Source: <https://www.inelectronics.co.uk/imec-advances-ferroelectric-memory-for-ai-systems/>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#14 Morgan Stanley Raises CoWoS Demand Forecast to 2.69 Million Wafers by 2027, Citing CPUs and ASICs as New Drivers

Published June 25, 2026 Industry Analysis / Moomoo Unknown



OVERVIEW

Morgan Stanley has significantly raised its demand forecast for TSMC's CoWoS packaging, projecting it to reach 2.69 million wafers annually by 2027. CPUs and ASICs are emerging as new key drivers for CoWoS demand, in addition to traditional GPUs. Non-TSMC OSAT vendors such as ASE/SPIL, Amkor, and Powertech are expected to capture a larger share of packaging for high-end PC CPUs and gaming GPUs, indicating a diversifying AI server market.

Key Findings

Morgan Stanley has substantially increased its demand forecast for TSMC's CoWoS (Chip-on-Wafer-on-Substrate) packaging, projecting it to reach 2.69 million wafers annually by 2027. This surge in demand is attributed to the emergence of CPUs and ASICs (Application-Specific Integrated Circuits) as new primary drivers, complementing the traditional role of GPUs.

Technical Details

CoWoS is an advanced packaging technology essential for AI, High-Performance Computing (HPC), and data center chips, enabling high bandwidth and low latency by integrating multiple chip dies (such as GPUs, HBM, CPUs, and ASICs) onto a silicon interposer. Morgan Stanley's latest analysis indicates a growing trend where advanced packaging like CoWoS is becoming mandatory for high-performance CPUs and custom ASICs, driven by the rapid evolution and adoption of AI chips. Concurrently, HBM (High Bandwidth Memory) demand is also projected to grow significantly, closely linked to AI chips, with HBM capacity per AI chip increasing substantially in 2026 and HBM module demand growing exponentially by 2027.

Background & Context

As semiconductor scaling approaches its physical limits, advanced packaging has become a crucial means of enhancing chip performance. While TSMC remains the pioneer and market leader in CoWoS technology, the explosive growth in demand is driving diversification within the supply chain. The new forecast anticipates that non-TSMC Outsourced Semiconductor Assembly and Test (OSAT) vendors, including ASE/SPIIL, Amkor, and Powertech, will secure a larger share in packaging high-end PC CPUs and gaming GPUs. This reflects the diversification of the AI server market, moving beyond NVIDIA's historical dominance to include the rise of Intel, AMD, and custom ASIC vendors.

Strategic Significance & Outlook

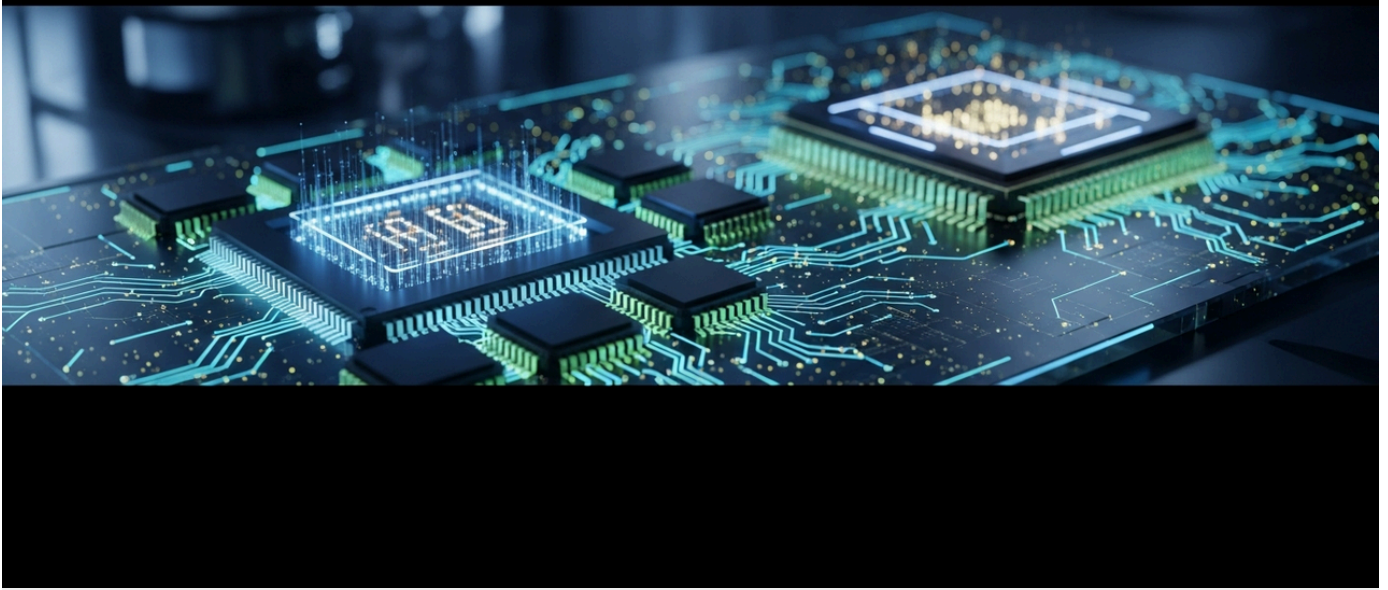
Morgan Stanley's upward revision of CoWoS demand forecasts clearly demonstrates the robust growth of the advanced packaging market and the increasing centrality of CoWoS within the AI ecosystem. The diversification of suppliers could mitigate the risk of over-reliance on a single vendor like TSMC, thereby improving overall supply chain resilience. Furthermore, with CPUs and ASICs becoming new demand drivers for CoWoS, the application scope for advanced packaging technologies will broaden, accelerating innovation across the entire semiconductor industry. Coupled with the surge in HBM demand, the advanced packaging sector is expected to remain a highly attractive area for investors and engineers alike.

Source: <https://news.futunn.com/en/post/75096132/morgan-stanley-raises-cowos-demand-forecast-to-reach-2-69>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#15 Imec Analyzes Transition to Chiplet-Based Designs: Enabling High-Bandwidth, Low-Energy AI/HPC Systems Beyond Monolithic ASICs

Published June 23, 2026 imec ベルギー



OVERVIEW

Imec has published a comprehensive analysis identifying the economic and technical inflection points for transitioning from monolithic ASICs to chiplet-based designs, particularly for AI, HPC, and data center applications. The research emphasizes that as silicon area approaches reticle size limits, advanced packaging, refined interposer materials, and finer bump pitches are crucial enablers for high-bandwidth, low-energy chiplet integration. This strategic shift is becoming indispensable for architecting future high-performance computing systems.

Background

With the deceleration of Moore's Law and the escalating demands of data-intensive applications like AI and High-Performance Computing (HPC), the semiconductor industry is actively seeking new scaling strategies. Chiplets, an approach where multiple smaller functional blocks are manufactured independently and then integrated into a single package using advanced packaging technologies, are widely recognized as one of the most promising solutions to this challenge. This strategy is already actively adopted by major players such as Intel (e.g., Meteor Lake with Foveros), AMD (e.g., Ryzen/EPYC with Zen chiplets), and NVIDIA (e.g., Hopper/Blackwell via CoWoS for GPU-HBM integration). However, the shift to chiplet designs entails new challenges in design, testing, and packaging, necessitating ecosystem-wide collaboration. Research institutions like Imec play a vital role in supporting the industry by providing foundational technologies and insights to facilitate this transition.

Key Findings

Imec has published an article analyzing the juncture at which it becomes economically and technically sensible to transition from monolithic Application-Specific Integrated Circuits (ASICs) to chiplet-based designs, particularly for AI, HPC, and data center applications. The analysis highlights that as silicon area approaches reticle size limits, advanced packaging technologies, coupled with improved interposer materials and finer bump pitches, are key to enabling high bandwidth and low energy transmission for chiplet integration.

Imec's article examines the thresholds that make this transition a rational decision, primarily through the following technical factors:

- **Silicon Area Limits:** As large monolithic ASICs approach the reticle size limit of photomasks (approximately 26mm x 33mm), manufacturing yields decrease sharply, making production costs prohibitive.
- **Interposer Technology:** High-performance interconnect platforms, such as silicon or organic interposers, are necessary for efficient connection of multiple chiplets. Improved materials contribute to reduced signal loss and enhanced thermal management.

- **Fine Bump Pitch:** To increase the connection density between chiplets, fine bump pitch technologies, such as microbumps or hybrid bonding, are essential. This enables high-bandwidth and low-energy data transmission.
- **System-Level Optimization:** Chiplets allow for the combination of IP blocks manufactured at their respective optimal process nodes, improving overall system performance while controlling costs.

These technical advancements establish the practicality and advantages of chiplet designs.

Chiplet-based designs are expected to become mainstream in AI and HPC systems within the next few years. Imec's research reinforces the technical and economic rationale for this trend, offering guidance for the industry to build next-generation systems more efficiently and innovatively. Continuous advancements in advanced packaging and substrate technologies will maximize the potential of chiplets, supporting the further evolution of AI technology and the expansion of its application domains. This is expected to accelerate a paradigm shift in semiconductor design and foster the emergence of new computing architectures.

Source: https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQGUfnEtn8ozr01r6TH9czp1RVEG-f9oSJGJfD1ZkySm6Fqx4hYfSgr9NhvVWp7YqwY4Kcs6uRiQK4mSDEJLXuo-YvLy3OraGCiOVbXfsXlnWYuwAMcTEYatZbsW1QebN0-fGwIGUI-PatnudECQ04XC82UtqCqI90XCeOe8-wjxpg_-s6NRYZlx11gSW9XMfGZnffVFEyZlxXLX9FaTMhIOGA==

#16 ASML, TSMC, and Imec Achieve Breakthrough 300mm Integration for Industry-Ready 2D-Material Transistors

Published June 21, 2026 The cleanroom Portal - Reinraum Online Germany



OVERVIEW

Imec, in collaboration with ASML and TSMC, presented a robust and scalable 300mm integration approach for n- and p-FETs based on 2D materials at the IEEE/JSAP Symposium 2026. This breakthrough brings industry-ready 2D-material transistors closer to reality, strengthening the fundamental semiconductor technology facing scaling limits. It represents a significant front-end process advancement that will impact future advanced packaging.

Key Findings

Imec, in close collaboration with ASML and TSMC, unveiled a robust and scalable 300mm integration approach for n-type and p-type Field-Effect Transistors (FETs) based on 2D materials at the IEEE/JSAP Symposium 2026. This groundbreaking achievement marks a significant step towards making 2D-material transistors viable for industrial applications, crucial for unlocking the next frontier in semiconductor scaling.

Technical Details

2D materials (e.g., transition metal dichalcogenides like MoS₂ and WSe₂) possess extremely thin atomic layer structures, offering the potential for superior performance efficiency and lower power consumption than conventional silicon-based transistors by suppressing short-channel effects and providing excellent gate control. However, uniformly and reproducibly integrating these materials on large 300mm wafers has been a long-standing challenge. Imec and its partners have overcome the following key technical hurdles:

- **Uniform Material Growth:** Developed a process for uniformly growing large-area, high-purity 2D material films on 300mm wafers.
- **Interface Quality Optimization:** Minimized interface defects between the gate dielectric and 2D materials, improving transistor electrical characteristics.
- **N-type and P-type FET Integration:** Established methods for efficiently integrating both n-type and p-type FETs, essential for building logic circuits, on the same platform.
- **Scalable Process:** Ensured compatibility with the 300mm wafer process, the semiconductor industry standard, paving the way for future mass production.

This integrated approach is an indispensable step in translating the theoretical advantages of 2D-material transistors into practical semiconductor devices.

Background & Context

The semiconductor industry faces physical limits to Moore's Law and is actively exploring new materials and device architectures. 2D-material transistors are garnering significant attention as next-generation scaling technology due to their potential to maintain performance even when channel lengths shrink to a few nanometers or less. However, scaling up laboratory-level achievements to an industrially viable level required solving complex challenges in material synthesis, process integration, and device design. The collaboration between core semiconductor ecosystem players—ASML, TSMC, and Imec—has accelerated the bridge from R&D to practical application, leading to a significant leap forward in this area of technological innovation.

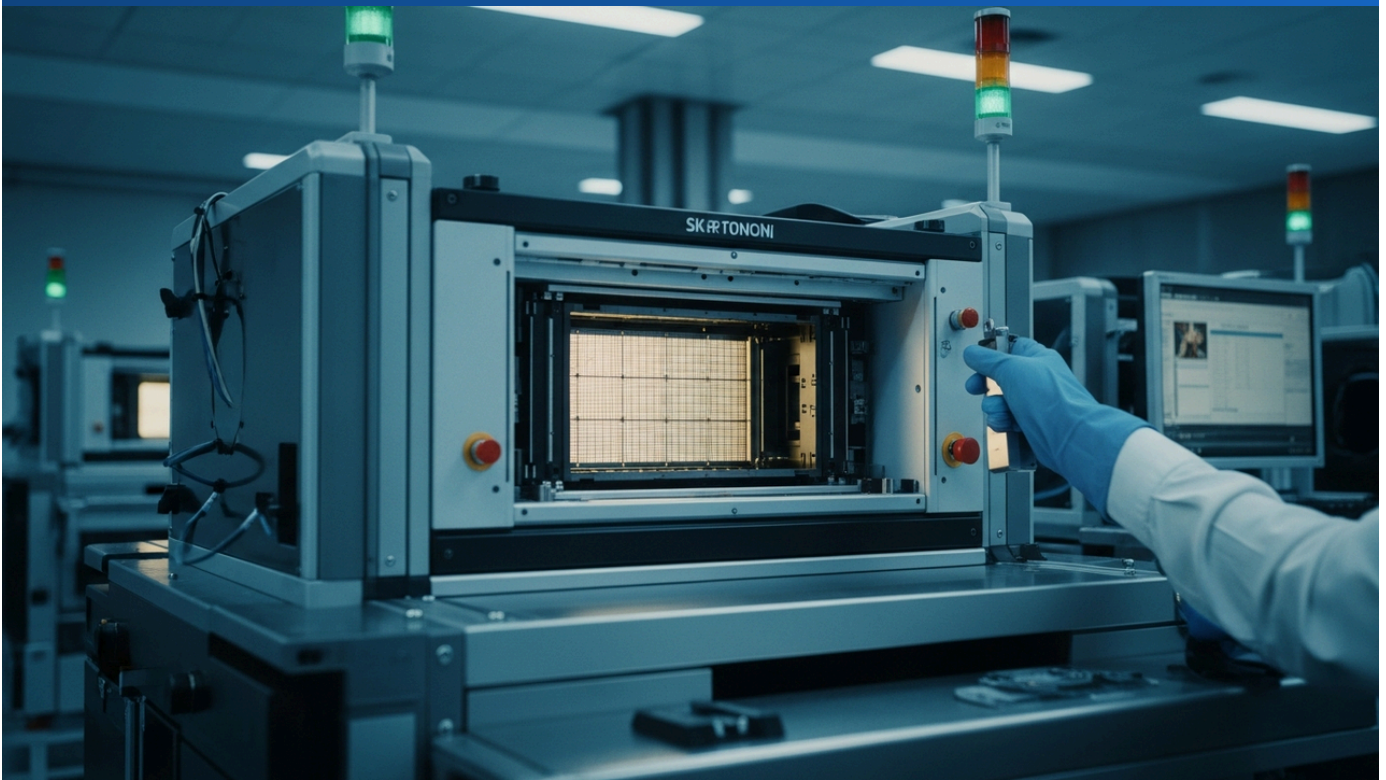
Strategic Significance & Outlook

This 300mm integration breakthrough has the potential to dramatically accelerate the commercialization of 2D-material transistors. This promises further performance improvements and energy efficiency gains in future microprocessors and memory devices. Moreover, this advancement in foundational front-end technology is closely related to the evolution of advanced packaging techniques like chiplet integration and 3D stacking. By providing new device layers that enable high-density integration, it will significantly impact the overall semiconductor industry roadmap. 2D materials are expected to open new avenues for boosting the performance of a wide range of applications, including AI, HPC, and mobile devices.

Source: <https://www.reinraum.de/en/news/asml-tsmc-and-imec-make-industrial-grade-transistors-from-2d-materials-more-tangible-through-groundbreaking-300-mm-integration.html>

#17 Hanmi Semiconductor Secures ₩44.2 Billion SK hynix Order for HBM4 TC Bonders, Signaling Robust Advanced Packaging Equipment Market Growth

Published June 20, 2026 HTX South Korea



OVERVIEW

Hanmi Semiconductor has received a significant ₩44.2 billion (approx. \$32 million) order from SK hynix for its TC Bonder 4.5 Griffin, crucial for next-generation HBM4 production, with delivery slated for early September 2026. This order underscores the surging demand for advanced packaging equipment, specifically Thermal Compression Bonders (TCB), driven by HBM stacking and AI chiplet integration. The broader market reflects this trend, with BESI reporting a 104.5% year-over-year surge in Q1 2026 orders to €269.7 million, and ASMPT also securing repeat orders for AI chip-focused TCB solutions, as the industry invests heavily in advanced logic, memory, and packaging for AI.

Key Findings

Hanmi Semiconductor has secured a substantial order from SK hynix, valued at ₩44.2 billion (approximately \$32 million), for its TC Bonder 4.5 Griffin systems. These advanced thermal compression bonders are essential for the production of SK hynix's next-generation HBM4 (High Bandwidth Memory), with deliveries expected to commence in early September 2026. This landmark deal highlights the intensified investment in advanced packaging, particularly as the semiconductor industry pivots towards meeting the escalating demands of artificial intelligence workloads.

Technical / Clinical Details

The TC Bonder 4.5 Griffin is a critical piece of equipment in the advanced packaging process, specifically for stacking multiple semiconductor dies with extreme precision. In HBM manufacturing, where numerous DRAM layers are vertically integrated, accurate bonding is paramount for achieving high performance and reliability. Hanmi's technology addresses the finer pitch and stringent alignment requirements of HBM4, ensuring robust electrical connections and improved thermal dissipation within the stacked memory modules.

Beyond Hanmi's specific win, the broader advanced packaging equipment market is experiencing robust growth. BE Semiconductor Industries (BSI) reported a remarkable 104.5% year-over-year increase in Q1 2026 orders, totaling €269.7 million. This surge is primarily attributed to the accelerating adoption of hybrid bonding for 2.5D AI-related data center and photonics applications. Similarly, ASMPT is seeing repeat orders for its Chip-to-Substrate (C2S) and Chip-to-Wafer (C2W) TCB solutions, crucial for AI chips and logic chiplets, respectively. These developments indicate that TCB technology, driven by HBM stacking, AI chip C2S, and logic chiplet C2W applications, is a cornerstone for future high-performance computing architectures.

Background & Context

The relentless demand for AI accelerators and high-performance computing (HPC) has shifted the primary bottleneck from front-end wafer fabrication to back-end packaging. Traditional 2D packaging can no longer accommodate the increasing number of transistors and the complex interconnectivity required. This has catalyzed the rapid adoption of 2.5D and 3D packaging technologies, with HBM being a prime example. The precise stacking of memory dies on a logic base, often via interposers, necessitates advanced bonding techniques like TCB.

Industry forecasts by SEMI predict global semiconductor manufacturing equipment sales to reach \$145 billion in 2026, primarily fueled by investments in advanced logic, memory, and packaging. This substantial growth underscores the strategic importance of the back-end segment in enabling next-generation silicon. The competitive landscape for HBM, with players like SK hynix, Samsung, and Micron vying for market leadership, directly translates into a strong demand for specialized packaging equipment.

Strategic Significance & Outlook

SK hynix's procurement of Hanmi Semiconductor's TC Bonders is a pivotal step towards the mass production of HBM4, which is expected to underpin the next wave of AI and HPC systems. For Hanmi, this order solidifies its position as a critical supplier in the burgeoning HBM ecosystem. The broader trend of escalating TCB and hybrid bonding demand signals a profound transformation in semiconductor manufacturing, where packaging is no longer merely an assembly step but a core technology for performance and power scaling. As chiplet architectures and optical interconnects become more prevalent, the market for advanced packaging equipment will likely continue its upward trajectory, fostering further innovation and investment in this crucial segment of the semiconductor supply chain.

Source: <https://www.htx.com/it-it/news/the-iron-rule-of-chip-equipment-is-being-broken-l97homtL>

#18 Semiconductor Startup Funding Diversifies Beyond AI Accelerators to Interconnects and Packaging; TSMC CoWoS Capacity to Quadruple by EOY 2026

Published June 18, 2026 New Market Pitch Global



OVERVIEW

Semiconductor startups attracted \$8.4 billion in Q1 2026, pushing cumulative funding to \$10.7 billion, with investments diversifying beyond AI accelerators to interconnects, optical I/O, memory, and advanced packaging. This shift highlights the industry's focus on resolving post-scaling bottlenecks in the back-end and integration. Critically, TSMC's CoWoS packaging capacity is projected to expand dramatically from ~35,000 wafers/month by end-2024 to 120,000-140,000 wafers/month by end-2026, signaling a significant easing of AI chip supply constraints.

IN DEPTH

Key Findings

In Q1 2026, semiconductor startups collectively raised a substantial \$8.4 billion across 80 companies, bringing the total accumulated funding to approximately \$10.7 billion. This investment trend reveals a crucial shift: capital is now flowing not just into AI accelerators themselves, but into a broader spectrum of enabling technologies across the semiconductor ecosystem. These include interconnects, optical I/O, memory, advanced packaging, Electronic Design Automation (EDA), power delivery, and cooling solutions, underscoring a holistic approach to next-generation chip development.

Technical / Clinical Details

The diversification of investment reflects a growing industry recognition that traditional transistor scaling (Moore's Law) is facing physical and economic limits. The new bottlenecks for performance, power efficiency, and data throughput are emerging in how chips communicate with each other and are integrated into a system. Advanced packaging technologies, such as 2.5D and 3D stacking, chiplets, and heterogeneous integration, are becoming critical to overcome these challenges. Innovations in optical I/O are particularly gaining traction to handle the massive data volumes and high bandwidth required by AI workloads, moving data at light speed rather than electron speed.

A pivotal development in this context is the projected expansion of TSMC's CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity. Forecasts indicate a dramatic increase from approximately 35,000 wafers per month by the end of 2024 to an estimated 120,000-140,000 wafers per month by the end of 2026. This nearly four-fold expansion is a direct response to the explosive demand for AI chips, particularly from major players like NVIDIA. It signifies a crucial de-bottlenecking in the supply chain for advanced AI chips, which have historically faced constraints due to limited CoWoS capacity.

Background & Context

The increasing complexity and scale of AI models necessitate unprecedented computational power and memory bandwidth. Monolithic chip designs struggle to meet these requirements efficiently, leading to the rise of heterogeneous integration, where specialized chiplets (e.g., compute, memory, I/O) are combined within a single package. This approach demands sophisticated interconnectivity and robust thermal management, making advanced packaging a strategic differentiator in the semiconductor industry.

The global semiconductor landscape is also influenced by geopolitical considerations and the imperative for supply chain resilience. Government incentives and subsidies in various regions are further catalyzing investments in domestic semiconductor capabilities, including R&D for advanced packaging and related technologies. Investors are increasingly looking beyond mere performance metrics of individual chips to the overall system-level efficiency and integration capabilities that these enabling technologies provide.

Strategic Significance & Outlook

The strategic shift in semiconductor funding and TSMC's aggressive CoWoS expansion mark a new era for AI-driven semiconductor innovation. Advanced packaging is no longer just a back-end process; it is a core technology driving power, performance, area, and cost (PPAC) improvements, alongside value and sustainability. The increased availability of advanced packaging capacity, particularly CoWoS, will alleviate supply chain pressures for AI accelerators, accelerating the deployment of next-generation AI infrastructure.

Continued investment in interconnects, optical I/O, and advanced cooling solutions will be vital for unlocking the full potential of chiplet architectures and heterogeneous integration. This trajectory is expected to redefine the semiconductor value chain, creating new opportunities for specialized startups and established players alike, as the industry moves towards more integrated, efficient, and powerful computing systems for the AI era.

#19 ASE Technology Holding、AIチップ需要急増に対応し15の新拠点を含む大規模なパッケージング能力拡張計画、2026年LEAP収益目標を35億ドル以上に上方修正

Published June 24, 2026 Crypto Briefing Taiwan



OVERVIEW

ASE Technology Holding is embarking on a significant global expansion, including 15 new facilities, to address the escalating demand for AI chips. This strategic move, leveraging their LEAP platform and VIPack technology for advanced packaging solutions, has led the company to raise its 2026 LEAP revenue target from \$3.2 billion to over \$3.5 billion, signaling robust confidence in the sustained growth of AI semiconductors and their competitive technological edge.

IN DEPTH

Background

The rapid advancement of generative AI has ignited unprecedented demand for NVIDIA GPUs and other AI accelerators. These sophisticated AI chips necessitate not only enhanced computational power but also tight integration with High Bandwidth Memory (HBM) and advanced thermal dissipation solutions. Such stringent requirements often exceed the capabilities of traditional packaging techniques, elevating advanced packaging technologies like 2.5D/3D packaging and chiplet integration to a critical role within the semiconductor ecosystem.

Outsourced Semiconductor Assembly and Test (OSAT) providers are contributing to semiconductor performance improvements in ways distinct from the foundry miniaturization race, thereby increasing their strategic importance as partners in the AI-era semiconductor supply chain. ASE's latest investment underscores its strong commitment to capturing this market growth opportunity and meeting the global demand for AI chips.

Key Findings

ASE Technology Holding, the world's largest independent semiconductor assembly and test (OSAT) service provider, has unveiled a massive global capacity expansion plan, including the establishment of 15 new facilities, to address the explosive demand for AI chips. This strategic expansion aims to bolster the supply of advanced packaging solutions, spearheaded by the company's proprietary LEAP (Low-cost, Efficient, Advanced Packaging) platform and VIPack technology. Driven by this aggressive investment and a favorable market outlook, ASE has revised its 2026 revenue target from LEAP services upwards from \$3.2 billion to over \$3.5 billion.

ASE Technology Holding has developed a comprehensive portfolio of advanced packaging technologies specifically tailored for AI and High-Performance Computing (HPC) applications. At the core is the LEAP platform, which integrates cost-effective, efficient, and advanced packaging techniques to support customers in developing complex multi-chip modules and heterogeneous integration products. This includes solutions such as 2.5D/3D stacking, chiplet integration, Fan-Out Wafer-Level Packaging (FOWLP), and System-in-Package (SiP).

Furthermore, VIPack technology stands as ASE's proprietary high-density integration platform, positioned to rival solutions like TSMC's CoWoS (Chip-on-Wafer-on-Substrate). It achieves superior interconnect density and enhanced thermal performance—critical attributes for AI chips demanding immense data processing capabilities, low latency, and high integration within confined spaces. ASE's capacity expansion directly translates to scaling up the production of these technologies, ensuring rapid market supply.

ASE Technology Holding's extensive capacity expansion and upward revision of its LEAP revenue target affirm the company's conviction that the AI semiconductor market will continue its robust growth for several years to come. The establishment of new facilities and sustained investment in advanced packaging technologies are poised to further solidify ASE's position as a market leader. This strategic move is expected to alleviate AI chip supply bottlenecks, accelerating the adoption and innovation of AI technologies. For researchers and engineers, this implies greater flexibility in designing higher-performance and more efficient AI systems, while for investors, it highlights the advanced packaging sector as an attractive investment opportunity with continued strong growth and profitability.

Source: <https://cryptobriefing.com/ase-technology-expands-capacity-ai-demand/>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#20 Singapore's Exports Soar to 22-Year High in May 2026, Driven by AI Semiconductor Supply Chain Contributions from Micron's HBM Packaging and UMC's 22nm Production

Published June 21, 2026 FSMOne Singapore



OVERVIEW

Singapore's non-oil domestic exports (NODX) recorded their highest growth in 22 years in May 2026, primarily due to the nation's deep integration into the AI semiconductor supply chain. Micron Technology's HBM advanced packaging facility in Singapore is expected to significantly boost supply from 2027, complementing UMC's 22nm manufacturing facility that commenced mass production in 2026. These investments highlight Singapore's robust semiconductor ecosystem, capitalizing on AI demand across memory, chip fabrication, and advanced packaging to drive economic growth.

Key Findings

Singapore's non-oil domestic exports (NODX) surged to their highest growth rate in 22 years in May 2026, a remarkable achievement largely attributed to the nation's deep integration into the global AI semiconductor supply chain. This surge positions Singapore at the forefront of the AI revolution, with significant contributions anticipated from Micron Technology's HBM advanced packaging facility slated for 2027 supply and United Microelectronics Corporation (UMC)'s 22nm manufacturing facility, which began mass production in 2026. These developments underscore Singapore's multifaceted engagement with AI demand, benefiting from its robust ecosystem in memory chips, chip manufacturing, and advanced packaging.

Technical / Clinical Details

Micron Technology's HBM advanced packaging facility in Singapore is poised to specialize in the sophisticated packaging of HBM memory, which is indispensable for next-generation AI accelerators. Scheduled to begin significant supply in 2027, this facility will play a crucial role in meeting the soaring demand for high-density, high-bandwidth AI memory. HBM leverages 3D packaging technology, vertically stacking multiple DRAM dies connected by Through-Silicon Vias (TSVs), offering exponentially higher data transfer rates and power efficiency compared to conventional memory solutions.

Concurrently, UMC's 22nm manufacturing facility in Singapore, a venture by the Taiwan-headquartered foundry, commenced mass production in 2026. The 22nm process is experiencing robust demand, particularly for diverse applications in IoT, automotive, and AI edge devices, thereby enhancing the versatility and resilience of Singapore's semiconductor ecosystem. These facilities collectively demonstrate Singapore's strengthening capabilities across both front-end (chip fabrication) and back-end (advanced packaging) processes, essential for navigating the complexities of the AI era.

Background & Context

The rapid expansion of the global AI market has generated unprecedented demand for high-performance semiconductors, specifically AI chips and their accompanying memory solutions. Singapore has long established itself as a leading global semiconductor manufacturing hub, characterized by advanced technological infrastructure, a highly skilled workforce, and a resilient supply chain ecosystem. Proactive government policies for investment attraction and a strong focus on research and development have further cemented Singapore's strategic node position within the AI semiconductor supply chain.

The investments by international semiconductor giants like Micron and UMC distinctly illustrate Singapore's comprehensive support for the AI ecosystem's growth, spanning memory chip production, logic chip foundry services, and the most complex advanced packaging technologies. This multi-layered benefit contributes significantly to Singapore's economic resilience and sustained growth trajectory.

Strategic Significance & Outlook

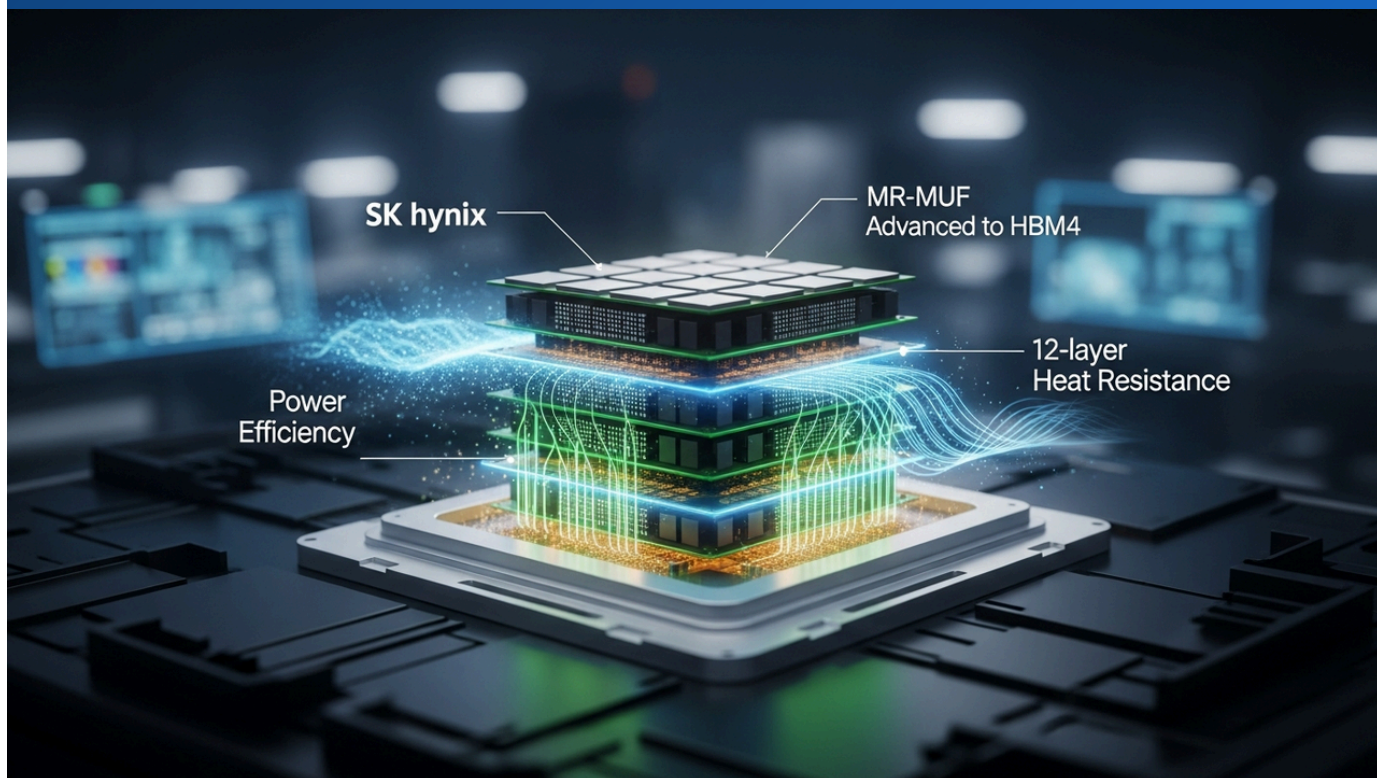
The record-breaking growth in Singapore's NODX, coupled with the strategic investments from Micron and UMC, strongly indicates the nation's pivotal role at the forefront of the AI semiconductor revolution. As Micron's HBM supply scales up from 2027, Singapore's export momentum is expected to accelerate further. This signifies Singapore's ability to combine advanced manufacturing capabilities with technological innovation, thereby enhancing its strategic value in the global high-tech supply chain.

For researchers and engineers, Singapore is emerging as an attractive hub for applied development in cutting-edge memory technologies like HBM and advanced processes such as 22nm. For investors, the country's position as a core location within the AI-driven semiconductor ecosystem promises continued growth and high profitability. Singapore is anticipated to expand its influence as a critical player in the global semiconductor industry in the years to come, solidifying its reputation as a nexus of technological advancement.

Collected: June 26, 2026 | Automated Research System (Gemini API)

#21 SK hynix Ships 12-Layer HBM4E Samples with Advanced MR-MUF Packaging, Achieving Over 20% Power Efficiency and 17% Thermal Resistance Improvement Over HBM4

Published June 22, 2026 Advanced Packaging News South Korea



OVERVIEW

SK hynix announced the sampling of its 12-layer HBM4E memory for next-generation AI systems, leveraging proprietary Advanced MR-MUF packaging. This innovation delivers 48GB capacity per stack and up to 16Gbps data transfer speeds, alongside a significant >20% improvement in power efficiency and 17% enhanced thermal resistance compared to HBM4. The company is currently engaged in customer qualification, planning for future mass production to address escalating AI memory demand.

Key Findings

SK hynix has announced the commencement of sampling for its 12-layer HBM4E (High Bandwidth Memory Extended) designed for next-generation AI systems. This groundbreaking HBM4E leverages the company's proprietary Advanced MR-MUF (Mass Reflow-Molded Underfill) packaging technology to achieve substantial performance enhancements. Specifically, it delivers a massive 48GB capacity per stack and data transfer speeds of up to 16Gbps. Crucially, it boasts over 20% improvement in power efficiency and a 17% enhancement in thermal resistance when compared to its HBM4 predecessor, setting a new benchmark for AI memory performance and reliability.

Technical / Clinical Details

HBM4E is critical for the advancement of AI accelerators and High-Performance Computing (HPC), providing the high data bandwidth and capacity demanded by increasingly complex workloads. The 12-layer vertical stacking of DRAM dies enables the impressive 48GB capacity within a compact footprint. The Advanced MR-MUF packaging technology is a sophisticated process that involves injecting a liquid underfill material after thermal compression bonding, followed by a mass reflow process for uniform curing. This approach enhances the reliability of inter-die connections while creating an efficient thermal dissipation path.

The specific improvements achieved with Advanced MR-MUF in HBM4E include:

- **Over 20% Improved Power Efficiency:** Optimized internal wiring structures and superior thermal management contribute to a significant reduction in overall AI system power consumption.
- **17% Enhanced Thermal Resistance:** The advanced thermal properties of the MR-MUF material and uniform underfill ensure stable operation of the memory chips under high loads, maintaining reliable performance.
- **Up to 16Gbps Data Transfer Speed:** With 16Gbps per pin, HBM4E alleviates data bottlenecks between the CPU/GPU and HBM, maximizing AI processing capabilities.

These characteristics are vital for significantly improving the efficiency and speed of large-scale AI model training and inference.

Background & Context

The rapid evolution of AI technology imposes unprecedented demands on semiconductor memory. The advent of generative AI, in particular, has driven the need for HBM to offer much higher bandwidth and larger capacities when paired with GPUs compared to conventional memory. As a pioneer in HBM technology, SK hynix has consistently led innovations across successive generations, including HBM2, HBM2E, and HBM3. The sampling of HBM4E marks a significant milestone in the HBM roadmap, representing a strategic move to bring next-generation technology to market ahead of competitors.

The Advanced MR-MUF technology is essential for increasing HBM stacking density and enhancing performance, playing a pivotal role in establishing SK hynix's leadership in the HBM market. This technology effectively addresses the critical issues of thermal management and power consumption in HBM, thereby enabling the realization of even higher-performance AI chips.

Strategic Significance & Outlook

SK hynix's sampling of 12-layer HBM4E is set to profoundly impact next-generation AI system development. Once HBM4E enters mass production following customer qualification, AI accelerators will gain access to even greater processing power and efficiency. This will facilitate the execution of larger and more complex AI models, accelerating the evolution of AI applications in sectors such as autonomous driving, high-performance computing, and data centers.

For researchers and engineers, the introduction of HBM4E opens new possibilities for designing novel architectures and realizing more ambitious AI projects that were previously unattainable. For investors, it serves as a strong signal that SK hynix maintains technological leadership in the AI memory market and is well-positioned to capture future growth opportunities. HBM4E is unequivocally set to increase its prominence as a primary driver of performance improvement in the AI-driven semiconductor industry.

Source: https://advancedpackaging.news/article/124523/SK_hynix_ships_HBM4E_samples

#22 TSMC and Amkor Technology Forge 10-Year Strategic Partnership to Expand Advanced Chip Packaging Capabilities in the US

Published June 18, 2026 Focus Taiwan USA



OVERVIEW

TSMC and Amkor Technology have entered a 10-year strategic agreement to significantly bolster advanced semiconductor packaging and test capacity in the United States. This partnership aims to expand advanced packaging capabilities, including the crucial CoWoS technology widely used in AI applications, in conjunction with TSMC's fabs under construction in Arizona. The collaboration supports the escalating demand for AI and HPC technologies while contributing to the US national objective of establishing a more resilient, domestically sourced chip manufacturing ecosystem.

IN DEPTH

Key Findings

Taiwan Semiconductor Manufacturing Company (TSMC), the world's largest dedicated independent semiconductor foundry, and Amkor Technology, a leading independent outsourced semiconductor assembly and test (OSAT) provider, have signed a 10-year strategic partnership agreement. This landmark deal is aimed at substantially enhancing advanced semiconductor packaging and test capabilities within the United States. The collaboration will specifically focus on expanding advanced packaging solutions, including the critical CoWoS (Chip-on-Wafer-on-Substrate) technology widely utilized in AI and High-Performance Computing (HPC) applications, in alignment with TSMC's state-of-the-art fabs being built in Arizona.

Technical / Clinical Details

CoWoS is a revolutionary 2.5D/3D packaging technology developed by TSMC, which integrates multiple semiconductor dies (e.g., high-performance CPUs/GPUs and HBM memory) onto a silicon interposer, which is then mounted onto a package substrate. This method dramatically shortens the interconnect distance between dies, leading to a significant increase in data transfer bandwidth and improved power efficiency. As the computational power and data throughput demands of AI chips grow exponentially, CoWoS stands as one of the most critical advanced packaging technologies, offering performance and integration levels unachievable with conventional 2D packaging.

Amkor Technology, as a leader in the OSAT industry, brings extensive experience and expertise in the high-volume production of complex advanced packaging solutions like CoWoS. Under this partnership, Amkor is expected to build or expand state-of-the-art packaging facilities in Arizona to handle the back-end processing of wafers manufactured by TSMC. This integrated approach will strengthen a domestic supply chain where chip manufacturing, packaging, and testing are completed within the US, thereby enhancing the stability and security of AI chip supply.

Background & Context

In recent years, rising geopolitical risks and concerns over supply chain vulnerabilities have driven the US to prioritize the strengthening of its domestic semiconductor manufacturing capabilities as a national strategic imperative. Policies such as the CHIPS Act have incentivized major semiconductor companies, including TSMC, to accelerate their investments in the United States. However, advanced semiconductor manufacturing requires not only front-end wafer fabrication but also sophisticated back-end packaging capabilities. Historically, a significant portion of advanced packaging has been concentrated in Asia, which has created a potential bottleneck in the US semiconductor supply chain.

The 10-year partnership between TSMC and Amkor is a crucial step toward alleviating this bottleneck and establishing a comprehensive advanced semiconductor ecosystem in the US. The growth of AI and HPC, in particular, is driving demand for highly integrated chip solutions, making the securing of domestic advanced packaging capacity vital for maintaining US technological leadership.

Strategic Significance & Outlook

This strategic alliance between TSMC and Amkor Technology holds historical significance for the US semiconductor industry. The expansion of advanced packaging capabilities in Arizona will accelerate the production of chips for AI and HPC, further bolstering US competitiveness in these critical sectors. This agreement serves as a model for building long-term supply chain resilience and may encourage similar domestic investments from other semiconductor companies.

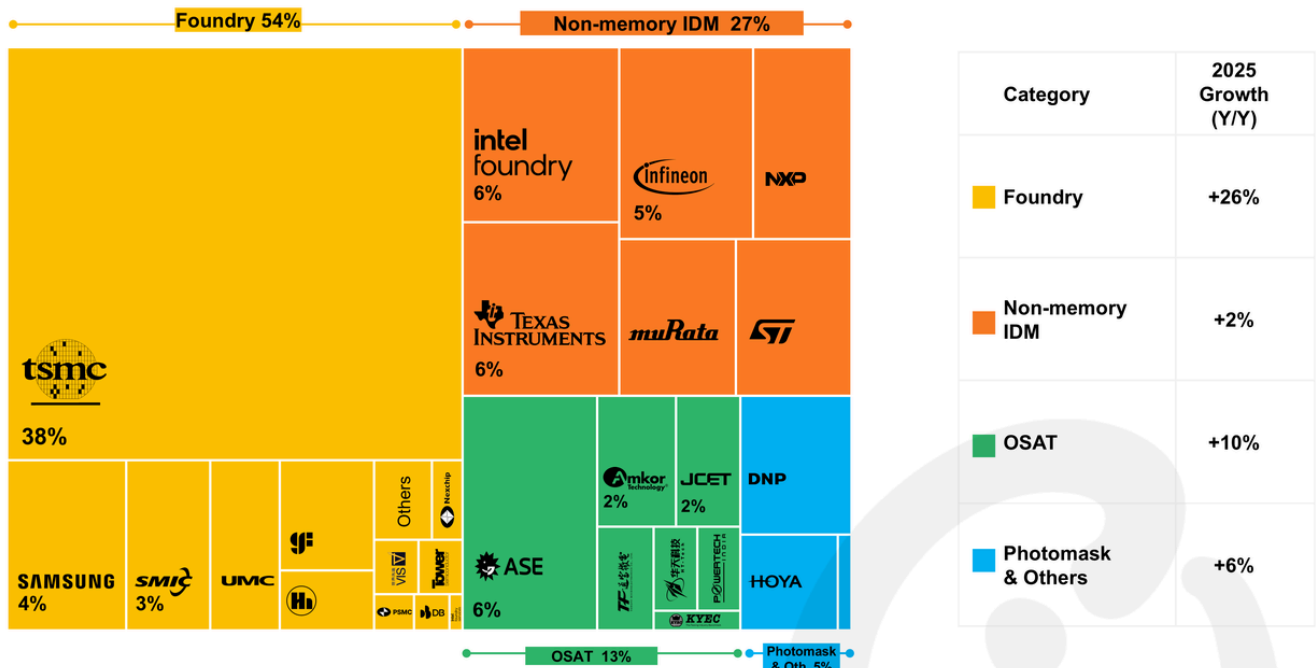
For researchers and engineers, it opens new opportunities to engage in cutting-edge packaging technology development and mass production within the United States. For investors, the geographical diversification of the semiconductor manufacturing ecosystem and the increasing demand for advanced packaging suggest sustainable growth drivers for companies like TSMC and Amkor, enhancing their long-term investment value. This partnership will play a pivotal role in constructing the semiconductor infrastructure that underpins the next generation of AI technologies.

Collected: June 26, 2026 | Automated Research System (Gemini API)

#23 OSAT Vendors Report Strong Q1 2026 Revenue Growth Driven by AI-Related Advanced Packaging Demand: ASE Up 18%, Amkor Up 25%

Published June 26, 2026 Counterpoint Research Global

Foundry 2.0 Market Revenue Share, 2025



OVERVIEW

The Outsourced Semiconductor Assembly and Test (OSAT) sector recorded robust revenue growth in Q1 2026, fueled by surging AI-driven advanced packaging demand. ASE Technology Holding reported an 18% year-over-year revenue increase, raising its 2026 LEAP advanced packaging revenue target to over \$3.5 billion. Amkor Technology also saw a 25% revenue jump, supported by high utilization rates in its advanced packaging lines. Both companies highlighted increased customer capacity commitments amid easing CoWoS supply constraints, underscoring OSAT's growing strategic importance in the AI semiconductor supply chain.

Key Findings

In the first quarter of 2026, the Outsourced Semiconductor Assembly and Test (OSAT) sector demonstrated strong revenue growth, significantly propelled by the escalating demand for advanced packaging, primarily driven by artificial intelligence (AI) advancements. ASE Technology Holding, the world's largest OSAT provider, reported a remarkable 18% year-over-year revenue increase. Capitalizing on this momentum, ASE subsequently revised its 2026 revenue target for its LEAP advanced packaging services upward, from an initial \$3.2 billion to over \$3.5 billion. Similarly, Amkor Technology recorded a substantial 25% year-over-year revenue surge, a performance largely underpinned by the high utilization rates across its advanced packaging lines.

Technical / Clinical Details

The impressive revenue growth witnessed by OSAT vendors is primarily a direct consequence of the increasing demand for sophisticated technologies such as 2.5D/3D packaging, chiplet integration, and HBM (High Bandwidth Memory) stacking. These advanced techniques are indispensable for maximizing the performance of AI processors, as they offer superior interconnect density, enhanced thermal management capabilities, and improved power efficiency. ASE's LEAP platform, which stands for Low-cost, Efficient, Advanced Packaging, provides flexible and highly efficient advanced packaging solutions tailored to meet diverse customer requirements.

Amkor, on the other hand, plays a pivotal role, particularly within the supply chain of TSMC's CoWoS (Chip-on-Wafer-on-Substrate) technology, delivering high-density packaging and testing services. CoWoS, a critical technology, integrates multiple chiplets (logic and memory) onto a silicon interposer, effectively addressing performance bottlenecks in AI accelerators. The emphasis by both companies on "easing CoWoS supply constraints" and "increasing customer capacity commitments" indicates that advanced packaging capacities are being expanded, thereby strengthening the supply infrastructure for AI chips.

Background & Context

The proliferation of AI, especially generative AI, has generated an unprecedented demand for high-performance semiconductors. Consequently, the primary bottleneck in semiconductor manufacturing has shifted from traditional front-end scaling (wafer fabrication) to back-end chip integration and packaging. OSAT companies are central to resolving this new bottleneck, working in close collaboration with foundry partners to deliver state-of-the-art AI chip solutions to the market.

The robust financial performance of ASE and Amkor unequivocally highlights the unprecedented strategic value of back-end processes in the semiconductor industry. This trend reflects the evolving landscape of semiconductor manufacturing, moving away from conventional vertically integrated models towards an era of heterogeneous integration, where specialized OSAT providers play a crucial role in driving innovation and accelerating time-to-market.

Strategic Significance & Outlook

The sustained revenue growth of OSAT vendors and the aggressive strategies adopted by ASE and Amkor clearly demonstrate the ongoing expansion of the AI semiconductor market and the central role of advanced packaging technologies in fueling this growth. Moving forward, as AI applications diversify and performance demands intensify, the need for more complex and innovative packaging solutions will undoubtedly escalate. OSAT companies are thus compelled to engage in continuous research and development and make significant capital investments to maintain their technological leadership.

For researchers and engineers, this presents increasing opportunities to work at the forefront of advanced packaging technologies, driving the importance of new integration methods and materials development. For investors, the OSAT sector represents an attractive investment opportunity with high growth potential, being an indispensable component of the semiconductor supply chain in the AI era. This trend is set to reshape the entire structure of the semiconductor industry, fostering new technological innovations and business models.

#24 BE Semiconductor Industries (BESI) Raises Long-Term Revenue Target to €2.2 Billion and Operating Margin Target to 45% Amid Surging Hybrid Bonding Demand

Published June 18, 2026 Bits&Chips Netherlands



OVERVIEW

BE Semiconductor Industries (BESI) has significantly raised its long-term annual revenue target from €1.5-1.9 billion to €1.7-2.2 billion, while also increasing the lower end of its operating margin target from 40% to 45%. This optimistic outlook is fueled by soaring demand for hybrid bonding in 2.5D AI-related data center and photonics applications, as well as new use cases in logic, memory, and Co-packaged optics. BESI views these advanced packaging technologies as indispensable for the semiconductor industry's next growth phase.

Key Findings

BE Semiconductor Industries (BESI) has substantially revised its long-term business outlook, elevating its annual revenue target from the previous range of €1.5-1.9 billion to €1.7-2.2 billion. Concurrently, the lower bound of its operating margin target has also been increased from 40% to 45%. This assertive revision stems from an unprecedented surge in demand, primarily driven by 2.5D packaging for AI applications, photonics integration in data centers, and emerging use cases for hybrid bonding in logic, memory, and Co-packaged optics (CPO). BESI firmly believes these advanced technologies are integral to the semiconductor industry's next phase of growth.

Technical / Clinical Details

Hybrid bonding is a direct die-to-die or die-to-wafer interconnect technology that achieves significantly higher interconnect density and shorter electrical paths compared to conventional wire bonding or flip-chip bonding. This leads to dramatic improvements in data transfer speeds and reductions in power consumption. In the context of 2.5D/3D packaging for AI accelerators and High-Performance Computing (HPC), where multiple chiplets (e.g., logic and HBM) must be integrated with extreme precision, hybrid bonding has emerged as a key enabling technology.

BESI is a leading equipment provider in hybrid bonding technology, with its bonders capable of joining dies with sub-micron level accuracy. This technology is driving demand in several critical areas:

- **2.5D AI-related Data Centers:** Providing high-speed, high-density connections within GPU packages integrating AI chips and HBM memory.
- **Photonics Applications:** Essential for the performance enhancement of silicon photonics chips and their integration with optical I/O components.
- **Advanced Logic and Memory Integration:** Used for high-density inter-chiplet connections as chiplet architectures become more prevalent.
- **Co-packaged Optics (CPO):** Plays a vital role in integrating switching chips and optical transceivers within a single package, enabling ultra-fast data transmission and low power consumption.

These technologies directly contribute to meeting the increasing bandwidth demands and improving the power efficiency of data centers, accelerating the evolution of AI infrastructure.

Background & Context

Facing the slowdown of Moore's Law, the semiconductor industry is increasingly focusing on performance enhancement through packaging innovation, rather than solely through transistor miniaturization. In this 'More than Moore' era, advanced packaging, especially hybrid bonding, is pivotal for the development of the chiplet ecosystem and the realization of heterogeneous integration. The rise of AI further accelerates this trend, as the exponential increase in data center power consumption and data traffic necessitates urgent improvements in semiconductor component integration density and efficiency.

Equipment manufacturers like BESI are at the forefront of this technological shift, with their innovative bonding solutions enabling the fabrication of next-generation semiconductors. BESI's upward revision of its targets clearly indicates the maturation of the hybrid bonding market and the strong growth momentum it imparts to the semiconductor manufacturing equipment market.

Strategic Significance & Outlook

BESI's elevated long-term revenue and operating margin targets validate the establishment of hybrid bonding technology as a sustainable growth engine for the semiconductor industry. As demand for AI, HPC, and data centers continues to accelerate, advanced packaging technologies like hybrid bonding will become even more indispensable. Consequently, BESI is highly likely to maintain high growth and profitability in the foreseeable future.

For researchers and engineers, hybrid bonding technology offers expanded opportunities for novel design freedom and performance improvements. Further miniaturization of chiplets and integration with optical devices will enable the creation of new applications previously unimaginable. For investors, BESI remains an attractive investment target as a company strategically positioned within the semiconductor supply chain, directly benefiting from the AI-driven economy. Hybrid bonding is set to strengthen its role not just as a manufacturing process, but as a foundational technology shaping next-generation semiconductor architectures.

Source: <https://bits-chips.com/article/besi-raises-long-term-targets-on-ai-packaging-and-hybrid-bonding-demand/>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#25 TSMC's CoWoS Capacity Dramatically Expands, Eliminating Supply Constraint for NVIDIA B300 Servers and Cutting Lead Times to 8-16 Weeks

Published June 24, 2026 Contrary Research Taiwan



OVERVIEW

TSMC's CoWoS (Chip-on-Wafer-on-Substrate) packaging capacity has significantly expanded, effectively resolving a major GPU procurement constraint that had persisted for over six months in 2025. As a result, new NVIDIA B300 servers are now available with a reduced lead time of 8-16 weeks and a 10-20% upfront payment. This pivotal development signals a dramatic improvement in the supply of GPU servers, the most expensive component of AI infrastructure, accelerating AI computing deployment and impacting market dynamics.

IN DEPTH

Key Findings

Taiwan Semiconductor Manufacturing Company (TSMC), the world's leading semiconductor foundry, has substantially expanded its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity. This expansion has effectively resolved a critical supply bottleneck for AI-driven GPUs, which had severely constrained procurement in 2025. As a direct consequence of this breakthrough, the latest NVIDIA B300 servers are now available with a significantly reduced lead time of 8-16 weeks, requiring only a 10-20% upfront payment. This pivotal development removes a major impediment to AI infrastructure deployment, promising to accelerate the growth and accessibility of AI computing capabilities.

Technical / Clinical Details

CoWoS is a sophisticated 2.5D packaging technology that integrates high-performance logic chips (such as GPUs) with multiple High Bandwidth Memory (HBM) dies onto a silicon interposer, which is then mounted onto a package substrate. This technology is paramount for achieving the ultra-high bandwidth and low-latency data transfer essential for AI chips. The production of CoWoS requires specialized, costly equipment and advanced technical expertise, and its limited capacity had previously been a primary constraint on the supply of AI accelerators, including NVIDIA's GPUs.

TSMC's capacity expansion is believed to have been achieved through a combination of new factory construction, optimization of existing lines, and enhanced collaboration with equipment suppliers. This scaling up of production has dramatically increased the output of integrated GPU-HBM packages, thereby accelerating the market availability of cutting-edge AI hardware like the NVIDIA B300 servers. The reduction in GPU procurement lead times from over six months to 8-16 weeks represents a profound advantage for AI development companies, enabling faster innovation cycles and deployment.

Background & Context

The rapid advancement of generative AI technologies has created unprecedented demand for AI accelerators, with GPUs at their core. Throughout 2023 and 2025, NVIDIA's H100 and subsequent generation GPUs were among the most sought-after and supply-constrained products in the market, primarily due to their superior performance and limited manufacturing capacity. The CoWoS packaging bottleneck, in particular, was a significant inhibitor of AI infrastructure investments, causing numerous companies to struggle in scaling up their AI computing capabilities.

TSMC holds an exceptionally strategic position within the AI-era semiconductor supply chain, and its expansion of CoWoS capacity is indispensable for the healthy growth of the entire AI market. The resolution of these supply constraints is expected to improve the cost-efficiency and accessibility of AI chips, enabling a broader range of companies and research institutions to leverage AI technologies. This development could accelerate the investment cycle in AI infrastructure and potentially democratize access to advanced AI computing.

Strategic Significance & Outlook

The dramatic expansion of TSMC's CoWoS packaging capacity marks a decisive turning point in the deployment of AI infrastructure. The shortened lead times for NVIDIA B300 servers mean that cloud service providers, enterprises, and startups can now scale up their AI computing capabilities more rapidly and efficiently. This will undoubtedly accelerate the training and deployment of AI models, fostering further innovation across the spectrum of AI technologies.

For researchers and engineers, easier access to high-performance GPUs will create opportunities to accelerate large-scale AI research and development projects that were previously hampered by resource limitations. For investors, it signals a revitalization of the AI infrastructure investment cycle and a strong indication that the semiconductor industry, particularly the back-end and AI-related hardware markets, is poised for sustained growth. This supply improvement is expected to have widespread positive impacts across the entire AI economy, contributing to the acceleration of next-generation technologies.

Source: <https://research.contrary.com/report/why-20-of-neoclouds-wont-survive-the-ai-boom>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#26 Analog Technologies Delivers Specialized Advanced Packaging for Demanding Defense Systems Requiring Superior Thermal Management and Miniaturization

Published June 21, 2026 Analog Technologies USA

Analog Technologies

Specialized advanced packaging for Defense systems requiring advanced thermal management and miniaturization.

ANTOLOGY NEWS

OVERVIEW

Analog Technologies offers specialized semiconductor packaging and interconnect capabilities for programs demanding advanced thermal management and miniaturized assemblies, particularly in defense systems. Their services, including wire bonding, silver sintering, flip-chip, chip-on-board, and chip-on-flex, support power electronics, sensor platforms, and defense applications. These high-density interconnect solutions enable multi-die and chip-scale assemblies, achieving compact designs for high-frequency and high-reliability environments.

Key Findings

Analog Technologies provides highly specialized semiconductor packaging and interconnect solutions tailored for programs demanding advanced thermal management and extreme miniaturization, particularly within defense systems and high-reliability applications. The company's comprehensive suite of services, encompassing wire bonding, silver sintering, flip-chip, Chip-on-Board (COB), and Chip-on-Flex (COF), enables efficient integration of high-density electronic circuits. This expertise ensures the reliability and durability of high-performance devices operating in harsh environments, a critical advantage for their target markets.

Technical / Clinical Details

The advanced packaging and interconnect capabilities offered by Analog Technologies are custom-engineered solutions optimized for specific application requirements. Key technologies and their benefits include:

- **Wire Bonding:** The most common method of connecting chips to substrates using gold or aluminum wires, offering high flexibility and adaptability to various applications.
- **Silver Sintering:** Provides superior thermal and electrical conductivity, ideal for thermal management in high-power electronics. It withstands higher temperatures than traditional soldering or brazing, significantly improving reliability.
- **Flip-Chip Bonding:** Directly connects the chip to the substrate, shortening interconnect lengths and enhancing electrical performance and signal integrity. This is optimal for high-frequency applications and AI modules requiring high-speed data transfer.
- **Chip-on-Board (COB) and Chip-on-Flex (COF):** Involve mounting bare chips directly onto rigid (COB) or flexible (COF) substrates, dramatically reducing package size and cost. This enables integration into space-constrained applications like sensor platforms and wearable devices.
- **Multi-Die and Chip-Scale Assemblies:** Technologies that integrate multiple chips within a single package, reducing overall system footprint and enhancing performance.

These technologies enable high-efficiency power conversion in power electronics, highly sensitive and compact detection modules in sensor platforms, and robust operation in extreme environments for defense systems.

Background & Context

Modern electronic systems face conflicting demands for miniaturization, high performance, and exceptional reliability. In critical sectors such as defense, aerospace, and medical, devices must endure extreme environmental conditions and possess extended lifespans, while simultaneously integrating complex functionalities into confined spaces. Traditional standard packaging technologies are increasingly challenged to meet these stringent requirements. Consequently, the value of customized advanced packaging solutions, as offered by specialized firms like Analog Technologies, is growing significantly.

With the advancement of AI, edge devices and embedded systems also demand rapid data processing and efficient power management. High-density interconnects and superior thermal management are foundational technologies for realizing these sophisticated systems, bridging the gap between chip-level performance and system-level integration.

Strategic Significance & Outlook

Analog Technologies' specialized advanced packaging services are poised to become increasingly vital in demanding application sectors. The modernization of defense systems, the proliferation of IoT devices, and the continued evolution of AI will persistently drive demand for packaging solutions that offer high-density interconnects, excellent thermal management, and ultra-miniaturization.

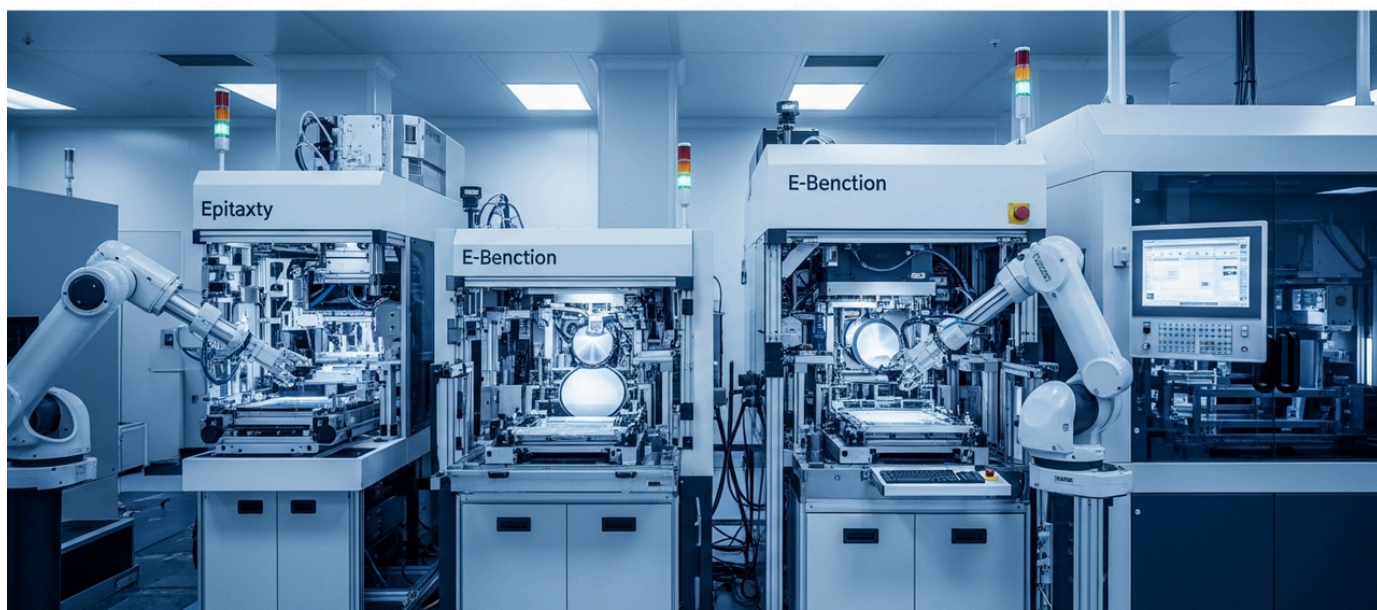
For researchers and engineers, these technologies expand the possibilities for designing new functional devices and systems, proving key in the pursuit of performance and reliability under extreme conditions. For investors, Analog Technologies' specialization in a niche yet high-value segment of the semiconductor packaging market presents an attractive proposition for stable growth and profitability. The company is expected to continue contributing to the realization of future high-performance electronic devices through its custom solutions.

Source: <https://analog-tech.com/services/advanced-packaging-interconnects/>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#27 Applied Materials Unveils New Systems for DRAM and Advanced Packaging to Accelerate AI Chip Manufacturing, Featuring Epitaxy, CMP, and E-beam Inspection Technologies

Published June 25, 2026 Barchart.com USA



OVERVIEW

Applied Materials has introduced a suite of new chipmaking systems designed to accelerate the construction of advanced 3D chip architectures powering next-generation AI. This includes epitaxy systems optimizing DRAM production and Chemical Mechanical Planarization (CMP), deposition, and e-beam inspection systems for advanced packaging. Notably, the new SEMVision™ G7AP enables high-resolution defect review and automated classification across silicon, organic, and glass substrates, drastically accelerating yield learning for advanced packaging. These innovations provide essential advancements for improving AI chip performance, reliability, and manufacturing efficiency.

Key Findings

Applied Materials has unveiled a comprehensive suite of new chip manufacturing systems aimed at accelerating the construction of cutting-edge 3D chip architectures essential for powering next-generation AI applications. This robust portfolio includes advanced epitaxy systems optimized for DRAM production, alongside Chemical Mechanical Planarization (CMP), deposition, and innovative e-beam inspection systems specifically designed to enhance quality and yield in advanced packaging processes. A standout innovation is the SEMVision™ G7AP, which offers high-resolution defect review and automated classification across silicon, organic, and glass substrates, promising to dramatically expedite the yield learning process in advanced packaging.

Technical / Clinical Details

The new systems introduced by Applied Materials are engineered to address critical bottlenecks in semiconductor manufacturing and meet the complex requirements of AI chips:

- **Epitaxy Systems for DRAM:** DRAM, crucial for high-speed, high-capacity HBM (High Bandwidth Memory), demands intricate structures and precise film thickness control. The new epitaxy systems optimize DRAM performance and yield by meeting these stringent requirements, vital for maximizing the memory bandwidth of AI chips.
- **CMP Systems for Advanced Packaging:** In chiplet and 3D stacking technologies, ultra-high surface planarity of wafers is indispensable for accurate die bonding. The new CMP systems enhance material removal uniformity and surface quality, enabling next-generation packaging technologies like hybrid bonding.
- **Deposition Systems:** High-quality, uniform thin film formation is critical for insulation and interconnects between layers in advanced packaging. Applied Materials' new deposition technologies meet these demands, ensuring signal integrity and reliable interconnectivity.

- **SEMVision™ G7AP E-beam Inspection System:** In advanced packaging, even microscopic defects on wafers and substrates can significantly impact the reliability of the final product. The SEMVision™ G7AP leverages high-resolution e-beam technology to rapidly and accurately detect and classify defects across a wide range of substrates, including silicon, organic (RDL), and glass. This capability enables early identification of root causes for defects, allowing for rapid optimization of manufacturing processes and dramatically shortening the yield learning cycle for AI chip production.

Background & Context

The increasing complexity and scale of AI models are revolutionizing semiconductor chip architectures. Facing the physical limits of traditional 2D scaling, the industry is shifting towards advanced packaging technologies such as 3D stacking, chiplets, and heterogeneous integration. These technologies are essential for improving data transfer rates, enhancing power efficiency, and achieving high performance within limited space. Leading semiconductor manufacturing equipment companies like Applied Materials play a central role in enabling this technological shift. The announcement of these new systems by Applied Materials clearly signifies an acceleration of innovation in AI-era semiconductor manufacturing.

Strategic Significance & Outlook

The new systems for DRAM and advanced packaging introduced by Applied Materials are critically important for resolving bottlenecks in AI chip manufacturing and accelerating the commercialization of next-generation AI technologies. Specifically, advanced inspection technologies like SEMVision™ G7AP are indispensable for improving yield and ensuring reliability in complex 3D packaging, contributing significantly to the mass production and cost efficiency of AI chips.

For researchers and engineers, these new tools provide the means to push the boundaries of DRAM design and explore more innovative packaging architectures. For investors, it is a strong signal that the growth of the AI market directly benefits the semiconductor manufacturing equipment sector, with technology leaders like Applied Materials poised for sustained growth. These technological innovations are set to enhance the performance and cost-efficiency of AI chips, further accelerating the adoption and integration of AI technology into society.

Source: <https://www.barchart.com/story/news/2648655/applied-materials-introduces-new-systems-to-accelerate-dram-and-advanced-packaging-for-ai-chips>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#28 ATLANT 3D, A*STAR IMRE, and NAMIC Establish AI-Driven Materials Discovery Hub in Singapore to Accelerate Semiconductor and Advanced Packaging Innovation

Published June 24, 2026 Yahoo Finance Singapore



OVERVIEW

ATLANT 3D, A*STAR Institute of Materials Research and Engineering (IMRE), and National Additive Manufacturing Innovation Cluster (NAMIC) have signed an MOU to establish an Advanced Materials Development Hub (A-HUB) in Singapore. This strategic partnership combines ATLANT 3D's proprietary Direct Atomic Layer Processing (DALP®) technology with A*STAR IMRE's materials science expertise to accelerate AI-driven materials discovery for semiconductors, silicon photonics, and advanced packaging. A-HUB will support high-throughput materials synthesis, autonomous materials discovery, and expedited technology development, reinforcing Singapore as a global hub for advanced materials research.

Key Findings

ATLANT 3D, the Agency for Science, Technology and Research's Institute of Materials Research and Engineering (A*STAR IMRE), and the National Additive Manufacturing Innovation Cluster (NAMIC) have formalized a Memorandum of Understanding to establish a groundbreaking Advanced Materials Development Hub (A-HUB) in Singapore. This strategic collaboration aims to integrate ATLANT 3D's patented Direct Atomic Layer Processing (DALP®) technology with A*STAR IMRE's extensive materials science expertise. The core objective is to accelerate innovation in crucial sectors such as semiconductors, silicon photonics, and advanced packaging through AI-driven materials discovery approaches.

Technical / Clinical Details

The A-HUB is designed to fundamentally transform traditional materials discovery processes. Conventional trial-and-error methods are time-consuming and costly, whereas AI-driven methodologies combine vast data analysis and simulation to dramatically accelerate the prediction of new material properties and optimization of synthesis conditions. The key technological components of this hub include:

- **Direct Atomic Layer Processing (DALP®):** Developed by ATLANT 3D, this technology enables precise, atomic-layer control over material deposition at the nanoscale. This capability facilitates the creation of extremely thin, uniform films and complex 3D structures, contributing to enhanced semiconductor device performance, optimized optical components in silicon photonics, and high-density interconnects in advanced packaging.
- **AI-Driven Materials Discovery Platform:** Utilizes machine learning algorithms and data science to analyze relationships between material composition, structure, and properties. This accelerates the identification of novel material candidates that meet specific application requirements and optimizes experimental design, thereby shortening R&D cycles.
- **High-Throughput Materials Synthesis:** Incorporates automated systems and robotics to synthesize and characterize numerous material samples concurrently, speeding up the discovery process.

By integrating these technologies, A-HUB will enable the development of new materials that enhance performance parameters such as power efficiency, data transfer rates, and reliability in semiconductor devices, particularly supporting the evolution of advanced packaging like HBM and chiplets.

Background & Context

The semiconductor industry, confronting the limits of Moore's Law, is increasingly turning to materials science and advanced packaging as new frontiers for performance enhancement. As demand for AI and High-Performance Computing (HPC) accelerates, challenges related to thermal management, electrical performance, and reliability—which existing materials struggle to address—have become prominent. The discovery and development of new materials are thus key to enabling next-generation semiconductor technologies. Singapore, with its advanced research infrastructure and robust ecosystem, actively invests in R&D for advanced manufacturing and materials science, and this partnership is a part of that strategy.

A*STAR IMRE is a global leader in materials research, and NAMIC is an organization dedicated to driving innovation in additive manufacturing. The collaboration with ATLANT 3D brings together the expertise and cutting-edge technologies of these entities, holding the potential to contribute to global problem-solving in the materials domain.

Strategic Significance & Outlook

The establishment of A-HUB in Singapore is set to maximize the potential of AI-driven materials discovery, dramatically accelerating innovation in the semiconductor, silicon photonics, and advanced packaging sectors. Its capabilities in high-throughput material synthesis and autonomous discovery are expected to significantly reduce the lead time for new material development, thereby expediting market introduction.

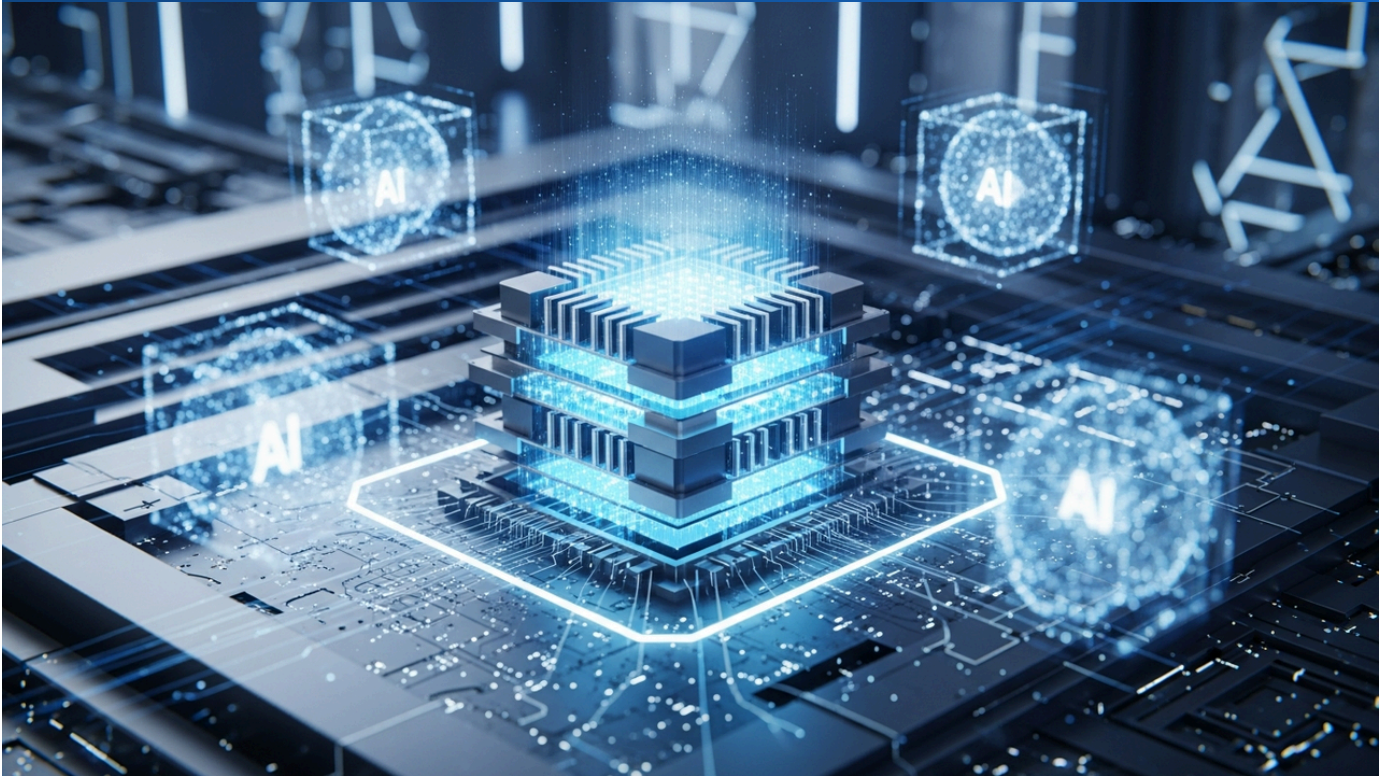
For researchers and engineers, this presents an unparalleled opportunity to engage in cutting-edge R&D at the intersection of atomic layer precision processing and AI-powered materials science. For investors, given that advanced materials technology underpins the growth of the AI-era semiconductor industry, investments in this sector are highly attractive from a long-term perspective. The success of A-HUB will not only establish Singapore as a global hub for advanced materials research but also provide a new model for contributing to technological innovation in the global semiconductor industry.

Source: <https://sg.finance.yahoo.com/news/atlant-3d-star-imre-namic-073000539.html>

Collected: June 26, 2026 | Automated Research System (Gemini API)

#29 HBM4E Set to Dominate High-Performance Memory Market by Late 2026-2027 with Up to 4.0 TB/s Single-Stack Bandwidth and 48GB+ Capacity, Accelerating AI Models

Published June 18, 2026 Ersa Electronics Global



OVERVIEW

HBM4E is projected to lead the high-performance memory market from late 2026 to 2027, offering a single-stack bandwidth of up to 3.6–4.0 TB/s and capacities exceeding 48GB, significantly boosting ultra-large AI model training efficiency. Samsung began HBM4E sampling in May 2026, SK hynix in June 2026, and Micron plans mass production by 2027. Achieving HBM4E's performance, including a ~17% reduction in thermal resistance and >20% improvement in energy efficiency, necessitates new packaging technologies like SK hynix's Advanced MR-MUF process.

Key Findings

High Bandwidth Memory Extended (HBM4E) is poised to dominate the high-performance memory market from late 2026 into 2027, driven by its groundbreaking capabilities. This next-generation HBM is projected to deliver an astounding single-stack bandwidth of up to 3.6–4.0 TB/s and capacities exceeding 48GB, promising a dramatic acceleration in the training efficiency of ultra-large AI models. Major memory manufacturers are already in motion, with Samsung initiating HBM4E sample shipments in May 2026, followed by SK hynix in June 2026, and Micron targeting mass production by 2027.

Technical / Clinical Details

HBM4E is meticulously engineered to address the critical data bottlenecks in AI accelerators and High-Performance Computing (HPC). Its core technical features and requirements include:

- **Ultra-High Bandwidth:** A single-stack bandwidth of 3.6–4.0 TB/s represents a revolutionary leap, significantly enhancing data delivery capacity to processors like GPUs. This directly translates to reduced AI model training times and improved responsiveness for real-time inference, marking a substantial performance uplift from HBM3E.
- **Large Capacity:** With capacities exceeding 48GB, HBM4E enables the processing of larger AI models directly within the HBM, minimizing data movement between DRAM and the processor and boosting overall system efficiency.
- **Advanced Packaging Technologies:** The manufacturing of HBM4E, involving the vertical stacking of numerous DRAM dies, necessitates extremely precise 3D packaging technologies. Innovative packaging solutions, such as SK hynix's Advanced MR-MUF (Mass Reflow-Molded Underfill) process, play a crucial role. These technologies are required to achieve approximately a 17% reduction in thermal resistance and over a 20% improvement in energy efficiency. This is vital for overcoming the heat generation challenges inherent in densely integrated memory stacks and maintaining high reliability.

- **Low Power Consumption:** Alongside performance enhancement, minimizing power consumption in data centers and edge devices is a strong imperative. HBM4E is designed with efficient internal architectures and thermal management to maximize performance per watt.

These technological advancements are set to unleash the full potential of AI chips, elevating AI-era computing capabilities to unprecedented levels.

Background & Context

The exponential growth in the number of parameters and complexity of AI models, particularly generative AI, has imposed unprecedented demands on semiconductor memory. HBM has emerged as a primary solution to this challenge, offering high bandwidth and low latency due to its physical proximity to GPUs and AI accelerators. The three leading memory manufacturers—Samsung, SK hynix, and Micron—are locked in fierce competition for leadership in the HBM market, with HBM4E representing the next major product on their roadmaps.

The evolution of HBM is inextricably linked to advancements in back-end semiconductor processes, especially advanced packaging technologies. Achieving higher stack counts and greater bandwidth necessitates innovations in thermal compression bonding, underfill materials, and sophisticated thermal management solutions. HBM4E will serve as a litmus test for how mature these technologies have become and their ability to contribute to next-generation AI infrastructure.

Strategic Significance & Outlook

The introduction of HBM4E will have a profound impact on the AI and high-performance computing sectors. Its anticipated market entry from late 2026 to 2027 will push the boundaries of AI model scale and complexity further, accelerating the development of data-intensive applications such as autonomous driving, drug discovery, and climate change modeling. A single-stack bandwidth of 4.0 TB/s and capacities exceeding 48GB open new avenues for researchers to conduct computations previously deemed impossible and for engineers to design more ambitious AI systems.

Researchers and engineers will focus on developing new algorithms and architectures to fully leverage the immense data processing capabilities offered by HBM4E. For investors, HBM4E is set to become a major growth driver in the high-performance memory market during the AI era, expanding investment opportunities in related memory manufacturers and advanced packaging technology providers. HBM4E is a key technology that will further deepen the impact of AI on our society and technology.

Source: <https://www.ersaelectronics.com/blog/hbm4-hbm4e>

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#30 SK hynix's Early Strategic Investment in AI and HBM Drives Market Value Lead Over Samsung, Bolstering Production Capacity for NVIDIA Demand

Published June 24, 2026 Reuters South Korea



OVERVIEW

SK hynix's early and aggressive investment in HBM (High Bandwidth Memory) technology and significant capacity expansion, anticipating future NVIDIA demand, has allowed it to differentiate from Samsung Electronics and gain a market value lead. Following a record operating loss in 2023, the company achieved a dramatic turnaround in 2024, driven by strong AI memory chip demand. While SK hynix manufactures key HBM components in-house, it relies on TSMC for base die production, a hybrid model crucial to its market dominance.

Key Findings

SK hynix has achieved a significant lead in market value over its rival, Samsung Electronics, attributed to its proactive and early strategic investments in High Bandwidth Memory (HBM) technology for the AI and High-Performance Computing (HPC) markets. The company accurately anticipated future demand from NVIDIA, making a decisive move to substantially expand its HBM production capacity. This strategic foresight proved pivotal, driving a dramatic recovery in financial performance in 2024, after the company experienced a record operating loss in 2023, largely propelled by the explosive demand for AI memory chips.

Technical / Clinical Details

HBM is a cutting-edge 3D packaging technology where multiple DRAM dies are vertically stacked and directly connected to a processor via Through-Silicon Vias (TSVs). This architecture enables significantly higher data bandwidth and superior power efficiency compared to conventional DDR memory. AI accelerators, particularly NVIDIA's GPUs, depend on HBM as an indispensable component for processing vast amounts of data at high speeds. SK hynix has been at the forefront of HBM technology, consistently advancing performance and integration with each generation, from HBM2 to HBM2E and HBM3.

SK hynix's production strategy employs a hybrid model: it vertically integrates the manufacturing of certain key HBM components within its own foundry division while outsourcing the production of critical base dies to Taiwan Semiconductor Manufacturing Company (TSMC). This model allows SK hynix to focus its expertise on HBM design and advanced packaging technologies, leveraging TSMC's state-of-the-art manufacturing processes to achieve rapid development and high-volume production. The collaboration with TSMC is especially crucial for next-generation technologies like HBM4, where the performance and interface of the base die are determinant factors for the entire HBM stack's performance.

Background & Context

The year 2023 saw a widespread downturn in the semiconductor industry, with the memory market, in particular, suffering from oversupply and declining prices. However, the rapid development of AI technology instigated a dramatic shift in the high-performance memory market from 2024 onwards. SK hynix, perceiving this trend early, made concentrated investments in HBM for AI, positioning itself ahead of competitors to meet demand from key customers like NVIDIA. In contrast, Samsung, while focusing on a broader portfolio of traditional DRAM and NAND flash, is considered to have been slower in its HBM investment decisions compared to SK hynix.

This market dynamic underscores how technological leadership and early investment in specific niche markets can significantly influence a company's overall competitive advantage within the semiconductor industry. Especially in the AI era, supply chain flexibility and strategic partnerships are key to responding swiftly to market changes.

Strategic Significance & Outlook

SK hynix's early and strategic investments in HBM have solidified its leadership in the high-performance memory market during the AI era. Its close collaboration with NVIDIA and partnership with TSMC are expected to further accelerate the development and mass production of next-generation HBM products, such as HBM4E, thereby contributing to enhanced AI accelerator performance. This success serves as a powerful lesson for other semiconductor companies, highlighting the importance of strategic investments aligned with the significant growth opportunities presented by the AI market.

For researchers and engineers, the evolution of HBM technology enables the design of more complex and higher-performing AI architectures, fostering new innovation opportunities. For investors, the expanding AI market provides a clear signal of sustained growth in the semiconductor memory industry, particularly in the HBM segment. SK hynix is expected to continue leading and driving growth in the AI memory market in the foreseeable future.

Collected: June 26, 2026 | Automated Research System (Gemini API)