Semiconductor_BackEnd

Weekly Intelligence Report

2026-07-05 | 22 articles | 7 countries

troy-technical.jp

This Week's Keyword

Advanced Packaging

AI-driven demand fuels capacity expansion

22	7	$64B	$10B
articles	countries	investment	sales
Total Articles Analyzed	Source Countries	SK Hynix AI Memory	Samsung HBM4 (proj.)

All 22 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	EU Funds 3D IC Packaging	Corporate Strategy	●●●○○	●●○○○	●●●●○	●●●○○	●●●●●	EU invests €210M in 3D IC packaging R&D; to boost strategic autonomy and competitiveness.
#02	AMAT New Systems for AI	New Product	●●●●○	●●●●○	●●●●○	●●●●○	●●●●●	Applied Materials launches new systems for DRAM and advanced packaging, boosting HBM for AI chips.
#03	ASE FOPLP Mass Production	Corporate Strategy	●●●○○	●●●●○	●●●●○	●●●●○	●●●●○	ASE to mass produce FOPLP by end-2026, expanding capacity for AI chips to ease bottlenecks.
#04	Intel/TSMC Champion PLP	Market Analysis	●●●○○	●●●○○	●●●●●	●●●○○	●●●●●	Intel and TSMC champion Panel-Level Packaging, projecting tenfold market expansion for AI/HPC chips.
#05	AMAT 'Logic-Class' Pkg	New Process	●●●○○	●●●●○	●●●●○	●●●●○	●●●●●	Applied Materials guides memory makers to logic-class precision in advanced packaging for AI HBM.
#06	ASE Pkg Quotes Up 20%	Market Trend	●○○○○	●●●●●	●●●●○	●●●○○	●●●●○	ASE raises advanced packaging prices over 20% due to surging AI chip demand and capacity crunch.
#07	AI Pkg Bottleneck Shifts	Market Analysis	●●●○○	●●●○○	●●●●○	●●●○○	●●●●●	CoWoS, wafer-scale, and CoWoP are key solutions addressing AI chip packaging bottlenecks.
#08	Lam Research Wafer-to-Panel	New Process	●●●●○	●●●○○	●●●●○	●●●●○	●●●●●	Lam Research expands wafer-to-panel processing for advanced packaging, cutting costs and boosting throughput.
#09	Samsung HBM4 $10B Sales	Market Report	●●●○○	●●●●●	●●●●○	●●●○○	●●●●○	Samsung's HBM4 sales projected to exceed $10B this year, driven by explosive AI demand.
#10	eWeek AI Chip Bottlenecks	Market Analysis	●○○○○	●●●●●	●●●●●	●●○○○	●●●●●	eWeek report highlights advanced packaging as the key solution to critical AI chip bottlenecks.
#11	BOE Glass Substrates	New Material	●●●●○	●●●○○	●●●●○	●●●○○	●●●○○	BOE ships glass substrate samples for advanced chip packaging, boosting China's material tech.
#12	SK Hynix $64B Investment	Corporate Strategy	●●○○○	●●●●○	●●●●●	●●●●○	●●●●○	SK Hynix invests $64B in South Korea for AI memory and advanced packaging capacity expansion.
#13	JCET Pkg Investment	Corporate Strategy	●●○○○	●●●●○	●●●●○	●●●○○	●●●○○	JCET invests heavily in advanced chip packaging, boosting capacity for AI, HPC, and automotive.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#14	Nomura Raises TSMC Target	Market Report	●○○○○	●●●●●	●●●●○	●●●○○	●●●●○	Nomura raises TSMC target price, citing AI infrastructure cycle and CoWoS demand as growth drivers.
#15	Kioxia Next-Gen Memory	Corporate Strategy	●●●○○	●●●●○	●●●●○	●●●○○	●●●○○	Kioxia accelerates next-gen memory mass production, including HBM, for AI boom-driven comeback.
#16	TSMC CoWoS Demand	Market Trend	●○○○○	●●●●●	●●●●●	●●●○○	●●●●●	TSMC's CoWoS packaging equipment supply chain sees robust demand amid AI chip surge.
#17	AMAT 6 New Systems	New Product	●●●●○	●●●●○	●●●●○	●●●●●	●●●●●	Applied Materials unveils six new systems for AI chip DRAM and advanced packaging, with sub-10nm defect detection.
#18	Samsung HBM4/Optical HBM	Corporate Strategy	●●●●○	●●●●○	●●●●●	●●●●○	●●●●○	Samsung dedicates half HBM production to HBM4, targets $10B sales, and plans optical HBM by 2028.
#19	EU Chips Act Funds 3D IC	Corporate Strategy	●●●○○	●●○○○	●●●●○	●●●○○	●●●●●	EU Chips Act funds €210M for 3D IC advanced packaging, benefiting Infineon, ASML sub, and Soitec.
#20	Fraunhofer Laser Grooving	Research	●●●●●	●○○○○	●●●○○	●●●●●	●●●●●	Fraunhofer develops DUV-assisted athermal laser grooving for low-κ dielectrics in advanced packaging.
#21	CXMT HBM Hurdles	Market Analysis	●●○○○	●●●○○	●●●○○	●●●○○	●●●○○	CXMT faces HBM production hurdles; yield and advanced packaging improvements key for 2027-2028.
#22	US CHIPS Act Attracts	Policy Analysis	●○○○○	●●●●●	●●●●●	●●●○○	●●●●●	US CHIPS Act attracts Taiwanese semiconductor suppliers, boosting advanced packaging and materials.

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI chip supply chain exposed to Asian capacity bottlenecks?

The surge in AI demand has led to severe advanced packaging capacity shortages (CoWoS, HBM), with Asian OSATs (ASE, TSMC) and memory makers (Samsung, SK Hynix) dominating. Does your procurement strategy account for potential delays and price hikes, or are you exploring alternative packaging solutions and regional diversification?

❷ Is your packaging roadmap ready for the Panel-Level Packaging (PLP) transition?

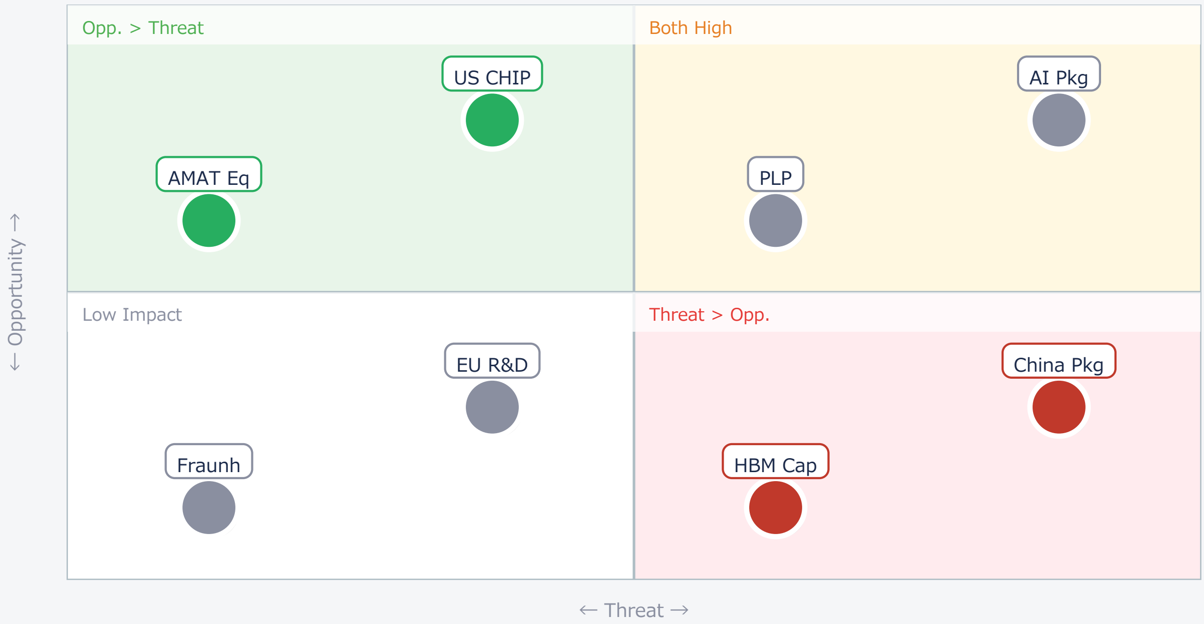
Intel, TSMC, and major equipment suppliers like Lam Research are aggressively pushing PLP for cost and throughput advantages. This shift could redefine packaging economics. Are your R&D; and manufacturing teams evaluating PLP adoption, and are your material/equipment suppliers aligned with this paradigm shift?

❸ How will China's HBM and advanced packaging progress impact global competition?

China's CXMT faces HBM hurdles but aims for 2027-2028 acceleration, while BOE ships glass substrate samples. This indicates a strategic push for indigenous advanced packaging. What is your competitive intelligence on Chinese capabilities, and how will their potential market entry affect your long-term IP and market share strategies?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
● AI Pkg	Critical	High demand/prices	Supply constraint
● PLP	Critical	Cost/thruput	Retooling risk
● US CHIP	Opp.	US supply chain	Higher cost
● AMAT Eq	Opp.	AI chip enabler	Competitor lag
● China Pkg	Threat	Diversify supply	Rising comp.

● HBM Cap	Threat	More HBM	Supply/cost
● EU R&D;	Ref.	EU tech base	Slow progress
● Fraunh	Ref.	New process	Early stage

Deep Dive ① — AMAT's 6 New Systems for AI Packaging

#17 | 2026/06/25 | Applied Materials (プレスリリース) | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●○ Data Reliability●●●●● US/EU Relevance●●●●●

Applied Materials has launched six new systems to accelerate DRAM and advanced packaging for AI chips, addressing critical challenges in HBM, 3D stacking, and chiplet architectures. Innovations span epitaxy, CMP, deposition, and eBeam metrology/defect review.

A standout is the new eBeam defect review system, offering sub-10 nanometer sensitivity. This capability significantly improves process control and yield for complex 3D packaging, boosting AI chip performance and power efficiency by enabling early defect identification.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The sub-10nm defect detection is a critical advancement, and the published specs from Applied Materials are likely realistic given their leadership. Technical barriers remain in scaling these precision tools for high-volume, cost-effective manufacturing across diverse packaging types. [Opportunity] for US/EU OEMs and device manufacturers to leverage these systems for higher-yield, higher-performance AI chips. [Threat] for non-US/EU equipment suppliers who lag in such precision tools, and for chip designers if competitors gain a yield advantage. Next Actions: [R&D;] Evaluate integration of these new AMAT systems into existing or planned advanced packaging lines by end-Q3 2026. [Procurement] Assess the cost-benefit of upgrading current equipment vs. new investments.

Deep Dive ② — AMAT Systems Propel DRAM & AI Packaging

#02 | 2026/06/25 | StockTitan | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●○ Data Reliability●●●●○ US/EU Relevance●●●●●

Applied Materials has unveiled a suite of new systems designed to dramatically enhance DRAM and advanced packaging processes, directly addressing the escalating performance demands of AI chips. These innovations specifically target High Bandwidth Memory (HBM) manufacturing.

The new platforms, including a hybrid bonding solution, enable higher data transfer rates and lower power consumption. They are critical for overcoming bottlenecks in AI workloads and accelerating the development of next-generation AI accelerators, supporting configurations like CoWoS.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: Applied Materials' focus on hybrid bonding and integrated solutions for HBM is a strong indicator of future packaging trends. The performance claims are likely achievable in controlled environments, but real-world yield and throughput at scale remain key challenges. [Opportunity] for US/EU materials & component suppliers to develop compatible materials for hybrid bonding, and for OEMs to design next-gen AI platforms leveraging these capabilities. [Threat] for companies reliant on older packaging methods, as this accelerates the performance gap. Next Actions: [R&D;] Benchmark current packaging capabilities against AMAT's stated improvements in HBM manufacturing by end-Q3 2026. [Business Dev] Explore partnerships with AMAT for early access or co-development opportunities.

Deep Dive ③ — Samsung's HBM4 & Optical HBM Roadmap

#18 | 2026/07/02 | Samsung (プレスリリース) | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●○

Samsung has strategically allocated half its HBM production to HBM4, achieving over $1 billion in sales in four months and targeting $10 billion annually. This aggressive pivot, including pausing HBM3E, aims to regain HBM market leadership.

Notably, Samsung announced plans for mass production of optical HBM by 2028. This innovative approach integrates silicon photonics within HBM stacks, aiming for dramatic improvements in bandwidth and energy efficiency by moving beyond traditional electrical signaling limitations.

> ▶ Strategic Analyst's Perspective
>
> Strategic Analyst's Perspective: Samsung's HBM4 sales figures are concrete, but the $10B annual projection is ambitious and dependent on overcoming yield challenges. Optical HBM by 2028 is a highly optimistic target, facing significant technical barriers in integration, thermal management, and cost. [Opportunity] for US/EU photonics companies to partner with Samsung on optical HBM development, and for AI chip designers to anticipate future bandwidth capabilities. [Threat] for US/EU memory competitors if Samsung achieves early market dominance in advanced HBM, and for current electrical interconnect IP holders. Next Actions: [R&D;] Initiate a feasibility study on optical interconnects for memory by Q4 2026. [Procurement] Diversify HBM sourcing strategies to mitigate reliance on any single supplier, given Samsung's aggressive HBM4 push.

Other Notable Articles

Intel and TSMC Champion Panel-Level Packaging (The Elec)
Tech Novelty●●●○○ Proximity●●●○○ Market Impact●●●●●

Major players pushing PLP signals a paradigm shift; US/EU equipment and materials suppliers must adapt quickly.

Lam Research Forges Advanced Packaging Future with Wafer-to-Panel Processing Expansion (Lam Research Newsroom)
Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○

Lam's wafer-to-panel strategy offers significant cost/throughput benefits, critical for next-gen AI chip manufacturing.

SK Hynix Announces Massive $64 Billion Investment in South Korea to Bolster AI Memory and Packaging Capabilities (Biggo Finance)
Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●●

SK Hynix's colossal investment will significantly boost global HBM supply, but capacity remains tight for now.

TSMC's CoWoS Packaging Equipment Supply Chain Sees Robust Demand Amid AI Surge (DigiTimes)
Tech Novelty●○○○○ Proximity●●●●● Market Impact●●●●●

Robust demand for CoWoS equipment highlights the severe AI packaging bottleneck and opportunity for tool makers.

CHIPS Act Successfully Attracts Taiwanese Semiconductor Suppliers to US, Creating New Opportunities in Advanced Packaging and Materials Supply (Fidelity Investments)
Tech Novelty●○○○○ Proximity●●●●● Market Impact●●●●●

US CHIPS Act is effectively diversifying the supply chain, creating domestic opportunities in advanced packaging.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Assess exposure to advanced packaging capacity crunch and potential price hikes from Asian OSATs like ASE.
- [Strategy] Evaluate the immediate impact of US CHIPS Act incentives on supply chain diversification and domestic partnership opportunities.

Short-term (1 month)

- [R&D;] Initiate a technical review of Panel-Level Packaging (PLP) readiness and its potential for cost/throughput benefits in future product roadmaps.
- [Business Dev] Explore collaboration opportunities with US equipment suppliers (Applied Materials, Lam Research) for next-generation packaging systems.
- [Procurement] Engage with HBM suppliers (Samsung, SK Hynix) to secure future HBM4/HBM4E allocations and understand their optical HBM roadmap.

Medium-long term (quarter+)

- [Strategy] Develop a long-term strategy for mitigating risks from China's growing advanced packaging capabilities (e.g., CXMT, BOE glass substrates).
- [R&D;] Monitor EU-funded 3D IC packaging R&D; (Infineon, ASML, Soitec) for potential technology licensing or partnership opportunities.
- [Executive] Conduct a comprehensive review of overall semiconductor supply chain resilience, focusing on advanced packaging as a critical choke point.

Semiconductor_BackEnd — Selected Articles

Date: 2026-07-05

Articles: 22

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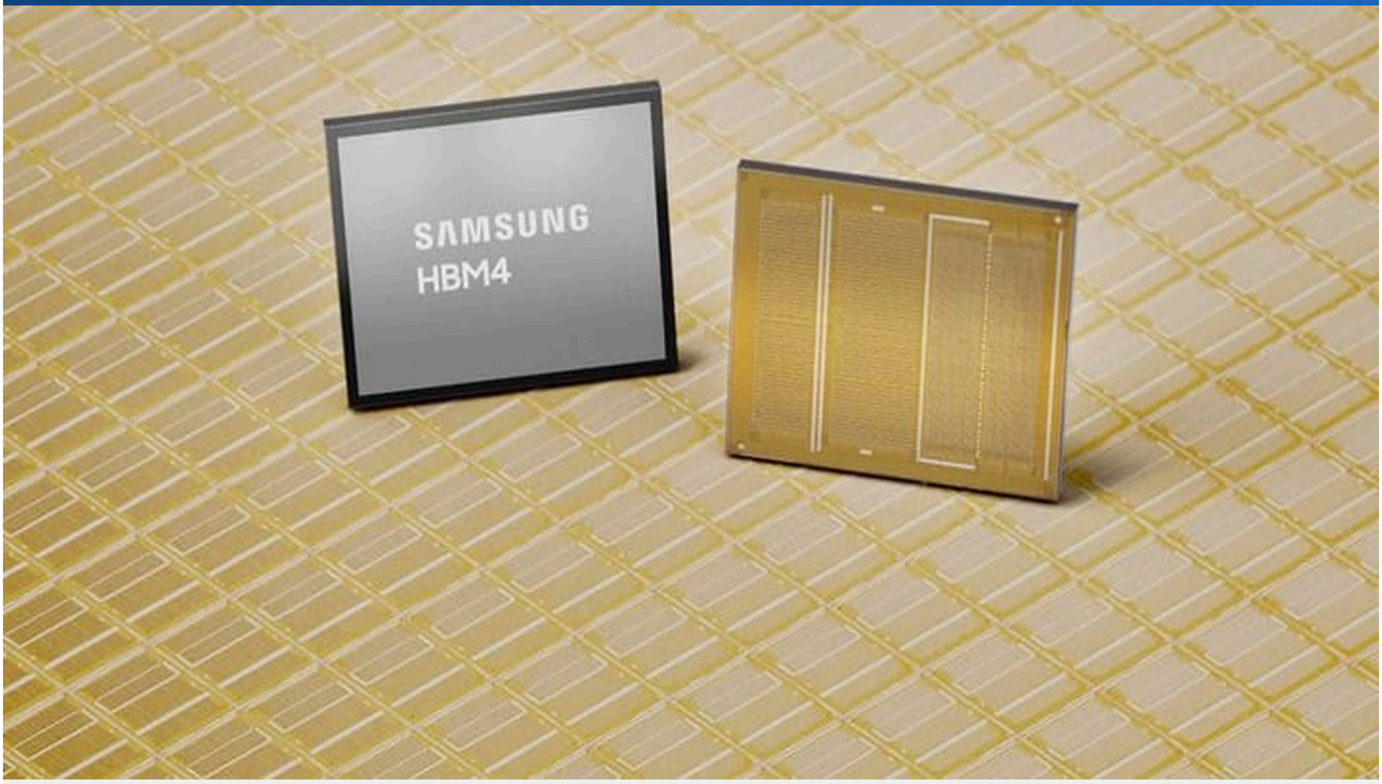
#01 EU Chips Act Allocates €210M to Bolster 3D IC Packaging R&D for Strategic Semiconductor Autonomy

Published June 25, 2026 The Chosun Daily EU



OVERVIEW

The European Union has committed €210 million under its EU Chips Act to accelerate research and development in next-generation 3D IC packaging technologies. This significant investment aims to enhance Europe's technological independence and competitiveness in semiconductor back-end processes, crucial for high-performance computing and AI applications. The funding specifically targets heterogeneous integration and 3D stacking, seeking to drive innovation and elevate Europe's strategic position within the global semiconductor supply chain.

IN DEPTH

Key Findings

The European Union has approved a substantial €210 million investment under the EU Chips Act to bolster research and development in advanced 3D IC packaging technologies. This move signals a critical commitment to strengthening Europe's position in the semiconductor value chain and fostering technological autonomy, particularly in back-end manufacturing processes.

Technical / Clinical Details

The allocated funds will primarily target projects focused on heterogeneous integration and 3D stacking. These technologies involve combining multiple disparate semiconductor dies and functionalities into a single package, promising significant improvements in performance, power efficiency, and form factor. Research initiatives will encompass advanced interconnect solutions, sophisticated thermal management strategies, and novel chiplet-based design methodologies. The objective is to overcome the limitations of conventional 2D packaging, enabling breakthroughs essential for high-growth sectors such as high-performance computing (HPC), artificial intelligence (AI), automotive, and telecommunications.

Background & Context

As the pace of innovation in front-end wafer fabrication decelerates, advanced packaging has emerged as a crucial driver for semiconductor scaling and performance enhancement, especially for demanding AI and HPC workloads. Historically, Europe has been heavily reliant on Asian manufacturers for both front-end and some back-end processes. The EU Chips Act aims to rebalance this by building a comprehensive domestic semiconductor ecosystem, from design to fabrication and packaging. This investment underscores Europe's determination to cultivate its own advanced packaging capabilities, reducing supply chain vulnerabilities and increasing its strategic influence globally.

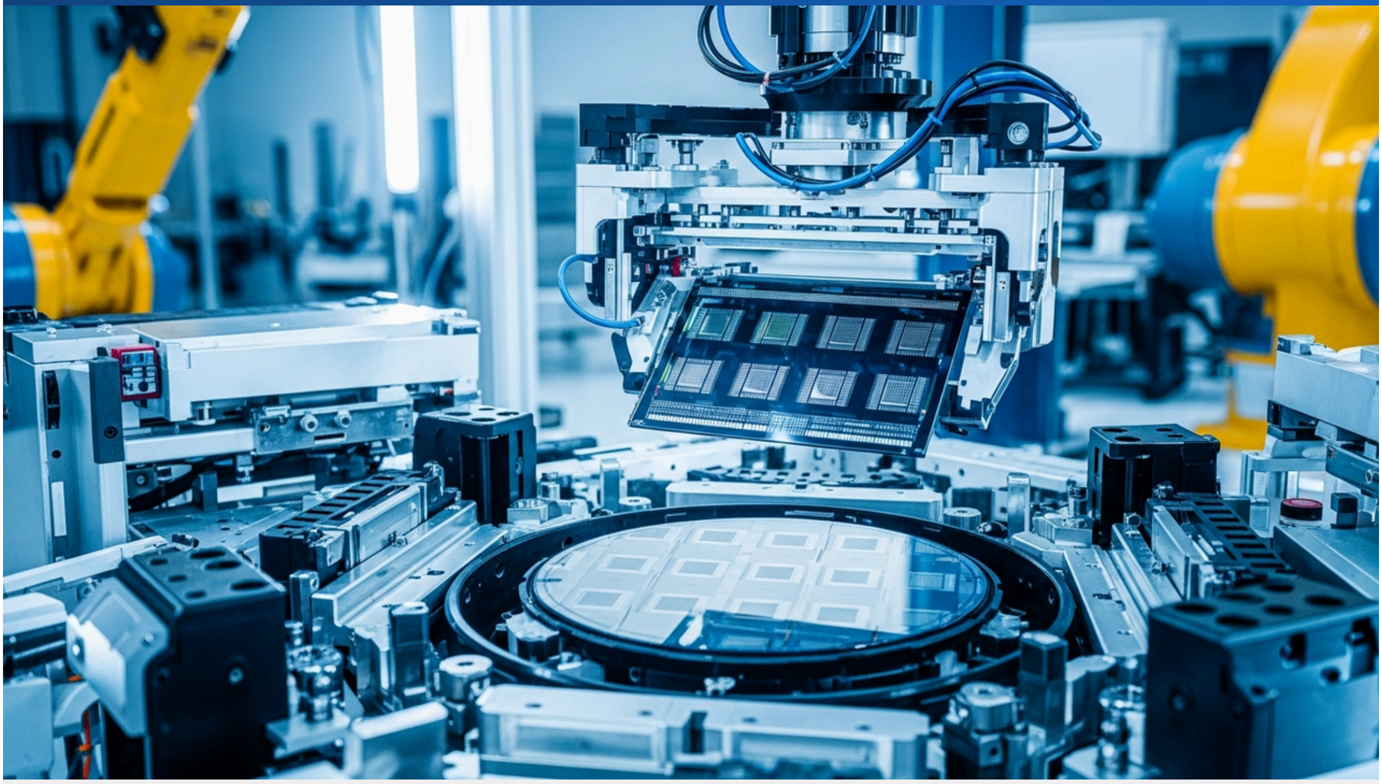
Strategic Significance & Outlook

This €210 million investment is expected to catalyze significant advancements in European semiconductor research institutions and companies. It will facilitate the establishment of pilot lines, accelerate proof-of-concept projects, and strengthen collaboration between academia and industry to rapidly commercialize research outcomes. Long-term, the initiative positions Europe to become a leading player in advanced packaging, contributing to a more resilient and diversified global semiconductor supply chain and reinforcing its standing as a hub for cutting-edge technology innovation.

Source: https://www.chosun.com/english/industry-en/2026/06/25/E5R4RKNI4BH4FJEIOPPSNDCH5Q/

#02 Applied Materials Unveils New Systems to Propel DRAM & Advanced Packaging for AI Chips

Published June 25, 2026 StockTitan USA



OVERVIEW

Applied Materials has introduced a suite of new systems designed to dramatically enhance DRAM and advanced packaging processes, directly addressing the escalating performance demands of AI chips. These innovations specifically target High Bandwidth Memory (HBM) manufacturing, boosting efficiency and reliability through advanced wafer bonding, deposition, and etch technologies. The new platforms, including a hybrid bonding solution, enable higher data transfer rates and lower power consumption, critical for overcoming bottlenecks in AI workloads and accelerating the development of next-generation AI accelerators.

IN DEPTH

Key Findings

Applied Materials has unveiled a groundbreaking suite of new systems engineered to significantly accelerate DRAM and advanced packaging processes, directly addressing the burgeoning performance requirements of artificial intelligence (AI) chips. These innovations are poised to dramatically enhance the manufacturing efficiency and reliability of High Bandwidth Memory (HBM), a critical component for modern AI accelerators.

Technical / Clinical Details

The new systems encompass solutions optimized for advanced scaling and stacking in DRAM manufacturing, targeting crucial processes such as wafer bonding, thin-film deposition, and etching essential for HBM production. Specifically, Applied Materials' new hybrid bonding platform is designed to maximize interconnect density between chips, shortening signal pathways to boost data transfer speeds while simultaneously reducing power consumption. Furthermore, advanced metrology platforms are integrated to improve process precision and yield, enabling rigorous quality control for complex 3D structures. These technologies are indispensable for advanced packaging configurations like CoWoS (Chip-on-Wafer-on-Substrate), which integrates AI processors with HBM, ensuring that next-generation AI accelerators meet stringent performance benchmarks.

Background & Context

The relentless advancement of AI demands unprecedented data processing capabilities, creating bottlenecks that conventional 2D semiconductor technologies struggle to overcome. The data bandwidth and latency between AI accelerators and HBM are particularly critical determinants of overall system performance. Applied Materials leverages its extensive expertise in materials engineering and process technology to deliver integrated solutions that alleviate these bottlenecks. These new systems provide a foundational framework for semiconductor manufacturers to efficiently produce next-generation memory like HBM4 and HBM5 at scale, meeting the high-performance computing demands of the AI era.

Strategic Significance & Outlook

Applied Materials' latest systems are expected to establish new benchmarks in AI chip design and manufacturing, driving technological innovation across the broader semiconductor industry. Through these solutions, the company aims to empower customers to deliver more powerful and energy-efficient AI semiconductors to market, thereby contributing to the wider adoption and evolution of AI technologies. The proliferation of hybrid bonding technology, in particular, holds the promise of enabling direct chiplet-to-chiplet connections in the future, leading to further performance gains and cost reductions.

Source: https://www.stocktitan.net/news/AMAT/applied-materials-introduces-new-systems-to-accelerate-dram-and-etwqxwf3t2d8.html

Collected: July 03, 2026 | Automated Research System (Gemini API)

#03 ASE to Commence FOPLP Mass Production by End-2026, Launching 15 Expansion Projects Amid AI Chip Boom

Published June 25, 2026 TrendForce Taiwan

OVERVIEW

ASE Technology, the world's largest semiconductor packaging and testing services provider, announced plans to begin mass production of Fan-out Panel-Level Packaging (FOPLP) by the end of 2026. This initiative, coupled with 15 expansion projects launched this year, aims to meet the surging demand for AI chips and address current advanced packaging bottlenecks. FOPLP offers enhanced cost-efficiency and productivity compared to wafer-level solutions, solidifying ASE's pivotal role in the AI semiconductor supply chain.

IN DEPTH

Key Findings

ASE Technology (Advanced Semiconductor Engineering), the world's largest provider of independent semiconductor assembly and test services, has announced plans to commence mass production of Fan-out Panel-Level Packaging (FOPLP) technology by the end of 2026. This strategic move comes in response to the explosive demand for artificial intelligence (AI) chips, with the company concurrently launching 15 expansion projects this year to significantly boost its AI-related advanced packaging capabilities.

Technical / Clinical Details

FOPLP is an advanced packaging technology that utilizes larger panel substrates compared to traditional Fan-out Wafer-Level Packaging (FOWLP), enabling the processing of more chips simultaneously, thereby enhancing cost-efficiency and overall productivity. This technology provides high-density interconnects and superior electrical performance, making it particularly suitable for integrating high-performance AI processors and High Bandwidth Memory (HBM). ASE's ambitious expansion projects include not only the establishment of FOPLP manufacturing lines but also the ramp-up of existing advanced packaging capacities, such such as Chip-on-Wafer-on-Substrate (CoWoS). This diversified approach ensures the provision of various high-performance and complex packaging solutions required by cutting-edge AI chips.

Background & Context

The current AI chip market is experiencing significant bottlenecks in advanced packaging capacity, notably with TSMC's CoWoS, where supply struggles to keep pace with soaring demand. ASE's substantial investment in FOPLP and its scheduled mass production are critical steps towards alleviating this bottleneck and accelerating the time-to-market for AI chips. FOPLP, by scaling from wafer-level to panel-level, offers advantages in reducing production costs and increasing throughput, contributing to the diversification and resilience of the AI semiconductor supply chain. This initiative is a core part of ASE's strategy to solidify its position as a leading packaging solution provider in the AI era.

Strategic Significance & Outlook

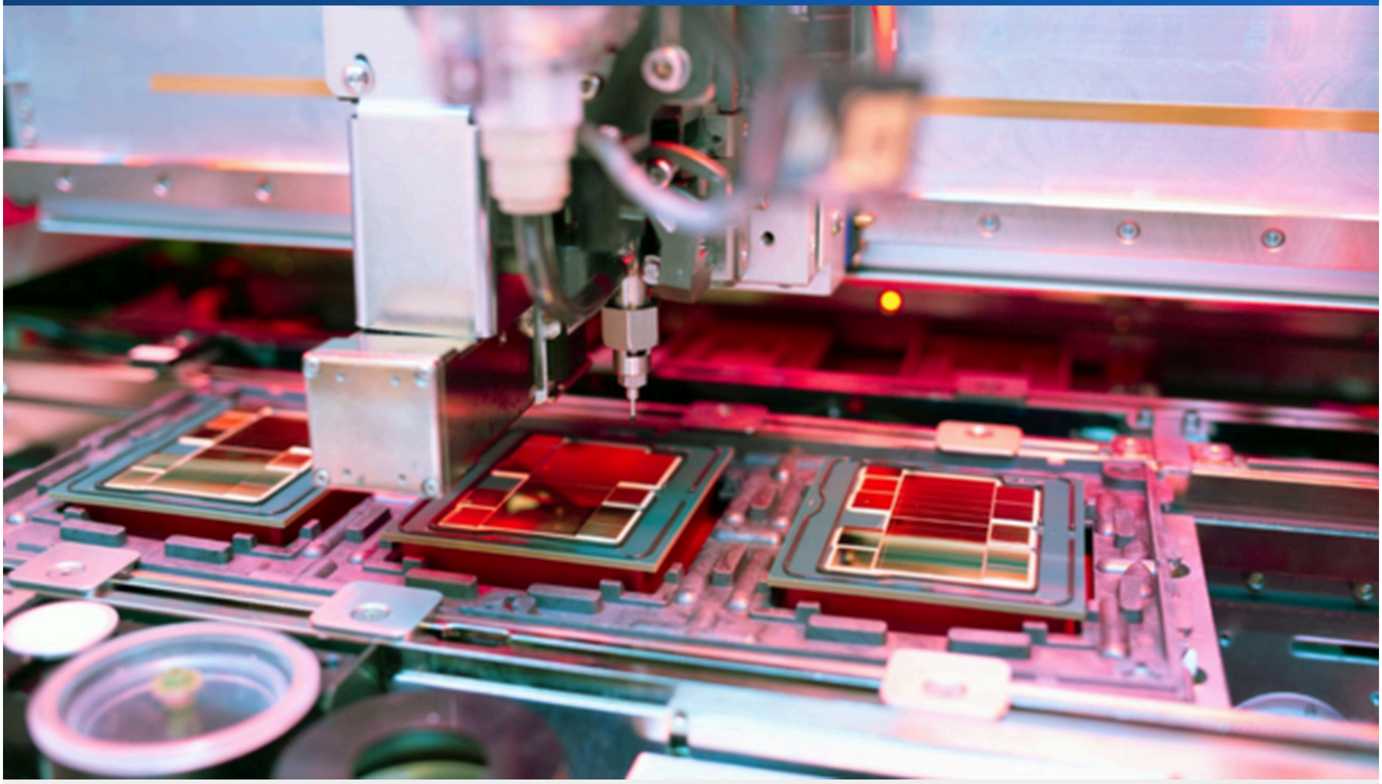
The commencement of ASE's FOPLP mass production and its aggressive capital expenditure are expected to further accelerate the growth of the AI semiconductor market. The company aims to capture demand from major AI chip manufacturers, including NVIDIA, AMD, and Intel, thereby expanding its market share. Moreover, FOPLP offers a distinct balance of cost and performance compared to CoWoS, providing flexible packaging options for a wider range of AI applications and fostering broader AI chip adoption. Through these efforts, ASE is building a comprehensive advanced packaging portfolio designed to meet diverse customer needs, establishing itself as an indispensable entity in the future development of the AI industry.

Source: https://www.trendforce.com/news/2026/06/25/news-ase-targets-foplp-mass-production-by-end-2026-launches-15-expansion-projects-this-year-amid-ai-boom/

Collected: July 03, 2026 | Automated Research System (Gemini API)

#04 Intel and TSMC Champion Panel-Level Packaging, Projecting a Tenfold Market Expansion

Published July 02, 2026   The Elec   South Korea



OVERVIEW

Intel and TSMC are aggressively pursuing Panel-Level Packaging (PLP) technology, a move anticipated to expand the associated market tenfold. PLP offers significant production efficiency and cost advantages over traditional wafer-level packaging, making it critical for AI and high-performance computing (HPC) chip manufacturing. This strategic push by both giants aims to alleviate current supply constraints in advanced packaging solutions like CoWoS and enable broader adoption of high-performance semiconductors. This innovation is pivotal for establishing mass production capabilities for next-generation chips.

IN DEPTH

Key Findings

Intel and TSMC, two pivotal forces in the semiconductor industry, are aggressively championing the adoption and advancement of Panel-Level Packaging (PLP) technology. This concerted effort is projected to expand the associated market by up to tenfold, signaling a significant shift in the landscape of high-performance semiconductor manufacturing, particularly for AI and High-Performance Computing (HPC) chips.

Technical / Clinical Details

Panel-Level Packaging involves packaging multiple chips simultaneously on larger, rectangular panel substrates instead of traditional round silicon wafers. This methodology significantly improves material utilization and overall throughput by minimizing waste from wafer edge losses. Intel has been actively integrating PLP concepts into its advanced packaging technologies such as 'Foveros' and 'EMIB,' including Fan-out Panel-Level Packaging (FO-PLP). TSMC, likewise, is exploring PLP as an evolution of its CoWoS (Chip-on-Wafer-on-Substrate) technology, seeking solutions to integrate more chiplets on larger substrates. PLP offers dense interconnection layers and superior thermal dissipation characteristics, making it particularly advantageous for integrating AI processors with High Bandwidth Memory (HBM).

Background & Context

The explosive demand for AI chips has created severe bottlenecks in existing advanced packaging capacities, notably with technologies like CoWoS, which currently limits the speed at which new chips can enter the market. Intel and TSMC's focus on PLP is a strategic response to mitigate these supply constraints and enable the mass production of high-performance chips in a more cost-effective manner. PLP has the potential to reduce manufacturing costs by 20-30%, which is expected to accelerate the proliferation of high-performance semiconductors not just for AI, but also across a broader range of applications including mobile devices, data centers, and automotive systems. This technological pivot is poised to usher the semiconductor industry into a new phase of growth.

Strategic Significance & Outlook

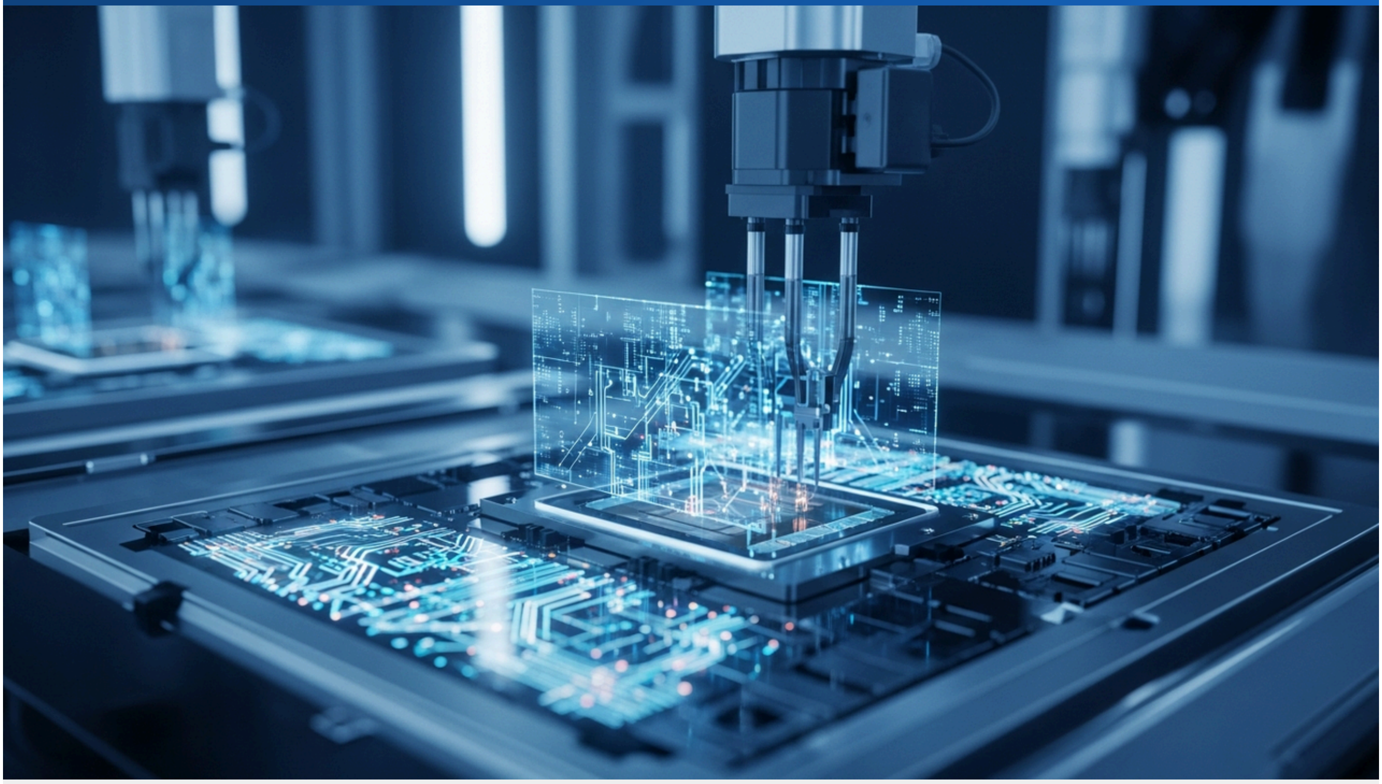
The aggressive pursuit of PLP by Intel and TSMC represents a paradigm shift in semiconductor manufacturing. As both companies push for the commercialization and mass production of this technology, the entire market for PLP-related equipment, materials, and services is expected to experience substantial growth, creating new business opportunities for equipment manufacturers and material suppliers. In the long term, PLP is anticipated to become one of the mainstream advanced packaging technologies, laying a foundational pillar for the continued evolution of AI and HPC. This innovation will significantly improve the cost-performance balance of next-generation semiconductors, benefiting a wide array of industrial sectors.

Source: https://www.thelec.net/news/articleView.html?idxno=11912

Collected: July 03, 2026 | Automated Research System (Gemini API)

#05 Applied Materials Guides Memory Makers to 'Logic-Class' Fabrication for Advanced Packaging

Published June 26, 2026 Futurum Group USA



OVERVIEW

Applied Materials is leading memory manufacturers to adopt 'logic-class' precision in advanced packaging processes, crucial for next-generation AI chips. The company's integrated solutions ensure ultra-precise bonding and high yields in HBM and 3D stacked die production, addressing key performance bottlenecks. This approach, leveraging advanced process control from logic manufacturing, is essential for meeting the increasing complexity and performance demands of memory in the AI era. Applied Materials aims to elevate the entire semiconductor industry's technological standards through these innovations.

IN DEPTH

Key Findings

Applied Materials has asserted that its advanced packaging solutions are elevating process control in memory manufacturing to a 'logic-class' precision, akin to that used in logic chip fabrication. This approach is pivotal for significantly improving the performance and yield of complex memory products, particularly High Bandwidth Memory (HBM) and 3D stacked dies, thereby accelerating the evolution of AI chips.

Technical / Clinical Details

The 'logic-class' manufacturing approach advocated by Applied Materials entails achieving sub-micron level precision alignment, uniform thin-film deposition, and defect-free etching processes in memory chip packaging. This involves applying advanced process control technologies and metrology, traditionally refined in logic chip manufacturing, to the back-end processes of memory production. Key focus areas include technologies that ensure high-precision alignment and robust bonding strength in wafer-to-wafer hybrid bonding, as well as sophisticated thermal management and stress mitigation techniques for stacking multiple dies. These advancements enhance connection reliability, optimize electrical performance, and maximize manufacturing yield for multi-layered memory structures like HBM.

Background & Context

With the exponential growth of AI, data transfer speed and bandwidth between AI processors and memory have become critical bottlenecks for system performance. HBM is an indispensable technology to overcome these bottlenecks, but its fabrication demands extremely sophisticated packaging techniques. While traditional memory packaging did not require the same stringent process control as logic chips, the increasing complexity of HBM and 3D stacked memory necessitates logic-chip-level precision. Applied Materials' strategy aims to resolve these technical challenges in memory back-end processes and establish new standards to meet the high-performance computing demands of the AI era.

Strategic Significance & Outlook

Applied Materials' 'logic-class' advanced packaging technology paves the way for memory manufacturers to efficiently produce next-generation HBM, 3D NAND, and other advanced memory products with high quality. The widespread adoption of this technology is expected to lead to even higher performance AI accelerators and reductions in power consumption. Leveraging its leadership in materials engineering and process technology, Applied Materials will continue to enhance the technological capabilities of the entire semiconductor industry and provide the foundational innovations for the AI era. This will strengthen the semiconductor supply chain and expand the application scope of AI technologies.

Source: https://futurumgroup.com/insights/applied-materials-master-class-schools-memory-makers-on-logic-class-fabrication/

#06 ASE Elevates Advanced Packaging Quotes Over 20% Amid Explosive AI Demand Crunch

Published July 02, 2026   SiliconAnalysts   Taiwan

OVERVIEW

ASE Technology, the world's largest outsourced semiconductor assembly and test (OSAT) provider, has increased its advanced packaging service prices by over 20%. This hike is a direct response to unprecedented demand for artificial intelligence (AI) chips, leading to severe supply constraints for solutions like CoWoS. The price adjustment aims to bolster profitability and fund continuous capital expenditures, contributing to the alleviation of bottlenecks in the AI semiconductor ecosystem. This move is expected to impact industry-wide cost structures and potentially prompt similar actions from other back-end service providers.

IN DEPTH

Key Findings

ASE Technology, the leading global provider of semiconductor packaging and testing services, has implemented a significant price increase of over 20% for its advanced packaging services tailored for AI chips. This decision is a direct consequence of an unprecedented surge in demand for advanced packaging capabilities, driven by the explosive growth of artificial intelligence (AI) technologies.

Technical / Clinical Details

The price adjustments primarily apply to advanced packaging technologies such as CoWoS (Chip-on-Wafer-on-Substrate), which are indispensable for integrating High Bandwidth Memory (HBM) and high-performance AI processors. These technologies enable the dense stacking and interconnection of multiple chiplets to maximize data transfer rates and minimize power consumption. The current market is characterized by overwhelming orders from leading AI chip developers like NVIDIA, AMD, and Intel, keeping ASE and other back-end service providers operating at full capacity. The more than 20% price increase reflects the substantial investment costs associated with expanding production lines, developing cutting-edge technologies, and the premium commanded by limited supply capabilities.

Background & Context

The evolution of AI has shifted bottlenecks from traditional front-end semiconductor manufacturing processes to the back-end, particularly in advanced packaging. While TSMC remains a primary supplier of CoWoS, OSAT (Outsourced Semiconductor Assembly and Test) companies like ASE complement this capacity and offer a diverse range of packaging solutions. In the current AI chip supply chain, advanced packaging capacity stands as the most severe constraint, with demand significantly outpacing supply. ASE's price hike underscores the gravity of this supply-demand imbalance and is likely to influence the overall market pricing for AI chips.

Strategic Significance & Outlook

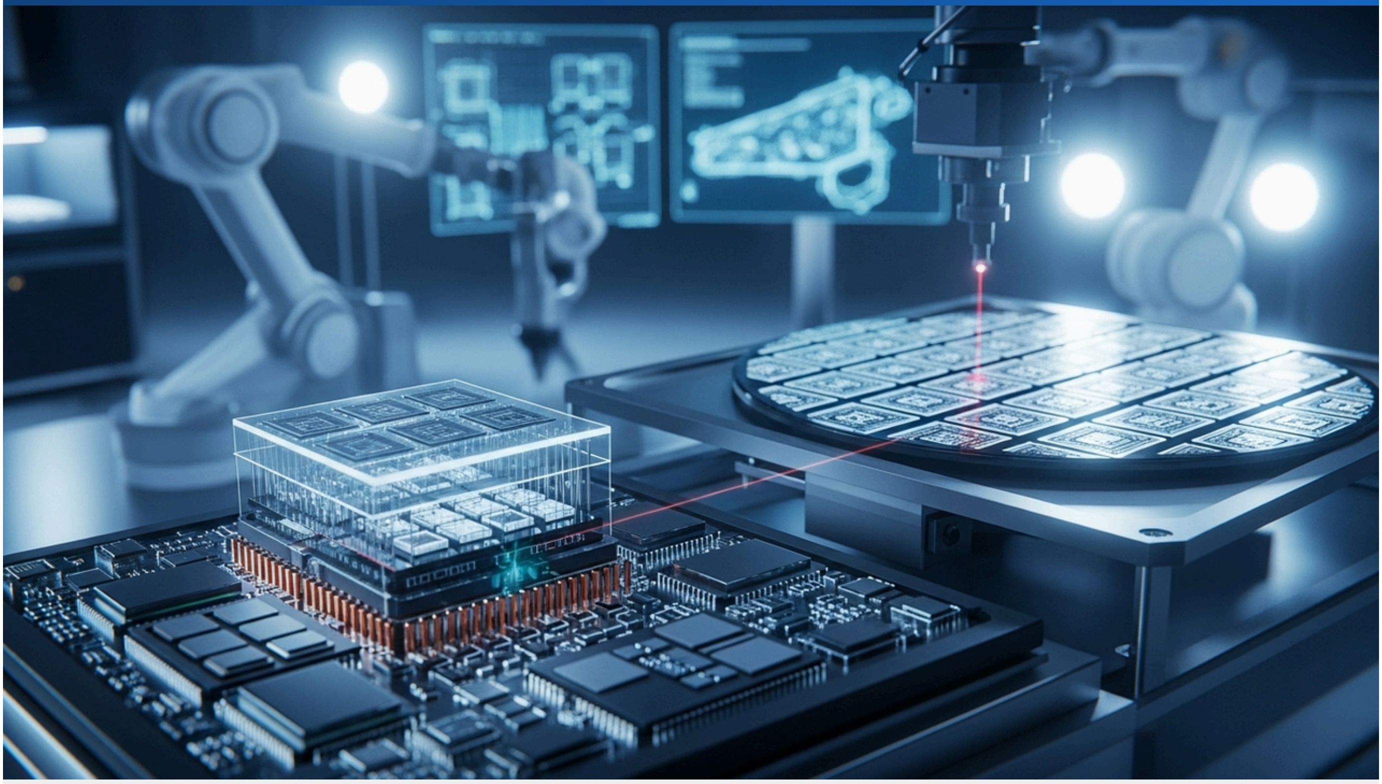
ASE's price increase is expected to enhance the company's profitability and cash flow, enabling further acceleration in research and development and capital expenditures. This will lead to long-term strengthening of advanced packaging capabilities, establishing a robust foundation to support the growth of the entire AI semiconductor industry. Furthermore, this move is likely to ripple across other back-end service providers, potentially prompting similar price adjustments and accelerated investments. Ultimately, while impacting the cost structure of AI chips, this development will spur innovation and expansion of production capacity in advanced packaging, serving as a critical milestone in accelerating technological advancements in the AI era.

Source: https://siliconanalysts.com/market/ase-advanced-packaging-quotes-surge-20-amid-ai-driven-demand-crunch-2026-07-02

Collected: July 03, 2026 | Automated Research System (Gemini API)

#07 AI Packaging Bottleneck Shifts: CoWoS, Wafer-Scale, and CoWoP Emerge as Key Solutions

Published June 26, 2026 EDN USA



OVERVIEW

The packaging bottleneck hindering AI chip performance is being addressed by advanced technologies such as CoWoS, wafer-scale packaging, and CoWoP. These innovations optimize the integration of AI processors and HBM by enhancing inter-die connection density and thermal efficiency. While CoWoS currently represents a major bottleneck, wafer-scale and CoWoP offer promising avenues for improved productivity and cost reduction. This expansion in packaging capacity is crucial for broadening AI chip availability and accelerating their adoption across diverse AI applications.

IN DEPTH

Key Findings

The primary bottleneck impeding the performance evolution of artificial intelligence (AI) chips is being overcome through groundbreaking innovations in packaging technology. Advanced approaches such as CoWoS (Chip-on-Wafer-on-Substrate), wafer-scale packaging, and CoWoP (Chip-on-Wafer-on-Package) are proving instrumental in tackling the challenges of integrating AI processors with High Bandwidth Memory (HBM), leading to significant performance enhancements and improved manufacturing efficiency.

Technical / Clinical Details

CoWoS is a 2.5D packaging technology that integrates multiple dies (logic chips and HBM) on an interposer, which is then mounted onto a package substrate. This allows for close proximity and short interconnects between dies, dramatically increasing data transfer speeds. However, the limited manufacturing capacity for CoWoS has become a major bottleneck in current AI chip supply. In response, wafer-scale packaging offers a method to process multiple chips simultaneously across an entire larger wafer, aiming to reduce manufacturing costs. Further evolution, CoWoP, maintains the benefits of CoWoS while leveraging larger package substrates to potentially further enhance CoWoS productivity and improve cost-efficiency. These technologies integrate fine-pitch copper-to-copper hybrid bonding, high-density redistribution layers (RDL), and advanced thermal management solutions to deliver the power efficiency and reliability essential for demanding AI workloads.

Background & Context

The increasing complexity of AI models and the exponential growth in data volumes place extremely high demands on both AI processor capabilities and the bandwidth and latency of connected memory. Traditional packaging technologies struggle to meet these requirements, contributing significantly to AI chip shortages and high costs. Leading foundries and IDMs like TSMC and Intel are investing heavily in CoWoS and other advanced packaging technologies to resolve this bottleneck and secure growth in the high-performance computing market of the AI era. Wafer-scale and CoWoP technologies complement the challenges of CoWoS by offering more scalable and economical solutions, thereby strengthening the entire AI semiconductor ecosystem.

Strategic Significance & Outlook

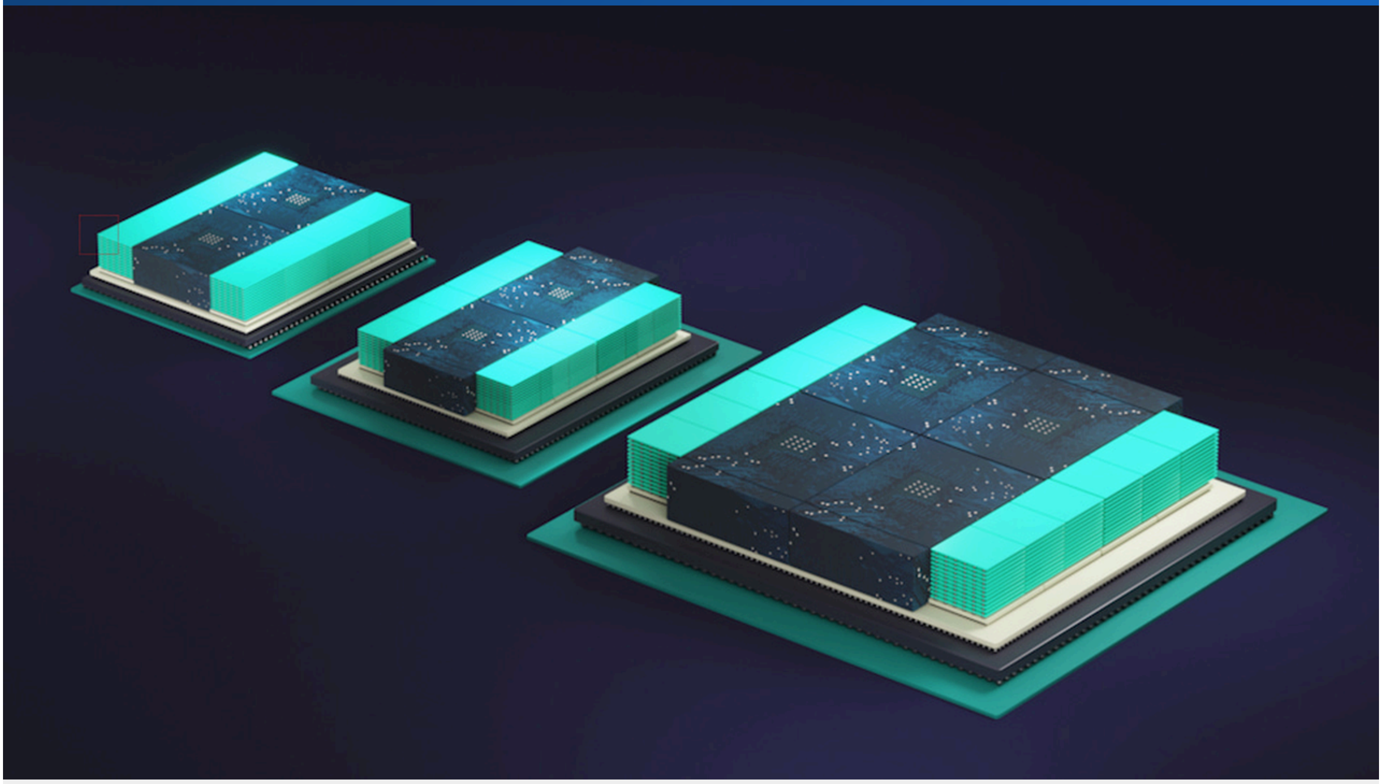
The evolution and widespread adoption of these advanced packaging technologies are poised to dramatically boost AI chip manufacturing capacity, enabling a broader range of AI applications. Should emerging technologies like CoWoP enter mass production, AI chip costs are expected to decrease, making high-performance AI hardware accessible to more companies and researchers. This will accelerate new innovations across all sectors where AI is leveraged, including autonomous driving, robotics, medical diagnostics, and large language models. The semiconductor industry, by placing packaging at the core of its innovation strategy, is reinforcing its role as a key growth engine for the AI era.

Source: https://www.edn.com/cowos-wafer-scale-and-cowop-why-ai-packaging-bottleneck-is-moving/

Collected: July 03, 2026 | Automated Research System (Gemini API)

#08 Lam Research Forges Advanced Packaging Future with Wafer-to-Panel Processing Expansion

Published June 26, 2026 Lam Research Newsroom USA



OVERVIEW

Lam Research is actively shaping the future of advanced packaging by expanding its wafer-to-panel processing technologies. The company is developing new platforms and processes for larger panel substrates, promising significant manufacturing cost reductions and throughput improvements compared to existing wafer-level techniques. This innovative approach addresses the diverse packaging demands of AI and High-Performance Computing (HPC) chips, setting new standards for scalability and efficiency in the semiconductor industry. Lam Research's advancements enable the integration of complex next-generation chips.

IN DEPTH

Key Findings

Lam Research, a leading supplier of semiconductor manufacturing equipment, is proactively shaping the future of advanced packaging by expanding its wafer-to-panel processing technologies. The company has developed new platforms and processes that enable simultaneous processing of multiple chips on larger panel substrates, delivering dramatic reductions in manufacturing costs and significant improvements in production throughput.

Technical / Clinical Details

Lam Research's 'wafer-to-panel' strategy focuses on executing advanced packaging processes on large, rectangular panels rather than traditional round wafers. This approach minimizes material waste typically generated at wafer edges, maximizing raw material utilization efficiency. Specifically, the company's new platforms are designed to perform high-precision etching, thin-film deposition, and cleaning processes at the panel level. This enables the processing of a greater number of chips at once, especially for technologies like Fan-Out Panel-Level Packaging (FOPLP), substantially reducing the cost per unit chip. This technology addresses the increasingly complex demands of next-generation semiconductors, including AI processors, High Bandwidth Memory (HBM), and chiplet integration.

Background & Context

The rapid advancements in artificial intelligence (AI) and high-performance computing (HPC) are posing new challenges to traditional semiconductor manufacturing technologies. Advanced packaging, in particular, is becoming an indispensable factor in determining chip performance, power consumption, and cost. However, existing wafer-level packaging technologies face limitations in terms of cost-efficiency and scalability for manufacturing large and complex AI chips. Lam Research's pivot to panel-level processing is a strategic answer to these challenges, paving the way for semiconductor manufacturers to mass-produce next-generation AI chips efficiently and economically.

Strategic Significance & Outlook

Lam Research's wafer-to-panel processing technology holds the potential to revolutionize the advanced packaging market. The widespread adoption of this technology is expected to reduce AI chip manufacturing costs, enabling high-performance AI functionalities to be integrated into a wider array of devices and applications. Through this innovation, the company aims to enhance the overall production efficiency and scalability of the semiconductor industry, accelerating technological advancements in all AI-centric sectors, including data centers, automotive, and mobile devices. As a leader in semiconductor manufacturing equipment, Lam Research will continue to drive the evolution of advanced packaging.

Source: https://newsroom.lamresearch.com/wafer-to-panel-lam-scaling-advanced-packaging-panel-level-processing?blog=true

#09 Samsung's HBM4 Sales Projected to Surpass $10 Billion, Driven by Surging AI Demand

Published June 26, 2026 GuruFocus South Korea

OVERVIEW

Samsung Electronics' next-generation High Bandwidth Memory (HBM4) sales are forecast to exceed $10 billion this year, propelled by an explosive surge in AI demand. The company has made substantial investments in HBM4 capacity expansion and technological innovation, catering to leading AI chip manufacturers like NVIDIA. This sales projection underscores HBM's increasing importance due to advanced AI models and marks a significant milestone for Samsung in solidifying its leadership in the memory semiconductor market. Samsung is maximizing HBM4 performance through advanced packaging technologies, including hybrid bonding.

IN DEPTH

Key Findings

Samsung Electronics' sales of its next-generation High Bandwidth Memory (HBM4) are projected to surpass an astounding $10 billion (approximately 1.6 trillion JPY) this year, fueled by an explosive increase in demand from artificial intelligence (AI) applications. This forecast clearly demonstrates Samsung's robust position in the HBM market and the critical importance of memory semiconductors in the AI era.

Technical / Clinical Details

HBM4 is engineered to deliver higher bandwidth, lower power consumption, and superior thermal characteristics compared to its predecessor, HBM3E. Samsung is actively employing advanced packaging technologies, particularly hybrid bonding, to maximize HBM4's performance. Hybrid bonding drastically reduces the connection pitch between chips, enhancing signal transmission efficiency and significantly boosting data transfer speeds. Furthermore, the company is increasing the number of HBM4 stacks and the capacity per die, providing the immense data processing capabilities required by AI accelerators. Leading AI chip manufacturers, including NVIDIA, are aggressively adopting HBM4 in their GPUs and ASICs, which is a powerful driver of Samsung's sales.

Background & Context

The evolution of AI, especially large language models (LLMs), demands not only tremendous computational power from AI processors but also immense data processing capabilities from connected memory. Consequently, data bandwidth between the processor and memory has become one of the most critical factors determining overall system performance. HBM stands as the only viable solution to overcome this bottleneck, leading to a rapid expansion of its demand. Samsung, leveraging its longstanding leadership in the DRAM market and aggressive investments in advanced packaging technologies, is driving growth in this HBM market during the AI era. While competitors are also focusing on HBM technology, Samsung has established a strong advantage through early mass production and continuous technological innovation.

Strategic Significance & Outlook

The projection of HBM4 sales exceeding $10 billion clearly positions HBM as a new growth engine for Samsung's semiconductor business. The company is expected to further ramp up HBM production capacity and actively engage in the development of next-generation technologies like HBM5 and beyond, maintaining its leadership in the high-performance computing market of the AI era. This expansion of the HBM market will also create significant business opportunities for related advanced packaging material and equipment suppliers, contributing to the revitalization of the entire semiconductor ecosystem. Samsung's HBM technology will continue to solidify its status as indispensable infrastructure supporting the advancement of AI.

Source: https://www.gurufocus.com/news/8929372/samsungs-hbm4-sales-surge-projected-to-exceed-10-billion?mobile=true

Collected: July 03, 2026 | Automated Research System (Gemini API)

#10 eWeek Reports on Critical AI Chip Bottlenecks: Advanced Packaging Identified as Key Solution

Published June 26, 2026 eWeek USA

OVERVIEW

A new eWeek report highlights that AI chip performance is confronting significant bottlenecks, deeming advanced packaging technologies essential for resolution. Critically, the scarcity of high-density integration technologies, such as TSMC's CoWoS, impedes rapid AI model deployment. The article emphasizes the importance of back-end processes in optimizing inter-chiplet data transfer efficiency and thermal management, beyond just silicon innovation. Overcoming these bottlenecks is vital for the sustained growth and advancement of the AI industry.

IN DEPTH

Key Findings

A recent investigative report by eWeek details the current state of major bottlenecks impeding the performance enhancement and market deployment of artificial intelligence (AI) chips, strongly emphasizing that advanced packaging technologies are paramount to their resolution. The report highlights that a severe shortage in the supply capacity of high-density integration technologies, such as TSMC's CoWoS, represents a critical challenge within the current AI chip supply chain.

Technical / Clinical Details

AI chip bottlenecks primarily arise from three aspects. First, limitations in data bandwidth between AI processors and connected High Bandwidth Memory (HBM). Conventional packaging struggles to achieve sufficient data transfer speeds, preventing AI's full computational power from being utilized. Second, the thermal management challenges of highly integrated AI chips. Efficiently dissipating heat generated from stacking numerous dies in advanced packaging is extremely difficult. Third, the manufacturing yield and cost of advanced packaging. Complex 3D structures and fine-pitch interconnections complicate manufacturing processes, leading to high costs and supply shortages. CoWoS (Chip-on-Wafer-on-Substrate) is a cutting-edge technology addressing these challenges, but limitations in manufacturing equipment and lengthy process times contribute to its bottleneck status. Alternative technologies like wafer-level packaging and panel-level packaging are being developed to improve scalability and cost efficiency.

Background & Context

The rapid advancement of large language models (LLMs) and generative AI has explosively increased demand for AI accelerators in data centers. However, while AI chip design and front-end manufacturing have made tremendous strides, advanced packaging capabilities have failed to keep pace. This has resulted in chronic AI chip shortages, with leading AI chip vendors like NVIDIA and AMD struggling to bring products to market. The eWeek report clearly frames this issue not merely as a silicon fabrication problem, but as a back-end challenge of efficiently and reliably integrating chips. The entire semiconductor industry is dedicating significant resources to resolving these bottlenecks.

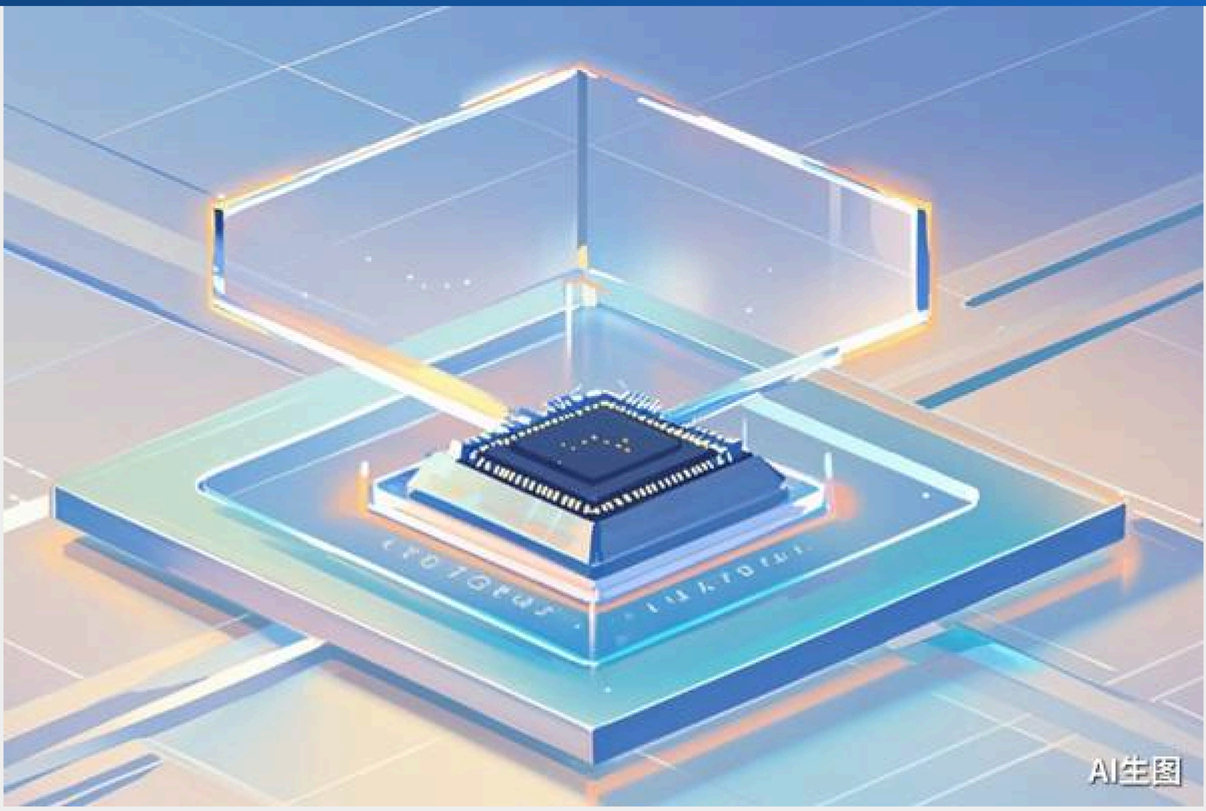
Strategic Significance & Outlook

Resolving AI chip bottlenecks is indispensable for the sustained growth of the AI industry. Continued investment and innovation in advanced packaging technologies are key to overcoming these challenges. Specifically, the development of hybrid bonding, panel-level packaging, and novel thermal management solutions will accelerate. This will lead to expanded AI chip supply capacity, reduced costs, and broader adoption across diverse AI applications. In the long term, packaging technology is expected to play a central role in driving AI evolution, with the semiconductor industry's innovation focus shifting towards more integrated, system-level solutions.

Source: https://www.eweek.com/news/ai-chip-bottlenecks/

#11 BOE Commences Sample Shipments of Glass Substrates for Advanced Chip Packaging to Domestic Customers, Signaling Innovation Boost

Published June 27, 2026 36Kr English China



OVERVIEW

Chinese display giant BOE Technology has initiated sample shipments of glass substrates for advanced chip packaging to domestic customers. This move signifies China's technological progress in next-generation semiconductor packaging materials, poised to enhance performance for AI and High-Performance Computing (HPC) chips. Glass substrates offer superior low thermal expansion, high rigidity, and flatness compared to organic counterparts, enabling finer wiring and denser chip stacking. BOE aims to establish a new role in the semiconductor supply chain through this innovation.

IN DEPTH

Key Findings

BOE Technology, a major Chinese display manufacturer, has commenced sample shipments of its newly developed glass substrates tailored for advanced chip packaging to domestic customers. This strategic development marks a significant advancement for China in the critical materials technology sector for semiconductor back-end processes, expected to contribute substantially to the performance enhancement of high-performance computing (HPC) and artificial intelligence (AI) chips.

Technical / Clinical Details

Glass substrates possess several distinct technical advantages over conventional organic packaging substrates. Firstly, their remarkably low coefficient of thermal expansion (CTE) significantly reduces stress mismatch between chips and the substrate under high-temperature conditions, thereby improving package reliability. Secondly, their high rigidity and superior flatness enable finer wiring (with potential for lines/spaces below 1/1μm) and higher-density chip stacking. These attributes maximize electrical performance and ensure signal integrity in multi-layer chiplet integration and connections with High Bandwidth Memory (HBM). BOE's glass substrates are designed to leverage these characteristics to meet the demanding requirements of next-generation 3D IC and 2.5D packaging.

Background & Context

The evolution of AI and HPC is pushing semiconductor packaging technologies to unprecedented limits, with traditional organic substrates beginning to show their limitations. To accommodate more transistors and process larger amounts of data at higher speeds, increasing packaging density, shortening signal transmission distances, and improving thermal management are indispensable. Glass substrates are emerging as a potential game-changer to address these challenges, with major semiconductor players like Intel and TSMC also accelerating their R&D efforts in this area. BOE's initiation of sample shipments positions China as a contender in this critical technology, aiming to enhance its presence in the global semiconductor supply chain.

Strategic Significance & Outlook

BOE's entry into the glass substrate market with sample shipments signals the start of new competition in advanced packaging materials. Should this technology transition to mass production, it could significantly contribute to performance gains and cost reductions for AI chips, ultimately driving the broader adoption of AI technologies. BOE aims to leverage its expertise in glass processing and large-scale manufacturing capabilities, honed in display production, to establish a new revenue stream in the semiconductor packaging sector. Long-term, glass substrates are expected to become one of the mainstream materials in advanced packaging, playing a crucial role in the AI-era semiconductor ecosystem.

Source: https://eu.36kr.com/en/p/3871173400073222

#12 SK Hynix Announces Massive $64 Billion Investment in South Korea to Bolster AI Memory and Packaging Capabilities

Published July 02, 2026   Biggo Finance   South Korea

OVERVIEW

SK Hynix has unveiled plans for a colossal $64 billion investment in memory chip and advanced packaging facilities within South Korea over the coming years. This strategic outlay aims to address the soaring demand for High Bandwidth Memory (HBM) driven by explosive AI growth, solidifying the company's leadership in AI memory. Key components include the construction of a new DRAM production fab, M17, and the expansion of the dedicated advanced packaging facility, P&T7. This investment will significantly enhance SK Hynix's supply capacity and technological superiority in the AI-era semiconductor supply chain.

IN DEPTH

Key Findings

SK Hynix has announced an unprecedented investment plan totaling $64 billion (over 10 trillion JPY) in its domestic memory chip and advanced packaging facilities over the next several years. This monumental investment aims to dramatically boost the production capacity of cutting-edge AI memory chips, such as High Bandwidth Memory (HBM), and the advanced packaging capabilities required to integrate them, thereby strengthening the company's leadership in the artificial intelligence (AI) memory market.

Technical / Clinical Details

The $64 billion investment will primarily be allocated to two major projects. The first is the construction of a new DRAM production facility, 'M17.' M17 will specialize in manufacturing advanced DRAM, including next-generation HBM products, and will incorporate state-of-the-art EUV (Extreme Ultraviolet) lithography technology to maximize production efficiency and yield. The second project involves the expansion of 'P&T7,' a dedicated advanced packaging facility. P&T7 will focus on research, development, and mass production of 2.5D/3D packaging technologies like CoWoS (Chip-on-Wafer-on-Substrate), which integrates HBM with AI processors. Specifically, the goal is to enhance HBM's electrical performance and reliability through the adoption of hybrid bonding technology and improved thermal management solutions.

Background & Context

The increasing complexity of AI models and the explosion of data volumes demand not only immense computational power from AI processors but also extraordinary data bandwidth from connected memory. HBM has emerged as the most effective solution to overcome this bottleneck, with demand skyrocketing from leading AI chip manufacturers such as NVIDIA, AMD, and Intel. As one of the pioneers in the HBM market, SK Hynix has already secured a significant market share with products like HBM3E. This latest investment is a strategic decision to maintain its lead in HBM4 and subsequent generations. The global semiconductor supply chain is facing severe shortages in advanced packaging capacity, and this investment is expected to contribute significantly to stabilizing the supply of AI semiconductors.

Strategic Significance & Outlook

SK Hynix's colossal $64 billion investment will further solidify its position as a dominant player in the AI-era memory semiconductor market. The construction and expansion of M17 and P&T7 will dramatically increase the company's production capacity to meet global HBM demand and enable it to maintain its technological edge. This investment is also expected to have ripple effects throughout South Korea's semiconductor industry, benefiting related equipment and material manufacturers. Long-term, SK Hynix's HBM technological innovations are anticipated to form the backbone supporting the further evolution of AI and its widespread adoption across various industries.

Source: https://finance.biggo.com/news/e666959f-3828-44a1-b119-5dfdb45f39ad

#14 JCET Shares Soar on Major Investment in Advanced Chip Packaging Capabilities

Published June 25, 2026 Morningstar (Dow Jones News) China

OVERVIEW

Shares of China-based OSAT leader JCET Group surged following the announcement of a significant new investment in its advanced chip packaging capabilities. This investment aims to substantially expand capacity for cutting-edge packaging technologies to meet demand from high-growth markets like AI, HPC, and automotive. JCET plans to enhance its competitiveness in areas such as flip-chip, fan-out, and 2.5D/3D packaging, thereby elevating its position in the global supply chain. The market anticipates strong future revenue growth for the company.

IN DEPTH

Key Findings

The stock price of JCET Group (Jiangsu Changjiang Electronics Technology Co., Ltd.), a leading China-based outsourced semiconductor assembly and test (OSAT) provider, experienced a significant surge following the announcement of a major new investment plan in its advanced chip packaging capabilities. This investment represents a strategic move to address the escalating demand from rapidly growing sectors such as artificial intelligence (AI), high-performance computing (HPC), and the automotive industry.

Technical / Clinical Details

JCET's investment plan focuses on expanding production capacity for state-of-the-art packaging technologies, including Flip-Chip, Fan-Out, and 2.5D/3D packaging. These technologies are crucial for highly integrating multiple chip dies, improving data transfer speeds, and reducing power consumption. AI chips and HPC processors demand fine-pitch interconnections, superior thermal management, and complex System-in-Package (SiP) solutions. Through the deployment of new equipment, upgrades to existing lines, and increased R&D funding, JCET aims to establish technological leadership and deliver high-value-added packaging services that meet these stringent requirements.

Background & Context

In the global semiconductor industry, as front-end scaling approaches its physical limits, back-end advanced packaging has emerged as the new frontier for chip performance enhancement. The proliferation of AI, 5G, and IoT is accelerating demand for more complex and higher-performance chips, leading to severe shortages in advanced packaging capacity. The Chinese government is strongly promoting domestic semiconductor production and technological self-sufficiency, and investments in major domestic players like JCET are part of this national strategy. JCET's latest investment is a clear indication of China's determination to boost its global competitiveness in advanced packaging and play a significant role in the global supply chain.

Strategic Significance & Outlook

JCET's substantial investment is expected to accelerate its market share expansion and revenue growth in the advanced packaging market. With demand for AI and HPC chips projected to remain robust, JCET is strategically positioned to maximize the benefits from these high-growth markets through enhanced capabilities. This investment is also anticipated to strengthen the entire domestic semiconductor ecosystem in China, positively impacting equipment manufacturers and material suppliers. The surge in JCET's stock price reflects strong market confidence in the company's long-term growth prospects and the recognition that advanced packaging will drive the future of the semiconductor industry.

Source: https://www.morningstar.com/news/dow-jones/20260625791/jcet-shares-surge-on-advanced-chip-packaging-investment

Collected: July 03, 2026 | Automated Research System (Gemini API)

#15 Nomura Raises TSMC Target Price, Citing AI Infrastructure Cycle as Key Growth Driver

Published June 27, 2026 Futu News Taiwan

OVERVIEW

Nomura has upgraded TSMC's target price, attributing its strong growth to the accelerating AI infrastructure cycle. The surging demand for AI chips has led to TSMC's advanced packaging technologies, particularly CoWoS, significantly outstripping supply capacity. The report emphasizes TSMC's indispensable role in resolving AI market bottlenecks, noting its technological leadership and capacity expansion as primary drivers for the stock upgrade. TSMC is expected to lead the semiconductor industry in the AI era through continuous innovation in advanced packaging.

IN DEPTH

Key Findings

Nomura has raised its target price for TSMC, citing the powerful momentum of the AI (artificial intelligence) infrastructure cycle as a key driver of the company's accelerated growth. This analysis underscores the indispensable role of TSMC's advanced semiconductor manufacturing and packaging solutions in meeting the explosive demand for AI chips.

Technical / Clinical Details

The report highlights that TSMC's advanced packaging technologies, such as CoWoS (Chip-on-Wafer-on-Substrate), play a decisive role in enhancing AI chip performance and expanding supply capacity. CoWoS is a 2.5D packaging technology that high-densely integrates multiple logic dies and High Bandwidth Memory (HBM) on an interposer, essential for maximizing the processing power of AI processors. Nomura's analysts anticipate that TSMC will continue to aggressively expand its CoWoS production capacity and invest in cutting-edge packaging technologies to resolve AI chip bottlenecks and meet the demands of key customers like NVIDIA and AMD. This strategy further solidifies TSMC's central position in the AI chip supply chain.

Background & Context

The rapid advancement of generative AI and large language models (LLMs) has pushed demand for AI accelerators in data centers to unprecedented levels. However, the manufacturing of high-performance AI chips is significantly constrained not only by front-end scaling but also by back-end advanced packaging capabilities. In the current market, the shortage of advanced packaging like CoWoS is one of the most severe bottlenecks, being a primary cause of AI chip supply delays and cost increases. TSMC, with its long-standing expertise in semiconductor manufacturing and massive investments in advanced packaging technologies, is positioned as the most crucial company for resolving this bottleneck.

Strategic Significance & Outlook

Nomura's upgrade of TSMC's target price reflects strong market expectations for the structural changes brought about by the AI infrastructure cycle and TSMC's strategic role within it. TSMC is expected to remain a core company driving the growth of the AI chip market by continuing to invest in and expand capacity for advanced packaging technologies, particularly CoWoS and its evolutions. This trend will also create significant business opportunities for related equipment and material suppliers, further accelerating technological innovation and growth across the entire semiconductor ecosystem. TSMC's continuous innovation will be an indispensable factor in strengthening the technological foundation of the AI era.

Source: https://news.futunn.com/en/post/75365973/nomura-commentary-raises-tsmc-target-price-ai-infrastructure-cycle-has

Collected: July 03, 2026 | Automated Research System (Gemini API)

#16 Kioxia Accelerates Next-Gen Memory Mass Production Amid AI Boom, Poised for Dramatic Comeback

Published June 26, 2026 Channel News Asia Japan

OVERVIEW

Japanese memory semiconductor giant Kioxia is accelerating preparations for mass production of next-generation memory products, driven by the explosive demand for AI technology. The company aims to strengthen its production capacity for high-performance NAND flash memory, including HBM, to provide high-speed, high-capacity storage solutions vital for AI data processing. This move underpins a dramatic recovery from past market downturns, positioning Kioxia to re-emerge as a key player in the AI-era memory market. Advanced packaging technologies are also contributing to enhanced product performance and reliability.

IN DEPTH

Key Findings

Kioxia, a leading Japanese memory semiconductor manufacturer, is accelerating its preparations for mass production of next-generation memory products, aiming to capitalize on the unprecedented demand driven by the explosive growth of artificial intelligence (AI) technology. This strategic initiative marks a crucial milestone for the company to achieve a dramatic recovery from past market downturns and re-establish itself as a key player in the AI-era memory market.

Technical / Clinical Details

Kioxia is primarily focusing on high-performance NAND flash memory and a broader portfolio of next-generation memory, including High Bandwidth Memory (HBM) in the future. AI applications demand massive amounts of high-speed data read/write capabilities and large storage capacities, and Kioxia's new memory products are engineered to meet these stringent requirements. Specifically, the company is further increasing the stacking layers of its 3D NAND technology to improve data density and I/O performance, thereby offering optimal solutions for AI data centers and edge AI devices. To enhance the reliability and efficiency of these high-performance memory products, advanced packaging technologies, such as chiplet integration and sophisticated thermal management solutions, are also being developed and adopted. The goal is to resolve bottlenecks between memory and processors, thereby improving the overall performance of AI systems.

Background & Context

For several years, the memory semiconductor market faced an oversupply and price downturn, leading to challenging business conditions for many manufacturers, including Kioxia. However, entering 2026, demand from sectors such as AI, data centers, and automotive has surged, putting the memory market on a recovery trajectory. HBM, in particular, has seen explosive growth in demand as an indispensable component for AI accelerators, strongly fueling Kioxia's recovery and growth. Kioxia is seizing this shift in market conditions to re-establish its market leadership through technological innovation and production capacity expansion.

Strategic Significance & Outlook

Kioxia's accelerated preparations for next-generation memory mass production are an indispensable element in supporting the development of the AI industry. The company will continue to invest in advanced memory technologies, including HBM, and strengthen collaborations with AI chip manufacturers to meet the diverse needs of the AI market. This will enable Kioxia to secure stable revenue streams and achieve sustainable growth, while also contributing to strengthening Japan's international competitiveness in the semiconductor industry. Long-term, Kioxia's memory technology innovations are anticipated to form the foundational infrastructure supporting the further evolution of AI and its widespread adoption across various industries.

Source: https://www.channelnewsasia.com/business/kioxia-readies-next-gen-memory-mass-production-ai-boom-fuels-dramatic-comeback-6229061

Collected: July 03, 2026 | Automated Research System (Gemini API)

#17 TSMC's CoWoS Packaging Equipment Supply Chain Sees Robust Demand Amid AI Surge

Published June 30, 2026 DigiTimes Taiwan

OVERVIEW

TSMC's CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging equipment supply chain is experiencing extremely strong demand, driven by the explosive growth of AI chips. Key equipment manufacturers are ramping up production to meet TSMC's requests for increased CoWoS capacity. This situation highlights the critical importance of advanced packaging in the AI era and underscores how its supply capacity is currently the most severe bottleneck in the semiconductor industry. The entire supply chain is accelerating investments to address this rising demand.

IN DEPTH

Key Findings

The manufacturing equipment supply chain for TSMC's advanced packaging technology, particularly CoWoS (Chip-on-Wafer-on-Substrate), is experiencing exceptionally strong demand. This surge is directly attributed to the explosive growth in demand for artificial intelligence (AI) chips, prompting major equipment manufacturers to significantly boost their production capacities to meet TSMC's requirements.

Technical / Clinical Details

CoWoS is a 2.5D packaging technology that integrates multiple logic dies and High Bandwidth Memory (HBM) onto a silicon interposer, which is then mounted onto a package substrate. This technology is indispensable for maximizing data transfer speeds and bandwidth between AI processors and memory, and it is widely adopted in high-performance AI chips such as NVIDIA's GPUs. CoWoS manufacturing requires a diverse array of specialized equipment, including high-precision die bonders, micro-bump formation tools, lithography systems, and inspection machines. The current supply chain struggles to keep pace with demand for these expensive and time-consuming-to-manufacture tools. Key players like Japan's Disco and SCREEN, and U.S.-based Applied Materials and Lam Research, hold crucial roles in CoWoS production lines.

Background & Context

The increasing complexity of AI models and data volumes has dramatically elevated the role of packaging in determining AI chip performance. While TSMC has long maintained a leading position in advanced packaging, it now faces a situation where AI chip demand far outstrips its supply capacity. This CoWoS capacity bottleneck is a major factor delaying AI chip time-to-market and hindering overall industry growth. In response to strong customer requests, TSMC is actively planning to expand its CoWoS production capacity, which in turn drives robust demand for equipment suppliers.

Strategic Significance & Outlook

The intense demand on the CoWoS manufacturing equipment supply chain underscores that strengthening advanced packaging capabilities is essential for supporting the sustained growth of the AI industry. Equipment manufacturers are expected to accelerate R&D and production investments to meet TSMC's requirements. This will lead to a gradual expansion of CoWoS production capacity, and a corresponding easing of AI chip supply shortages. Long-term, further evolution of CoWoS technology and competition from alternative solutions like Fan-out Panel-Level Packaging (FOPLP) are anticipated to drive innovation across the advanced packaging market, further strengthening the AI-era semiconductor ecosystem.

Source: https://www.digitimes.com/news/a20260630PD239/tsmc-supply-chain-cowos-packaging-equipment.html

#18 Applied Materials Unveils Six New Systems to Accelerate AI Chip DRAM & Advanced Packaging, Featuring Sub-10nm Defect Detection

Published Published June 25, 2026   Applied Materials (プレスリリース)   USA

OVERVIEW

Applied Materials has launched six innovative systems to significantly accelerate the development and manufacturing of DRAM and advanced packaging for next-generation AI chips. These solutions tackle critical challenges in HBM, 3D stacking, and chiplet architectures across epitaxy, CMP, deposition, and eBeam metrology. Crucially, a new eBeam defect review system achieves sub-10nm sensitivity, promising unprecedented improvements in process control and yield for complex 3D packaging, ultimately enhancing AI chip performance and power efficiency.

IN DEPTH

Background

As AI capabilities rapidly advance, the demand for increased memory bandwidth and power efficiency in AI chips has become paramount. With traditional 2D chip designs nearing their physical limits, advanced packaging technologies such as High Bandwidth Memory (HBM), 3D stacking, and chiplet architectures are crucial for overcoming these constraints, directly addressing the 'memory wall' challenge. Applied Materials' strategy focuses on bringing wafer-fab-level precision process control to memory manufacturing to meet these evolving technological demands, ensuring that physical design can keep pace with computational advancements.

Key Findings

In response to these escalating demands, Applied Materials has launched six innovative new systems aimed at enhancing performance and manufacturing efficiency for next-generation AI chips, specifically targeting DRAM and advanced packaging. These systems are engineered to resolve manufacturing hurdles in advanced chip architectures like HBM and 3D stacking.

- **Enhanced Centura Prime Epi System:** Delivers logic-class fabrication precision for next-generation DRAM perimeter transistors.
- **Opta Quad CMP System:** Addresses uniformity and yield challenges in thick, non-uniform packaging structures critical for HBM and 3D stacking. This system is engineered for superior planarization.
- **Nokota VMax 2 ECD and Producer Avila 2 PECVD Systems:** These deposition technologies enable high-yield chip stacking for 3D stacking and HBM architectures, ensuring robust interconnections.
- **VeritySEM 7AP CD Metrology System:** An eBeam-based metrology system that enhances process control in advanced packaging, providing critical dimension measurements with high accuracy.
- **SEMVision G7AP Defect Analysis System:** This eBeam system detects microscopic defects in 3D packaging with sub-10 nanometer sensitivity, revolutionizing defect review. It allows for early identification and resolution of issues, significantly improving overall manufacturing yield in increasingly complex processes.

These new systems are poised to expand AI chip production capacity and potentially reduce manufacturing costs. The high-precision defect detection, particularly from the eBeam systems, is expected to dramatically improve yields in complex packaging processes, contributing to a more stable supply of next-generation AI accelerators. This technological leap is critical for accelerating the broader adoption and further development of AI applications, strengthening the entire AI hardware ecosystem. The ability to precisely control and verify advanced packaging processes sets a new industry benchmark, enabling more robust and higher-performing AI solutions.

Source: https://ir.appliedmaterials.com/static-files/97be2049-edfd-4399-b6ca-ffa0e8ea464f

#19 Samsung Allocates Half HBM Production to HBM4, Achieving $1 Billion Sales in 4 Months, Targets Optical HBM Mass Production by 2028

Published Published July 02, 2026 Samsung (プレスリリース) South Korea

OVERVIEW

Samsung Electronics has aggressively pivoted half of its High Bandwidth Memory (HBM) production capacity to HBM4, achieving over $1 billion in sales within four months and projecting $10 billion annually by year-end. This strategic move, which includes pausing HBM3E production, aims to reclaim HBM market leadership and solidify its position in the AI era. Samsung also unveiled HBM4E and LPDDR5X-based SOCAMM2 modules at COMPUTEX 2026, alongside plans for optical HBM mass production by 2028.

IN DEPTH

Key Findings

Samsung Electronics has strategically committed half of its High Bandwidth Memory (HBM) production capacity to the next-generation HBM4, achieving over $1 billion in sales within just four months of its global debut in February 2026. The company projects annual HBM4 sales to reach $10 billion by the end of the year, signaling an aggressive push to reclaim leadership in the burgeoning HBM market. To facilitate this accelerated ramp-up, production of HBM3E, currently experiencing lower demand, has been temporarily halted, with resources reallocated to HBM4.

Technical & Product Details

- **HBM4 Focus:** Samsung is dedicating approximately 75,000 of its 150,000 monthly HBM DRAM wafer production capacity to HBM4. This significant strategic prioritization directly addresses the critical role HBM4 is expected to play in NVIDIA's forthcoming next-generation AI platform, 'Rubin.'
- **COMPUTEX 2026 Showcase:** At COMPUTEX 2026, Samsung showcased the HBM4E along with its LPDDR5X-based SOCAMM2 server module. The HBM4E features a cutting-edge 1c DRAM-based core die and a base die manufactured using Samsung Foundry's advanced 4nm process technology. It supports data rates up to 14Gbps per pin, with a clear roadmap for scalability to 16Gbps, enabling aggregate bandwidth exceeding 4TB/s.
- **HBM Economics:** HBM economics are increasingly critical: HBM stacks represent approximately 34-45% of the total manufacturing cost for AI accelerators, a figure projected to exceed 45% for Blackwell-generation chips. Consequently, HBM yield and rigorous qualification processes are direct determinants of system-level economics. Samsung is reportedly navigating some initial challenges in HBM4 yield and qualification, which it aims to resolve through aggressive investment and optimization.

- **Optical HBM Roadmap:** Samsung further outlined an ambitious roadmap for mass production of optical HBM, targeting 2028. This innovative approach entails integrating silicon photonics technology directly within HBM stacks and processor packages. The goal is to achieve dramatic improvements in bandwidth and energy efficiency by transcending the inherent limitations of traditional electrical signaling. This push aligns with broader industry trends, including Qualcomm's High Bandwidth Compute (HBC) concept and NVIDIA's SOCAMM specification for modularizing LPDDR memory in server CPUs.

Background & Industry Context

The escalating complexity and scale of artificial intelligence models demand immense data processing capabilities and unprecedented memory bandwidth for AI accelerators. Consequently, high-bandwidth memory (HBM) has emerged as a critical bottleneck and a strategic component in the AI chip supply chain. Samsung's aggressive investment in HBM4 is designed to fortify its competitive position in the high-stakes AI memory market, serving not only a pivotal client like NVIDIA but also major cloud hyperscalers—such as Google, Amazon, and Microsoft—that are increasingly developing their custom AI accelerators.

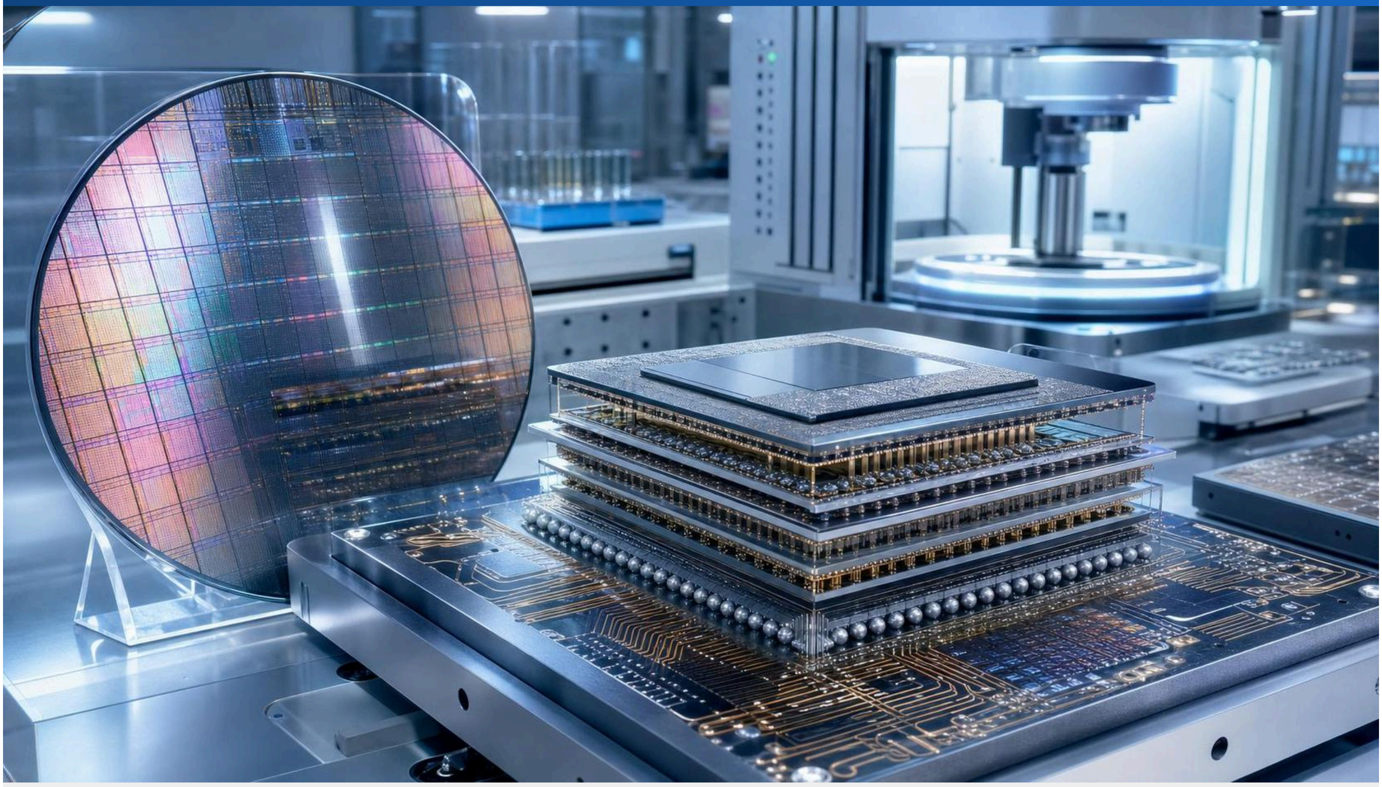
Strategic Significance & Outlook

Samsung's aggressive expansion of HBM4 production capacity, coupled with its forward-looking roadmap encompassing HBM4E, SOCAMM2, and especially optical HBM, is poised to significantly strengthen its competitive stance in the burgeoning AI semiconductor market. Optical HBM, in particular, holds transformative potential, capable of revolutionizing AI chip performance by transcending current electrical transmission limitations and marking a crucial milestone for future technological innovation. The consistent supply and continuous performance improvement of HBM are indispensable factors for the sustained evolution and widespread adoption of AI technologies, thereby solidifying Samsung's critical role as a key enabler of the ongoing AI revolution.

Source: https://semiconductor.samsung.com/news-events/tech-blog/samsung-showcases-nextgenerationa-ai-semiconductor-innovations-at-computex-2026/

#20 EU Chips Act Funds €210 Million for 3D IC Advanced Packaging, Benefiting Infineon, ASML Subsidiary, and Soitec

Published June 25, 2026 Qishuai-cn Germany



OVERVIEW

The European Commission announced its first EU Chips Act-funded project, allocating a total of €210 million to Germany's Infineon, an ASML subsidiary in the Netherlands, and France's Soitec. This funding is dedicated to 3D IC heterogeneous integration and advanced packaging development, with the resulting technologies mandated to be accessible to certified EU suppliers. This initiative aims to create new opportunities for IC packaging material and advanced substrate suppliers, bolstering Europe's semiconductor autonomy.

IN DEPTH

Key Findings

The European Commission has unveiled the first major project to receive funding under the EU Chips Act, allocating a total of €210 million (approximately $225 million USD) to German semiconductor giant Infineon, a subsidiary of Dutch semiconductor equipment leader ASML, and French materials manufacturer Soitec. This significant investment is specifically targeted at the development of next-generation 3D IC heterogeneous integration and advanced packaging technologies.

Technical Details

- **Funding Allocation:** The grants will be utilized for research and development aimed at achieving highly efficient and high-performance 3D IC architectures. This includes technologies for vertically or horizontally integrating multiple chips (e.g., processors, memory, sensors) within a single package.
- **Heterogeneous Integration:** This technology seeks to enhance system performance, reduce power consumption, and optimize manufacturing costs by combining chiplets produced using different fabrication processes. Specific advancements include heterogeneous integration using Fan-Out Wafer-Level Packaging (FOWLP) for GaN and Si chiplets, and the development of reliable interconnection technologies utilizing electrolytic indium bumps.
- **Access Requirements:** A key condition of this project is that the technologies developed must be made available to certified suppliers within the EU. This mandate is part of the EU's broader strategy to enhance the competitiveness of its entire semiconductor supply chain and ensure technological autonomy in critical areas.

Background & Industry Context

The EU Chips Act is a massive initiative, committing €43 billion in public and private investment by 2030, aimed at strengthening Europe's position in the global semiconductor supply chain and safeguarding against geopolitical risks. With the escalating demand for AI and High-Performance Computing (HPC), advanced packaging has emerged as a primary means to improve system performance as transistor scaling approaches its physical limits. This funding represents a crucial step in bolstering Europe's technological foundation and fostering innovation in this vital sector.

Strategic Significance & Outlook

This substantial financial injection is expected to generate new business opportunities within the European semiconductor ecosystem, particularly for IC packaging material and advanced substrate suppliers. Infineon, the ASML subsidiary, and Soitec will lead this project, forming a cornerstone for Europe to enhance its presence as a significant player in the global semiconductor race. The technologies developed are anticipated to contribute to next-generation electronic devices across various sectors, including data centers, automotive, and industrial IoT, thereby accelerating the overall digitalization of the European economy.

Source: https://www.qishuai-cn.com/news/Specialty_Chemicals/Specialty_Polymers_for_IC_Packaging/EU_Chips_Act_Funds_210M_for_3D_IC_

#21 Fraunhofer Develops DUV-Assisted Athermal Laser Grooving for Low-κ Dielectrics in Advanced Packaging

Published June 29, 2026 Karriere Fraunhofer-Gesellschaft Germany

OVERVIEW

Fraunhofer ILT is exploring a novel dual-pulse approach, DUV-assisted athermal laser grooving, for low-κ dielectrics in advanced microelectronics packaging. This technology temporarily generates free carriers within low-κ materials using a DUV pulse, enabling subsequent laser pulses to remove layers without damaging the substrate. This enhances precision and reliability for the microfabrication crucial for next-generation high-performance semiconductor packaging.

IN DEPTH

Key Findings

Fraunhofer ILT is advancing research into an innovative "DUV-assisted athermal laser grooving" technology for the microfabrication of low-κ dielectric materials, which are essential for advanced microelectronics packaging. This novel dual-pulse approach allows for high-precision material removal while minimizing thermal damage to the substrate.

Technical Details

- **Dual-Pulse Approach:** The technology begins with a Deep Ultraviolet (DUV) laser pulse that delivers energy exceeding the bandgap of the low-κ material, temporarily generating free carriers (electrons and holes) within it. This alters the material's electrical properties, making it absorptive to a subsequent laser pulse, whereas it would normally be transparent.
- **Athermal Processing:** A second laser pulse, precisely timed after the free carrier generation, selectively removes the modified layer without inducing thermal damage to the underlying substrate. Traditional laser processing often struggles with heat-affected zone damage; this athermal approach ensures high-precision grooving while maintaining the structural integrity of delicate low-κ materials.
- **Importance of Low-κ Materials:** Low-κ dielectrics are crucial for reducing signal delay and power loss within microelectronic chips. In advanced packaging, particularly 3D ICs and chiplet integration, the ability to precisely microfabricate these materials without damage directly impacts overall performance and reliability.

Background & Industry Context

The evolution of AI and High-Performance Computing (HPC) has dramatically increased semiconductor chip integration density and operating frequencies. Consequently, interconnect capacitance within chips has become a significant source of signal delay and crosstalk, limiting overall chip performance. Low-κ dielectrics were introduced to mitigate this issue, but their inherent mechanical weakness and thermal fragility have made them extremely challenging to process. Therefore, the development of non-destructive and high-precision fabrication techniques is an urgent industry imperative.

Strategic Significance & Outlook

This DUV-assisted athermal laser grooving technology has the potential to solve long-standing challenges in low-κ material processing, contributing to the realization of next-generation ultra-dense, high-performance semiconductor packaging. By paving the way for smaller, faster, and more power-efficient AI chips and HPC systems, it will drive innovation across a wide range of electronic device sectors. Future research will focus on improving processing speed, scalability, and applicability to various low-κ materials, solidifying its role as a key enabling technology for future microelectronics.

Source: https://jobs.fraunhofer.de/job/Aachen-Thesis-DUV-Assisted-Athermal-Laser-Grooving-of-Low-%CE%BA-Dielectrics-for-Advanced-Packaging-52074/1409293533/

Collected: July 03, 2026 | Automated Research System (Gemini API)

#22 China's CXMT Faces Technical Hurdles in HBM Production; Yield and Advanced Packaging Improvements Key for 2027-2028 Acceleration

Published Published July 02, 2026 South China Morning Post (SemiAnalysis引用) China

OVERVIEW

Chinese DRAM manufacturer CXMT continues to grapple with significant technical challenges in establishing stable commercial production of High Bandwidth Memory (HBM), according to SemiAnalysis. While demonstrating progress in core DRAM processes, the firm critically needs advancements in wafer yield, chip stacking, and advanced packaging to compete with global HBM leaders. SemiAnalysis forecasts a substantial acceleration in CXMT's HBM wafer capacity beginning in 2027-2028, indicating potential breakthroughs in this period.

IN DEPTH

Background

The rapid advancements in AI, High-Performance Computing (HPC), and data centers demand ultra-high bandwidths that conventional memory solutions cannot provide, making HBM an indispensable component. Currently, the HBM market is largely dominated by three players: SK Hynix, Samsung, and Micron, with SK Hynix holding a leading position due to early qualification with NVIDIA platforms. Amidst U.S. export restrictions limiting access to advanced semiconductor technologies, China has made establishing indigenous HBM technology one of its top national strategic priorities.

Key Findings

According to an analysis by SemiAnalysis, CXMT (Changxin Memory Technologies), a Chinese DRAM manufacturer, is still encountering significant technical hurdles in establishing a stable commercial supply of High Bandwidth Memory (HBM). While the company has demonstrated progress in its DRAM process technology, the report highlights that substantial improvements in wafer yield, chip stacking techniques, and advanced packaging capabilities are urgently needed for CXMT to effectively compete with leading global players in this advanced memory sector.

Technical Challenges & Future Outlook

- **Complexity of HBM Production:** HBM features an extremely complex architecture involving the vertical stacking of multiple DRAM dies interconnected through minuscule Through-Silicon Vias (TSVs). Achieving high-performance HBM products demands impeccable precision across all stages: individual die quality (yield), accurate stacking, and final packaging (thermal management, electrical connections).
- **CXMT's Challenges:** CXMT is specifically cited for struggles with low HBM wafer yields, immature stacking technology, and insufficient advanced packaging capabilities, which are impeding its full entry into the market. These challenges potentially increase HBM production costs and compromise product reliability.

- **Future Outlook:** SemiAnalysis forecasts an acceleration in CXMT's HBM wafer production capacity in 2027 and 2028, suggesting that significant progress in overcoming these technical challenges might be achieved during this period. This acceleration is likely driven by China's national push for semiconductor self-sufficiency and the rising domestic demand for HBM from its burgeoning AI industry.

Strategic Implications & Global Impact

CXMT's ability to overcome its technical challenges in HBM and achieve stable supply will significantly impact the future of China's AI and HPC industries, and potentially diversify the global semiconductor supply chain. Crucially, improvements in wafer yield and the mastery of advanced packaging technologies, including TSV and micro-bump interconnections, will be key for the company to gain competitiveness in the HBM market. Such developments could also strengthen the overall HBM supply ecosystem and potentially foster greater price competition globally.

Source: https://amp.scmp.com/tech/big-tech/article/3359168/inside-cxmts-us43b-ipo-soaring-profits-meet-us-export-threat-and-high-stakes-hbm-race

#23 CHIPS Act Successfully Attracts Taiwanese Semiconductor Suppliers to US, Creating New Opportunities in Advanced Packaging and Materials Supply

Published July 01, 2026 Fidelity Investments USA

OVERVIEW

The U.S. CHIPS Act's $39 billion manufacturing incentives are successfully drawing Taiwan-based semiconductor manufacturers to the United States, providing concrete economic reasons for establishing new facilities or partnering with U.S. entities. The CHIPS for America program also funds manufacturing, advanced packaging, equipment, and materials production, bolstering U.S. semiconductor supply chain resilience and fostering new opportunities in cutting-edge technological fields.

IN DEPTH

Key Findings

The $39 billion in manufacturing incentives provided by the U.S. CHIPS Act are serving as a powerful economic catalyst, successfully attracting leading Taiwan-based semiconductor manufacturers to the United States. This policy aims to strengthen America's semiconductor manufacturing capabilities and create new opportunities, particularly in advanced packaging, manufacturing equipment, and materials production.

Technical & Strategic Details

- **CHIPS Act Incentives:** The "CHIPS for America" program offers substantial financial support to companies constructing semiconductor manufacturing facilities within the U.S. This initiative is designed not only to boost manufacturing capacity but also to strengthen the entire supply chain, with funding directed across a wide range of areas including advanced packaging, manufacturing equipment, and semiconductor materials production.
- **Attraction of Taiwanese Companies:** Leading foundry companies like TSMC are advancing plans to build large-scale factories in Arizona, U.S. Following suit, numerous companies within Taiwan's semiconductor ecosystem are actively considering and executing plans to establish operations or partner with existing U.S. companies. Policy support, alongside considerations of cost reduction and market access, is a significant driving factor.
- **Enhancing Supply Chain Resilience:** The current semiconductor supply chain, concentrated in specific regions, is vulnerable to geopolitical risks and natural disasters. The CHIPS Act aims to decentralize this risk and build a more robust and secure domestic supply chain, with a particular focus on bringing advanced semiconductor manufacturing capabilities back to the U.S.

Background & Industry Context

Semiconductors form the foundation of virtually all modern technology, and their supply stability is recognized as a paramount national security issue. Over the past few decades, global semiconductor manufacturing capacity has tended to concentrate in Asia, especially Taiwan. However, the U.S.-China technology rivalry and supply chain disruptions caused by the COVID-19 pandemic have prompted many nations to bolster their domestic manufacturing capabilities. The U.S. aims to re-establish its global leadership in semiconductor manufacturing through the CHIPS Act.

Strategic Significance & Outlook

The incentives offered by the CHIPS Act are expected to revitalize the U.S. semiconductor industry and foster innovation across diverse semiconductor technology sectors. The establishment of Taiwanese companies in the U.S. promises technology transfer, job creation, and closer collaborative relationships. Advanced packaging technology, in particular, is a critical factor determining the performance of high-performance semiconductors like AI chips, and strengthening domestic capabilities in this area is essential for enhancing U.S. technological autonomy and competitiveness. However, the higher costs associated with manufacturing in the U.S. will be a critical factor to watch regarding long-term global market competitiveness.

Source: https://www.fidelity.com/news/article/technology/202607010830PRIMZONEFULLFEED9755329