

# Semiconductor\_BackEnd

## Weekly Intelligence Report

2026-07-12 | 18 articles | 7 countries  
troy-technical.jp

This Week's Keyword

## AI Packaging Bottleneck

HBM, CoWoS, & Substrate Supply Crunch Intensifies

18

articles

Total Articles Analyzed

7

countries

Source Countries/Regions

\$252.5B

USD

SK/Samsung Pkg Investment

93%

surge

CoWoS Demand Forecast

### All 18 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

| #   | Article Title             | Type               | Tech Novelty                                                       | Market Proximity                                                   | Market Impact                                                      | Data Reliability                                                   | US/EU Relevance                                                    | Summary                                                                                                                                                                   |
|-----|---------------------------|--------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|--------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #01 | Lam AI Pkg & Panel        | Corporate Strategy | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | Lam Research highlights advanced packaging, chiplets, and panel-based manufacturing as critical for AI performance and power efficiency, with Salzburg leading.           |
| #02 | Nvidia Blackwell Prod     | New Product        | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | Nvidia begins volume production of Blackwell AI accelerators using TSMC's CoWoS-L, but supply will remain tight through Q4 2026 due to HBM3E and substrate shortages.     |
| #03 | Amkor \$3B US Pkg         | Corporate Strategy | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | Amkor Technology commits \$2.5-3.0B to advanced packaging facilities in Arizona and Korea, with the Arizona plant starting production in 2028 to meet AI demand.          |
| #04 | Korea \$252B HBM Pkg      | Corporate Strategy | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | Samsung and SK Group invest \$252.5B in Chungcheong Province for HBM manufacturing and advanced packaging, aiming to establish a global AI semiconductor hub.             |
| #05 | AT&S; AI Substrate Prod   | New Product        | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | AT&S; begins high-volume production of advanced AI substrates at its Malaysia plant, backed by customer commitments, projecting 45-55% revenue growth.                    |
| #06 | TSMC CoWoS Expansion      | Corporate Strategy | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | TSMC plans to nearly quadruple CoWoS capacity by end 2026 and produce 14-reticle packages by 2028, but supply still lags AI demand.                                       |
| #07 | HBM & ABF Shortages       | Market Report      | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | Critical shortages of HBM and Ajinomoto Build-up Film (ABF) are intensifying AI chip supply bottlenecks, with ABF facing a 20% gap by 2027.                               |
| #08 | Lasers & Glass Bottleneck | Trend Article      | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | AI memory shortage triggers advanced packaging crisis, with ultrafast lasers and glass substrates emerging as new bottlenecks due to thermal demands.                     |
| #09 | AT&S; Fehring PCB Hub     | Corporate Strategy | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | AT&S; invests €10M in its Austrian Fehring plant to strengthen its PCB business and expand expertise in power/thermal management, transforming it into an innovation hub. |
| #10 | Micron HBM Expansion      | Corporate Strategy | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | <div><div></div><div></div><div></div><div></div><div></div></div> | Micron invests \$9.3B in Hiroshima for HBM production by 2028 and expands packaging capacity in Singapore, addressing HBM as a strategic AI bottleneck.                   |

| #   | Article Title          | Type               | Tech Novelty | Market Proximity | Market Impact | Data Reliability | US/EU Relevance | Summary                                                                                                                                                                           |
|-----|------------------------|--------------------|--------------|------------------|---------------|------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| #11 | KITECH 4x HBM Density  | Research           | ●●●●●<br>●   | ●○○○○<br>○       | ●●●●○<br>○    | ●●●●●<br>●       | ●●●●○<br>○      | Korea Institute of Industrial Technology develops a novel chip integration process achieving approximately four times the integration density of commercial HBM.                  |
| #12 | HBM Hybrid Delay       | Analysis           | ●●●●○<br>○   | ●●●●○<br>○       | ●●●●●<br>○    | ●●●●○<br>○       | ●●●●●<br>○      | Samsung and SK hynix are reportedly reconsidering the timeline for widespread hybrid bonding in HBM, possibly delaying adoption until 16-high HBM4E.                              |
| #13 | Intel EMIB-T & XBM     | New Technology     | ●●●●●<br>○   | ●●●●○<br>○       | ●●●●●<br>○    | ●●●●○<br>○       | ●●●●●<br>●      | Intel's EMIB-T emerges as a CoWoS alternative for AI accelerators, and a new XBM memory architecture aims to alleviate the AI memory bottleneck by ditching silicon interposers.  |
| #14 | CoWoS Demand Surge     | Market Report      | ●○○○○<br>○   | ●●●●●<br>●       | ●●●●●<br>●    | ●●●●○<br>○       | ●●●●●<br>●      | Morgan Stanley forecasts a 93% surge in CoWoS demand by 2027, with Nvidia remaining the largest consumer and AMD's Venice CPU anticipated to adopt CoWoS.                         |
| #15 | China HBM/HB Advance   | Corporate Strategy | ●●●●●<br>○   | ●●●●○<br>○       | ●●●●●<br>○    | ●●●●○<br>○       | ●●●●●<br>○      | China's memory industry accelerates HBM3/3E development, with YMTC leading in wafer-to-wafer hybrid bonding patents, signaling global supply chain restructuring.                 |
| #16 | Micron HBM Orders Full | Market Report      | ●○○○○<br>○   | ●●●●●<br>●       | ●●●●●<br>●    | ●●●●○<br>○       | ●●●●●<br>●      | Micron's HBM order book is fully committed through 2028, securing silicon wafer supply with a 10-year GlobalWafers off-take agreement, indicating supply is the constraint.       |
| #17 | HLSI & Co-Pkg Optics   | Trend Article      | ●●●●●<br>○   | ●●●●●<br>○       | ●●●●●<br>●    | ●●●●○<br>○       | ●●●●●<br>●      | Semiconductor industry pivots to Heterogeneous Large-Scale Integration (HLSI) and Co-Packaged Optics (CPO) as AI reshapes chip design, pushing beyond copper interconnect limits. |
| #18 | SK Hynix EUV & Indiana | Corporate Strategy | ●●●●○<br>○   | ●●●●○<br>○       | ●●●●●<br>●    | ●●●●○<br>○       | ●●●●●<br>●      | SK hynix invests heavily in ASML EUV for HBM production in Korea and a \$4B advanced packaging facility in Indiana, bolstering HBM supply and tech leadership.                    |

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article



## Three Questions That Demand Your Decision This Week

### ❶ Is your AI strategy resilient to HBM/CoWoS bottlenecks?

Nvidia's Blackwell production is constrained by HBM3E and substrate shortages, and TSMC's CoWoS capacity remains tight despite massive expansion. Morgan Stanley forecasts a 93% CoWoS demand surge by 2027. Does your procurement strategy account for these critical supply limitations through 2028?

### ❷ Are your advanced packaging roadmaps competitive with Intel's alternatives?

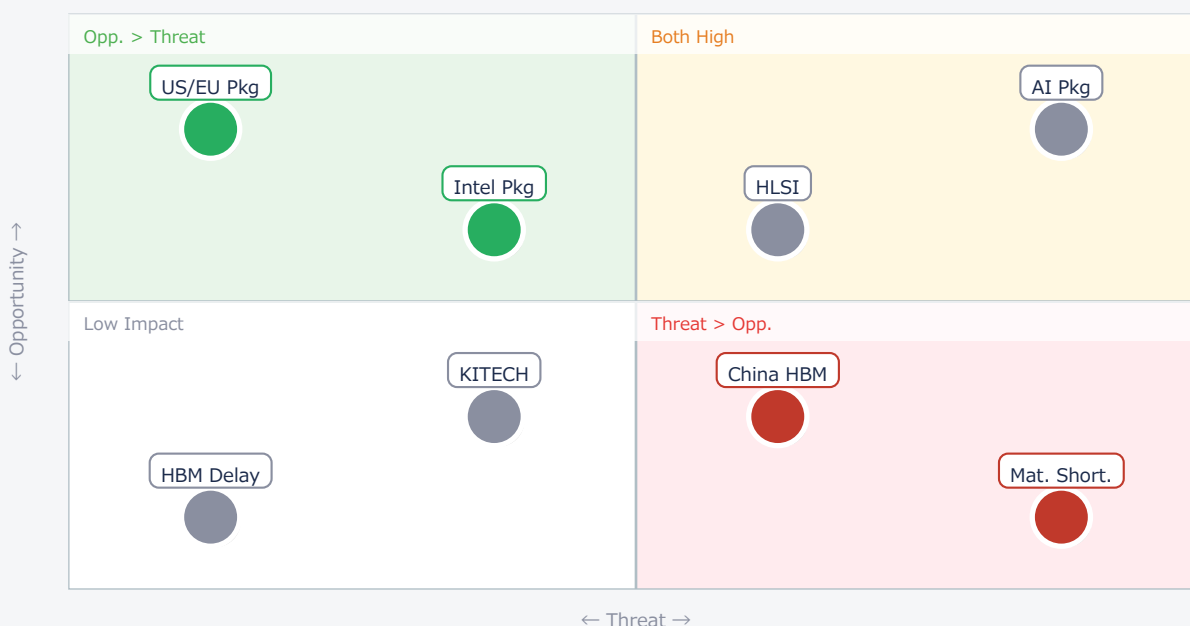
Intel's EMIB-T is emerging as a credible CoWoS alternative, targeting certification by late 2026, and its patented XBM architecture aims to eliminate costly silicon interposers. Does your R&D; team actively evaluate these US-based innovations to diversify packaging options and reduce reliance on dominant Asian suppliers?

### ❸ How will China's HBM/hybrid bonding advances impact your market share?

China's CXMT is accelerating HBM3/3E development, and YMTC leads in wafer-to-wafer hybrid bonding patents. This signals a restructuring of the global memory supply chain. Have you assessed the competitive threat and potential for market disruption from these rapidly advancing Chinese players?

## Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



| Item          | Quadrant | ↑ Opportunity     | ↓ Threat        |
|---------------|----------|-------------------|-----------------|
| ● AI Pkg      | Critical | Market share gain | Supply crunch   |
| ● US/EU Pkg   | Opp.     | Local capacity    | Global comp.    |
| ● Mat. Short. | Threat   | Alt. supply       | Production halt |
| ● Intel Pkg   | Opp.     | New tech          | CoWoS comp.     |
| ● China HBM   | Threat   | IP licensing      | Market erosion  |
| ● HLSI        | Critical | New arch.         | Design shift    |
| ● HBM Delay   | Ref.     | TCB focus         | Roadmap shift   |

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|          |      |           |                |
|----------|------|-----------|----------------|
| ● KITECH | Ref. | Future IP | Long-term R&D; |
|----------|------|-----------|----------------|

## Deep Dive ① — Nvidia Blackwell Production & CoWoS-L

#02 | 2026/07/02 | MetalSemi Asia | Tech Novelty●●●○○ Proximity●●●●● Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●●

Nvidia has commenced high-volume production of its next-generation Blackwell AI accelerators using TSMC's 4NP process and advanced CoWoS-L packaging. This move solidifies Nvidia's AI market leadership, but demand is projected to outstrip supply through Q4 2026.

The primary bottlenecks are shortages in HBM3E memory and complex substrate materials, despite TSMC prioritizing CoWoS capacity for Nvidia. CoWoS-L enables seamless integration of compute dies and HBM3E stacks for ultra-high bandwidth and power efficiency.

### ► Strategic Analyst's Perspective

Strategic Analyst's Perspective: The commencement of Blackwell production is a critical milestone, but the persistent HBM and substrate shortages are a realistic and immediate concern. This highlights the fragility of the advanced packaging supply chain. [Opportunity] for US/EU materials and equipment suppliers who can rapidly scale production of HBM components and high-performance substrates. [Threat] of continued reliance on Asian packaging capacity and potential delays in AI infrastructure deployment for US/EU OEMs. Next Actions: [Procurement] must secure long-term HBM and substrate contracts immediately. [R&D;] should explore alternative materials and packaging designs to reduce dependency by Q4 2026.

## Deep Dive ② — Intel's EMIB-T & XBM Memory Architecture

#13 | 2026/07/07 | Tom's Hardware | Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○ Data Reliability●●●○○ US/EU Relevance●●●●●

Intel's EMIB-T (Embedded Multi-die Interconnect Bridge-Tile) 2.5D packaging technology is emerging as a credible alternative to TSMC's CoWoS for large-package AI accelerators, expanding validation for 36/35 μm bump pitch to 4.5x reticle silicon packages, targeting certification by late 2026.

Additionally, Intel has patented a new XBM (eXtended Bandwidth Memory) architecture that eliminates HBM's costly silicon interposer. XBM utilizes a backend-transistor DRAM stack with UCIe links and built-in repair capabilities, demonstrating a multi-faceted approach to easing the AI memory bottleneck.

### ► Strategic Analyst's Perspective

Strategic Analyst's Perspective: Intel's EMIB-T offers a viable, potentially more cost-effective alternative to CoWoS, which is crucial for supply chain diversification. The XBM architecture, while further out, represents a significant technical leap by removing the interposer. [Opportunity] for US/EU OEMs and device manufacturers to diversify their advanced packaging sources away from TSMC and potentially reduce costs. For IP holders, XBM could be a significant licensing opportunity. [Threat] to TSMC's CoWoS dominance and to traditional HBM suppliers if XBM proves scalable. Next Actions: [Strategy] should evaluate Intel Foundry's EMIB-T offerings as a near-term alternative by Q3 2026. [R&D;] should assess the technical feasibility and long-term potential of XBM by Q1 2027.

## Deep Dive ③ — HLSI & Co-Packaged Optics Reshape AI Chips

#17 | 2026/07/02 | Next Move Strategy Consulting (via EE Times) | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●●

Driven by surging AI workloads, the semiconductor industry is dramatically shifting beyond traditional System-on-Chip (SoC) paradigms towards Heterogeneous Large-Scale Integration (HLSI). This involves 3D integration and hybrid bonding for denser die-to-die connections with near-monolithic performance.

TSMC's Co-Packaged Optics (CPO) technology is now in production, redefining high-performance computing for the AI era. CPO integrates optical links closer to the processor, addressing the power and bandwidth limits of traditional copper interconnects and enabling ultra-high-speed data transmission between AI clusters.

### ► Strategic Analyst's Perspective

Strategic Analyst's Perspective: HLSI and CPO are not just incremental improvements but fundamental shifts in chip design, driven by the insatiable demands of AI. CPO's production readiness indicates a realistic path to overcoming I/O bottlenecks. [Opportunity] for US/EU photonics companies, optical component suppliers, and system integrators to lead in this new paradigm. OEMs must adapt their system architectures. [Threat] to traditional SoC designers and copper interconnect suppliers whose technologies are reaching their limits. Next Actions: [R&D;] teams must immediately invest in optical interconnect research and HLSI design methodologies. [Business Dev] should explore partnerships with CPO developers and optical module manufacturers by Q4 2026 to integrate these technologies into future platforms.

## Other Notable Articles

TSMC Significantly Expands CoWoS Advanced Packaging Capacity, to Begin Production of 14-Reticle-Size Packages by 2028 for Surging AI Demand (Biya Global Limited)

Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●●

TSMC's CoWoS expansion is critical, but demand still outstrips supply, indicating persistent bottlenecks for AI chips.

HBM and ABF Shortages Intensify AI Chip Supply Bottlenecks, Ajinomoto Forecasts Over 20% ABF Supply Gap by 2027 (Semiconductor Engineering)

Tech Novelty●○○○○ Proximity●●●●● Market Impact●●●●●

The ABF shortage, with a projected 20% gap by 2027, is a severe, near-term threat to AI chip production across the industry.

China's Memory Industry Accelerates HBM3/3E Development; YMTC Leads in Wafer-to-Wafer Hybrid Bonding Patents (BloomingBit.io)

Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○

China's rapid HBM and hybrid bonding advancements signal intensifying competition and potential disruption to global memory supply chains.

AT&S; Secures Key Customer Commitments for AI Substrate Expansion, Commences High-Volume Production at Malaysia Kulim Plant, Projects 45-55% Revenue Growth for FY26/27 (boerse-social.com)

Tech Novelty●●●○○ Proximity●●●●● Market Impact●●●●○

Austrian AT&S;'s high-volume AI substrate production in Malaysia highlights European contribution to critical AI supply chain components.

SK Hynix to Heavily Invest in ASML EUV for HBM Production in Yongin and Cheongju, Expanding Indiana Packaging Facility (Seeking Alpha)

Tech Novelty●●●○○ Proximity●●●○○ Market Impact●●●●●

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SK hynix's EUV investment for HBM and \$4B Indiana packaging plant directly strengthens US supply chain and global HBM capacity.

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## Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

### ■ Immediate (this week)

- [Procurement] Review HBM3E and advanced substrate supplier contracts and lead times, especially for Ajinomoto ABF, given projected 20% gap by 2027.
- [Strategy] Assess current AI accelerator supply chain exposure to CoWoS capacity constraints and identify alternative packaging options.

### ■ Short-term (1 month)

- [R&D;] Initiate feasibility studies on glass substrates and ultrafast laser processing for advanced packaging to mitigate thermal warping issues.
- [Business Dev] Engage with Intel Foundry to understand EMIB-T capabilities and XBM architecture as potential alternatives to TSMC's CoWoS.
- [Executive] Evaluate investment opportunities in domestic (US/EU) advanced packaging facilities and materials to enhance supply chain resilience.

### ■ Medium-long term (quarter+)

- [R&D;] Invest in optical interconnect technologies (e.g., Co-Packaged Optics) and heterogeneous large-scale integration (HLSI) to prepare for next-gen AI chip designs.
- [Legal/IP] Monitor China's advancements in HBM and hybrid bonding patents (YMTC) to assess competitive threats and potential IP licensing opportunities.
- [Strategy] Develop a long-term strategy for HBM supply diversification, including exploring alternative memory architectures like Intel's XBM or KITECH's high-density integration.

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# **Semiconductor\_BackEnd — Selected Articles**

Date: 2026-07-12

Articles: 18

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- #04 South Korean Conglomerates Samsung and SK Group Invest \$252.5 Billion in Chungcheong Province, Bolstering HBM Packaging and AI Semiconductor Supply Chain
- #05 AT&S Secures Key Customer Commitments for AI Substrate Expansion, Commences High-Volume Production at Malaysia Kulim Plant, Projects 45-55% Revenue Growth for FY26/27
- #06 TSMC Significantly Expands CoWoS Advanced Packaging Capacity, to Begin Production of 14-Reticle-Size Packages by 2028 for Surging AI Demand
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- #08 AI Memory Shortage Sparks Advanced Packaging Crisis: Ultrafast Lasers and Glass Substrates Emerge as New Bottlenecks
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#16 Micron's HBM Order Book Fully Committed Through 2028, Secures Silicon Wafer Supply with 10-Year GlobalWafers Offtake Agreement

#17 Semiconductor Industry Pivots to Heterogeneous Large-Scale Integration (HLSI) as AI Reshapes Chip Design

#18 SK Hynix to Heavily Invest in ASML EUV for HBM Production in Yongin and Cheongju, Expanding Indiana Packaging Facility

# #01 Lam Research Drives AI Performance with Advanced Packaging, Tackling Bottlenecks and Boosting Power Efficiency through Chiplets and Panel-Based Manufacturing

Published July 09, 2026   Lam Research   USA



## OVERVIEW

Lam Research highlights advanced packaging as the critical innovation frontier for AI, addressing the limitations of traditional semiconductor scaling. By enabling chiplets to function as a single system, this approach significantly reduces bottlenecks, increases memory bandwidth, and improves power efficiency, leading to substantial AI performance gains. The industry is transitioning from wafer-based to larger panel-based packaging to support more complex AI architectures, with Lam Research's Salzburg Panel Center of Excellence spearheading large-scale manufacturing.

### Key Findings

Lam Research is introducing advanced packaging technologies as the new frontier for semiconductor scaling, crucial for meeting the explosive demand from artificial intelligence (AI). The company emphasizes that chiplet technology and the transition to panel-based packaging are key enablers for dramatically boosting AI performance.

### Technical Details

According to Audrey Charles, Lam Research's Senior Vice President of Corporate Strategy and Advanced Packaging, AI growth is outpacing traditional semiconductor process scaling, making advanced packaging indispensable for bridging this gap. Chiplet technology involves integrating multiple independent dies (chiplets) within a single package, allowing them to function as a unified system. This approach significantly reduces data transmission bottlenecks, dramatically increases memory bandwidth through integration with High-Bandwidth Memory (HBM), and improves overall power efficiency. These characteristics directly address the immense data processing power and low power consumption required by AI workloads.

Furthermore, the industry is shifting from conventional wafer-based packaging to larger panel-based packaging formats to enhance manufacturing efficiency and reduce costs. To support this transformation, Lam Research has established its Salzburg Panel Center of Excellence, building large-scale advanced packaging manufacturing capabilities at the panel level. Panel-based processes enable the simultaneous processing of a much greater number of chips, offering potential cost reductions compared to wafer-based methods, especially in fan-out packaging.

### Background & Context

The semiconductor industry is encountering the physical limits of Moore's Law, where scaling transistor density alone is insufficient to meet the performance demands of AI applications. Consequently, advanced packaging, which improves inter-chip connectivity, memory bandwidth, and power delivery, has emerged as a primary means to achieve next-generation performance gains. AI processors, in particular, necessitate the efficient and high-density integration of GPUs and HBM, driving the need for sophisticated packaging technologies.

## Strategic Significance & Outlook

Lam Research views panel-based packaging technology as a foundational element for future growth in the AI and high-performance computing (HPC) markets. The company's technologies are expected to provide the scalability and efficiency required for increasingly complex AI architectures, accelerating innovation across the semiconductor industry. This strategic shift will likely impact a broad supply chain, including materials suppliers and equipment manufacturers, creating new business opportunities and reshaping the competitive landscape.

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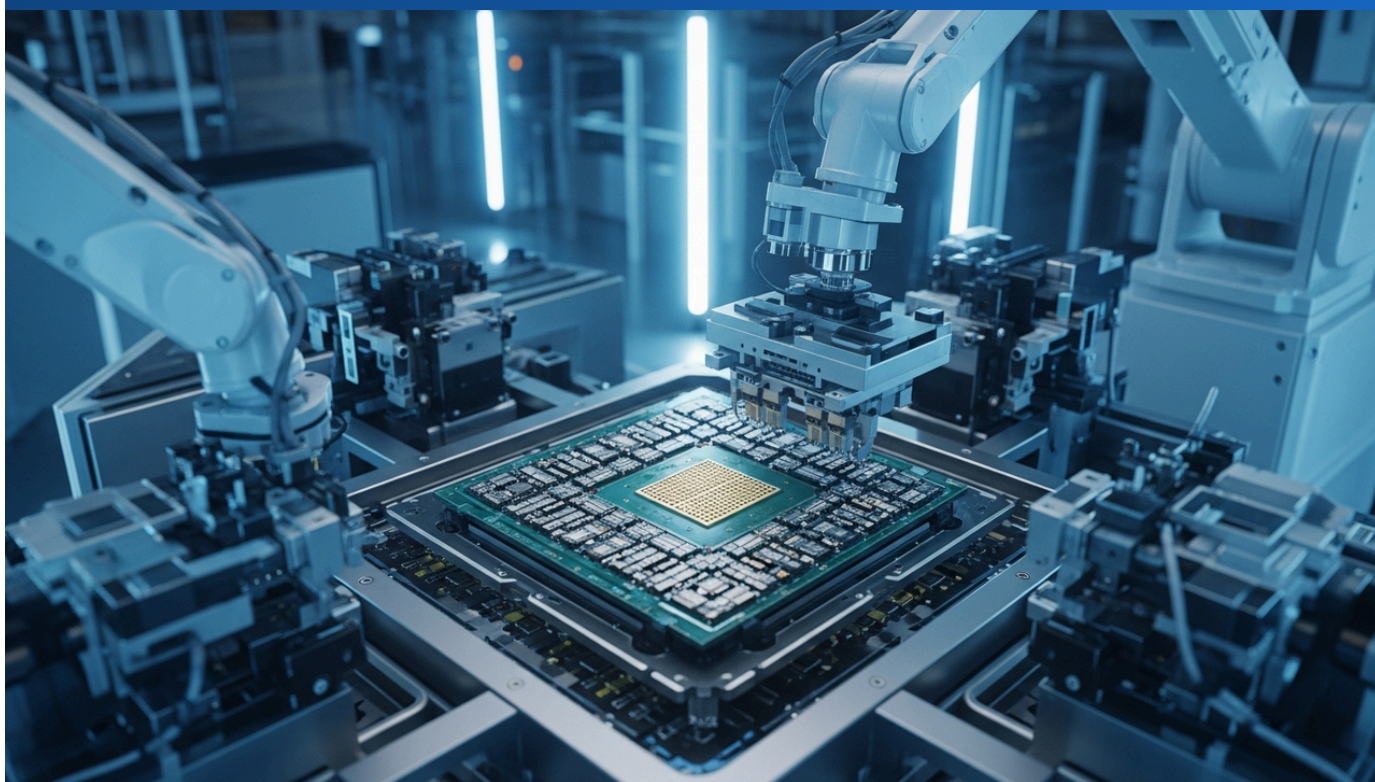
Source: <https://newsroom.lamresearch.com/advanced-packaging-for-ai-semiconductor-scaling>

Collected: July 10, 2026 | Automated Research System (Gemini API)



# #02 Nvidia Kicks Off Volume Production of Blackwell AI Accelerators with TSMC's CoWoS-L, Supply to Remain Tight Through Q4

Published July 02, 2026   MetalSemi Asia   Taiwan



## OVERVIEW

Nvidia has commenced volume production of its next-generation Blackwell AI accelerators at TSMC, leveraging the 4NP process and advanced CoWoS-L packaging. Cloud service provider demand is projected to outstrip supply through Q4 2026, affirming Nvidia's dominant position in the AI training market. Despite TSMC prioritizing CoWoS capacity for Nvidia, initial shipments may be constrained by shortages in HBM3E memory and complex substrate materials.

### Key Findings

Nvidia has initiated high-volume production of its Blackwell AI accelerators at TSMC, a critical step that will bolster its leadership in the rapidly expanding AI infrastructure market. This strategic ramp-up underscores Nvidia's commitment to meeting the escalating demand for high-performance computing essential for advanced AI workloads. The Blackwell chips are manufactured using TSMC's cutting-edge 4NP process and innovative CoWoS-L packaging technology, promising significant performance gains for AI computation.

### Technical / Clinical Details

The Blackwell AI accelerators utilize TSMC's 4NP process node, optimized for peak performance in AI-driven computations. A cornerstone of its advanced design is CoWoS-L (Chip-on-Wafer-on-Substrate with Localized backside power delivery network) packaging, a sophisticated heterogeneous integration technique. CoWoS-L enables the seamless integration of multiple large compute dies and HBM3E memory stacks on a silicon interposer, facilitating ultra-high bandwidth and superior power efficiency compared to traditional packaging. This architecture is vital for handling the immense data throughput required by complex AI models in training and inference. However, the unprecedented demand for AI chips has created bottlenecks, particularly in HBM3E memory and high-performance substrate materials, which are anticipated to limit initial Blackwell shipment volumes.

### Background & Context

The explosive growth of AI data centers globally is pushing the semiconductor industry to new manufacturing frontiers, with HBM and advanced packaging technologies like CoWoS emerging as critical supply chain choke points. Nvidia, supported by robust demand from hyperscale cloud providers such as OpenAI, Google, and Microsoft, maintains a commanding lead in the AI training sector. TSMC, as the leading CoWoS provider, is aggressively expanding its capacity to meet this surge. The commencement of Blackwell production highlights the ongoing race in AI technology and the pivotal role of advanced hardware in driving its evolution. The current supply chain challenges, including material shortages and equipment constraints, emphasize the interconnectedness and fragility of this high-stakes ecosystem.

## Strategic Significance & Outlook

The volume production of Blackwell chips marks a significant milestone for Nvidia and the broader AI industry. While it promises to unlock new levels of AI performance, it also exposes the persistent vulnerabilities within the semiconductor supply chain. Nvidia forecasts that demand will outstrip supply through Q4 2026, indicating the immense appetite for its AI accelerators and placing considerable pressure on suppliers to scale up. HBM manufacturers (SK hynix, Samsung, Micron) and advanced substrate producers are investing billions to expand capacity, intensifying competition and innovation in these crucial segments. Furthermore, the global push for regional semiconductor manufacturing capabilities, particularly in the U.S. and Asia, suggests a future landscape with more diversified and potentially resilient supply chains for advanced chips.

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Source: <https://www.setin.asia/nvidia-blackwell-production-ramp-tsmc>

Collected: July 10, 2026 | Automated Research System (Gemini API)



# #03 Amkor Technology Commits \$2.5B-\$3.0B to Advanced Packaging Facilities for AI Demand, Arizona Plant Slated for 2028 Production

Published July 08, 2026 Hudson Labs USA



## OVERVIEW

Amkor Technology plans a substantial capital expenditure of \$2.5 billion to \$3.0 billion for fiscal year 2026, driven by accelerating demand for advanced packaging in AI and data center computing. The investment will primarily fund new advanced packaging and test facilities in Arizona and Korea. The first phase of the Arizona facility is expected to complete in 2027, with production commencing in 2028, bolstering the U.S. semiconductor supply chain.



### Key Findings

Amkor Technology announced a record-breaking capital expenditure plan of \$2.5 billion to \$3.0 billion for fiscal year 2026, primarily targeting the expansion of its advanced packaging and test capabilities. This significant investment is strategically directed towards new state-of-the-art facilities in Peoria, Arizona, and Korea, aiming to meet the escalating demand from the AI and high-performance computing markets. The Arizona facility's first phase is projected for completion in 2027, with production slated to begin in 2028, aligning with U.S. initiatives to strengthen its domestic semiconductor supply chain.

### Technical / Clinical Details

Amkor's investment will focus on critical advanced packaging technologies essential for AI accelerators, including 2.5D/3D packaging, High-Bandwidth Memory (HBM) integration, chiplet technologies, and next-generation test solutions. The new Arizona packaging campus is expected to incorporate capabilities for advanced chiplet integration and CoWoS-like (Chip-on-Wafer-on-Substrate) technologies. This facility will enable complex AI chip assembly and rigorous testing, incorporating advanced thermal management and power delivery solutions. In Korea, the investment will expand existing capacities to support the growing demand for advanced packaging of next-generation memory and logic semiconductors. This substantial outlay will position Amkor to deliver packaging solutions that meet the demanding performance, power efficiency, and reliability requirements of the AI era.

## Background & Context

The explosive growth of AI has dramatically increased the demand for AI chips such as GPUs and ASICs, whose performance is increasingly dependent on advanced packaging rather than just process node miniaturization. Historically, much of the advanced packaging capacity has been concentrated in Asia. However, geopolitical concerns and the drive for supply chain resilience have prompted governments, particularly in the U.S., to promote domestic semiconductor manufacturing and packaging capabilities. Amkor's Arizona plant, in conjunction with TSMC's fabs in Arizona, will contribute to building an end-to-end semiconductor supply chain within the U.S., from front-end fabrication to back-end packaging and test. This effort is further solidified by Amkor's 10-year strategic partnership with TSMC, announced in June 2026, aimed at deepening cooperation and expanding packaging capacity across the U.S. semiconductor ecosystem.

## Strategic Significance & Outlook

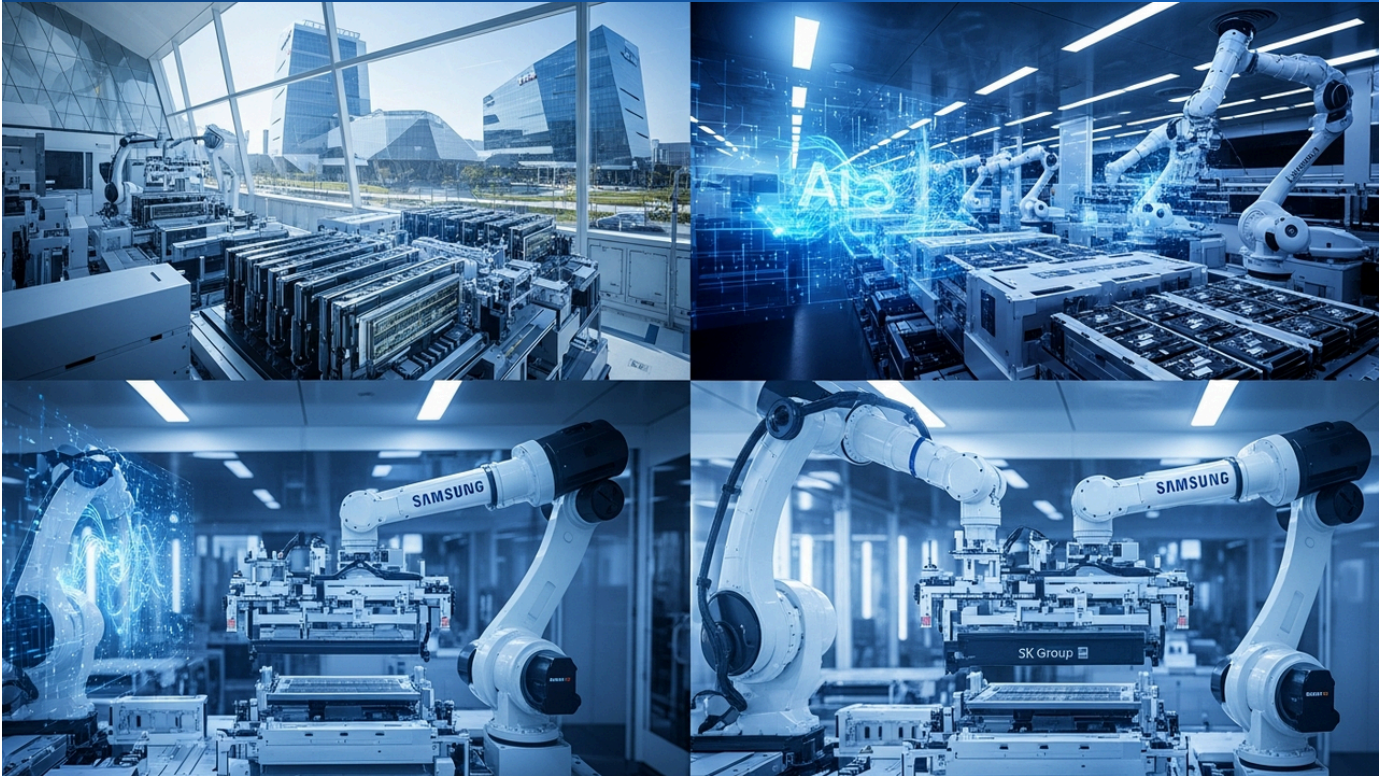
Amkor's strategic investment is a powerful catalyst for its growth in the AI-driven semiconductor market. The operationalization of the Arizona facility in 2028 will enable Amkor to provide critical advanced packaging services within the U.S., serving key clients like Nvidia, AMD, and Intel. This move is expected to bolster the U.S. semiconductor supply chain, fostering greater regional diversification in advanced packaging. Beyond enhancing Amkor's competitive edge as an OSAT provider, this investment represents a crucial step towards ensuring a stable and resilient supply of semiconductors for the evolving AI landscape, reflecting a broader industry shift towards more distributed and secure manufacturing capabilities.

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Source: <https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQEp8JbWuYtiEInnag8tNzUjRavy1UeM2IFNOICI863RJ1bpk-peEE4goQLu2PJnX2lYsTpDlBhOMeIHyzL34yKHpwgJCGeCpRhC7tkDSm-gZb6k7ZHEWA81sx-yzkzs4Ll1OwXH9G4MQA0Vn5UY3skpgFcZkvA==>

# #04 South Korean Conglomerates Samsung and SK Group Invest \$252.5 Billion in Chungcheong Province, Bolstering HBM Packaging and AI Semiconductor Supply Chain

Published July 02, 2026    The Korea Herald    South Korea



## OVERVIEW

South Korean giants including Samsung Electronics, SK hynix, and Celltrion announced a combined 392 trillion won (approximately \$252.5 billion) investment in Chungcheong Province across semiconductors, displays, batteries, and biopharmaceuticals. Samsung Electronics will allocate 56 trillion won for HBM manufacturing and advanced packaging, while SK hynix commits 100 trillion won to NAND flash and advanced packaging facilities. This massive investment aims to establish Chungcheong as a global hub for AI semiconductor production, addressing the surging demand for HBM.

### Key Findings

Leading South Korean conglomerates, including Samsung Electronics, SK hynix, and Celltrion, have unveiled a monumental investment plan totaling 392 trillion won (approximately \$252.5 billion) in Chungcheong Province. This strategic initiative targets the reinforcement of their positions in semiconductors, displays, batteries, and biopharmaceuticals, with a strong emphasis on establishing Chungcheong as a global hub for AI semiconductor supply chain. Specifically, Samsung Electronics will inject 56 trillion won into HBM manufacturing and advanced packaging, while SK hynix is dedicating 100 trillion won to its NAND flash and advanced packaging facilities.

### Technical / Clinical Details

Samsung Electronics' 56 trillion won investment is earmarked for establishing new HBM chip manufacturing and packaging facilities in Onyang and Cheonan. This move aims to dramatically enhance HBM production capacity and technological prowess, critical for the performance of advanced AI accelerators. HBM offers significantly higher bandwidth and power efficiency compared to conventional DRAM, making it an indispensable component for maximizing AI chip performance. SK hynix, on the other hand, plans to invest 100 trillion won in expanding its existing NAND flash production base (M17) and constructing a new dedicated HBM fab (P&T7) focused on advanced packaging. This will enable the company to mass-produce next-generation HBM, such as HBM4 and HBM4E, and deliver sophisticated packaging solutions leveraging chiplet and 3D stacking technologies. The integration of advanced processes like EUV lithography and hybrid bonding is also under consideration for these facilities, pushing the boundaries of semiconductor manufacturing.

## Background & Context

The exponential growth of AI has created an unprecedented demand for high-performance AI chips, with HBM emerging as a significant bottleneck. South Korea has historically been a global leader in memory semiconductors, but the advent of the AI era has shifted the competitive landscape towards HBM production capacity and advanced packaging techniques. This large-scale investment in Chungcheong Province can be viewed as part of a national strategy to maintain a leading position in the global AI semiconductor race. Moreover, in light of the U.S. efforts to strengthen its domestic semiconductor manufacturing, these substantial investments by major Asian players like Samsung and SK hynix signal increasing diversification and intensifying regional competition within the global supply chain. The inclusion of biopharmaceutical companies like Celltrion suggests a broader vision to develop Chungcheong into a multi-faceted advanced industry hub.

## Strategic Significance & Outlook

This historic investment is poised to establish Chungcheong Province as a global center for AI semiconductors and related technologies, driving South Korea's economic growth and technological innovation. The significant enhancement of HBM and advanced packaging capabilities by Samsung and SK hynix will undoubtedly elevate Korea's prominence in the global AI chip supply chain. Looking ahead, the HBM market is expected to witness accelerated capacity expansion and technological innovation, potentially leading to intensified price competition. Simultaneously, other nations, including the U.S., Japan, and Taiwan, are also undertaking massive semiconductor industry investments, indicating a period of significant global realignment. The Chungcheong investment is not merely about increasing production capacity but is also anticipated to generate ripple effects in research and development, talent cultivation, and the formation of a robust related industry ecosystem.

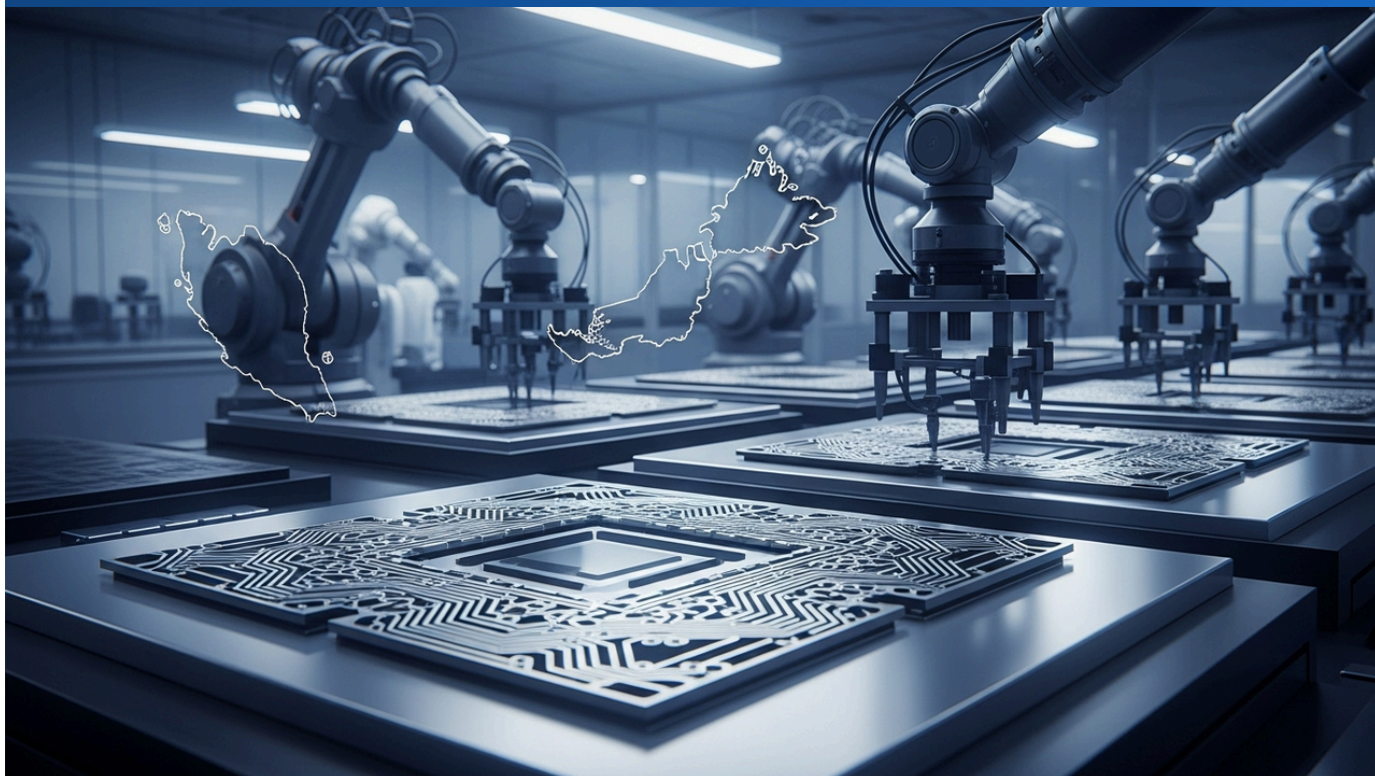
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Source: <https://www.koreaherald.com/article/10795719>



# #05 AT&S Secures Key Customer Commitments for AI Substrate Expansion, Commences High-Volume Production at Malaysia Kulim Plant, Projects 45-55% Revenue Growth for FY26/27

Published July 09, 2026 boerse-social.com オーストリア



## OVERVIEW

AT&S, a leading Austrian manufacturer of high-end IC substrates, has commenced high-volume production of advanced AI substrates at its new Kulim, Malaysia, facility. This expansion, supported by long-term customer commitments from major technology firms like AMD, is part of a 2 billion euro investment to boost capacity across Malaysia and China. Consequently, AT&S has raised its revenue growth forecast for fiscal year 2026/27 to an impressive 45-55%, driven by the surging demand from the AI and high-performance computing markets.

### Background

The AI revolution has unleashed unprecedented demand and innovation in the semiconductor industry, with IC substrates serving as vital components that dictate overall chip performance. As AI chip designs increasingly shift towards chiplet-based heterogeneous integration, high-performance substrates are enhancing their role as fundamental 'infrastructure' for efficiently connecting multiple dies, managing thermal dissipation, and delivering power. Even in advanced packaging technologies like TSMC's CoWoS, the ultimate performance is heavily reliant on the quality of the underlying substrate. AT&S's investment in its Malaysian facility unequivocally demonstrates the rapidly accelerating demand for advanced materials and packaging technologies, especially as Asia continues to be a pivotal manufacturing hub in the global semiconductor supply chain. The secured customer commitments underscore both the severity of supply bottlenecks in the AI market and the concentration of demand on key suppliers.

### Key Findings

AT&S has officially commenced high-volume production of high-end IC substrates for AI and High-Performance Computing (HPC) at its state-of-the-art new plant in Kulim, Malaysia. This pivotal achievement is supported by robust, long-term customer commitments from leading technology companies, including AMD. The Austrian firm is strategically investing up to 2 billion euros (approximately \$2.1 billion) to significantly expand its substrate production capabilities across Malaysia and China. Based on these secured agreements, AT&S has substantially upgraded its currency-adjusted revenue growth forecast for fiscal year 2026/27 to an impressive 45–55%, signaling a direct and strong positive impact from the burgeoning AI market.



## Technical Details

The IC substrates produced at AT&S's Kulim facility are engineered to meet the extremely stringent technical requirements of AI accelerators and HPC chips. These substrates feature complex multi-layer structures and ultra-fine line patterns, meticulously designed to support advanced chiplet technologies and 2.5D/3D packaging architectures. The high-density wiring layers are crucial for enabling high-speed data communication between CPUs, GPUs, and High-Bandwidth Memory (HBM), facilitating the massive data processing capabilities indispensable for AI workloads. The company's investment encompasses the integration of cutting-edge manufacturing equipment and cleanroom technologies, establishing a high-yield production system that addresses the supply stability and quality standards demanded by the AI market. Collaboration between AT&S's European R&D centers and its Asian production sites ensures the application of innovative materials and process technologies in substrate manufacturing.

## Strategic Significance & Outlook

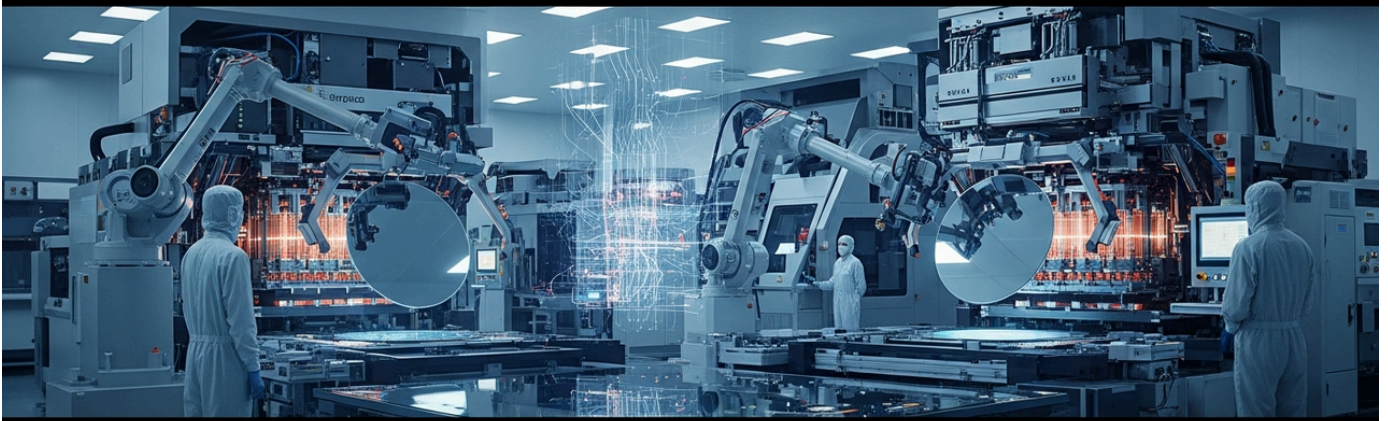
The initiation of high-volume production at AT&S's new Kulim plant, coupled with a significant upward revision of its financial outlook, solidifies the company's strategic position in the AI market. Securing long-term customer contracts guarantees future revenue stability and growth, ensuring that AT&S directly benefits from the expansion of the AI hardware market. Over the coming years, demand for AI accelerators is projected to continue its robust growth, and AT&S is poised to ride this wave as a leading supplier of advanced IC substrates. The company's investments also contribute to the geographic balance of the global semiconductor supply chain, with strengthened production capabilities in Asia becoming key to supporting the development of global AI infrastructure. Through continuous technological innovation and production capacity expansion, AT&S is expected to play a crucial role in pushing the boundaries of semiconductor performance in the AI era.

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Source: [https://www.boerse-social.com/page/newsflow/wie\\_ats\\_erste\\_group\\_porr\\_voestalpine\\_sbo\\_und\\_strabag\\_fur\\_gesprachsstoff\\_im\\_atx\\_s](https://www.boerse-social.com/page/newsflow/wie_ats_erste_group_porr_voestalpine_sbo_und_strabag_fur_gesprachsstoff_im_atx_s)

# #06 TSMC Significantly Expands CoWoS Advanced Packaging Capacity, to Begin Production of 14-Reticle-Size Packages by 2028 for Surging AI Demand

Published July 09, 2026   Biya Global Limited   Taiwan



## OVERVIEW

TSMC is substantially expanding its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity to meet the surging demand for AI chips. The company aims to nearly quadruple CoWoS capacity to 130,000 wafers per month by the end of 2026 and plans to commence production of 14-reticle-size CoWoS packages by 2028, capable of integrating approximately 10 large compute dies and 20 HBM stacks. This expansion reflects the growing importance of packaging and system integration in determining AI chip value, beyond process node miniaturization.

### Key Findings

TSMC is significantly boosting its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity, a critical differentiator for the company in response to the explosive demand for AI chips. The company aims to nearly quadruple its CoWoS capacity to 130,000 wafers per month by the end of 2026, yet supply is still projected to lag demand through 2027. Notably, TSMC plans to initiate production of an unprecedented 14-reticle-size CoWoS package by 2028, capable of integrating approximately 10 large compute dies and 20 HBM (High-Bandwidth Memory) stacks, driving the next wave of AI chip performance enhancement.

### Technical / Clinical Details

CoWoS technology enables the integration of multiple logic dies and HBM stacks onto a silicon interposer, which is then connected to an organic substrate, achieving ultra-high-speed and energy-efficient data transfer. This technology is indispensable for cutting-edge AI accelerators like Nvidia's Blackwell and AMD's MI300X. TSMC is extending its CoWoS technology to support larger and more complex packages. The planned 14-reticle-size CoWoS package for 2028 is roughly twice the size of existing CoWoS packages, offering significantly higher integration density and processing power. This large-scale package addresses the growing demands for computational power and memory bandwidth driven by increasingly complex AI models, requiring extremely fine bump pitches and high-precision alignment for inter-chiplet connections. Beyond its current wafer-based CoWoS, TSMC is also developing CoPoS (Chip-on-Panel-on-Substrate), which utilizes square panels instead of round wafers, aiming for further cost efficiency and larger integration scales.

## Background & Context

The evolution of AI has shifted the semiconductor manufacturing bottleneck from traditional wafer fabrication to advanced packaging. HBM and CoWoS, in particular, have become crucial determinants of AI chip supply. TSMC holds a dominant market share in CoWoS, with its capacity fully booked by major clients, including Nvidia, which consumes approximately 60% of the allocation. This situation highlights that the value of AI chips is increasingly derived not just from smaller process nodes, but significantly from packaging technology that efficiently integrates multiple components for high performance. Amid efforts to strengthen the U.S. semiconductor supply chain, TSMC is planning two advanced packaging plants in Arizona and has forged a 10-year strategic alliance with Amkor Technology to bolster CoWoS and 3D-IC capabilities within the U.S. These investments are essential steps to ensure a stable supply for global AI infrastructure.

## Strategic Significance & Outlook

TSMC's substantial CoWoS capacity expansion is critically important for sustaining the growth of the AI industry. However, given that demand continues to outpace supply expansion, CoWoS is expected to remain a primary bottleneck for AI chips. This scenario creates significant business opportunities for advanced packaging equipment suppliers such as Applied Materials, BEI, Disco, and Tokyo Electron. Concurrently, the development of alternative packaging technologies like Intel's EMIB-T and Samsung's HCB is accelerating, indicating intensifying market competition. In the coming years, the technological evolution and capacity expansion of CoWoS will profoundly impact AI chip pricing, supply stability, and the ultimate proliferation of AI solutions. TSMC's CoWoS technology and investment strategy will undoubtedly be a key factor shaping the direction of the global AI industry for years to come.

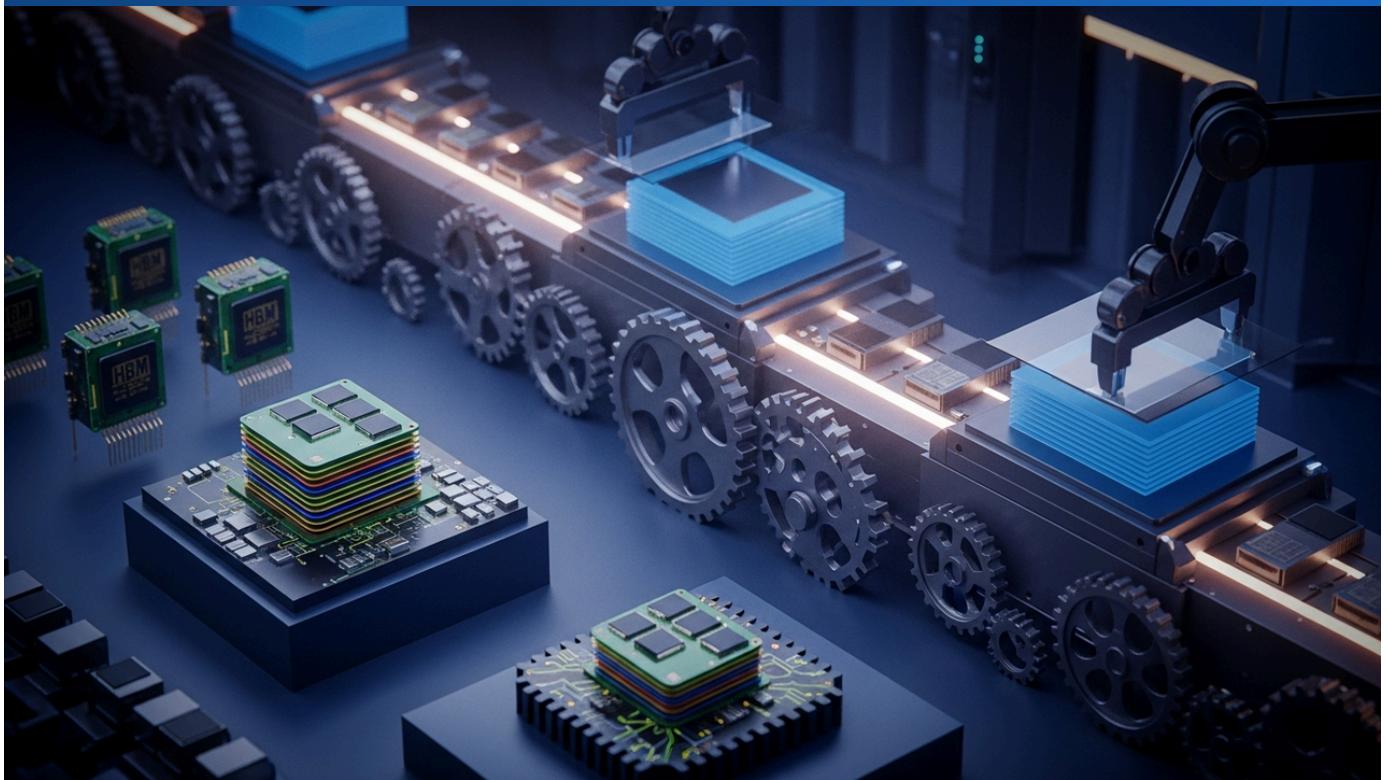
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# #07 HBM and ABF Shortages Intensify AI Chip Supply Bottlenecks, Ajinomoto Forecasts Over 20% ABF Supply Gap by 2027

Published July 06, 2026   Semiconductor Engineering   USA



## OVERVIEW

The primary bottlenecks for AI chip production are the critical shortage of High-Bandwidth Memory (HBM) and the complex packaging capacity required for GPUs/XPUs by Nvidia, AMD, and Google, coupled with a supply deficit of Ajinomoto Build-up Film (ABF) on which all foundries depend. Ajinomoto projects an ABF supply gap exceeding 20% by 2027, severely constraining the efficient delivery of AI chips. This issue highlights challenges not only in standard wafer fabrication but also across the entire advanced back-end supply chain.

### Key Findings

The semiconductor supply chain for AI chips is facing severe bottlenecks, primarily due to the scarcity of High-Bandwidth Memory (HBM), indispensable for GPUs/XPUs from leading manufacturers like Nvidia, AMD, and Google, and the complex packaging capacity it demands. A further critical constraint is the global shortage of Ajinomoto Build-up Film (ABF), a foundational material for virtually all advanced semiconductor packaging. Ajinomoto anticipates an ABF supply gap exceeding 20% by 2027, which is expected to significantly restrict the production and delivery of AI chips.

### Technical / Clinical Details

HBM is a technology that vertically stacks multiple DRAM dies, enabling ultra-fast and low-power data exchange, crucial for determining the performance of AI accelerators. Producing more HBM requires not only DRAM wafer fabrication capacity but also sophisticated packaging capabilities such as CoWoS (Chip-on-Wafer-on-Substrate). In this packaging process, ABF is extensively used as an insulating layer in IC package substrates. ABF plays a vital role in transmitting electrical signals, dissipating heat, and providing mechanical protection, directly impacting the manufacturing yield and performance of advanced semiconductors. However, the explosion in AI demand has led to a rapid surge in demand for specialized materials like ABF, outstripping suppliers' ability to scale up. Ajinomoto's projected supply gap of over 20% presents a substantial hurdle for future AI infrastructure deployment.



## Background & Context

The exponential growth of AI data centers has profoundly reshaped the entire semiconductor supply chain. While logic chip miniaturization processes once represented the primary bottleneck, today, HBM, advanced packaging, and the specialized materials they require are the biggest impediments to the efficient supply of AI accelerators. The ABF shortage, exacerbated by Ajinomoto's near-monopoly in the market, is having widespread repercussions across the industry. This situation underscores that semiconductor manufacturing now faces complex challenges spanning material science, back-end processing, and global supply chain management. Governments and semiconductor companies worldwide are focusing on strengthening regional manufacturing capabilities and developing alternative materials to enhance supply chain resilience, but immediate solutions remain elusive.

## Strategic Significance & Outlook

The HBM and ABF shortages are expected to constrain AI chip supply in the short term, potentially leading to price increases and delays in AI infrastructure development. Semiconductor manufacturers must enhance both DRAM wafer fab and packaging capacities for HBM production, but increasing the output of specialized materials like ABF takes time. Although Ajinomoto is investing in increased production, it is anticipated to take time to catch up with demand growth. This bottleneck could prompt AI chip designers to explore alternative memory solutions (e.g., using GDDR6 or new memory architectures), develop ABF substitutes, or seek more efficient packaging methods. In the long run, supply chain diversification and the establishment of regional production capabilities for critical materials and components will be essential for the sustainable growth of the semiconductor industry in the AI era.

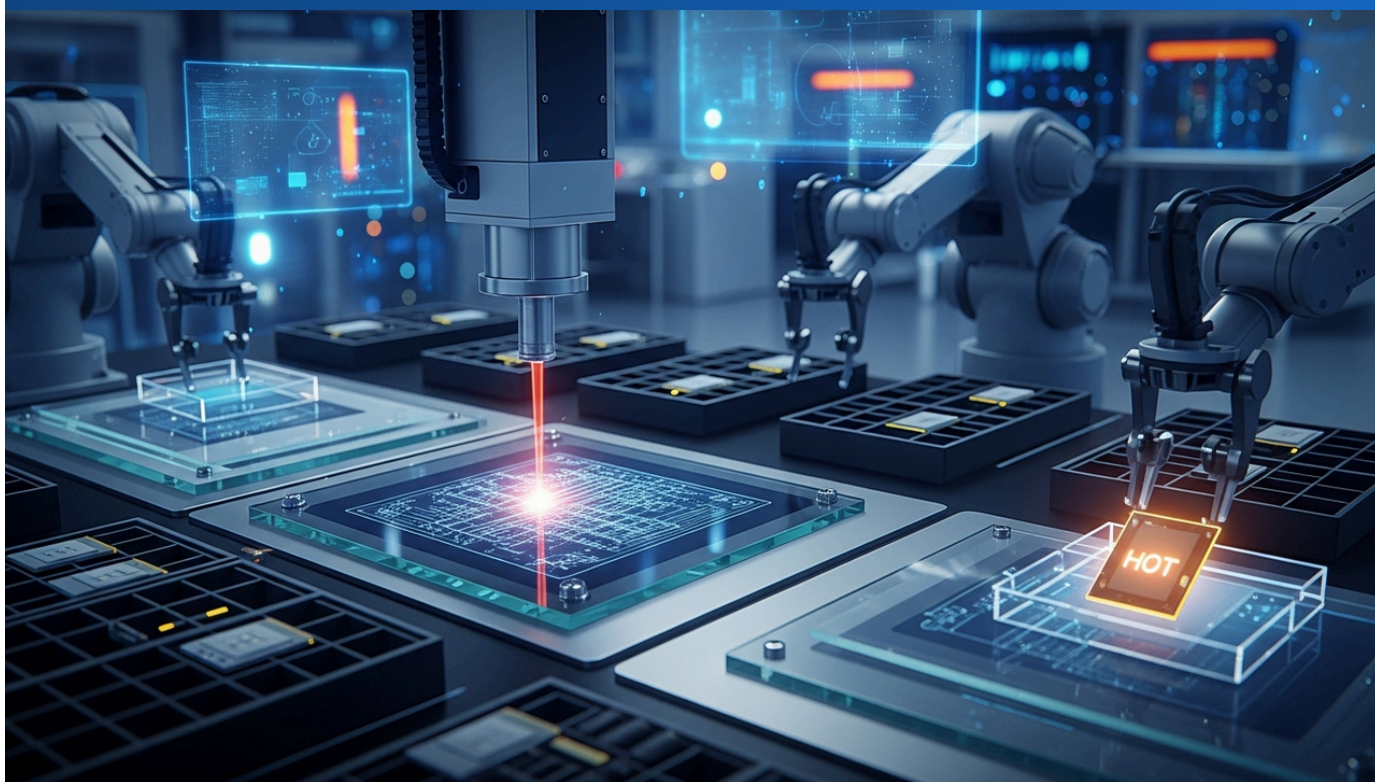
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Source: <https://semiengineering.com/data-center-ai-growth-faces-challenging-bottlenecks/>

Collected: July 10, 2026 | Automated Research System (Gemini API)

# #08 AI Memory Shortage Sparks Advanced Packaging Crisis: Ultrafast Lasers and Glass Substrates Emerge as New Bottlenecks

Published July 03, 2026   Chanelink   China



## OVERVIEW

A 'capacity crisis' in advanced packaging processes, triggered by the AI memory shortage, is causing ultrafast laser suppliers to become a new bottleneck in the supply chain. AI accelerators demand highly advanced packaging, and with traditional plastic packaging prone to warping at high temperatures, the industry is rapidly transitioning to glass substrates. Companies like LITILIT are building high-capacity femtosecond laser facilities to meet the demand for precise material stripping in advanced chip manufacturing.

### Key Findings

The shortage of AI memory has led to a 'capacity crisis' in advanced packaging processes, causing ultrafast laser suppliers to emerge as a new critical bottleneck in the supply chain. The increasing performance requirements of AI accelerators necessitate advanced packaging solutions. As conventional plastic packaging risks warping and cracking under high thermal loads, the industry is accelerating its shift towards glass substrates, which offer superior thermal stability and precision processing capabilities. To address this demand, key players like LITILIT are rapidly constructing high-capacity femtosecond laser facilities, enabling the ultra-precise material removal essential for advanced chip manufacturing.

### Technical / Clinical Details

AI chips, particularly GPUs and ASICs, integrating High-Bandwidth Memory (HBM), exhibit extremely high power densities and generate significant heat. This thermal challenge directly impacts the choice of packaging materials, as traditional organic or plastic packages face increased risks of warpage and cracking due to heat, leading to reduced reliability and yield. Glass substrates are gaining prominence as a solution. Glass offers a low coefficient of thermal expansion, high rigidity, and excellent flatness, making it ideal for high-precision multi-layer wiring and 3D stacking. However, processing glass substrates demands ultra-precise techniques difficult to achieve with conventional mechanical or chemical methods. This is where ultrafast lasers, such as femtosecond lasers, become crucial. Femtosecond lasers deliver energy in extremely short pulses, minimizing thermal impact while precisely cutting and removing material from brittle substrates like glass. Laser equipment manufacturers like LITILIT are increasing their supply capacity for high-power, high-precision femtosecond laser systems tailored for these applications, recognizing their indispensable role in enabling next-generation packaging.

## Background & Context

As the semiconductor industry approaches the limits of Moore's Law, it is increasingly focusing on advanced packaging technologies as a means to boost performance beyond simple miniaturization. Technologies such as chiplets and 2.5D/3D integration enhance system performance by integrating multiple functional dies into a single package. The explosion in AI chip demand has driven an unprecedented need for these advanced packaging solutions, simultaneously creating a bottleneck in HBM supply. This bottleneck has cascaded down to packaging materials, specifically glass substrates, and the specialized equipment, like ultrafast lasers, required to process them. Existing laser suppliers have struggled to keep pace with this sudden surge in demand, creating a new vulnerability in the supply chain. The industry-wide search for more robust and thermally stable packaging solutions is accelerating investment in glass substrates and the laser technologies that enable them.

## Strategic Significance & Outlook

Ultrafast laser technology and glass substrates will be integral to future performance enhancements and reliability assurance for AI accelerators. The current capacity constraints faced by ultrafast laser suppliers may impact AI chip supply in the short term, but the significant facility constructions by companies like LITILIT are expected to help alleviate this issue. In the long term, the adoption of glass substrates will accelerate the realization of next-generation packaging technologies (e.g., glass panel-level packaging) offering higher integration density, superior electrical characteristics, and enhanced thermal management. This will serve as a foundational enabler for semiconductor technology evolution across a wide range of fields beyond AI chips, including high-performance computing, 5G/6G communications, and automotive electronics. Further advancements in laser technology and cost reductions in glass materials will be key to future market expansion.

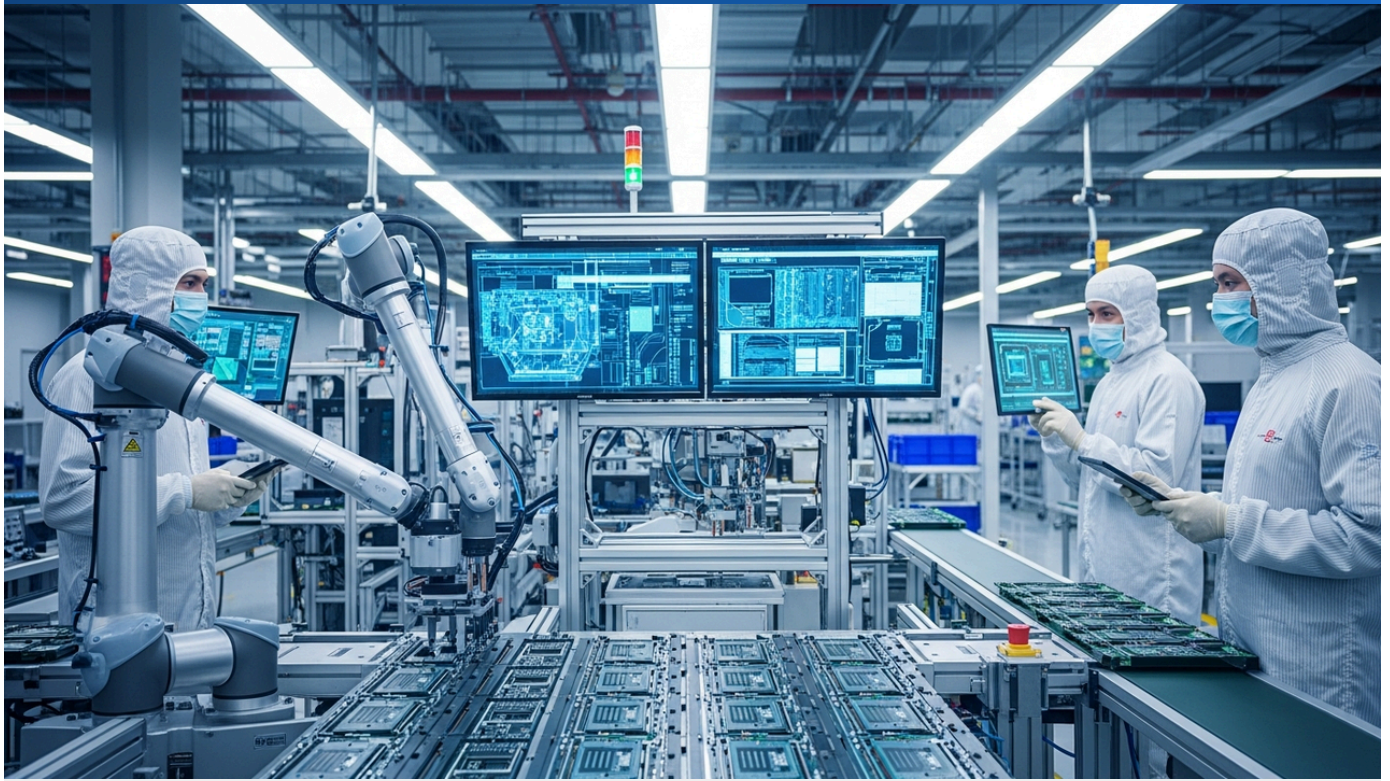
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Source: <https://www.chanelink.com/news/ai-memory-shortage-triggers-chip-packaging-crisis-ultrafast-lasers-become-the-next-supply-bottleneck-1288>



# #09 AT&S Invests €10 Million in Austrian Fehring Plant to Bolster PCB Business, Transforming it into an Innovation Hub

Published July 03, 2026 AT&S (Press Release) オーストリア



## OVERVIEW

AT&S, a global leader in high-end PCBs and IC substrates, is investing approximately €10 million in its Fehring plant in Austria. This strategic upgrade aims to establish the facility as an innovation hub, expanding its expertise in power and thermal management solutions crucial for next-generation electronics in AI, HPC, and automotive applications, while creating up to 50 new jobs and strengthening Europe's technological resilience.

### Background

The relentless miniaturization and performance enhancement of electronic devices are placing unprecedented demands on Printed Circuit Boards (PCBs). In burgeoning fields such as artificial intelligence (AI) and autonomous driving, high-reliability, high-density, and high-frequency PCBs are indispensable for processing vast amounts of data with speed and efficiency. Concurrently, advancements in semiconductor packaging, including chiplet integration and 2.5D/3D packaging, are evolving PCBs beyond mere component interconnection platforms into critical components that determine overall system performance. This evolution necessitates sophisticated solutions for managing power delivery and thermal dissipation. Furthermore, as the European Union (EU) actively promotes the strengthening of its domestic semiconductor ecosystem, investments by European-based companies like AT&S in local technological innovation and capacity expansion are vital for geopolitical risk diversification and enhancing supply chain resilience.

### Key Findings

AT&S, a global leader in high-end Printed Circuit Boards (PCBs) and IC substrates, has announced a substantial strategic investment of approximately 10 million euros (approximately \$10.7 million) in its Fehring plant in Austria. This significant capital infusion is primarily aimed at fortifying AT&S's PCB business and substantially expanding its specialized expertise in advanced power and thermal management solutions. Through this initiative, the Fehring plant is poised to be transformed into a cutting-edge innovation hub, which is also projected to create up to 50 new, high-skilled jobs.



## Technical Focus

The investment will be meticulously allocated towards modernizing production equipment and significantly upgrading the technological capabilities at the Fehring facility. This modernization includes advancing manufacturing processes for next-generation PCBs characterized by superior high-frequency performance, increased wiring density, and enhanced thermal conductivity. Elevated power consumption and the resulting heat generation in increasingly sophisticated electronic devices—particularly in AI accelerators, High-Performance Computing (HPC), advanced automotive electronics, and precision medical equipment—present significant engineering challenges. AT&S aims to address these by developing novel substrate technologies with high heat dissipation efficiency, integrating advanced embedded component technologies, and pioneering precise thermal path designs. These innovations are critical for improving the overall performance, reliability, and longevity of electronic systems. The Fehring plant will serve as an integrated R&D and manufacturing hub within Austria, strategically positioned to rapidly introduce innovative solutions to the market and collaborate closely with customers on next-generation designs.

## Strategic Significance & Outlook

This substantial investment in the Fehring plant represents a crucial strategic step for AT&S to solidify its technological leadership within the highly competitive PCB business and expand its market share in high-growth sectors. By enhancing the plant's function as a dedicated innovation hub, AT&S aims to accelerate new product development cycles and foster deeper collaborative research with its global clientele, thereby improving its agility and responsiveness to dynamic market needs. Looking ahead, demand for advanced electronic solutions is expected to intensify across diverse and critical fields, including cutting-edge semiconductor technology, complex medical devices, and robust security and defense applications. Through this strategic investment, AT&S is poised to expand its portfolio of high-value PCB products, establishing a significant competitive advantage in these pivotal markets. Beyond its commercial implications, the creation of new high-tech jobs will also contribute substantially to regional economic revitalization, further strengthening Austria's position within the global technology industry.



# #10 Micron Invests \$9.3 Billion in Hiroshima for HBM Production Launching 2028, Expands Packaging Capacity in Singapore

Published July 04, 2026   TechsCurrent   Japan



## OVERVIEW

Micron Technology has broken ground on a \$9.3 billion expansion of its Hiroshima, Japan factory to bolster High-Bandwidth Memory (HBM) production, with shipments expected around summer 2028, supported by Japan's Ministry of Economy, Trade and Industry. Concurrently, Micron is expanding HBM packaging capacity in Singapore, set to commence operations in 2026 and contribute significantly by H1 2027. These investments address HBM as a strategic bottleneck for AI infrastructure, strengthening Micron's competitive edge in the global AI race.

### Key Findings

Micron Technology has initiated a massive expansion project at its Hiroshima, Japan factory, committing approximately \$9.3 billion (around 1.4 trillion JPY) to enhance High-Bandwidth Memory (HBM) production, crucial for AI processors. The new facility aims to begin shipments around summer 2028 and is receiving substantial support from Japan's Ministry of Economy, Trade and Industry. Concurrently, Micron is actively expanding its HBM packaging capacity in Singapore, with operations scheduled to start in 2026 and significant additional capacity anticipated by H1 2027. These investments represent a strategic move to alleviate the HBM supply shortage, which has become a primary bottleneck for AI infrastructure, and to solidify Micron's competitive position in the global AI race.

### Technical / Clinical Details

HBM is an innovative memory technology that vertically stacks multiple DRAM dies, interconnected using Through-Silicon Vias (TSVs), to achieve ultra-high-speed and low-power data transfer. AI accelerators, which require processing vast amounts of data at high speeds, rely on HBM for bandwidth and efficiency that traditional DRAM cannot provide. Micron's Hiroshima facility will incorporate state-of-the-art HBM manufacturing processes, supporting HBM3E and future HBM4 generations. The expansion of packaging capacity in Singapore reflects the critical importance of back-end processes in HBM production, with advanced technologies like 3D stacking and Thermo-Compression Bonding (TCB) expected to be deployed. HBM production demands extremely high yields; even minor defects can render an entire multi-layer stack unusable, necessitating precise manufacturing techniques and rigorous quality control. Micron's investment aims to overcome these technical challenges and enable large-scale, reliable HBM supply.

## Background & Context

The exponential growth of AI has dramatically boosted the demand for high-performance AI chips, making HBM the most significant bottleneck in their supply. Leading AI chip manufacturers, such as Nvidia and AMD, are strengthening long-term agreements with memory suppliers to secure a stable HBM supply. Micron's investment in its Hiroshima factory aligns perfectly with Japan's government strategy to bolster its semiconductor industry, emphasizing economic security and domestic manufacturing capabilities, thus receiving substantial subsidies. This move is part of a global trend to diversify supply chains and secure more stable manufacturing bases amid intensifying geopolitical competition, particularly between the U.S. and China. Samsung and SK Hynix in South Korea are also making substantial investments in HBM packaging capacity, indicating a heated competitive landscape in the AI memory market.

## Strategic Significance & Outlook

Micron's significant investments in Hiroshima and Singapore are expected to substantially expand HBM supply capacity in the long term, supporting the sustained growth of the AI industry. The Hiroshima plant's operation from 2028 onwards is particularly anticipated to contribute significantly to HBM supply for next-generation AI infrastructure. However, the pace of HBM demand growth is exceptionally fast, and these investments may not fully resolve short-term supply shortages. Competition in the HBM market will increasingly be determined not just by production capacity, but also by yield rates, power efficiency, and the ability to adopt next-generation technologies (HBM4, HBM4E, hybrid bonding). Micron's strategy is poised to establish the company as a key player in the HBM market, playing a crucial role in supporting the future evolution of AI technology.

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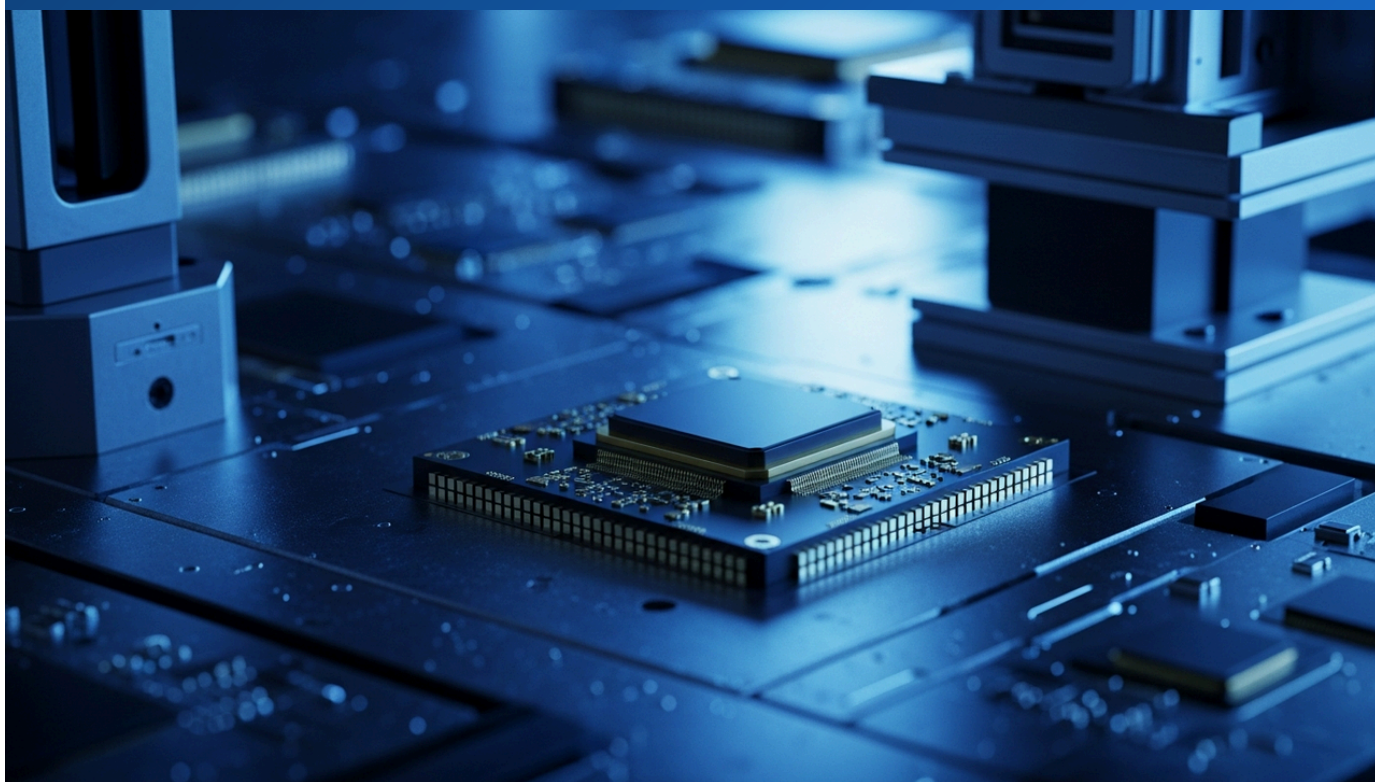
Source: <https://techcurrent.com/2026/07/micron-hiroshima-hbm-ai-memory-supply/>

Collected: July 10, 2026 | Automated Research System (Gemini API)



# #11 Korea Institute of Industrial Technology Develops Novel Chip Integration Process Achieving 4x Commercial HBM Density

Published July 07, 2026    EurekAlert!    South Korea



## OVERVIEW

Researchers at the Korea Institute of Industrial Technology (KITECH) have developed an innovative chip integration process that achieves approximately four times the integration density of commercial High-Bandwidth Memory (HBM). This new technology combines simultaneous chip transfer with highly efficient metallic interconnection formation, dramatically increasing the number of chips that can be integrated within a given space. This breakthrough enables significant advancements in AI semiconductor performance and is expected to have broad applications, particularly in chiplet-based heterogeneous integration.

### Key Findings

A research team at the Korea Institute of Industrial Technology (KITECH) has developed a groundbreaking chip integration process that achieves approximately four times the integration density compared to existing commercial High-Bandwidth Memory (HBM). This innovative technology allows for a dramatic increase in the number of chips integrated within a limited space by combining simultaneous chip transfer with efficient metallic interconnection formation. This breakthrough holds immense potential to significantly enhance the computational power of AI semiconductors and is expected to find broad applications in next-generation packaging technologies such as chiplet-based heterogeneous integration.

### Technical / Clinical Details

The novel process developed by KITECH's research team first involves precisely placing chips onto a carrier wafer, followed by applying a unique technique for forming metallic interconnections. The core of this technology lies in its ability to efficiently transfer multiple chips simultaneously and create high-density, electrically superior metallic connections compared to previous micro-bump bonding methods. While conventional HBM typically stacks 8 to 12 layers of DRAM dies, this new technology enables even greater stacking or the integration of smaller chips. As a result, it achieves an unprecedented integration density, approximately four times that of commercial HBM, within a given footprint. This promises dramatic improvements in memory bandwidth, reduced data transfer latency, and a significant boost in overall system performance for AI accelerators and high-performance processors. The process is also designed with manufacturing yield and scalability in mind, paving the way for future mass production.

## Background & Context

The semiconductor industry is grappling with the physical limits of Moore's Law, making performance enhancement through mere miniaturization increasingly challenging. Consequently, heterogeneous integration, which combines different types of chips, and the integration of smaller functional blocks (chiplets) are becoming mainstream approaches for next-generation semiconductor design. HBM is already a critical factor determining the performance of AI chips, but its integration density and cost have always been challenges. KITECH's achievement opens new avenues not only for existing high-performance memory like HBM but also for integrating diverse chips such as CPUs, GPUs, and Application-Specific Integrated Circuits (ASICs) at much higher densities. This technology will provide the immense data processing power and memory bandwidth necessary to efficiently handle complex AI workloads, fostering further advancements in AI. South Korea, a global leader in memory semiconductors, views the development of such advanced packaging technologies as crucial for maintaining its competitive edge.

## Strategic Significance & Outlook

The ultra-high-density chip integration process developed by KITECH, published in *\*Results in Engineering\**, has the potential to significantly impact the AI semiconductor market. If commercialized, this technology could lead to AI accelerators that are much smaller yet dramatically more powerful. This could not only improve power efficiency in data centers but also accelerate the adoption of AI in a broader range of applications, including edge AI devices and mobile AI applications. Its applicability to chiplet-based heterogeneous integration is expected to play a vital role in optimizing individual chiplet manufacturing processes while achieving the best overall system performance and cost efficiency. Future efforts will focus on addressing challenges for mass production (cost, yield, reliability) through further R&D and collaboration with industry partners. This breakthrough signifies that the semiconductor industry is entering a new phase of 'semiconductor skyscrapers.'

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Source: <https://www.eurekalert.org/news-releases/1135221>

# #12 Samsung and SK hynix Reportedly Reconsidering Hybrid Bonding Timeline for HBM, 16-High HBM4E May Be Earliest Adoption

Published July 07, 2026   TrendForce   Taiwan



## OVERVIEW

Samsung Electronics and SK hynix are reportedly reassessing the timeline for the widespread adoption of hybrid bonding technology in High-Bandwidth Memory (HBM). While initial expectations pointed to HBM4, both companies continue to rely on conventional thermo-compression bonding, with industry forecasts now suggesting 16-high HBM4E as the earliest likely adoption point. This reconsideration, driven by technology complexity, cost, and existing technology maturity, could impact the HBM technical roadmap.



### Key Findings

Samsung Electronics and SK hynix, two dominant suppliers of High-Bandwidth Memory (HBM), are reportedly re-evaluating the widespread adoption timeline for hybrid bonding technology in their HBM products. Although initial expectations anticipated its prominent use in the HBM4 generation, both companies are currently maintaining conventional thermo-compression bonding (TCB) as their primary interconnection method. New industry forecasts suggest that hybrid bonding may not see widespread deployment until at least the HBM4E generation, which features a 16-layer stack. This reassessment is a crucial decision, as it significantly impacts HBM performance enhancements and manufacturing costs.

### Technical / Clinical Details

Hybrid bonding is a technology that directly connects chips via fine copper-to-copper bonds, offering significantly higher interconnection density, shorter signal paths, and superior electrical characteristics compared to traditional micro-bump bonding with TCB. This was expected to further boost HBM bandwidth and power efficiency, enabling thinner designs and performance retention, especially in highly stacked HBM (e.g., 16-layer stacks), which are challenging with conventional methods. However, hybrid bonding is a highly complex and costly manufacturing process, demanding stringent cleanroom environments, ultra-high alignment precision, and intricate process control. Furthermore, existing TCB technologies have continued to evolve through material and process improvements, potentially meeting the performance requirements for the initial stages of the HBM4 generation. The reported re-evaluation by both companies likely stems from a comprehensive consideration of these technical challenges, economic factors, and yield concerns.

## Background & Context

The explosive growth of AI has led to a dramatic surge in HBM demand, positioning it as the most critical component influencing AI accelerator performance. SK hynix, Samsung, and Micron are locked in fierce competition within the HBM market, and the timing of next-generation technology adoption directly impacts market competitiveness. Hybrid bonding was anticipated to enable further HBM performance improvements and higher stacking. A delay in its adoption could thus influence the HBM roadmap and the design of future AI chips. Additionally, news that China's YMTC (Yangtze Memory Technologies Co.) is leading in patent acquisition for wafer-to-wafer hybrid bonding further intensifies international competition in advanced packaging technology. The technological choices made by key players have significant repercussions for the entire semiconductor ecosystem, including manufacturing equipment and material suppliers, making these developments highly scrutinized.

## Strategic Significance & Outlook

The reported reconsideration of the HBM hybrid bonding adoption timeline by Samsung and SK hynix highlights the complexity of technological competition within the HBM market. In the short term, this could mean that TCB remains dominant for initial HBM4 products, and substantial capital investment in hybrid bonding might be deferred. Long-term, hybrid bonding remains an indispensable technology for achieving further HBM stacking and performance improvements, and it will likely be widely adopted in the HBM4E generation or beyond. This delay may not necessarily slow the pace of HBM innovation but rather provide suppliers with an opportunity to more carefully evaluate technology maturity, cost efficiency, and the stability of mass production capabilities. As AI chip demand continues to expand, HBM suppliers are challenged to balance the optimization of existing technologies with the strategic introduction of next-generation solutions.

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Source: [https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQETtYhp1xjwVqr9J24b7eLtCu8MX1ozdyHn\\_Zu2tpXKJEfi4XV\\_6iseWCadaEuGLI8UTmY2ZywUWxnFNqM0si8Y3KdelUcLJQBL-BQE44n1s68K-aeCuX-](https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQETtYhp1xjwVqr9J24b7eLtCu8MX1ozdyHn_Zu2tpXKJEfi4XV_6iseWCadaEuGLI8UTmY2ZywUWxnFNqM0si8Y3KdelUcLJQBL-BQE44n1s68K-aeCuX-)

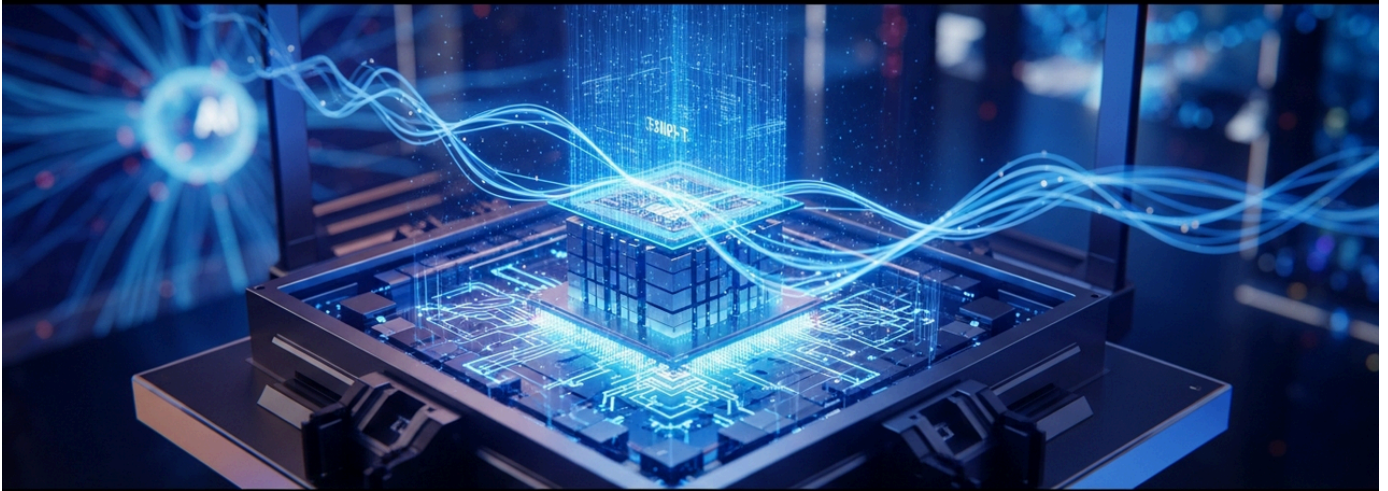


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Collected: July 10, 2026 | Automated Research System (Gemini API)

# #13 Intel's EMIB-T Emerges as CoWoS Alternative, New XBM Memory Architecture to Alleviate AI Memory Bottleneck

Published July 07, 2026 Tom's Hardware USA



## OVERVIEW

Intel's 2.5D packaging technology, EMIB-T, is emerging as a credible alternative to TSMC's CoWoS for large-package AI accelerators, expanding validation for 36/35  $\mu\text{m}$  bump pitch to 4.5x reticle silicon packages, targeting certification by late 2026.

Furthermore, Intel has patented a new XBM memory architecture that ditches HBM's costly silicon interposer, utilizing a backend-transistor DRAM stack with UCle links and built-in repair, demonstrating a multi-faceted approach to easing the AI memory bottleneck.

### Key Findings

Intel's advanced 2.5D packaging technology, EMIB-T (Embedded Multi-die Interconnect Bridge-Tile), is rapidly gaining traction as a reliable alternative to TSMC's CoWoS (Chip-on-Wafer-on-Substrate) for large-package AI accelerators. EMIB-T is expanding its validation for 36/35  $\mu\text{m}$  bump pitch to 4.5x reticle-sized silicon packages, with certification targeted by the end of 2026. Moreover, to address HBM (High-Bandwidth Memory) challenges, Intel has unveiled a patented new XBM (eXtended Bandwidth Memory) architecture. This innovative design eliminates the need for expensive silicon interposers by utilizing a backend-transistor DRAM stack with UCle (Universal Chiplet Interconnect Express) links and built-in repair capabilities, signaling Intel's multi-pronged approach to resolving the AI memory bottleneck.

### Technical / Clinical Details

EMIB-T is Intel's proprietary technology designed to efficiently connect multiple chiplets on a relatively large substrate. Unlike CoWoS, which relies on a silicon interposer, EMIB uses embedded bridge dies to achieve high-speed inter-die connectivity. This approach has the potential to deliver comparable high-performance packaging while reducing the manufacturing complexity and cost associated with CoWoS. Validation at a 36/35  $\mu\text{m}$  bump pitch is currently underway, catering to the high-density interconnection requirements of next-generation AI chips. Intel Foundry is reportedly booking packaging for over 3 million Tensor Processing Units (TPUs) in 2028, and EMIB technology is being tested for HBM integration.

Meanwhile, Intel's patented XBM memory architecture aims to resolve the inherent challenges of traditional HBM, particularly the high cost and manufacturing complexity of silicon interposers. XBM employs a backend-transistor (BET) DRAM stack that connects directly to the processor via UCIe interconnects. This design directly stacks DRAM dies onto the logic chip, using fine copper-to-copper bonds or other direct bonding technologies, thereby eliminating the need for a silicon interposer. Furthermore, XBM incorporates built-in repair capabilities, which can efficiently bypass defective cells within the DRAM stack, potentially improving manufacturing yields and reducing overall costs. Concurrently, Samsung is also actively researching HBM thermals, comparing thermo-compression bonding (TCB) and hybrid copper bonding (HCB), with HCB demonstrating significant potential for reducing thermal resistance.

## **Background & Context**

The explosive growth of AI has created new challenges and opportunities for the semiconductor industry. The supply of high-performance AI chips is increasingly dependent not only on the logic performance of CPUs and GPUs but also on HBM availability and advanced packaging technologies. While TSMC's CoWoS has established itself as a primary packaging solution for AI accelerators, its capacity is constrained, prompting competitors like Intel and Samsung to develop alternative technologies. Intel, benefiting from U.S. government initiatives to strengthen domestic semiconductor manufacturing, is positioning EMIB-T as a strong alternative to CoWoS, aiming to expand its market share through its Intel Foundry ecosystem. The development of innovative memory architectures like XBM is designed to fundamentally address the HBM supply bottleneck and increase flexibility in future AI chip designs. This signifies that technological innovation in the AI era is progressing across all layers of semiconductor design and manufacturing.

## Strategic Significance & Outlook

If Intel's EMIB-T technology receives certification by the end of 2026 and is widely adopted for HBM integration, Intel's competitiveness in the AI accelerator market will significantly increase. EMIB-T could become an attractive option for customers seeking to bolster packaging capabilities, especially within the U.S. Meanwhile, the XBM architecture holds great promise as a long-term solution to the AI memory bottleneck. Reducing the reliance on silicon interposers could lead to cost efficiencies and simplified manufacturing processes, potentially accelerating the proliferation of AI chips. Moving forward, Intel is expected to integrate both EMIB-T and XBM technologies to offer comprehensive AI hardware solutions, thereby strengthening its presence in the AI market. Samsung's research into HBM thermal management will also be a critical factor influencing the direction of future HBM technology. These developments clearly demonstrate that packaging and memory, alongside process node miniaturization, are strategically crucial areas in AI chip design.

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Source: [https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQH8cjA4nUA8BCaIT3NwKti5yHIHjoi5SEWzWSGVq7aNScbT6PLKg9yuckrOFUxS3V1O3cVEXup3Amv7HIFHEr5pc5i5KM97-\\_8AXfxYpdGDLbBpcmkC9hcgQK-4ek3DzoxApGuCst0lsq5b5wcxGvCFf\\_z5vhzjU3wcrm5drqZ2sXI4VzG7nMrXHbdO9gqYzLW-TgQKOeX0RFp3nZYX0wEK03JQgW2GP7DI4rcry-OUskuctFHI8NygthpQAdvhJZfEfHo91r57uvbSy9UP7C9JGESibWnvSO0vflsGc9T6jG-WdtaWy\\_1Cc920AqitG2Soab1P\\_dOGA==](https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQH8cjA4nUA8BCaIT3NwKti5yHIHjoi5SEWzWSGVq7aNScbT6PLKg9yuckrOFUxS3V1O3cVEXup3Amv7HIFHEr5pc5i5KM97-_8AXfxYpdGDLbBpcmkC9hcgQK-4ek3DzoxApGuCst0lsq5b5wcxGvCFf_z5vhzjU3wcrm5drqZ2sXI4VzG7nMrXHbdO9gqYzLW-TgQKOeX0RFp3nZYX0wEK03JQgW2GP7DI4rcry-OUskuctFHI8NygthpQAdvhJZfEfHo91r57uvbSy9UP7C9JGESibWnvSO0vflsGc9T6jG-WdtaWy_1Cc920AqitG2Soab1P_dOGA==)



# #14 Morgan Stanley Forecasts 93% Surge in CoWoS Demand by 2027, Anticipates AMD Venice CPU Adoption

Published July 09, 2026   Phemex News   USA



## OVERVIEW

Morgan Stanley projects a staggering 93% surge in global demand for CoWoS (Chip-on-Wafer-on-Substrate) technology by 2027, reaching 2.694 million units. Nvidia is expected to remain the largest consumer, accounting for 45% of this demand. Notably, AMD's next-generation Venice CPU is anticipated to adopt CoWoS packaging for the first time, with production managed by ASE/SPIL, Amkor, and Powertech Technology, signaling CoWoS's increasing standard status in AI and high-performance computing.

### Key Findings

According to the latest projections from Morgan Stanley, global demand for CoWoS (Chip-on-Wafer-on-Substrate) technology is set to experience an extraordinary 93% surge by 2027, reaching a total of 2.694 million units. This explosive growth is primarily fueled by the burgeoning AI and high-performance computing markets. Nvidia is expected to remain the dominant consumer, accounting for approximately 45% of this demand. A particularly significant development is the anticipated adoption of CoWoS packaging by AMD's next-generation Venice CPU, with production entrusted to leading OSAT (Outsourced Semiconductor Assembly and Test) providers such as ASE/SPIL, Amkor, and Powertech Technology.

### Technical / Clinical Details

CoWoS is an advanced packaging technology that integrates multiple logic dies and HBM (High-Bandwidth Memory) stacks onto a silicon interposer, which is then connected to an organic substrate. This technology dramatically enhances inter-chip data transfer speeds and improves power efficiency, making it indispensable for maximizing the performance of AI accelerators and HPC processors. AMD's adoption of CoWoS for its Venice CPU marks a critical strategic shift, aimed at bolstering its competitiveness in the AI and data center markets. The Venice CPU is expected to be based on the Zen 5 architecture for the server market, and its CoWoS implementation will enable the efficient integration of large L3 caches, multiple CPU cores, and HBM stacks within a single package. This configuration will deliver exceptionally high processing power and memory bandwidth, previously unachievable with conventional packaging, significantly improving the efficiency of AI workloads.

## Background & Context

The evolution of AI has introduced a new 'bottleneck' in semiconductor manufacturing: packaging. As chip miniaturization approaches its physical limits, performance gains are increasingly dependent on how efficiently and effectively multiple chips can be integrated for high performance. CoWoS stands at the forefront of this heterogeneous integration, having been widely adopted in Nvidia's GPUs and becoming a de facto standard for AI computing. AMD's embrace of CoWoS, following Nvidia, clearly indicates that major AI chip manufacturers consider this technology essential. This trend presents a significant business opportunity for OSAT providers, with companies like ASE/SPIR, Amkor, and Powertech Technology investing heavily in expanding CoWoS capacity and technical expertise. Morgan Stanley's forecast emphasizes that CoWoS is not merely a single technology but a new growth driver for the semiconductor industry in the AI era.

## Strategic Significance & Outlook

The projected 93% surge in CoWoS demand will further accelerate investment and innovation within the semiconductor industry, particularly in the advanced packaging sector. With Nvidia continuing to drive significant demand and AMD entering the CoWoS market, both technological competition and adoption are expected to intensify. OSAT providers will need to rapidly scale up their CoWoS and related 2.5D/3D packaging capabilities to meet this demand, although HBM supply and equipment availability may remain potential bottlenecks. In the long term, the evolution of CoWoS technology and improvements in its cost efficiency will enable its deployment in a wider array of AI applications, further expanding the AI chip market size. This forecast serves as a critical re-evaluation for investors, researchers, and engineers, underscoring advanced packaging as an extremely strategic domain within the semiconductor ecosystem.

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# #15 China's Memory Industry Accelerates HBM3/3E Development; YMTC Leads in Wafer-to-Wafer Hybrid Bonding Patents

Published July 05, 2026   BloomingBit.io   China



## OVERVIEW

China's memory industry is rapidly advancing, with companies like CXMT focusing on HBM3 and HBM3E development, thereby narrowing the technology gap with South Korea. Notably, Yangtze Memory Technologies Co. (YMTC), a leading NAND flash player, has taken an early lead in patenting wafer-to-wafer hybrid bonding, an advanced packaging technology crucial for ultra-high-layer NAND. This progress signals a restructuring of the global memory supply chain and intensifying competition.

### Key Findings

The Chinese memory industry is demonstrating rapid technological advancement in High-Bandwidth Memory (HBM) development, with major players like CXMT (ChangXin Memory Technologies) accelerating their readiness for HBM3 and HBM3E mass production. This push is significantly narrowing the technology gap with leading nations, particularly South Korea. Furthermore, YMTC (Yangtze Memory Technologies Co.), a prominent player in NAND flash, has emerged as a global leader in patent acquisition for wafer-to-wafer hybrid bonding, an advanced packaging technology deemed critical for ultra-high-layer NAND. These developments underscore China's growing influence in the global memory market and are poised to reshape future supply chains and competitive landscapes.

### Technical / Clinical Details

CXMT's HBM3 and HBM3E development aims to establish domestic supply capabilities for high-performance memory, essential for AI accelerators. HBM involves vertically stacking multiple DRAM dies connected by Through-Silicon Vias (TSVs), enabling ultra-fast data transfer and superior power efficiency. Concurrently, YMTC's pioneering wafer-to-wafer hybrid bonding is a breakthrough technology that allows for direct chiplet-to-chiplet or wafer-to-wafer connections. Compared to traditional micro-bump thermo-compression bonding, this technology promises finer interconnection pitches, higher connection density, shorter signal paths, and potentially lower manufacturing costs. This method is crucial for YMTC's advanced high-layer 3D NAND flash, facilitating efficient and reliable stacking of multiple memory layers, leading to dramatic increases in storage capacity and performance. YMTC's lead in patent acquisition indicates its establishing a significant technological advantage in this next-generation packaging area.

## Background & Context

Amid escalating technological competition between the U.S. and China, Beijing has prioritized semiconductor self-sufficiency, channeling massive investments into its domestic semiconductor industry. HBM is now regarded as a 'strategic material' in the AI era, making its domestic development and production critical for China's economic security. While South Korea's Samsung and SK hynix, along with the U.S.'s Micron, have long dominated the HBM market, China's rapid advancements could disrupt this oligopoly. YMTC's early lead in wafer-to-wafer hybrid bonding patents is clear evidence of China's increasing international competitiveness in advanced packaging. This technology is applicable not only to NAND but also to HBM and logic chiplet integration, promising wide-ranging impacts on future semiconductor design and manufacturing. This trend highlights the growing regional diversification in global supply chains and intensifying competition for technological supremacy.

## Strategic Significance & Outlook

The rapid technological progress of China's memory industry is poised to restructure the global HBM and advanced packaging markets. CXMT's impending mass production of HBM3/3E could intensify price competition in the global market and promote diversification of HBM supply. YMTC's advantage in hybrid bonding technology could not only expand its market share, particularly in ultra-high-layer NAND, but also enhance the overall technological prowess of China's semiconductor ecosystem through applications in other advanced packaging fields, including HBM. However, advanced semiconductor manufacturing involves complex challenges across materials, equipment, process technology, and talent development. How China overcomes these hurdles and sustains innovation will be key to its continued competitiveness in the global market. These developments underscore the need for researchers, engineers, and investors to closely monitor trends within the Chinese semiconductor industry.

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Source: [https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQGwLbuwhMU3DPZEltzcwHm7v25mCBwOQUzKkKrDdMpD8AngfKaB3MK\\_rM4n9XjDkheP9VvxJ8p9oj9Ew==](https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQGwLbuwhMU3DPZEltzcwHm7v25mCBwOQUzKkKrDdMpD8AngfKaB3MK_rM4n9XjDkheP9VvxJ8p9oj9Ew==)



# #16 Micron's HBM Order Book Fully Committed Through 2028, Secures Silicon Wafer Supply with 10-Year GlobalWafers Offtake Agreement

Published July 09, 2026 Investing.com USA



## OVERVIEW

Micron Technology's High-Bandwidth Memory (HBM) order book is fully committed through 2026 and 2027, with customer bookings extending into 2028, clearly indicating that supply, not demand, is the binding constraint for HBM. To ensure a reliable flow of raw silicon wafers essential for HBM production, Micron has directly financed GlobalWafers and signed a decade-long off-take agreement. This move highlights Micron's strong positioning in the AI memory market and its proactive approach to securing the supply chain.

### Key Findings

Micron Technology has revealed that its High-Bandwidth Memory (HBM) order book is fully committed through 2026 and 2027, with customer bookings already extending into 2028. This situation unequivocally indicates that the current bottleneck in the HBM market stems from production capacity, i.e., supply, rather than demand. To secure a stable supply of high-quality silicon wafers, which are indispensable for HBM production, Micron has directly invested in GlobalWafers, a major wafer manufacturer, and simultaneously entered into a 10-year long-term off-take agreement. This strategic move underscores Micron's robust position in the AI memory market and its proactive commitment to enhancing overall supply chain resilience.

### Technical / Clinical Details

HBM is a critical component influencing the performance of AI accelerators. It is a high-density memory technology that vertically stacks multiple DRAM dies, interconnected using Through-Silicon Vias (TSVs). Its manufacturing involves a highly complex process, from DRAM wafer production to advanced packaging. The 'yield wall' in HBM production, particularly for high-layer stacks like 12-layer configurations, means that a single defective die can render the entire package unusable, demanding extremely stringent quality control and precise manufacturing techniques. Micron's off-take agreement with GlobalWafers aims to secure a stable supply of silicon wafers, the starting material for HBM production. This is expected to reduce uncertainties in Micron's production planning and establish a stable supply system for HBM3E and future HBM4/HBM4E generations. Furthermore, this agreement supports GlobalWafers' investment in increased production, creating a win-win relationship for both the supplier and the customer.

## Background & Context

The explosive growth of AI has led to unprecedented demand for HBM within the semiconductor industry. HBM is crucial for maximizing AI chip performance due to its ability to deliver high bandwidth and low power consumption simultaneously. However, HBM manufacturing is highly technology-intensive, with advanced packaging capabilities and the supply of high-quality DRAM wafers acting as key bottlenecks. Micron's order status and long-term supply agreement highlight the strategic nature of supply chains in the AI era. Against a backdrop of intensifying technological competition between the U.S. and China and rising geopolitical risks, governments and major corporations globally are focusing on domesticating/regionalizing semiconductor supply chains and securing stable supplies of specific materials and components. Investments and collaborations with wafer suppliers like GlobalWafers are part of this global restructuring.

## Strategic Significance & Outlook

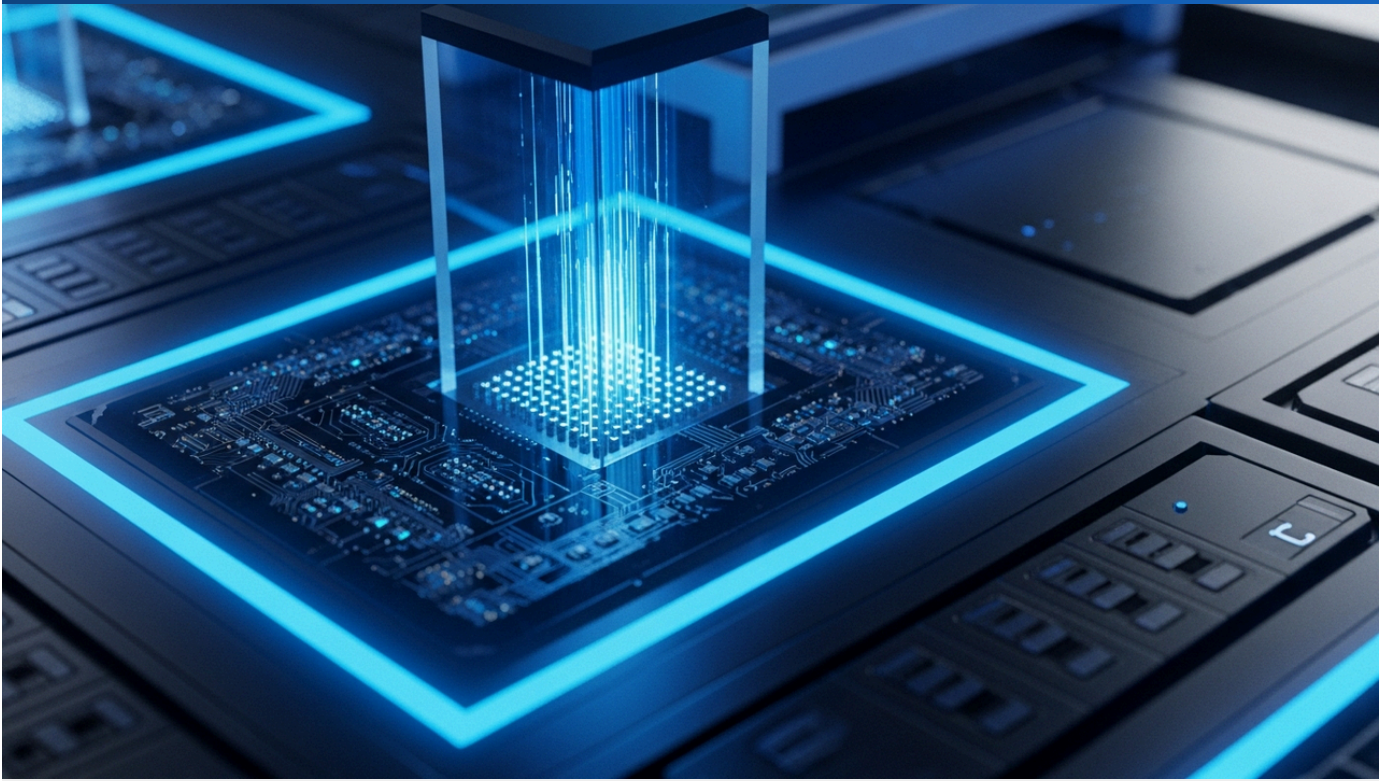
Micron's robust HBM order backlog and the secure long-term silicon wafer supply agreement form a critical foundation for the company to maintain its strong leadership in the AI memory market. This enables Micron to leverage stable supply capabilities in its competition with rivals like SK hynix and Samsung in the HBM market. The HBM market is projected to expand rapidly in the coming years, and Micron's strategy will further enhance its profitability and market share in this high-growth sector. Furthermore, such long-term agreements suggest a potential trend towards vertical integration within the semiconductor industry or closer collaboration between key suppliers and customers. As AI technology continues to evolve, securing HBM and its foundational materials will remain an indispensable factor for the sustainable growth of the semiconductor industry.

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Source: <https://www.investing.com/analysis/micron-rally-tests-whether-ai-memory-has-broken-the-cycle-200683657>

# #17 Semiconductor Industry Pivots to Heterogeneous Large-Scale Integration (HLSI) as AI Reshapes Chip Design

Published July 02, 2026   Next Move Strategy Consulting (via EE Times)   USA



## OVERVIEW

Driven by surging AI workloads, the semiconductor industry is dramatically shifting beyond traditional System-on-Chip (SoC) paradigms towards Heterogeneous Large-Scale Integration (HLSI). Advances in 3D integration and hybrid bonding enable denser die-to-die connections with near-monolithic performance. TSMC's Co-Packaged Optics technology, now in production, is redefining high-performance computing for the AI era by integrating optical links closer to the processor, as copper interconnects hit power and bandwidth limits.



### Key Findings

Fueled by the explosive growth of AI workloads, the semiconductor industry is undergoing a dramatic shift, moving beyond the confines of traditional System-on-Chip (SoC) designs towards Heterogeneous Large-Scale Integration (HLSI). This paradigm shift is being enabled by significant advancements in 3D integration and hybrid bonding, which allow for high-density connections of multiple functional dies within a single package, delivering near-monolithic performance. TSMC's Co-Packaged Optics (CPO) technology, now in production, is fundamentally redefining high-performance computing design for the AI era by bringing optical interconnects closer to the processor, as copper wiring approaches its inherent limits in bandwidth and power consumption.

### Technical / Clinical Details

HLSI represents an approach where multiple functional chiplets (e.g., CPU, GPU, memory, I/O), fabricated using different process technologies, are integrated into a single system using advanced packaging. This allows individual chiplets to be manufactured with processes optimized for their specific function, thereby balancing performance, cost, and power efficiency. 3D integration technology vertically stacks chiplets and connects them using Through-Silicon Vias (TSVs), drastically shortening wiring lengths and boosting bandwidth. Furthermore, hybrid bonding is a direct chip-to-chip connection technology that uses fine copper-to-copper bonds, offering higher density and superior electrical performance compared to conventional micro-bump bonding. This effectively elevates inter-die connection density to a near-monolithic level.

TSMC's Co-Packaged Optics (CPO) technology is a crucial innovation for addressing I/O bottlenecks in AI/HPC systems. In traditional systems, processors and optical modules existed separately, connected by electrical signals. However, as AI chip performance increases, electrical interconnects hit data transfer speed limits and increased power consumption. CPO directly integrates optical interconnects within the processor package, shortening the distance for electrical-to-optical signal conversion, achieving ultra-high-speed data transmission and significant power efficiency improvements. This enables a dramatic increase in connection bandwidth between AI clusters in data centers.

## Background & Context

The deceleration of Moore's Law prompted the semiconductor industry to seek new ways to improve chip performance and reduce costs. The immense data processing capabilities and low latency required by fields such as AI, data centers, and 5G/6G communication can no longer be met by traditional SoC approaches alone. HLSI and chiplets have emerged as powerful solutions to this challenge, leading to the development of various advanced packaging technologies like Intel's EMIB, Samsung's I-Cube, and TSMC's CoWoS/SolC. CoWoS, in particular, has been widely adopted in Nvidia's AI accelerators, becoming a de facto standard for AI chip design. The introduction of CPO signifies a new phase where I/O bottlenecks constrain overall system performance, implying that optical technology is becoming an indispensable component of semiconductor packaging.

## Strategic Significance & Outlook

The shift towards HLSI will continue to fundamentally redefine semiconductor industry design and manufacturing for years to come. With increasing complexity of AI workloads and data volumes, the demand for higher-density and more efficient chip integration will only grow. Technologies like 3D integration, hybrid bonding, and Co-Packaged Optics are key to pushing the boundaries of AI performance, enabling new applications and services. This trend fosters collaboration and innovation across the entire semiconductor ecosystem, from chip designers to packaging engineers, material scientists, and manufacturing equipment suppliers. The commencement of CPO mass production will significantly impact AI data center architectures, contributing to the realization of more energy-efficient, high-performance computing infrastructure. HLSI is not just a technical advancement, but a strategic turning point for the semiconductor industry to overcome physical and economic constraints and build the foundation for next-generation computing.

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Source: <https://www.nextmsc.com/news/chiplet-market-pivots-to-hlsi-as-ai-reshapes-chip-design>



# #18 SK Hynix to Heavily Invest in ASML EUV for HBM Production in Yongin and Cheongju, Expanding Indiana Packaging Facility

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## OVERVIEW

SK hynix plans to extensively deploy ASML's EUV (Extreme Ultraviolet) lithography equipment at its Yongin Semiconductor Cluster and Cheongju advanced packaging facilities, significantly bolstering High-Bandwidth Memory (HBM) production capacity. This strategy includes a \$4 billion investment in an advanced packaging facility in Indiana, aiming to secure technological leadership and supply stability in HBM production. This move addresses strong demand for HBM3E and HBM4, maintaining competitiveness in the AI memory market.

### Key Findings

SK hynix is moving forward with plans for a large-scale deployment of ASML's EUV (Extreme Ultraviolet) lithography equipment at its Yongin Semiconductor Cluster and advanced packaging facilities in Cheongju, South Korea. This strategic investment is aimed at dramatically enhancing High-Bandwidth Memory (HBM) production capacity, specifically to stabilize the supply of next-generation AI memories such as HBM3E and HBM4. Additionally, the company is investing \$4 billion in an advanced packaging facility in Indiana, USA, diversifying its global production footprint while striving to secure technological leadership and supply stability in HBM production.

### Technical / Clinical Details

EUV lithography is the most advanced technology currently available for forming fine circuit patterns in semiconductor manufacturing, essential for DRAM miniaturization and performance enhancement. SK hynix's adoption of EUV equipment will improve the density and efficiency of the DRAM dies that constitute HBM, allowing for more memory layers to be stacked while maintaining footprint. This will further expand HBM bandwidth, maximizing AI accelerator performance. Furthermore, the advanced packaging facilities in Cheongju are expected to implement sophisticated 2.5D/3D packaging technologies to integrate EUV-manufactured DRAM dies onto substrates. The Indiana facility will primarily focus on final HBM packaging and testing, complementing the AI chip manufacturing ecosystem within the U.S. This represents SK hynix's comprehensive strategy to establish technological leadership in both front-end (DRAM manufacturing) and back-end (packaging) processes for HBM production.

## Background & Context

The explosive growth of AI has driven HBM demand to unprecedented levels, making it a major bottleneck in the AI chip supply chain. SK hynix has been a pioneer in the HBM market, leading the way by supplying HBM3E to key customers like Nvidia. The adoption of EUV is a crucial step to overcome the limits of miniaturization and maintain a competitive edge, especially as HBM's technological complexity increases. The significant investment in the U.S. is a response to escalating technological competition between the U.S. and China and rising geopolitical risks, aligning with U.S. policies (such as the CHIPS Act) to disperse supply chains geographically and strengthen domestic advanced semiconductor manufacturing capabilities. Samsung, another South Korean giant, is also making substantial investments in HBM production capacity, intensifying competition in the AI memory market.

## Strategic Significance & Outlook

SK hynix's deployment of EUV lithography equipment and massive investments in Yongin, Cheongju, and Indiana will significantly enhance its HBM production capacity and technological leadership, solidifying its position in the AI memory market. Strong demand for HBM3E and HBM4 is projected to continue, and SK hynix's expanded supply capabilities will be an essential contribution to the development of global AI infrastructure. However, the introduction of expensive EUV equipment and large-scale investments may impact HBM manufacturing costs, potentially intensifying price competition in the market. In the long term, proficiency in EUV technology and advanced packaging capabilities is expected to be a critical factor determining the competitiveness of HBM suppliers. This strategy represents a significant step for SK hynix to remain at the forefront of technological innovation in the AI era.

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Source: <https://seekingalpha.com/article/4921058-micron-its-hbm4-crucial-catalyst-is-still-being-ignored>