

Semiconductor_BackEnd

Weekly Intelligence Report

2026-07-19 | 33 articles | 6 countries

troy-technical.jp

This Week's Keyword

Advanced Packaging

AI demand fuels capacity race & new tech

33

articles

Total Articles Analyzed

6

countries

Source Countries

93

%

CoWoS Demand Surge (2027)

2028

year

ABF Shortage Persistence

All 33 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	Adv. Pkg. New AI Bottleneck	Market Overview						Advanced packaging, especially CoWoS, is the new AI chip bottleneck, driving global capex and Nvidia's supply diversification.
#02	ASE Doubles CoWoS Capacity	Corporate Strategy						ASE plans its largest global expansion to double CoWoS capacity to 45,000 wafers/month by late 2027, addressing AI chip demand.
#03	Applied Mat. New 3D Pkg Sys	New Product						Applied Materials launches seven new systems for DRAM scaling and 3D packaging, including hybrid bonding and TSV tools, to resolve AI chip bottlenecks.
#04	ABF Shortage Thru 2028	Market Analysis						ABF substrate shortage to continue until 2028 due to AI demand, affecting high-end chip production, costs, and capacity.
#05	Amkor Expands US Pkg Cap.	Corporate Strategy						Amkor expands its Arizona campus with CHIPS Act funding to build the first high-volume US advanced packaging OSAT facility, boosting domestic capacity.
#06	Samsung 2.xD SiPh Pkg	Research /New Technology						Samsung develops '2.xD' advanced packaging integrating HBM, logic, and silicon photonics to resolve AI data center power/data bottlenecks.
#07	ABF: True AI Bottleneck	Industry Analysis						ABF substrates are a more critical bottleneck than DRAM for AI, with supply constraints delaying AI chip market entry, benefiting key manufacturers.
#08	Wah Lee/Asahi Photoresist	Corporate Strategy						Wah Lee and Asahi Kasei double high-resolution dry film photoresist capacity in Tainan to meet surging ABF substrate demand, fortifying the supply chain.
#09	Morgan Stanley CoWoS F'cast	Market Forecast						Morgan Stanley forecasts a 93% CoWoS demand surge by 2027, driven by AMD's Venice CPUs, expanding CoWoS beyond AI accelerators.
#10	AMAT Hybrid Bonding Key	Corporate Technical Report						Applied Materials highlights material engineering, especially hybrid bonding, as critical for scaling AI chip performance across logic, DRAM, HBM, and packaging.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#11	TSMC Chiayi Pkg Plants	Corporate Strategy						TSMC plans three advanced packaging plants in Chiayi, targeting mass production by 2027 for AI and quantum tech, developing CoPoS and glass-core substrates.
#12	AMAT Pkg Rev. Growth	Market Analysis						Applied Materials forecasts over 50% advanced packaging revenue growth in 2026; Micron boosts HBM packaging, highlighting back-end equipment investment.
#13	AMAT MES for Adv. Pkg	Corporate Technical Report						Applied Materials emphasizes MES's critical role in recovering capacity and managing complexity for advanced packaging and test facilities, reducing 10-20% capacity loss.
#14	Rapidus 2nm AI by 2027	Corporate Strategy						Japan's Rapidus aims for 2nm AI chip mass production by 2027, stimulating demand across the semiconductor ecosystem, with IBM partnership.
#15	HBM Dual Bottlenecks	Market Analysis						HBM faces dual bottlenecks in DRAM wafer production and advanced packaging/test, deepening the supply crunch amid fierce competition from Samsung, SK Hynix, Micron.
#16	TSMC CoWoS 200K/Mo	Corporate Strategy						TSMC accelerates CoWoS capacity expansion to 200K wafers/month by 2027 to meet AI demand, critical for alleviating AI accelerator bottlenecks.
#17	TSMC CPO vs. Samsung 2.xD	Technology Comparison						TSMC leads in CPO switches with Broadcom/NVIDIA, while Samsung develops '2.xD' packaging integrating HBM, logic, and SiPh for future AI optical I/O.
#18	TSMC N3/CoWoS for Nvidia	Market Analysis						TSMC's N3 node and expanding CoWoS capacity secure Nvidia's future, while HBM4 multi-vendor qualification reduces supply risk for higher-capacity memory.
#19	TSMC Q2 Record, CoWoS Booked	Corporate Earnings						TSMC reports record Q2 revenue, CoWoS fully booked through 2026, and plans 14-reticle packaging, raising capex for advanced packaging.
#20	Rapidus IBM 2nm P'ship	Corporate Strategy						Japan's Rapidus partners with IBM on 2nm semiconductor manufacturing to bolster Indo-Pacific supply chain resilience, targeting 2027 mass production.
#21	ABF Orders Surge, Gap Widens	Market Analysis						AI-driven advanced packaging orders surge, widening the ABF carrier board supply-demand gap, benefiting suppliers like Unimicron, Ibiden, and AT&S.;
#22	Rapidus/Cadence AI SoC	Corporate Strategy						Rapidus partners with US-based Cadence on Agentic AI for advanced SoC design, driving system-level co-optimization across design, manufacturing, and packaging.
#23	TSMC Glass Core Substrate	Research/New Technology						TSMC, with NVIDIA, is developing 'glass core substrates' to revolutionize AI chip manufacturing by 2028, suppressing warpage and improving power integrity.
#24	NVIDIA CoWoS F'cast Up	Market Forecast						KeyBanc raises NVIDIA's 2027 CoWoS supply forecast to 1.1M interposers (69% increase); AMD also sees over 50% growth, indicating strong demand.
#25	NVIDIA Bottleneck, Intel EMIB	Market Analysis						TSMC's CoWoS capacity is fully booked through 2026, bottlenecking NVIDIA's AI chip supply, prompting consideration of Intel's EMIB as an alternative.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#26	CoWoS Bottleneck for AI GPU	Industry Analysis	●●●○ ○	●●●● ●	●●●● ●	●●●○ ○	●●●● ○	CoWoS capacity, distinct from HBM shortage, is the core manufacturing integration bottleneck for AI GPU shipments, impeding final delivery.
#27	Taiwan TGV Glass Adv.	New Technology	●●●● ○	●●●○ ○	●●●● ○	●●●○ ○	●●●● ●	Taiwan's TGV glass substrate supply chain advances with E&R; Engineering shipping laser modification equipment to a US client, accelerating mass production.
#28	AT&S;/Ibiden ABF Invest	Corporate Strategy	●●●○ ○	●●●● ○	●●●● ○	●●●○ ○	●●●● ●	AT&S; invests €1.5-2B in Malaysian ABF capacity (with AMD backing), and Ibiden allocates ¥500B for AI/HPC substrate expansion, addressing shortages.
#29	Malaysia HBM4 Pilot Line	Government Initiative	●●●○ ○	●●●○ ○	●●●○ ○	●●●○ ○	●●●○ ○	Malaysia launches a RM92M government-backed initiative to develop an HBM4 advanced packaging pilot line, aiming for a higher semiconductor value chain.
#30	Samsung 2.xD Pkg Adv.	Research/New Technology	●●●● ●	●●●○ ○	●●●● ●	●●●● ○	●●●○ ○	Samsung advances "2.xD" packaging, integrating HBM, logic, and silicon photonics using panel-based RDL interposers to resolve AI power/heat bottlenecks.
#31	AMAT TSMC Pact, NEXX Acq.	Corporate Strategy	●●●○ ○	●●●● ●	●●●● ○	●●●○ ○	●●●● ●	Applied Materials strengthens AI advanced packaging with a 10-year TSMC partnership and NEXX acquisition, aligning its roadmap with TSMC's AI build-out.
#32	Micron US DRAM/HBM Invest	Corporate Strategy	●●●○ ○	●●●● ○	●●●● ○	●●●○ ○	●●●● ●	Micron invests \$500M in GlobalWafers' Texas plant, aiming for 40% US DRAM production by 2035, with HBM packaging ramping in Singapore (2026) and US (2028).
#33	Samsung vs Ibiden Substrates	Corporate Strategy	●●●● ○	●●●○ ○	●●●● ○	●●●○ ○	●●●○ ○	Samsung Electro-Mechanics challenges Ibiden in AI server package substrates by enhancing FC-BGA and pushing next-gen glass substrate technologies.

●●●●○ High ●●●○● Med-High ●●●○● Med ●●●○● Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI supply chain exposed to critical packaging bottlenecks?

The CoWoS and ABF substrate shortages are projected to persist through 2028, directly impacting AI chip production. Nvidia is already diversifying beyond TSMC. Have you identified your critical dependencies and secured long-term capacity?

❷ Does next-gen packaging make your current platform obsolete?

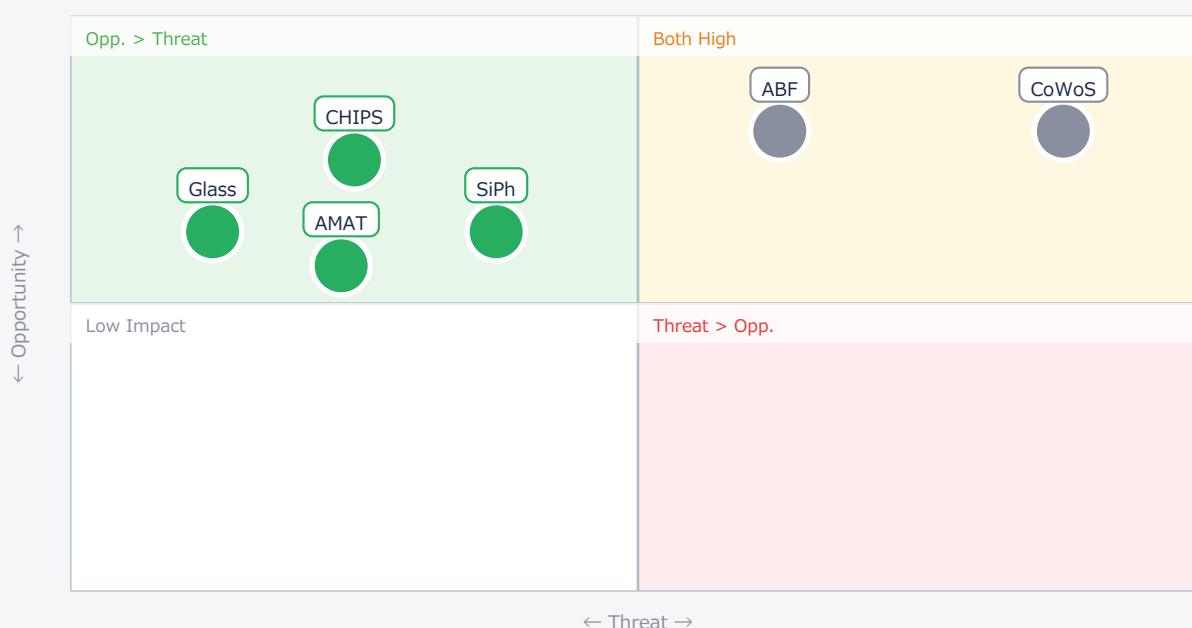
Samsung's 2.xD with SiPh and TSMC's glass core substrates promise revolutionary power/performance gains. These technologies could redefine AI system architecture. Are your R&D; teams evaluating these shifts and their impact on your product roadmap?

❸ Are you leveraging CHIPS Act incentives for advanced packaging?

Amkor and Micron are making significant US investments in advanced packaging and HBM production, backed by CHIPS Act funding. Is your company strategically positioned to benefit from or compete with this domestic capacity build-out?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
● CoWoS	Critical	Capacity growth	Supply limits
● ABF	Critical	Pricing power	Production delays
● Glass	Opp.	Next-gen perf	Tech shift risk
● SiPh	Opp.	Optic I/O	Lagging tech
● CHIPS	Opp.	Domestic supply	Geo-risk
● AMAT	Opp.	Tool sales	Outdated tech

Deep Dive ① — Advanced Packaging: The New AI Bottleneck

#01 | 2026/07/14 | The Economy | Tech Novelty ●●○○○ Proximity ●●●●● Market Impact ●●●●● Data Reliability ●●●○○ US/EU Relevance ●●●●●

Advanced packaging, particularly TSMC's CoWoS, has superseded process technology as the primary bottleneck in AI chip production, compelling major players like Nvidia to diversify supply chains, potentially including Intel's EMIB.

This shift is driving a global surge in capital expenditure across OSATs and material suppliers, with Amkor planning a \$7B Arizona facility and ASE projecting \$3.5B+ in advanced packaging revenue, highlighting critical investment needs.

► Strategic Analyst's Perspective

Strategic Analyst's Perspective: The published numbers on capacity expansion and revenue growth appear realistic, reflecting the intense demand. The primary technical barrier is the sheer complexity and capital intensity of scaling CoWoS and similar advanced packaging. [Opportunity] for US/EU equipment suppliers (e.g., Applied Materials) and OSATs (e.g., Amkor) to capture market share and government incentives. [Threat] for US/EU OEMs reliant on single-source advanced packaging, risking supply chain exposure and delayed product launches. Next actions: [Procurement] Conduct immediate supply chain audits for CoWoS/HBM dependencies; [Strategy] Evaluate alternative packaging technologies (e.g., Intel EMIB) by next month.

Deep Dive ② — Samsung's 2.xD: HBM, Logic, SiPh Integration

#06 | 2026/07/13 | DigiTimes | Tech Novelty ●●●●● Proximity ●●●○○ Market Impact ●●●●● Data Reliability ●●●○○ US/EU Relevance ●●●○○

Samsung is developing '2.xD' advanced packaging that integrates HBM, logic chips, and silicon photonics (SiPh) into a single package, aiming to resolve critical power consumption and data transfer bottlenecks in AI data centers.

This innovation leverages panel-based redistribution layer (RDL) interposers and evolving bonding techniques from micro bumps to bumpless hybrid bonding, maximizing inter-chip data transfer speeds and minimizing power consumption.

► Strategic Analyst's Perspective

Strategic Analyst's Perspective: Samsung's '2.xD' concept is highly ambitious and technically sound, leveraging their unique 'triple-play' portfolio. The challenge lies in achieving high yields and cost-effectiveness for bumpless hybrid bonding and panel-based RDL interposers at scale. [Opportunity] for US/EU companies in optical interconnects, advanced materials, and specialized equipment for SiPh integration. [Threat] for US/EU chip designers and data center operators if they cannot access or develop similar integrated optical packaging solutions, leading to competitive disadvantage in AI efficiency. Next actions: [R&D;] Initiate feasibility studies on SiPh integration into advanced packaging within 1 month; [Business Dev] Explore potential partnerships with SiPh component suppliers immediately.

Deep Dive ③ — TSMC & NVIDIA Pioneer Glass Core Substrates

#23 | 2026/07/15 | 三立新聞網SETN.COM | Tech Novelty●●●●● Proximity●●●○○ Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●●

TSMC, in collaboration with NVIDIA, is developing 'glass core substrates' to revolutionize AI chip manufacturing by 2028. This technology is crucial for suppressing chip warpage, improving power integrity, and enhancing AI computing power.

Glass core substrates offer superior flatness, lower CTE, and finer wiring capabilities than organic substrates, enabling higher-density 3D stacking and improved signal integrity for next-gen AI accelerators.

► Strategic Analyst's Perspective

Strategic Analyst's Perspective: The potential of glass core substrates is transformative, and the involvement of TSMC and NVIDIA validates its realism. Key technical barriers include manufacturing large-sized, defect-free glass substrates and developing precise TGV (Through-Glass Via) formation and metallization processes. [Opportunity] for US/EU materials suppliers (e.g., specialty glass, laser equipment) and packaging equipment manufacturers to become key enablers. [Threat] for US/EU companies heavily invested in traditional organic substrates or silicon interposers if they fail to pivot quickly, risking technological obsolescence and market share loss. Next actions: [R&D;] Establish a task force to evaluate glass substrate technology and TGV manufacturing by end of quarter; [Strategy] Identify potential M&A; targets or strategic partners in glass processing technology.

Other Notable Articles

Applied Materials Unveils Seven New Systems for AI Chip DRAM Performance and Advanced 3D Packaging, Accelerating Bottleneck Resolution (Industry News)

Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●○

New AMAT tools for hybrid bonding, TSVs, and metrology are critical enablers for next-gen AI packaging and HBM production.

Global ABF Substrate Shortage to Persist Through 2028 Due to Soaring AI Demand, Impacting High-End Chip Production (DigiTimes)

Tech Novelty●●○○○ Proximity●●●●● Market Impact●●●●●

The prolonged ABF shortage is a major supply chain risk for all high-end AI/HPC chip manufacturers; diversification is paramount.

Amkor Technology Expands Arizona Campus with 67-Acre Acquisition, Bolstering U.S. Advanced Packaging OSAT Capacity (AllMind AI News)

Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●○

Amkor's US expansion, backed by CHIPS Act, is a significant step towards domestic advanced packaging, enhancing supply chain resilience.

TSMC Plans Three Advanced Packaging Plants at Chiayi Science Park, Targeting Mass Production by 2027 for AI and Quantum Tech (Taiwan News)

Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○

TSMC's aggressive CoWoS expansion and development of CoPoS/glass-core substrates will shape future AI and quantum computing packaging.

AT&S; to Invest €1.5-2 Billion in Malaysian ABF Capacity, While IBIDEN Allocates ¥500 Billion for AI/HPC Substrate Expansion in Japan & Overseas (Sector Signals)

Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●○

Major investments by AT&S; (EU) and Ibiden (Japan) in ABF substrates are crucial to alleviate the global AI/HPC supply crunch.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

■ Immediate (this week)

- [Procurement] Conduct urgent audit of advanced packaging (CoWoS, HBM, ABF) supply chain dependencies and identify single points of failure.
- [Executive] Schedule a cross-functional meeting to assess the immediate impact of CoWoS/ABF shortages on Q3/Q4 production forecasts and customer commitments.
- [Strategy] Begin preliminary evaluation of Intel's EMIB and other alternative advanced packaging options for AI chip integration.

■ Short-term (1 month)

- [R&D;] Task a dedicated team to research and benchmark emerging packaging technologies (e.g., glass core substrates, SiPh integration) against current roadmaps.
- [Business Dev] Initiate discussions with new or expanding advanced packaging OSATs (e.g., Amkor, ASE) and material suppliers (e.g., Ibiden, AT&S;) to secure future capacity.
- [Legal/IP] Review IP landscape for next-generation packaging materials and processes, identifying potential licensing opportunities or infringement risks.

■ Medium-long term (quarter+)

- [Strategy] Develop a multi-year strategy for advanced packaging, including potential domestic manufacturing investments (leveraging CHIPS Act) and strategic partnerships.
- [R&D;] Invest in internal capabilities for advanced packaging design, simulation, and characterization to reduce reliance on external expertise.
- [Procurement] Establish long-term, multi-vendor supply agreements for critical advanced packaging materials and services to enhance supply chain resilience.

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Semiconductor_BackEnd — Selected Articles

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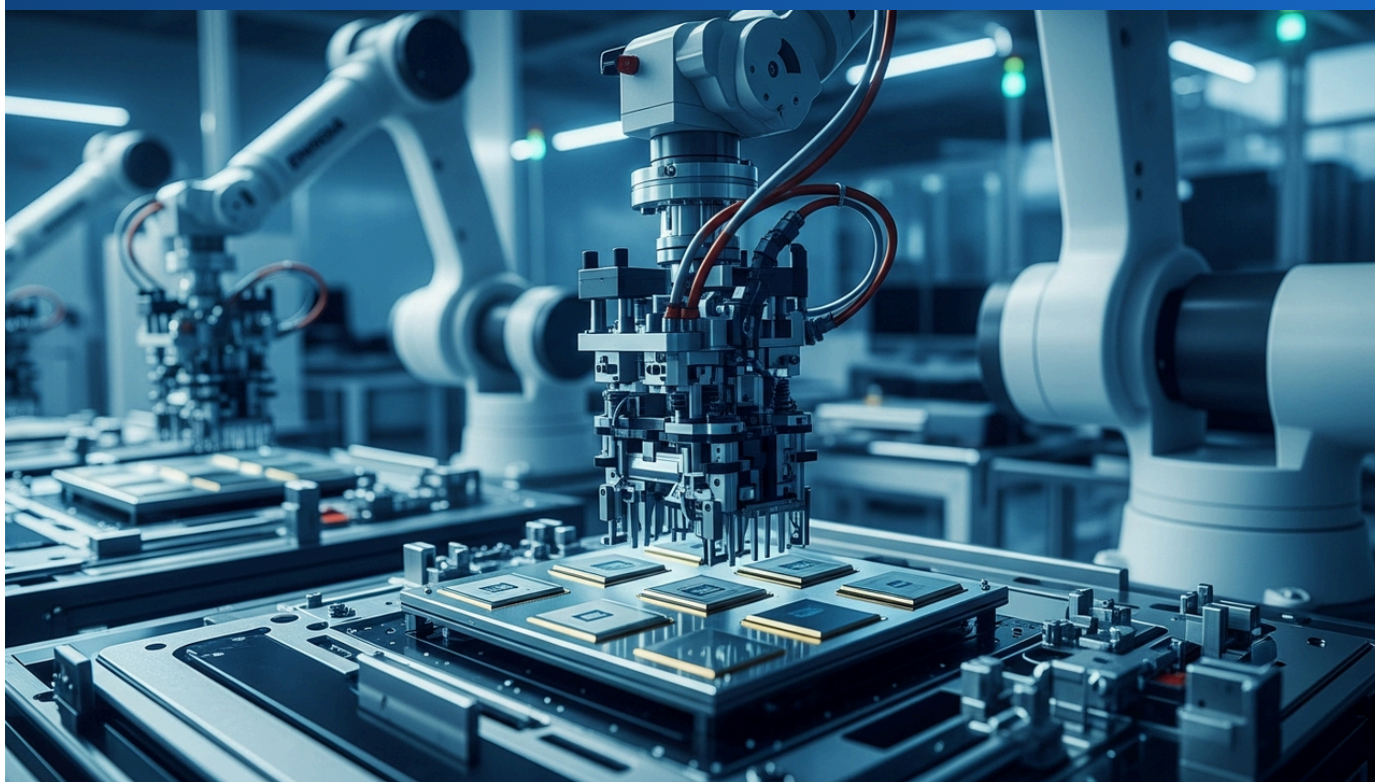
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- #29 Malaysia Launches RM92 Million Government-Backed Initiative to Develop HBM4 Advanced Packaging Pilot Line, Targeting Higher Semiconductor Value Chain
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#01 Advanced Packaging Becomes the New Bottleneck for AI Chip Production, Driving Global Capex Race and Nvidia's Supply Diversification Efforts

Published July 14, 2026 The Economy International



OVERVIEW

Advanced packaging, not process technology, is now the primary bottleneck in AI chip production, prompting Nvidia to explore diversifying its CoWoS supply, potentially including Intel's EMIB. This shift is fueling a global surge in capital expenditure across OSATs and material suppliers. ASE projects advanced packaging revenue exceeding \$3.5 billion (10% growth) this year, while Amkor plans a \$7 billion Arizona facility, highlighting the critical investment needed to meet escalating AI demand.

Key Findings

The primary bottleneck in AI chip production has decisively shifted from advanced process technology to advanced packaging capacity, triggering an intense global capital expenditure race. Crucially, the limited supply of TSMC's CoWoS (Chip-on-Wafer-on-Substrate) technology is compelling major AI chip developers, including Nvidia, to explore diversifying their supply chains, potentially incorporating competing solutions like Intel's EMIB process.

Technical and Clinical Details

The semiconductor industry is witnessing rapid expansion in High Bandwidth Memory (HBM) wafer production, stacking, packaging, and testing capabilities, with South Korean memory chipmakers significantly ramping up investments. Taiwan's ASE anticipates its advanced packaging revenue to surpass \$3.5 billion this year, reflecting a 10% growth, underscoring the escalating demand. Concurrently, Amkor is planning a monumental investment of up to \$7 billion for a new facility in Arizona, with initial production targeted for early 2028. Japan's Ibiden forecasts substantial growth in IC substrates for AI servers by 2030, while Ajinomoto maintains over 95% market share in the global ABF (Ajinomoto Build-up Film) substrate market. SK Hynix has further enhanced HBM4E thermal resistance through its proprietary MR-MUF process, demonstrating ongoing innovation in performance. China's leading OSAT provider, JCET, is investing approximately \$1.15 billion in a new advanced packaging and testing facility in Shanghai, reflecting the global nature of this expansion.

Background and Industry Context

The exponential performance gains in AI chips are no longer solely dependent on transistor scaling but increasingly on advanced packaging techniques that efficiently integrate multiple chiplets and HBM. Technologies such as CoWoS are vital for achieving higher data transfer rates and lower power consumption, yet their manufacturing demands sophisticated processes and substantial capital, leading to current supply shortfalls. The scarcity of key packaging materials like ABF substrates and overall manufacturing capacity is pressing, driving semiconductor manufacturers to bolster in-house capabilities and forge partnerships with OSATs to alleviate these bottlenecks. This situation elevates advanced packaging from a 'back-end' process to a strategic, front-and-center component of the semiconductor value chain.

Strategic Significance and Outlook

The sustained surge in AI chip demand guarantees continued acceleration of investments in advanced packaging. Nvidia's consideration of Intel's technology signals not only heightened competition but also potential cross-industry technical collaborations to overcome critical supply limitations. With ABF substrate and CoWoS capacity shortages projected to persist through 2028, innovation and expansion in advanced packaging are paramount for the development of next-generation AI infrastructure. A concerted effort involving material suppliers, equipment manufacturers, OSATs, and foundries is essential to resolve these systemic bottlenecks and enable the full potential of AI.

Source: <https://economy.ac/news/2026/07/202607289543>

#02 ASE Initiates Largest-Ever Global Expansion to Double CoWoS Capacity to 45,000 Wafers/Month by Late 2027

Published July 17, 2026 Industry Blog/Analysis International



OVERVIEW

ASE is undertaking its largest global factory expansion in history, commencing construction of six new packaging and testing plants in 2026. This aggressive ramp aims to increase monthly CoWoS capacity from 20,000 wafers by end-2026 to 40,000-45,000 by end-2027. This monumental investment addresses surging AI chip demand, reinforcing advanced packaging's critical role in the semiconductor supply chain.

Key Findings

ASE, a global leader in advanced packaging, is embarking on its largest-ever factory expansion project worldwide to meet the explosive demand for AI chips. The company plans to initiate construction of six new packaging and testing plants globally in 2026, targeting a substantial increase in its monthly CoWoS (Chip-on-Wafer-on-Substrate) capacity to 20,000 wafers by the end of 2026 and further doubling it to 40,000-45,000 wafers by the end of 2027.

Technical and Clinical Details

ASE's ambitious expansion involves an investment exceeding NT\$108.3 billion (approximately \$3.4 billion) in Kaohsiung Renwu, Taiwan, and the acquisition of Innolux's Southern Science Park Fab5 for establishing advanced production lines. This strategy is designed to significantly boost its CoWoS and related advanced packaging capabilities. Concurrently, Amkor is expanding its Arizona campus and has inked a ten-year agreement with TSMC to secure CoWoS packaging and testing capacity in the U.S. Samsung also intends to establish a \$4 billion packaging and testing hub in Thai Nguyen Province, Vietnam, initially focusing on traditional memory testing with long-term plans to evolve into HBM packaging. TSMC's Arizona project is equally comprehensive, including eight wafer fabs and four advanced packaging facilities, with local packaging mass production anticipated around 2028.

Background and Industry Context

The relentless advancement of AI is driving unprecedented demand for high-performance semiconductors such as CPUs, GPUs, and HBM. These chips necessitate sophisticated advanced packaging technologies for complex 3D stacking and heterogeneous integration. CoWoS has emerged as a core technology for high-performance AI accelerators, and its limited availability has become a critical bottleneck constraining overall AI chip shipments. OSAT companies like ASE are responding with record-breaking capital expenditures to mitigate this bottleneck and prepare for future AI demand. This trend unequivocally highlights the strategic importance of back-end packaging, which now plays as crucial a role as front-end lithography in semiconductor manufacturing.

Strategic Significance and Outlook

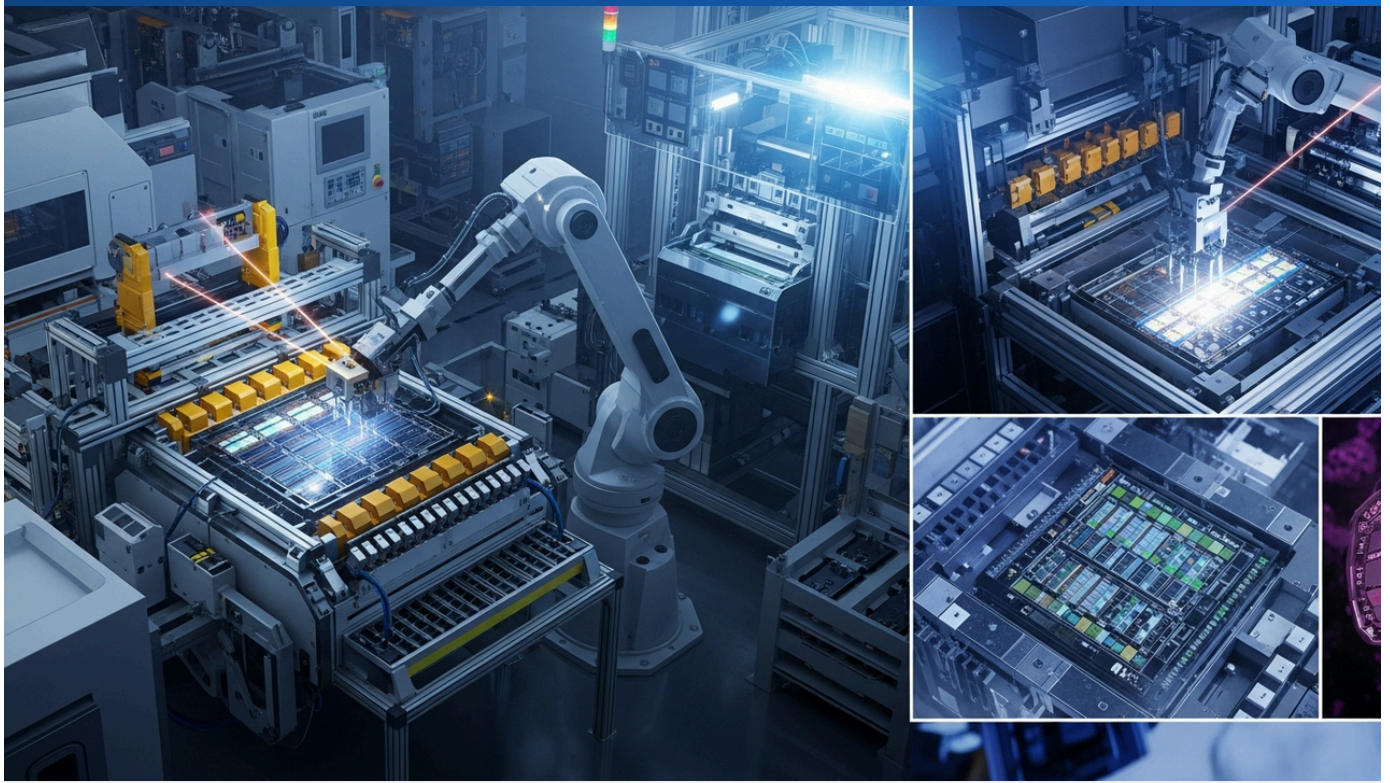
ASE's massive expansion, coupled with strategic collaborations among industry leaders, heralds a 'golden age' for advanced packaging in the AI era. The increased CoWoS capacity will help stabilize the supply of AI chips from major vendors like Nvidia and AMD, accelerating the broader adoption of AI technologies. Furthermore, the geographic diversification of manufacturing footprints by these companies is expected to enhance supply chain resilience and mitigate geopolitical risks. Advanced packaging will continue to be a pivotal factor in driving AI chip performance improvements and cost efficiencies in the foreseeable future.

Source: <https://eu.36kr.com/en/p/3899029791623044>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#03 Applied Materials Unveils Seven New Systems for AI Chip DRAM Performance and Advanced 3D Packaging, Accelerating Bottleneck Resolution

Published July 09, 2026 Industry News International



OVERVIEW

Applied Materials introduced seven new semiconductor manufacturing systems designed to address bottlenecks in AI chip production, specifically enhancing DRAM performance scaling and advanced 3D packaging. Key innovations include an enhanced Centura Prime Epi system for DRAM, Opta Quad CMP for hybrid bonding, Nokota VMax 2 for TSVs and microbumps, and advanced eBeam metrology. These tools aim to improve yields in high-bandwidth memory (HBM) and chiplet-based designs, critical for the AI era.

Key Findings

Applied Materials has launched seven innovative semiconductor manufacturing systems aimed at resolving critical bottlenecks in AI chip production, with a focus on DRAM performance scaling and advanced 3D packaging. These new systems are designed to improve yields in high-bandwidth memory (HBM) and chiplet-based designs, thereby facilitating the high-performance demands of AI chips.

Technical and Clinical Details

The newly introduced suite of systems addresses two primary domains. For DRAM performance scaling, an enhanced Centura Prime Epi epitaxy system has been developed. This system optimizes crucial film deposition processes in DRAM manufacturing, contributing to the performance improvement of next-generation memory. For advanced packaging, three pivotal process tools have been introduced: The Opta Quad CMP system is engineered for chemical mechanical planarization (CMP), a critical step for hybrid bonding technology, ensuring exceptional flatness and uniformity. The Nokota VMax 2 electrochemical deposition system enables high-precision copper filling for Through-Silicon Vias (TSVs) and microbumps. Additionally, two eBeam systems, including the VeritySEM 7AP, provide critical dimension (CD) metrology on heterogeneous substrates, guaranteeing the accuracy and quality of complex 3D structures. These tools directly contribute to optimizing fine interconnections and yields, which are major challenges in HBM and chiplet integration.

Background and Industry Context

The explosive growth of AI has made high-performance CPUs, GPUs, and high-capacity, high-bandwidth memory (HBM) indispensable. These AI chips necessitate advanced packaging technologies that integrate multiple distinct chiplets and HBM stacks beyond mere transistor density. However, this intricate packaging process has emerged as a new manufacturing bottleneck, characterized by challenges in fine interconnections, thermal management, and yield optimization. Applied Materials' new systems directly confront these challenges, aiming to expand AI chip manufacturing capabilities from the perspectives of materials engineering and process technology.

Strategic Significance and Outlook

These innovative systems from Applied Materials are poised to be crucial enablers for accelerating AI chip performance enhancement and mass production. Advanced technologies like hybrid bonding and TSVs are particularly important for significantly improving interconnection density and efficiency between chiplets, essential for next-generation AI accelerators and data center processors. These tools not only refine existing processes but also establish new benchmarks for semiconductor manufacturing in the AI era, paving the way for the realization of more complex and higher-performing chip designs, thereby exerting a significant impact across the industry.

Source: <https://datatech.disruptsmedia.com/semiconductors/applied-materials-launches-seven-systems-ai-chip-dram-and-packaging>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#04 Global ABF Substrate Shortage to Persist Through 2028 Due to Soaring AI Demand, Impacting High-End Chip Production

Published July 14, 2026 DigiTimes Taiwan



OVERVIEW

The global market for ABF (Ajinomoto Build-up Film) substrates is projected to remain in shortage through 2028, driven by escalating demand for AI hardware. This scarcity directly impacts the production of high-end processors like CPUs, GPUs, and AI accelerators, potentially leading to increased costs, delayed capacity, and uneven access to advanced chips. Expanding ABF substrate production is complex and capital-intensive, making a swift resolution unlikely.

Key Findings

The global market for ABF (Ajinomoto Build-up Film) substrates is anticipated to endure a severe supply shortage until 2028, a direct consequence of the escalating demand for AI hardware. This prolonged scarcity is significantly impacting the manufacturing capacity of high-end processors, including CPUs, GPUs, and AI accelerators.

Technical and Clinical Details

ABF substrates are indispensable materials for the advanced packaging of high-performance AI and High-Performance Computing (HPC) chips. Their multi-layered structure and fine wiring technology are crucial for ensuring high-speed data transfer and signal integrity between chips. However, ABF substrate manufacturing is not only technologically demanding but also requires enormous capital investment for factory construction and specialized equipment, coupled with lengthy lead times. The current rate of production capacity expansion (approximately 15-20% annually) cannot keep pace with the explosive growth in AI demand, leading to a widening supply-demand gap. Consequently, major chipmakers and foundries such as Intel, AMD, Nvidia, and TSMC, along with substrate suppliers like Unimicron and Ibiden, are directly affected by this situation.

Background and Industry Context

The recent surge in demand for high-performance semiconductors across AI, 5G, data centers, and automotive sectors has led to increasingly complex chip packaging requirements. As traditional packaging technologies struggle to meet these new demands, the importance of advanced packaging materials like ABF substrates has risen dramatically. ABF substrates are particularly vital for enabling chiplet technology and 3D stacking. However, the confluence of supply chain disruptions since the COVID-19 pandemic and the subsequent AI boom has exacerbated the pre-existing constraints on ABF substrate supply. This has empowered substrate suppliers with increased pricing power while simultaneously subjecting them to immense pressure to expand production rapidly.

Strategic Significance and Outlook

The persistent ABF substrate shortage could lead to higher manufacturing costs for AI chips and delays in market entry, potentially influencing the overall growth trajectory of the semiconductor industry. While this situation presents revenue opportunities for substrate suppliers, it also incentivizes accelerated capital investment and technological innovation. Companies are now focused on securing stable supply and establishing mass production capabilities through long-term customer commitments and strategic alliances. With AI demand expected to remain high beyond 2028, strengthening the ABF substrate supply chain will continue to be a critical factor shaping the semiconductor industry's evolution for years to come.

Source: <https://www.digitimes.com/news/a20260714PD214/demand-abf-substrate-2028-market-chip-supply.html>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#05 Amkor Technology Expands Arizona Campus with 67-Acre Acquisition, Bolstering U.S. Advanced Packaging OSAT Capacity

Published Date unknown AllMind AI News USA



OVERVIEW

Amkor Technology has acquired an additional 67 acres in Arizona to significantly expand its U.S. advanced semiconductor packaging and test capacity. This expansion, supported by up to \$407 million in CHIPS Act funding, aims to meet surging demand from AI, HPC, automotive, and communications markets. The new facility will be the first high-volume advanced packaging OSAT in the U.S., strengthening domestic semiconductor manufacturing.

Key Findings

Amkor Technology has announced a significant expansion of its advanced semiconductor packaging and test capabilities in the United States, acquiring an additional 67-acre parcel adjacent to its existing Peoria campus in Arizona. This strategic move is specifically designed to address the escalating demand from critical markets such as AI, High-Performance Computing (HPC), automotive, and communications. The project is bolstered by up to \$407 million in federal funding under the CHIPS Act and is poised to establish the U.S.'s first high-volume advanced packaging Outsourced Semiconductor Assembly and Test (OSAT) facility, marking a crucial step in fortifying the domestic semiconductor manufacturing base.

Technical and Clinical Details

Amkor's substantial expansion focuses on state-of-the-art packaging technologies essential for integrating complex chips required by AI and HPC applications. This specifically includes enhancing capabilities for chiplet integration, High Bandwidth Memory (HBM) stacking, and heterogeneous integration. The new facility is expected to provide advanced packaging and test services, including for CoWoS (Chip-on-Wafer-on-Substrate) technologies, supported by a 10-year agreement with TSMC. This development is paramount for the U.S. to close gaps in its semiconductor manufacturing capacity, particularly in strengthening the industrial base for defense electronics. The investment goes beyond mere capacity expansion, aiming to deliver higher-performance and more reliable semiconductor solutions through advancements in process technology and quality control.

Background and Industry Context

In recent years, rising geopolitical risks and concerns over supply chain vulnerabilities have prompted nations to prioritize semiconductor manufacturing repatriation and domestic capacity enhancement. In the U.S., the CHIPS Act was enacted to allocate significant funding for domestic semiconductor research, development, manufacturing, and workforce development. Amkor's Arizona expansion aligns perfectly with this national strategy. Packaging, once considered a 'back-end' process, is now recognized as a 'critical' element for maximizing AI chip performance and enhancing overall system efficiency. This paradigm shift in perception is accelerating investments in OSAT companies like Amkor.

Strategic Significance and Outlook

The expansion of Amkor's Arizona facility will significantly bolster advanced packaging capabilities within the U.S. semiconductor supply chain, making a vital contribution to the nation's high-tech industries. This facility will serve as a foundational pillar for future innovations in AI, HPC, autonomous driving technologies, and more, proving indispensable for maintaining U.S. technological leadership. Furthermore, this investment sends a strong signal to other semiconductor companies and related industries, encouraging further domestic investment. CEO Kevin Engel emphasized that this represents a significant stride toward building indigenous advanced semiconductor manufacturing capacity, underscoring its profound long-term strategic importance.

Source:

<https://allmind.ai/news/1c98de754956f2b91b3767a3151875b7ba78c5246364e44142ca7f571a496f13>

#06 Samsung Develops '2.xD' Advanced Packaging Integrating HBM, Logic, and SiPh to Tackle AI Data Center Power and Data Bottlenecks

Published July 13, 2026 DigiTimes Taiwan



OVERVIEW

Samsung Electronics is developing '2.xD' advanced packaging technology that integrates HBM, logic chips, and silicon photonics (SiPh) into a single package. This innovation aims to resolve critical power consumption and data transfer bottlenecks in AI data centers. The technology leverages panel-based redistribution layer (RDL) interposers and evolving bonding techniques from micro bumps to bumpless hybrid bonding.

Key Findings

Samsung Electronics is developing a groundbreaking '2.xD' advanced packaging technology that integrates high-bandwidth memory (HBM), logic chips, and silicon photonics (SiPh) into a single, cohesive package. This innovative solution is specifically designed to address the escalating power consumption and data transfer bottlenecks prevalent in modern AI data centers, promising a significant leap in AI system efficiency and performance.

Technical and Clinical Details

The '2.xD' packaging leverages panel-based redistribution layer (RDL) interposers as its core, substantially enhancing wiring density and data transfer efficiency between HBM, logic, and SiPh chips. The bonding technology is also evolving from traditional micro bumps to bumpless hybrid bonding, enabling finer and more robust connections. Specifically, this technology aims to maximize inter-chip data transfer speeds and minimize power consumption for AI accelerators and server CPUs that demand extremely high bandwidth and low latency. Introduced at the Nano Korea 2026 forum, the successful implementation of this technology necessitates overcoming advanced manufacturing challenges such as fine particle control and substrate warpage, areas where Samsung is actively focusing its R&D efforts.

Background and Industry Context

The increasing complexity of AI models and the explosive growth in data volume have led to significant challenges in semiconductor chip performance limits and power consumption within data centers. Conventional packaging technologies often result in longer data transmission distances between chips, leading to unavoidable signal delays and power loss. Consequently, there is a surging demand for advanced packaging solutions that can physically bring together and more efficiently integrate chips with disparate functionalities, such as HBM, logic, and optical communication devices. Samsung benefits from a unique 'triple-play' portfolio comprising memory, foundry (logic), and silicon photonics, which allows for internal co-design and optimization of these diverse components.

Strategic Significance and Outlook

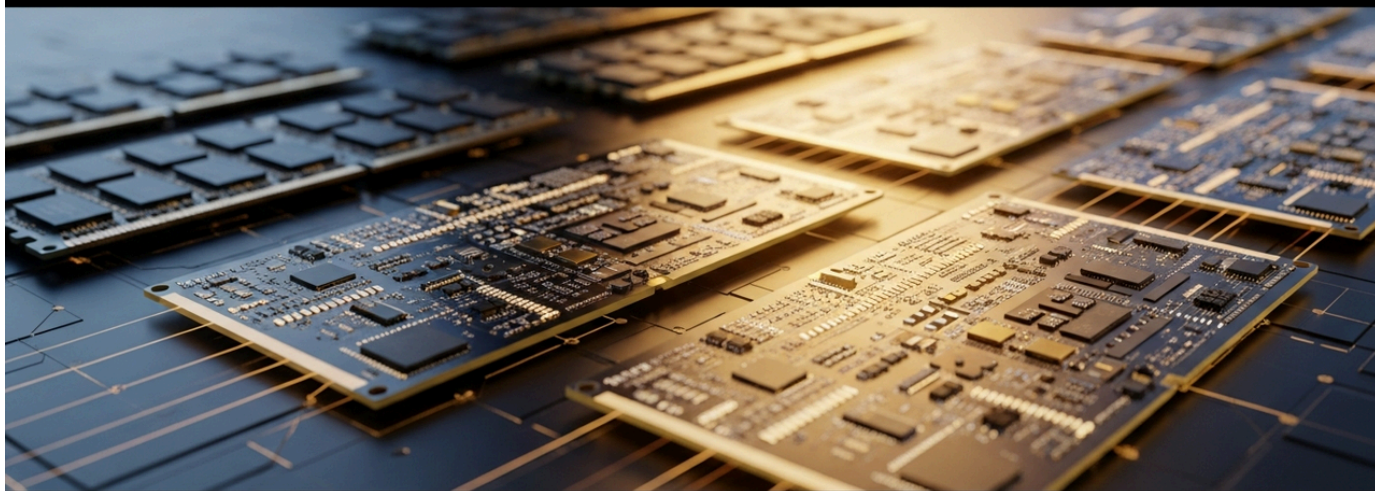
Samsung's '2.xD' packaging technology is poised to profoundly impact the design of next-generation AI computing infrastructure. By directly integrating HBM and logic chips with silicon photonics for optical data transmission, it becomes possible to create ultra-high-speed, low-power systems that transcend the limitations of electrical signals. This directly translates into reduced power consumption and a substantial increase in computational power for AI data centers, serving as a key accelerator for future AI advancements. Through this technology, Samsung aims to establish leadership in the AI packaging market, directly competing with co-packaged optics (CPO) technologies being jointly developed by NVIDIA and Broadcom with TSMC.

Source: <https://www.digitimes.com/news/a20260713VL223/samsung-hbm-optics-siph-packaging-chips.html>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#07 ABF Substrates Emerge as the True Bottleneck in the AI Era, More Critical Than DRAM for High-Performance Computing

Published July 11, 2026 Industry Analysis International



OVERVIEW

ABF (Ajinomoto Build-up Film) substrates, not DRAM, are becoming the more critical bottleneck in the AI supply chain. Leading manufacturers like Ibiden and Unimicron are poised to benefit directly from the surge in server and AI accelerator packaging demand. The increasing complexity of AI chips necessitates more layers, finer wiring, and tighter tolerances in substrates, exacerbating manufacturing difficulty and overall supply constraints.

Key Findings

While attention often focuses on DRAM shortages in the AI semiconductor supply chain, ABF (Ajinomoto Build-up Film) substrates are emerging as a more profound and challenging bottleneck. These substrates are indispensable for packaging high-performance AI accelerators and servers, with their supply constraints becoming a primary factor delaying AI chip market entry.

Technical and Clinical Details

ABF substrates are crucial interconnect materials for packaging high-performance semiconductors such as CPUs, GPUs, and ASICs (Application-Specific Integrated Circuits). As AI chips evolve, the need to integrate more chiplets and HBM (High Bandwidth Memory) demands ABF substrates with a greater number of layers, finer wiring, and tighter tolerances. This escalating technical requirement makes ABF substrate manufacturing highly complex and capital-intensive, hindering rapid production capacity expansion. Japan's Ibiden and Taiwan's Unimicron are prominent ABF substrate manufacturers directly exposed to the rising demand for AI server and accelerator packaging, elevating their strategic value. Furthermore, AT&S, with its dual strength in ABF substrates and high-end PCBs (Printed Circuit Boards), is gaining attention as an investment vehicle for the AI theme.

Background and Industry Context

The explosive growth of AI applications demands a dramatic leap in data processing capabilities, prompting a shift in semiconductor chip design from traditional monolithic structures to advanced packaging techniques like chiplets and heterogeneous integration. In these new architectures, where multiple functional chips are integrated within a single package, ABF substrates become critically important for inter-chip signal transmission. However, ABF substrate manufacturing requires specialized materials (Ajinomoto Build-up Film) and sophisticated production processes, creating high barriers to entry and leading to market dominance by a few key players. This dynamic has resulted in supply failing to keep pace with surging demand, clearly highlighting ABF substrates as a bottleneck for the entire AI supply chain.

Strategic Significance and Outlook

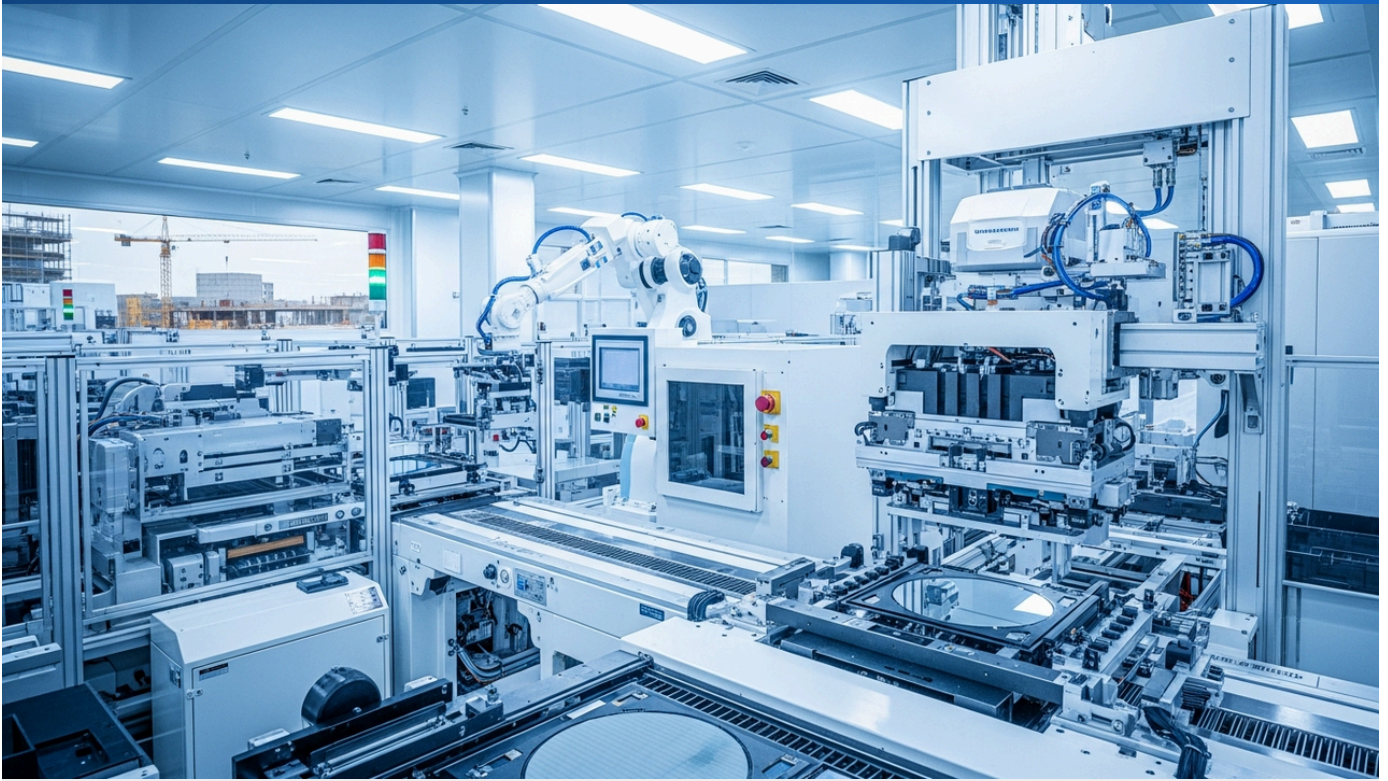
The ABF substrate shortage is projected to persist until 2028, significantly impacting AI chip supply plans. While substrate manufacturers benefit from strong pricing power, they are simultaneously compelled to undertake massive capital investments to meet customer demands for increased production. This situation underscores the growing importance of long-term strategic partnerships between semiconductor manufacturers and ABF substrate suppliers. For investors, beyond DRAM and GPU manufacturers, ABF substrate suppliers such as Ibiden, Unimicron, and AT&S may represent the hidden 'golden stocks' poised to truly benefit from the AI boom. Technological innovation and capacity expansion in ABF substrates will be key determinants of the AI industry's growth trajectory going forward.

Source: <https://denisdoroshenko.substack.com/p/forget-dram-the-real-ai-shortage>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#08 Wah Lee and Asahi Kasei Double Photoresist Capacity in Tainan to Capitalize on AI Advanced Packaging Boom and ABF Substrate Demand

Published July 15, 2026 BigGo Finance International



OVERVIEW

Wah Lee and Asahi Kasei are doubling high-resolution dry film photoresist capacity in Tainan to meet surging ABF substrate demand driven by AI, HPC, and advanced packaging. With the ABF substrate shortage projected to persist through 2028, this expansion aims to build a more resilient global semiconductor materials supply chain. Wah Lee's photoresist is already utilized by major Taiwanese ABF substrate manufacturers, achieving high double-digit revenue growth.

Key Findings

Taiwanese company Wah Lee and Japan's Asahi Kasei have announced a significant increase in their high-resolution dry film photoresist production capacity in Tainan, doubling it to address the surging demand for ABF (Ajinomoto Build-up Film) substrates. This demand is primarily fueled by the rapid advancements in AI, High-Performance Computing (HPC), and advanced packaging technologies. The expansion is a strategic response to the projected ABF substrate shortage, expected to last until 2028, aiming to fortify the global semiconductor materials supply chain.

Technical and Clinical Details

Photoresist is an indispensable photosensitive material used in semiconductor manufacturing and packaging processes to transfer circuit patterns onto substrates. High-resolution dry film photoresist is particularly crucial for forming the intricate circuits on ABF substrates, and its quality and stable supply are paramount for achieving the high-density, multi-layered packaging required by AI chips. Wah Lee's photoresist products are already widely adopted by major Taiwanese ABF substrate manufacturers such as Unimicron, Nan Ya PCB, and Kinsus, with related business revenues recording high double-digit growth. This doubling of production capacity is a strategic move to meet market expectations and prepare for future demand expansion. Specifically, it involves expanding and optimizing production lines to significantly increase supply, helping alleviate production bottlenecks for substrate manufacturers.

Background and Industry Context

The performance enhancement of AI chips heavily relies on advanced packaging techniques like chiplet technology and 3D stacking, which are closely linked to the evolution of ABF substrates. ABF substrates are key materials for forming the complex circuits of high-performance AI chips, but their manufacturing requires advanced technology, specialized materials, and long lead times, always posing a risk of supply shortages. As Ajinomoto supplies over 95% of the global ABF film market, this market is dependent on a few specialized companies, leading to a severe shortage of materials across the supply chain. The collaboration and investment by Wah Lee and Asahi Kasei are crucial efforts to address this bottleneck and contribute to the stabilization of the entire semiconductor ecosystem.

Strategic Significance and Outlook

The doubling of high-resolution dry film photoresist production capacity will directly contribute to alleviating the ABF substrate shortage and, by extension, support the expansion of AI chip production. This will accelerate the development of various fields requiring high-performance semiconductors, including AI, HPC, and autonomous driving technologies. Strengthening the supply chain reduces the risk of concentration in a single market and fosters stable growth for the global semiconductor industry. Going forward, strategic investments in substrate materials and specialty chemical suppliers will continue to be indispensable factors in supporting semiconductor manufacturing in the AI era.

Source: <https://finance.biggo.com/news/b932f968-9a1d-46c6-b2d3-6698bfb48dad>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#09 Morgan Stanley Forecasts 93% CoWoS Demand Surge by 2027, Driven by AMD's Venice CPU Shipments

Published July 09, 2026 KuCoin International



OVERVIEW

Morgan Stanley forecasts global CoWoS (Chip-on-Wafer-on-Substrate) demand to nearly double to 2.694 million wafers in 2027, a 93% increase from 1.394 million in 2026. This growth is predominantly driven by AMD's Venice CPU shipments, with AMD's CoWoS demand projected for a staggering 308% growth rate. This signifies CoWoS applications are expanding beyond AI accelerators to server CPUs, making advanced packaging capacity a crucial competitive factor.

Key Findings

A recent research report by Morgan Stanley predicts a dramatic increase in global CoWoS (Chip-on-Wafer-on-Substrate) demand, projecting a nearly 93% growth by 2027 compared to 2026. Specifically, demand is expected to reach 2.694 million wafers in 2027, with AMD's Venice CPU shipments identified as the primary catalyst for this surge.

Technical and Clinical Details

CoWoS is an advanced 2.5D/3D packaging technology designed to integrate GPUs, HBM (High Bandwidth Memory), and chiplets. This technology is critical for achieving high bandwidth and low latency, essential for enhancing the performance of AI accelerators and High-Performance Computing (HPC) applications. While NVIDIA remains the largest consumer of CoWoS, Morgan Stanley's report highlights AMD's emergence with an impressive 308% growth rate, driven largely by its Venice CPU shipments. This indicates that high-performance server CPUs are leveraging CoWoS to directly handle AI workloads, expanding CoWoS technology's application beyond dedicated AI accelerators into broader data center infrastructure.

Background and Industry Context

The evolution of AI and data science demands unprecedented computational power and data processing speeds, dramatically elevating the importance of semiconductor packaging technologies. Traditional 2D packaging faced challenges like longer data transmission distances, signal delays, and increased power consumption between chips. CoWoS overcomes these limitations by horizontally connecting multiple chips via a silicon interposer and vertically stacking HBM. However, CoWoS manufacturing requires sophisticated technology and substantial capital investment, making its supply capacity a bottleneck that restricts the overall supply of AI chips. Against this backdrop, foundries and OSAT (Outsourced Semiconductor Assembly and Test) providers are intensely focused on expanding CoWoS capacity, making its availability a decisive competitive factor among semiconductor manufacturers.

Strategic Significance and Outlook

The rapid expansion of CoWoS demand will further accelerate capital investment across the semiconductor industry, particularly in advanced packaging. AMD's increased adoption of CoWoS in the server CPU market creates a new, significant demand source alongside NVIDIA, fostering market diversification. This intensification of competition for CoWoS supply will compel TSMC and its OSAT partners to further boost production and innovation. In the coming years, securing CoWoS capacity will be a critical metric determining success for companies in the AI chip market, significantly impacting the entire infrastructure supporting AI's evolution.

Source: <https://www.kucoin.com/news/flash/morgan-stanley-report-cowos-demand-to-double-by-2027-amd-and-asics-drive-ai-chip-growth>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#10 Applied Materials' Material Engineering Innovations, Led by Hybrid Bonding, Key to Scaling AI Chip Performance in the AI Era

Published July 12, 2026 Applied Materials (Official Blog/Article) USA



OVERVIEW

Applied Materials emphasizes that material engineering innovations, including its Kinex hybrid bonding system, are critical for scaling AI chip performance. The company is advancing packaging technologies that integrate multiple chiplets for higher bandwidth and energy efficiency. Breakthroughs in materials engineering, such as the Xtera epitaxy system for 2nm and beyond GAA transistors, are crucial across five key AI system architecture areas: logic, DRAM, HBM, advanced packaging, and power electronics.

Key Findings

Applied Materials underscores the paramount importance of material engineering innovations, including its 'Kinex' hybrid bonding system, for achieving exponential leaps in chip performance within the Artificial Intelligence (AI) era. The company views advanced packaging technologies that efficiently integrate multiple chiplets, delivering higher bandwidth and superior energy efficiency, as foundational to next-generation AI infrastructure.

Technical and Clinical Details

Applied Materials identifies five core areas defining AI system architecture: 1. Leading-edge logic, 2. High-performance DRAM, 3. HBM (High Bandwidth Memory), 4. Advanced packaging, and 5. Power electronics. Breakthroughs in materials engineering are indispensable across all these domains. For instance, to support the scaling of Gate-All-Around (GAA) transistors at 2nm and beyond, innovative thin-film technologies, such as Applied Materials' 'Xtera' epitaxy system, are crucial. Hybrid bonding technology, by directly and electrically connecting different chiplets, achieves significantly higher interconnection density and shorter wiring distances compared to conventional microbumps, dramatically improving data transfer speeds and energy efficiency. Precise thin-film deposition, patterning, and inspection techniques are essential to ensure the manufacturing yield and reliability of these advanced structures.

Background and Industry Context

The increasing complexity of AI models and the explosion in data volume demand unprecedented computational power and efficiency from semiconductor chips. Traditional chip design struggles to meet these requirements, leading to a prevalent shift towards 'heterogeneous integration' via chiplets and advanced packaging technologies. In this new architectural paradigm, not only the miniaturization of individual chips but also how efficiently and power-consciously they are interconnected has become a new differentiator for AI chip performance. Applied Materials, leveraging its expertise in materials science and process technology, is at the forefront of providing equipment and solutions to address this evolving landscape in semiconductor manufacturing.

Strategic Significance and Outlook

The material engineering and advanced packaging innovations championed by Applied Materials are pivotal for scaling AI chip performance. The widespread adoption of hybrid bonding technology is set to revolutionize the design and manufacturing of AI accelerators, HPC, and future physical AI (edge AI) devices. The company's solutions pave the way for semiconductor manufacturers to implement GAA transistors at 2nm and beyond process nodes and mass-produce increasingly complex 3D packaging structures. This will accelerate the further evolution and adoption of AI technologies, leading to substantial economic and social impacts across a wide range of industries.

Source: <https://www.appliedmaterials.com/jp/ja/the-ai-era.html>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#11 TSMC Plans Three Advanced Packaging Plants at Chiayi Science Park, Targeting Mass Production by 2027 for AI and Quantum Tech

Published July 14, 2026 Taiwan News Taiwan



OVERVIEW

TSMC plans three advanced packaging plants at Taiwan's Chiayi Science Park, with two slated for mass production by 2027. These facilities will focus on AI, heterogeneous integration, and quantum technology, leveraging TSMC's CoWoS. The company is also developing next-generation packaging like CoPoS and glass-core substrates, validating processes and materials for large-sized substrates. This strategy addresses soaring AI demand and strengthens TSMC's packaging leadership.

Key Findings

TSMC is progressing with a massive plan to construct three advanced packaging plants in Taiwan's Chiayi Science Park, with two of these facilities slated to commence mass production by 2027. These new sites will specialize in cutting-edge fields such as Artificial Intelligence (AI) chips, heterogeneous integration packaging, and quantum technology, further solidifying TSMC's flagship CoWoS (Chip-on-Wafer-on-Substrate) technology.

Technical and Clinical Details

The two plants in the first phase of Chiayi Science Park are targeted for mass production starting in 2027, offering complex chip integration solutions essential for AI accelerators and High-Performance Computing (HPC). While CoWoS remains central, TSMC is also actively developing next-generation packaging technologies, including 'CoPoS (Chip-on-Package-on-Substrate)' and 'glass-core substrates.' Glass-core substrates are expected to offer superior mechanical stability, thermal properties, and finer wiring capabilities compared to traditional organic substrates, significantly contributing to chip warpage reduction and improved power integrity. The current development phase focuses heavily on validating processes, material characteristics, and flatness for these large-sized substrates. These technologies are crucial for enabling future AI chip performance enhancements and miniaturization.

Background and Industry Context

The explosive demand for AI has pushed requirements for semiconductor chip computational power and data bandwidth to unprecedented levels. To meet this, beyond single-chip miniaturization, advanced packaging technologies that efficiently integrate multiple chiplets have become the new frontier in semiconductor manufacturing. TSMC has long played a leading role in this area, but the surge in AI demand has caused a severe shortage in CoWoS capacity. The investment in Chiayi Science Park is a strategic move to alleviate this bottleneck and support the production of next-generation AI chips for key customers like NVIDIA and AMD. Furthermore, adopting innovative materials such as glass-core substrates is vital for the further evolution of packaging technology and establishing TSMC's technological advantage over competitors.

Strategic Significance and Outlook

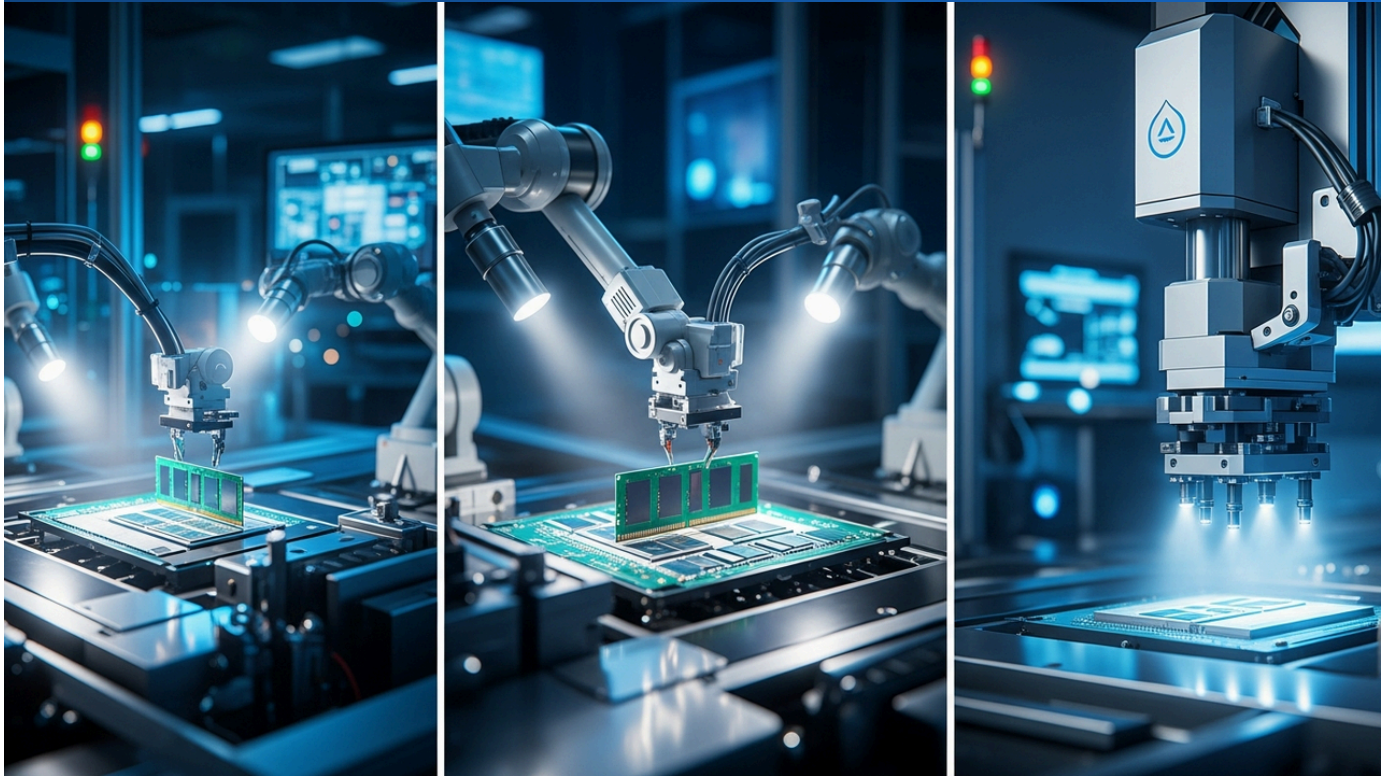
The advanced packaging plants in Chiayi Science Park will solidify TSMC's position within the AI chip ecosystem. Mass production starting in 2027 will contribute to stabilizing the supply of AI accelerators, fostering further advancements in AI technology. The development of CoPoS and glass-core substrate technologies lays the groundwork for meeting the demands of future AI and quantum computing. These investments are also crucial for Taiwan to maintain its status as a global semiconductor hub, further strengthening TSMC's strategic advantage in the global high-tech competition. Advanced packaging will continue to be an indispensable element for maximizing AI chip performance and efficiency going forward.

Source: <https://www.taiwannews.com.tw/en/news/6400586>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#12 AI Era Semiconductor Equipment Theme: Applied Materials Forecasts Over 50% Advanced Packaging Revenue Growth in 2026, Micron Boosts HBM Packaging Capabilities

Published July 16, 2026 TradingKey International



OVERVIEW

As AI chip evolution heavily relies on chiplets and advanced packaging beyond transistor shrinkage, Applied Materials anticipates over 50% growth in its advanced packaging revenue in 2026, while KLA expects its advanced packaging portfolio to reach approximately \$1 billion. Micron announced its U.S. investment plan includes end-to-end HBM packaging capability, covering bonding, wafer thinning, inspection, and materials handling. This indicates the AI boom is accelerating investment in the semiconductor equipment market, particularly for back-end processing.

Key Findings

The evolution of AI chips is increasingly dependent on chiplet architectures and advanced packaging technologies, rather than solely transistor miniaturization, establishing a new growth driver for the semiconductor manufacturing equipment market. Applied Materials forecasts its revenue from advanced packaging to increase by over 50% in 2026, while KLA expects its advanced packaging portfolio to generate approximately \$1 billion in revenue for the same year. Micron has announced plans to build end-to-end HBM (High Bandwidth Memory) packaging capabilities as part of its U.S. investment strategy.

Technical and Clinical Details

As AI chip designs become progressively complex, advanced packaging techniques, which integrate multiple functional blocks (chiplets) with high density within a single package, are becoming indispensable. This necessitates precise materials engineering and numerous processing steps, making equipment from providers like Applied Materials—covering etching, deposition, planarization, and inspection—extremely critical. Micron's initiative to build end-to-end HBM packaging capability specifically involves integrating wafer bonding for HBM stack formation, wafer thinning for thermal management, advanced inspection for quality assurance, and precise material handling technologies. This comprehensive approach is expected to enhance HBM production yield and reliability, thereby maximizing the overall performance and efficiency of AI chips. KLA's portfolio focuses on defect detection and metrology within the packaging process, contributing to manufacturing optimization.

Background and Industry Context

The explosive growth of AI has dramatically increased demand for computational power and bandwidth in data centers, exposing the limitations of traditional 2D chip designs. Technologies like HBM and chiplets were developed to overcome these challenges, and advanced packaging is key to their realization. Historically, semiconductor equipment investment focused primarily on front-end miniaturization. However, in the AI era, the importance of back-end packaging, testing, and material processing has risen to an equivalent, if not greater, level. The revenue forecasts from Applied Materials and KLA clearly reflect this market shift, indicating that semiconductor equipment manufacturers are becoming significant beneficiaries of the AI boom.

Strategic Significance and Outlook

The trend of AI chip performance evolution being deeply dependent on advanced packaging and materials engineering will persist. Equipment suppliers like Applied Materials and KLA are expected to capitalize on this structural change for long-term growth opportunities. Micron's substantial investment in HBM packaging illustrates a strategy for memory manufacturers to capture AI-driven HBM demand and strengthen vertically integrated manufacturing capabilities. These developments signify an accelerating focus on back-end technologies within the overall semiconductor industry supply chain, serving as a powerful impetus for AI infrastructure development. Technological innovation and capital investment in this sector will be key to unlocking the potential of next-generation AI.

Source: <https://www.tradingkey.com/analysis/stocks/us-stocks/262033406-semiconductor-equipment-stocks-ai-capex-hbm-tradingkey>

#13 Applied Materials Highlights MES's Critical Role in Recovering Capacity and Managing Complexity for Advanced Packaging and Test Facilities

Published July 17, 2026 Applied SmartFactory Solutions (Applied Materials) USA



OVERVIEW

Applied Materials emphasizes the crucial role of Manufacturing Execution Systems (MES) in advanced packaging and test (ATP) facilities for capacity recovery, loss reduction, and complexity management. Modern ATP facilities, handling heterogeneous substrates, HBM, and chiplet designs, require front-end discipline like detailed traceability, automated process control, and real-time exception management. MES is essential to mitigate up to 10-20% capacity loss from manual handling and errors.

Key Findings

Applied Materials highlights that Manufacturing Execution Systems (MES) play an indispensable role in capacity recovery, reducing production losses, and managing complexity for advanced packaging and test (ATP) facilities. It is estimated that MES implementation can significantly cut capacity losses, which can otherwise reach 10-20% due to manual operations and errors in ATP facilities.

Technical and Clinical Details

Unlike traditional 'back-end' operations, modern ATP facilities deal with cutting-edge technologies such as heterogeneous substrates, High Bandwidth Memory (HBM), and chiplet-based designs. These complex processes demand rigorous discipline akin to front-end semiconductor manufacturing. Specifically, MES provides functionalities like: detailed traceability to accurately track the manufacturing history and material sources of each chiplet and package, ensuring stringent quality control. Automated process control to guarantee optimization and consistency of manufacturing parameters. Real-time exception management capabilities to enable swift responses during anomalies, minimizing potential losses. This significantly enhances operational efficiency and yield in advanced packaging environments where a diverse range of high-value products are processed simultaneously.

Background and Industry Context

The surging demand for AI, High-Performance Computing (HPC), and data centers has driven semiconductor chips to evolve towards 'heterogeneous integration,' combining multiple disparate chiplets. This advanced packaging is key to enhancing performance and reducing power consumption, but its manufacturing process is extremely complex and presents significant technical challenges. Integrating chips produced through different processes, fine interconnections, and thermal management have been particularly difficult for traditional manufacturing systems. Manual data entry and process adjustments increase the risk of errors, leading to the loss of valuable production capacity. To address these challenges, Applied Materials provides MES solutions specifically tailored for the AI era, supporting intelligent automation and optimization of ATP facilities.

Strategic Significance and Outlook

The advanced implementation of Manufacturing Execution Systems (MES) is vital for dramatically improving the efficiency and productivity of advanced packaging and test facilities. As demand for AI chips continues to expand, ATP facilities must cope with increasingly complex designs and higher production volumes. MES will drive the digitalization and automation of manufacturing processes, minimizing human errors and contributing to the stable supply of high-quality AI chips. Applied Materials' solutions enhance overall supply chain resilience while providing a foundation for semiconductor manufacturers to maintain competitiveness and accelerate next-generation AI innovations. In the future, MES is expected to further increase its importance as a core technology for realizing 'smart factories' in semiconductor back-end processes.

Source: <https://appliedsmartfactory.com/semiconductor-blog/manufacturing-execution/how-advanced-packaging-mes-helps-atp-facilities-recover-capacity/>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#14 Rapidus to Establish 2nm AI Chip Mass Production by 2027, Bolstering Japan's Semiconductor Ecosystem

Published July 14, 2026 DataM Intelligence International



OVERVIEW

Japan's Rapidus, backed by government and private funding, aims to establish domestic 2nm advanced semiconductor manufacturing and mass produce AI chips by 2027. This initiative will stimulate demand across lithography, deposition, etch, cleaning, inspection, materials, and advanced packaging equipment. Applied Materials also introduced new systems in June 2026 for AI chip DRAM and packaging, enhancing thinning, bonding, interconnect, planarization, and inspection technologies for HBM and 3D architectures.

Key Findings

Japan's Rapidus, with substantial financial backing from both government and private sectors, is driving a national project to establish domestic advanced semiconductor manufacturing using the 2nm (nanometer) process. The company aims to commence mass production of Artificial Intelligence (AI) chips by 2027, an endeavor expected to stimulate significant demand for manufacturing equipment and materials across Japan's entire semiconductor industry ecosystem.

Technical and Clinical Details

Rapidus' 2nm plan necessitates the integration of cutting-edge front-end processes such as Extreme Ultraviolet (EUV) lithography, Atomic Layer Deposition (ALD), high-precision etching, advanced cleaning, and stringent inspection technologies, alongside advanced packaging. AI chips are increasingly adopting 'chiplet architectures' to achieve high performance by combining multiple smaller functional units. This approach requires wafer thinning, hybrid bonding, high-density interconnections, precise planarization, and comprehensive inspection. Applied Materials, in June 2026, unveiled new semiconductor manufacturing systems designed for AI chip DRAM and advanced packaging. These systems specialize in the production of HBM (High Bandwidth Memory) and complex 3D architectures, aiming to resolve technical challenges in back-end processes such as wafer thinning, chip bonding, fine interconnection formation, chemical mechanical planarization (CMP), and advanced defect inspection.

Background and Industry Context

In response to escalating geopolitical risks and global calls for more resilient semiconductor supply chains, nations are focusing on strengthening their domestic semiconductor manufacturing capabilities. Japan, aiming to regain its past prominence in the semiconductor industry, is pursuing a national strategy centered around Rapidus. Amidst the explosive growth in AI chip demand, cutting-edge technologies like the 2nm process are critically important for ensuring national economic security and technological superiority. Furthermore, AI chip performance improvements are increasingly dependent not only on front-end miniaturization but also on back-end advanced packaging, prompting equipment manufacturers like Applied Materials to accelerate product development in response to this market shift.

Strategic Significance and Outlook

Rapidus' 2nm process development and mass production target are expected to revitalize Japan's semiconductor industry and enhance its presence in the global supply chain. Collaboration with IBM on advanced packaging technology will further strengthen its competitiveness. This initiative is also anticipated to generate significant ripple effects across Japan's semiconductor materials and equipment industries, leading to accelerated R&D investments and new job creation. Coupled with technological innovations from global equipment manufacturers like Applied Materials, AI-era semiconductor manufacturing will evolve into an even more complex and integrated process. Rapidus' success is thus deemed to hold strategic significance in contributing to the establishment of a resilient Indo-Pacific semiconductor ecosystem.

Source: <https://www.datamintelligence.com/blogs/semiconductor-manufacturing-equipment-ai-usa-japan>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#15 HBM Supply Crunch Deepens: DRAM Wafer Production and Advanced Packaging/Test Emerge as Dual Bottlenecks Amid Samsung, SK Hynix, Micron Rivalry

Published July 15, 2026 Industry Analysis International



OVERVIEW

High Bandwidth Memory (HBM), central to AI, faces dual bottlenecks in both DRAM wafer manufacturing and advanced packaging/test capacity. HBM achieves high bandwidth and energy efficiency through 3D stacking, TSVs, microbumps, and advanced packaging, but the complexity of these processes constrains supply. Samsung is actively developing HBM4, projecting significant sales growth in 2026, and focusing on customer qualification and yield recovery amidst fierce competition with SK Hynix and Micron.

Key Findings

High Bandwidth Memory (HBM), a core component in Artificial Intelligence (AI) technology, is facing severe supply bottlenecks not only in DRAM wafer production but also in subsequent advanced packaging and testing capabilities. This dual constraint is the primary factor preventing the industry from meeting the surging HBM demand in the AI era.

Technical and Clinical Details

HBM employs 3D stacking technology, where multiple DRAM dies are vertically stacked and interconnected through Through-Silicon Vias (TSVs). This architecture enables significantly wider data bus widths and shorter signal paths, delivering dramatically higher bandwidth and superior energy efficiency compared to conventional DRAM solutions. The process necessitates wafer thinning, TSV formation, microbump bonding, and advanced packaging techniques like CoWoS (Chip-on-Wafer-on-Substrate). Each of these steps is highly complex and demands extreme precision, making yield assurance challenging and production costs high. Samsung is actively developing HBM4, the next generation of HBM, and anticipates a substantial increase in HBM-related sales in 2026. The company is focused on accelerating customer qualification and improving yield recovery, engaging in fierce competition with key rivals like SK Hynix and Micron for leadership in the AI memory market.

Background and Industry Context

The increasing scale of AI models and the explosive growth in data processing volumes demand unprecedented bandwidth and capacity from the memory integrated into AI chips, requirements that conventional Double Data Rate (DDR) memory cannot satisfy. HBM was developed to meet these demands and is widely adopted in NVIDIA's GPUs and AMD's AI accelerators. However, HBM manufacturing processes are far more complex than traditional memory production. Specifically, advanced packaging steps such as TSV formation and microbump bonding require specialized expertise, dedicated equipment, and long lead times. Consequently, while DRAM manufacturers continue to invest heavily to boost HBM production, packaging capacity constraints remain a primary factor limiting overall supply.

Strategic Significance and Outlook

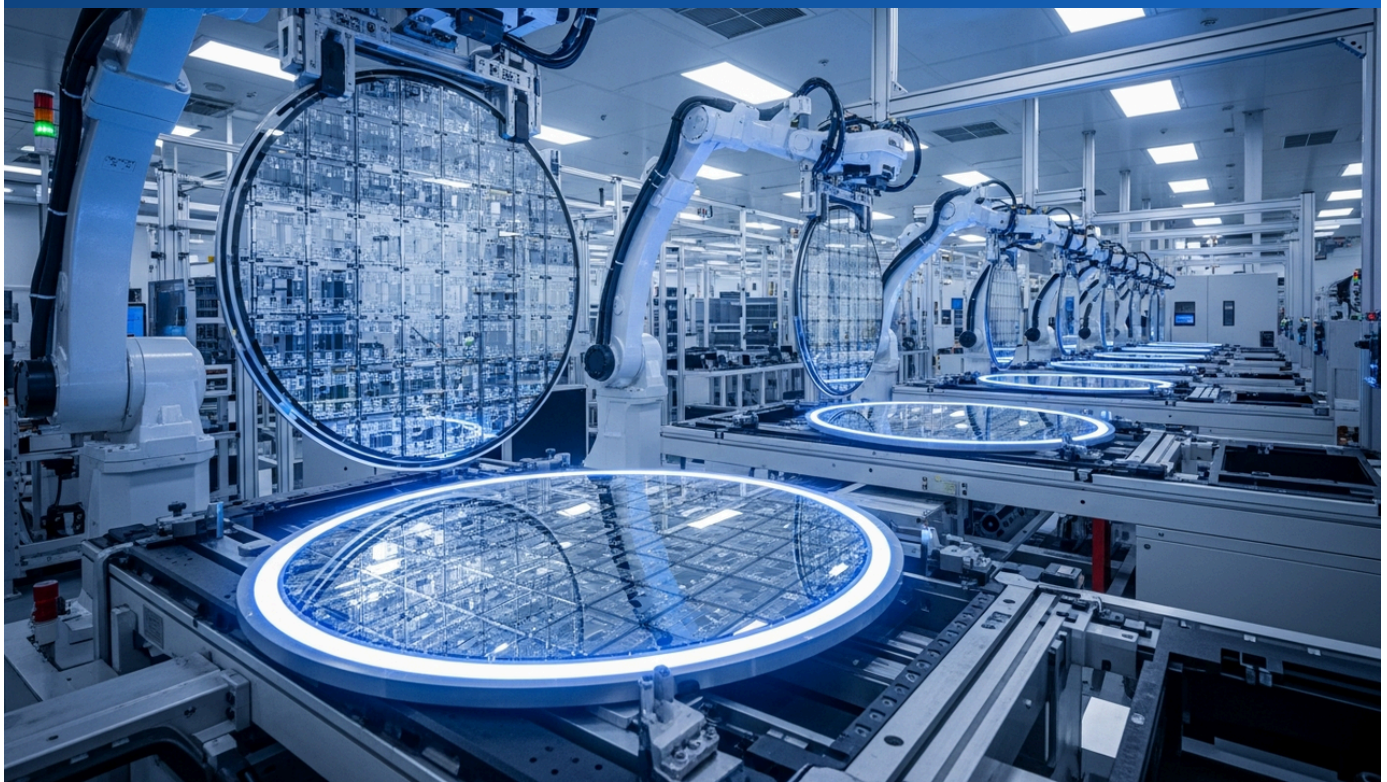
The HBM supply bottleneck will continue to significantly impact the pace of AI chip market entry and AI infrastructure expansion for several years. Major HBM suppliers—Samsung, SK Hynix, and Micron—must accelerate technological innovation and capacity expansion to overcome these constraints. Particularly, rapid customer qualification and stable yield are decisive factors for gaining market share. AI chip manufacturers must forge robust partnerships with HBM suppliers to ensure a stable supply. The evolution of HBM technology and the expansion of its supply capacity will be a critical key to driving the performance improvement and widespread adoption of next-generation AI computing.

Source: <https://www.biyapay.com/en/blogdetail/4403-what-are-hbm-concept-stocks-samsung-sk-hynix-micro>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#16 TSMC's CoWoS Supply to Reach At Least 200K Wafers Monthly by 2027, Accelerating Expansion to Meet Soaring AI Demand

Published July 10, 2026 DigiTimes Taiwan



OVERVIEW

TSMC is accelerating its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity expansion to meet robust AI chip demand, with market indications suggesting monthly output will reach at least 200,000 wafers by 2027. Equipment makers are awaiting TSMC's final order allocation, and current lead times of 7-9 months suggest continued constraints before new capacity comes fully online. This expansion is critical for alleviating AI accelerator supply bottlenecks.

Key Findings

TSMC is rapidly accelerating the expansion of its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity to meet the explosive demand for AI chips. Market forecasts indicate that TSMC's monthly CoWoS output is expected to reach at least 200,000 wafers by 2027, marking a crucial step towards alleviating the supply bottleneck for AI accelerators.

Technical and Clinical Details

CoWoS is a 2.5D/3D packaging technology that integrates multiple chiplets (such as GPUs and HBM) onto a silicon interposer, maximizing AI chip performance by achieving high bandwidth and low power consumption. TSMC's CoWoS capacity has been the biggest bottleneck influencing the product shipments of major AI chip vendors like Nvidia and AMD, making its expansion an urgent priority for the entire industry. Currently, lead times for the specialized semiconductor manufacturing equipment required for CoWoS production are lengthy, ranging from 7 to 9 months, which prolongs the period until new production capacity becomes available. Equipment manufacturers are awaiting final order allocations from TSMC, which is collaborating with OSAT (Outsourced Semiconductor Assembly and Test) partners like Amkor to expand capacity in addition to its in-house efforts.

Background and Industry Context

The increasing complexity of AI models and the explosive growth in data volume demand unprecedented computational power and data processing speeds from AI chips. As the limitations of traditional 2D chip designs become apparent, advanced packaging technologies like CoWoS have become a primary means to achieve performance improvements beyond Moore's Law. However, CoWoS manufacturing requires sophisticated technology and substantial capital investment, making technical hurdles high and limiting the number of companies capable of supplying it. Leading AI chip companies, particularly Nvidia, are believed to have secured the majority of CoWoS capacity, thereby restricting access for other players. This supply shortage has led to increased costs and delayed market entry for AI chips, impacting the overall growth of the semiconductor industry.

Strategic Significance and Outlook

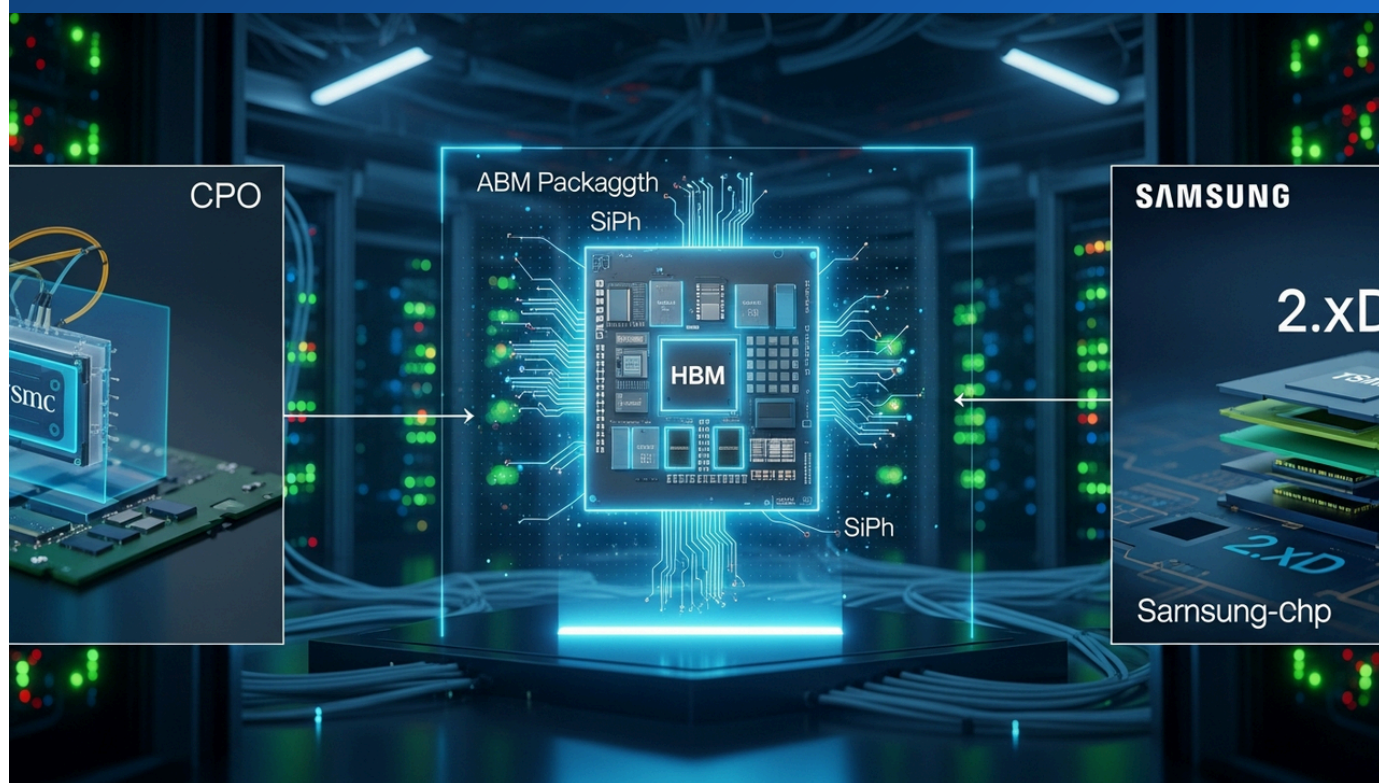
TSMC's target of reaching 200,000 CoWoS wafers by 2027 represents a significant milestone towards stabilizing AI chip supply. This will enable major AI chip vendors like Nvidia and AMD to ship more products, further accelerating the adoption and development of AI technology. However, given the long lead times for equipment and the current order situation, CoWoS supply constraints will not be entirely resolved in the short term. TSMC and its OSAT partners must continue to invest in CoWoS technological innovation and capacity expansion to meet the demands of the AI era. The trajectory of CoWoS supply will remain a key determinant of AI industry development in the coming years.

Source: <https://www.digitimes.com/news/a20260710PD226/tsmc-cowos-2027-packaging-capacity.html>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#17 TSMC Leads in Data Center Co-Packaged Optics, While Samsung Pursues Future AI Packaging with HBM, Logic, and SiPh Integration in '2.xD' Technology

Published July 12, 2026 KuCoin International



OVERVIEW

TSMC leads the data center co-packaged optics (CPO) switch market, with Broadcom and NVIDIA already sampling or shipping CPO switches based on TSMC's technology. Concurrently, Samsung is developing '2.xD' advanced packaging that integrates HBM, logic chips, and silicon photonic chips into a single package, aiming to address optical I/O for future AI computing. Samsung's unique 'triple-play' portfolio (HBM, logic foundry, silicon photonics) enables internal co-design, potentially differentiating its AI packaging strategy.

Key Findings

TSMC has established a leading position in the data center co-packaged optics (CPO) switch market, having already commenced sampling or shipping products in collaboration with Broadcom and NVIDIA. Simultaneously, Samsung is actively developing '2.xD' advanced packaging technology that integrates high-bandwidth memory (HBM), logic chips, and silicon photonic (SiPh) chips into a single package, focusing on resolving future optical I/O challenges in AI computing.

Technical and Clinical Details

TSMC's CPO technology dramatically shortens data transmission distances by physically packaging optical engines and electrical chips in close proximity, thereby improving power efficiency and bandwidth. This directly addresses network bottlenecks and power consumption issues in data centers. Samsung's '2.xD' packaging, on the other hand, integrates SiPh chips alongside HBM and logic chips, enabling optical signal data transmission within and between chips. This technology specifically targets the enormous data transfer volumes and power consumption challenges of AI data centers. Samsung leverages its unique 'triple-play' portfolio, which includes DRAM (HBM), logic foundry, and silicon photonics, providing a distinct advantage in co-designing and optimizing these components internally. This internal capability holds the potential for system-level performance optimization and cost efficiency.

Background and Industry Context

The evolution of AI has significantly increased demands not only for semiconductor chip computational power but also for inter-chip and inter-system data transmission bandwidth. Traditional electrical signal transmission faces physical limitations and power consumption challenges. Advanced packaging technologies like CPO and '2.xD' aim to overcome these hurdles by enabling optical signal transmission at the chip level, thus laying the groundwork for next-generation AI infrastructure. TSMC, as a leading foundry, is pioneering CPO technology in collaboration with key customers. Meanwhile, Samsung leverages its vertically integrated strengths, from memory to foundry, to differentiate itself with comprehensive, proprietary solutions.

Strategic Significance and Outlook

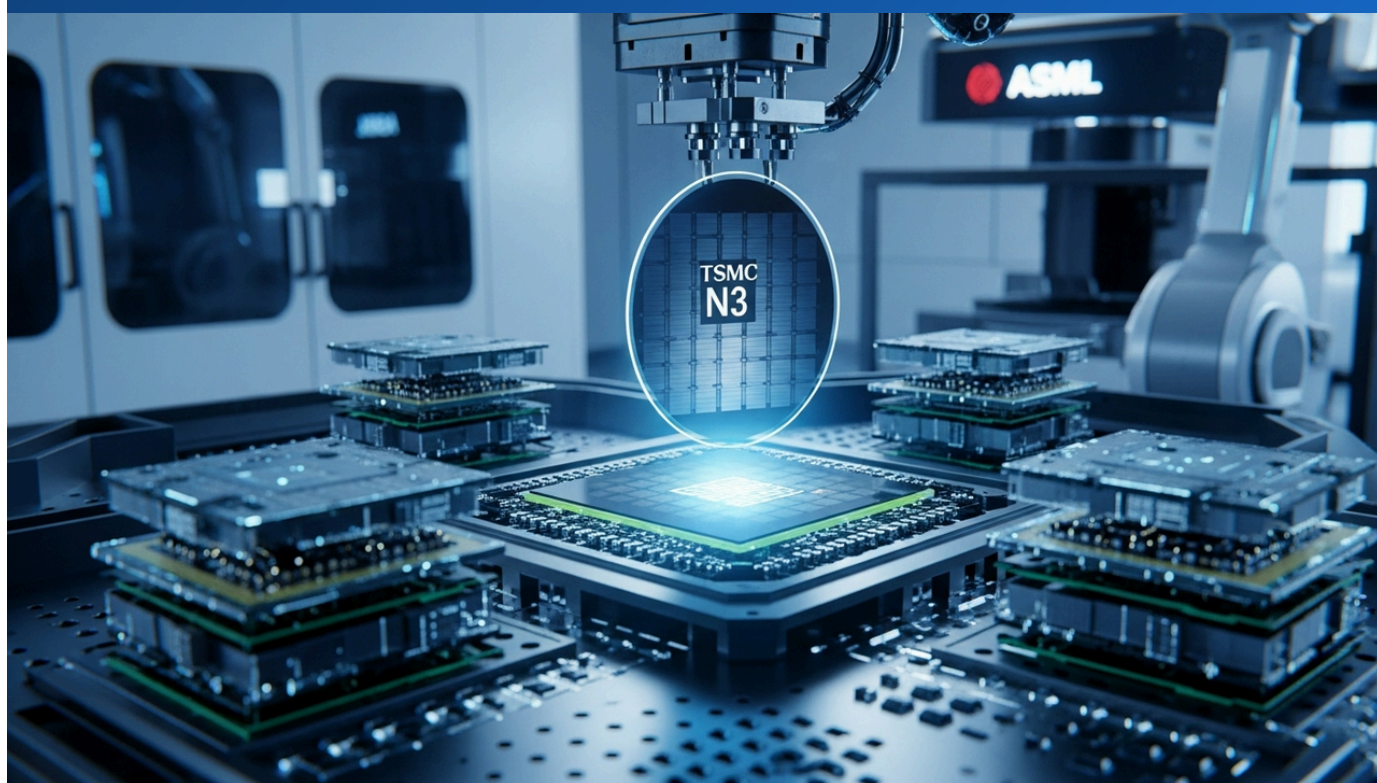
The widespread adoption of TSMC's CPO technology will bring about a major transformation in data center architectures, improving the efficiency of AI workloads. Samsung's '2.xD' packaging technology has the potential to establish new standards in future AI chip design, offering a comprehensive solution to power and performance challenges. The technological rivalry between these two giants is critically important for shaping the future of AI computing, indicating the advent of an era where optical I/O technology becomes mainstream in semiconductor packaging. Researchers, engineers, and investors must closely monitor the advancements in these advanced packaging technologies and their implications for AI infrastructure.

Source: <https://www.kucoin.com/news/flash/tsmc-leads-in-switch-cpo-samsung-bets-on-future-ai-packaging>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#18 TSMC's N3 Node and Expanding CoWoS Capacity Solidify Nvidia's Future, While HBM4 Multi-Vendor Qualification Reduces Supply Risk

Published July 16, 2026 Seeking Alpha USA



OVERVIEW

TSMC and ASML's raised guidance confirms persistent AI infrastructure demand-supply imbalance. TSMC's N3 node, utilized for Nvidia's Rubin GPUs, is fully booked, and CoWoS advanced packaging capacity is expanding by nearly 50%, with Nvidia reportedly securing over half for the next two years. Additionally, the multi-vendor qualification of HBM4 by Samsung, SK Hynix, and Micron mitigates supply chain risk as the industry transitions to higher-capacity 16-Hi HBM4 memory, firmly supporting Nvidia's future.

Key Findings

The upward revision of earnings guidance by TSMC and ASML has unequivocally confirmed that demand for AI (Artificial Intelligence) infrastructure continues to outstrip supply capacity. Notably, TSMC's N3 node, essential for Nvidia's next-generation Rubin GPUs, is fully booked, and its CoWoS advanced packaging capacity is expanding by approximately 50%, with reports indicating Nvidia has secured over half of this expanded capacity for the next two years. Concurrently, the multi-vendor qualification of HBM4 by Samsung, SK Hynix, and Micron is mitigating supply chain risks associated with the transition to higher-capacity 16-Hi HBM4 memory, further solidifying Nvidia's future growth trajectory.

Technical and Clinical Details

The N3 node represents TSMC's most advanced process technology, forming the core of high-performance AI accelerators like Nvidia's Rubin GPUs. This node significantly boosts transistor density and power efficiency, dramatically enhancing AI workload processing capabilities. CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging technology is indispensable for integrating N3-processed GPU dies with multiple HBM stacks, enabling ultra-high bandwidth and low latency. The 50% expansion of CoWoS capacity demonstrates TSMC's proactive efforts to resolve AI chip supply bottlenecks. HBM4, the next generation of high-speed memory, offers further improvements in capacity and bandwidth compared to HBM3E; its 16-Hi configuration doubles the memory capacity per single stack by layering more DRAM dies. Multi-vendor qualification of HBM4 diversifies dependency risks and creates an environment where AI chip manufacturers can reliably secure high-performance memory.

Background and Industry Context

The explosive growth of AI has propelled demands for computational power and memory bandwidth in data centers to unprecedented levels. Nvidia, at the forefront of this AI boom with its GPU product lines, heavily relies on TSMC's cutting-edge foundry technology and CoWoS packaging capacity. However, these capacities are limited, and with competitors like AMD also developing high-performance AI chips, securing supply has become a critical competitive factor. The manufacturing of specialized memory like HBM involves complex processes in both DRAM wafer production and advanced packaging, leading to persistent supply shortages. Early multi-vendor qualification of HBM4 is crucial for mitigating this supply chain vulnerability and fostering healthy growth across the entire AI chip market.

Strategic Significance and Outlook

Securing TSMC's N3 node and CoWoS capacity is a decisive factor for Nvidia to maintain its leadership in the AI semiconductor market and successfully launch its next-generation Rubin GPUs. The continuous expansion of CoWoS capacity will stabilize the supply of AI chips and drive further innovation in AI technology. Stable HBM4 supply from multiple sources will benefit not only Nvidia but also other AI chip development companies, enhancing supply chain resilience. The combination of these factors suggests that the AI industry is poised for further growth and evolution in the coming years, accelerating investment and innovation across the entire semiconductor ecosystem.

Source: <https://seekingalpha.com/article/4922584-ai-supply-chain-just-confirmed-nvidia-future>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#19 TSMC Achieves Record Q2 Revenue of \$40.2B with 67.7% Gross Margin, CoWoS Fully Booked Through 2026, and Maps 14-Reticle Packaging

Published July 16, 2026 LongYield - Substack International



OVERVIEW

TSMC reported record Q2 2026 consolidated revenue of \$40.20 billion and a gross margin of 67.7%, driven by robust AI chip demand and leading-edge nodes (7nm and below accounting for 77% of wafer revenue). The company reiterated that CoWoS advanced packaging capacity remains fully booked through 2026 and outlined a roadmap towards 14-reticle packaging for larger AI silicon. TSMC raised its 2026 capital budget to \$60-64 billion, allocating 10-20% to advanced packaging, testing, and mask making, projecting even higher capex in the next three years.

Key Findings

TSMC achieved a record consolidated revenue of \$40.20 billion and an impressive gross margin of 67.7% in Q2 2026. This robust performance was primarily fueled by the strong demand for AI chips, with the company's leading-edge nodes (7nm and below) continuing to drive 77% of wafer revenue. TSMC reaffirmed that its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity remains fully booked through 2026 and outlined a roadmap towards 14-reticle packaging to accommodate future, larger AI silicon.

Technical and Clinical Details

TSMC's CoWoS technology is a 2.5D/3D packaging solution critical for high-density integration of GPUs, HBM (High Bandwidth Memory), and chiplets. It is indispensable for maximizing AI chip performance by achieving ultra-high bandwidth and low latency, and its limited supply capacity has been a bottleneck constraining overall AI chip shipments. The earnings announcement re-emphasized TSMC's aggressive efforts to expand CoWoS capacity. Specifically, the '14-reticle packaging' roadmap suggests a technological evolution capable of integrating even larger silicon dies than current CoWoS, a necessary step for future ultra-large-scale AI accelerators. The company increased its 2026 capital expenditure budget to \$60-64 billion, allocating 10% to 20% to back-end areas like advanced packaging, testing, and mask making. This clearly indicates that back-end technologies, not just front-end miniaturization, are crucial for performance improvement in the AI era.

Background and Industry Context

The increasing complexity of AI models and the explosive growth in data volume demand unprecedented computational power and data bandwidth from semiconductor chips, dramatically boosting the demand for advanced packaging technologies like CoWoS. Leading AI chip vendors, such as NVIDIA, rely heavily on CoWoS for many of their products, making its supply a critical competitive factor. TSMC, as a leader in foundry services, drives the market in both cutting-edge process technology and advanced packaging. However, CoWoS capacity shortages remain an industry-wide challenge. This earnings report clearly illustrates the structural changes brought by the AI boom to the semiconductor industry and TSMC's strategic investments to address them.

Strategic Significance and Outlook

TSMC's strong financial performance and ambitious capital expenditure plans strongly underscore the long-term growth of the AI semiconductor market. The fully booked status of CoWoS capacity through 2026 and plans for further expansion will contribute to stabilizing AI chip supply, accelerating the adoption and development of AI technology. Advances in 14-reticle packaging technology will enable the design and manufacturing of even higher-performance and more complex AI chips, fostering the realization of next-generation AI applications. TSMC's projection of even higher capital expenditures over the next three years suggests that the semiconductor industry is in a sustained growth phase in the AI era, representing a crucial trend for researchers, engineers, and investors to monitor.

Source: <https://longyield.substack.com/p/tsmc-the-ai-foundry-prints-again>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#20 Japan's Rapidus Partners with IBM on 2nm Semiconductor Manufacturing to Bolster Indo-Pacific Supply Chain Resilience

Published July 10, 2026 Geopolitical Analysis / Think Tank International



OVERVIEW

Japan's Rapidus, in partnership with IBM, aims to establish 2nm advanced semiconductor manufacturing in Japan, strengthening the Indo-Pacific supply chain, including ASEAN countries. This initiative positions Japan as a manufacturing hub for ASEAN logic semiconductor companies, accelerating technological collaboration and human capital development in semiconductor assembly, testing, and packaging across the region.

Key Findings

The Rapidus project in Japan extends beyond merely strengthening domestic semiconductor manufacturing; it aims to establish advanced 2nm (nanometer) semiconductor production in Japan through a strategic partnership with IBM. This initiative seeks to enhance the resilience of the entire Indo-Pacific semiconductor supply chain, encompassing ASEAN nations. This vision carries broader strategic implications for geopolitical stability and economic security.

Technical and Clinical Details

Rapidus plans to leverage IBM's 2nm process technology to manufacture cutting-edge logic semiconductors. This involves innovative processes such as Extreme Ultraviolet (EUV) lithography and Gate-All-Around (GAA) transistor structures. The collaboration with IBM is not limited to front-end manufacturing but also extends to advanced packaging technologies, which are essential for AI chips. This will enable Rapidus to offer complex back-end solutions, including chiplet integration and High Bandwidth Memory (HBM) stacking. The project aims for Japan to become a hub for cutting-edge semiconductor R&D and manufacturing, with Rapidus expected to serve as a manufacturing base for ASEAN semiconductor design companies in the future.

Background and Industry Context

Amid global vulnerabilities in semiconductor supply chains, nations are rushing to rebuild and strengthen their domestic semiconductor manufacturing capabilities for economic security. Japan, once a semiconductor powerhouse, has lost its competitive edge over the past few decades. Rapidus is a national endeavor to reverse this trend and revitalize Japan's semiconductor industry. Strengthening the resilience of the entire semiconductor ecosystem in the Indo-Pacific region is particularly emphasized within international cooperation frameworks, such as the U.S. CHIPS Act. ASEAN countries play a crucial role in semiconductor assembly, testing, and packaging (ATP), and collaboration with Rapidus could contribute to enhancing technological standards and human resource development across the region.

Strategic Significance and Outlook

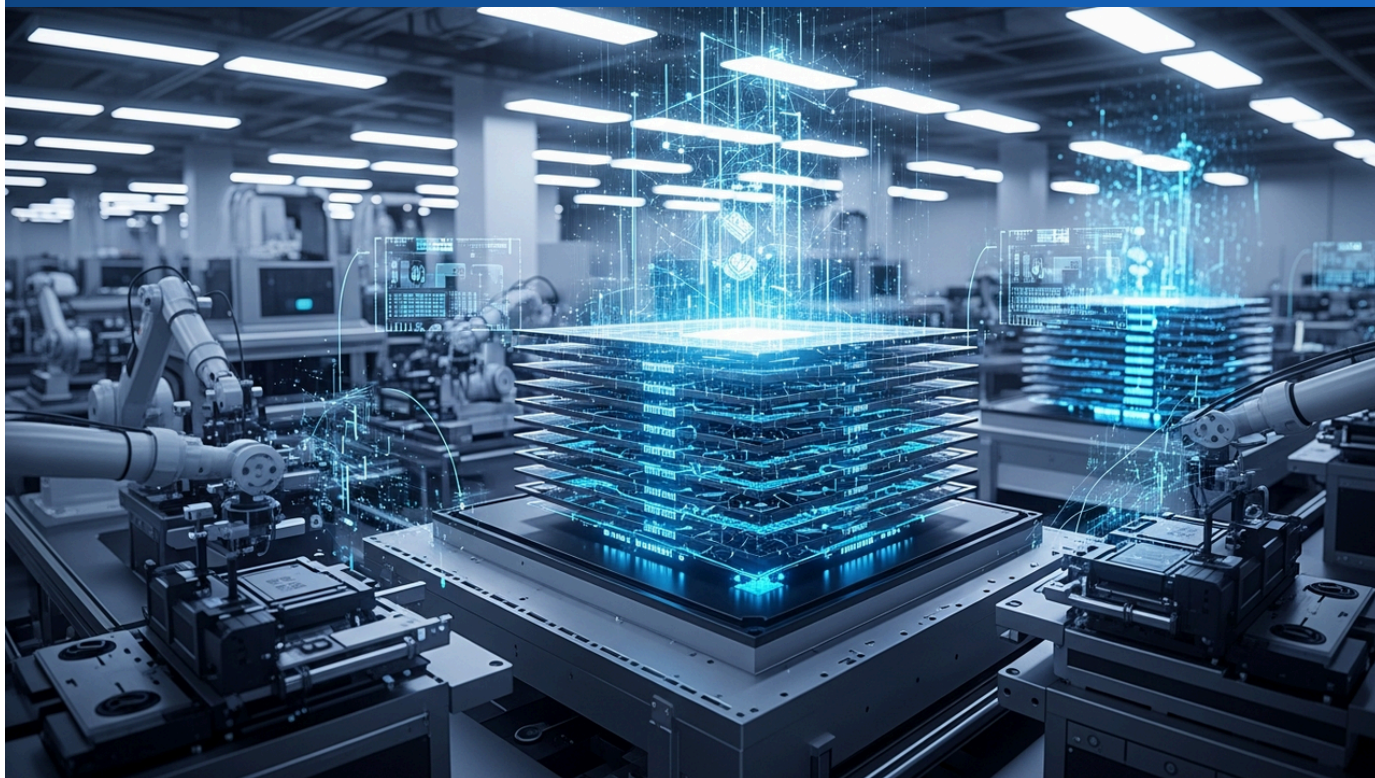
The commencement of mass production using Rapidus' 2nm process (targeted for 2027) will mark a significant milestone for Japan's semiconductor industry. The technological partnership with IBM and the contribution to strengthening the Indo-Pacific supply chain will further enhance Rapidus' strategic value. This project not only holds the potential for Japan to once again become a major global player in cutting-edge semiconductor technology but is also expected to play an indispensable role in fostering deeper technological cooperation with ASEAN countries and accelerating human capital development in the semiconductor sector, thereby building a more stable regional ecosystem. This is a crucial initiative that contributes not only to economic benefits but also to geopolitical stability.

Source: <https://japan-forward.com/rapidus-resilient-indo-pacific-semiconductor-ecosystem-satoshi-nohara/>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#21 AI-Driven Advanced Packaging Orders Surge, Widening ABF Carrier Board Supply-Demand Gap, Benefiting Industry with Both Volume and Price Increases

Published July 15, 2026 AlphaWire International



OVERVIEW

Nomura Securities reports the semiconductor packaging substrate industry is experiencing a strong AI-driven recovery, with global packaging substrate shipments up 36% year-on-year in June 2026. This growth is primarily fueled by ABF (Ajinomoto Build-up Film) carrier boards for AI GPUs, ASICs, and HBM. With ABF carrier board capacity expansion limited to 15-20% annually, the supply-demand gap is widening, enabling suppliers like Xinxing Electronics (Unimicron), Ibiden, and AT&S to benefit from both volume and price increases.

Key Findings

According to a recent report by Nomura Securities, the semiconductor packaging substrate industry is experiencing a robust recovery driven by Artificial Intelligence (AI) demand. Global packaging substrate shipments recorded a significant 36% year-on-year increase in June 2026. This growth is primarily accelerated by ABF (Ajinomoto Build-up Film) carrier boards, essential for high-performance AI chips such as AI GPUs, ASICs (Application-Specific Integrated Circuits), and HBM (High Bandwidth Memory).

Technical and Clinical Details

ABF carrier boards are critical materials for forming the complex circuits of high-performance AI chips and connecting multiple semiconductor components like chiplets and HBM. Their multi-layered structure and fine wiring technology are paramount for ensuring high-speed data transfer and signal integrity between chips. However, the manufacturing of ABF carrier boards demands advanced technology, substantial capital investment, and long lead times, limiting the pace of production capacity expansion to approximately 15% to 20% annually. This constrained expansion cannot keep up with the explosive growth in AI chip demand, resulting in a continuously widening supply-demand gap. Key ABF carrier board suppliers like Xinxing Electronics (Unimicron), Ibiden, and AT&S are in an advantageous position regarding both product volume and pricing in this tight supply environment, expanding their revenue opportunities.

Background and Industry Context

The increasing demand for high-performance semiconductors across AI, High-Performance Computing (HPC), 5G, and automotive sectors is pushing the limits of traditional packaging technologies, driving a shift towards advanced packaging solutions. ABF carrier boards are one of the core materials for this advanced packaging, becoming key to achieving performance improvements through chiplet technology and 3D stacking, particularly as Moore's Law slows. Given that Ajinomoto dominates over 95% of the global ABF film market, this market relies on a few specialized companies, leading to a severe material shortage across the supply chain. The surge in AI demand has further exposed this existing structural challenge, enhancing the strategic importance of ABF substrates.

Strategic Significance and Outlook

The surge in AI-driven advanced packaging demand and the consequent widening of the ABF carrier board supply-demand gap are projected to continue for several years. This situation will allow major suppliers like Unimicron, Ibiden, and AT&S to maintain strong pricing power and stable order backlogs, ensuring continued robust growth.

Semiconductor manufacturers will find it imperative to strengthen long-term strategic partnerships with these substrate material suppliers to ensure a stable supply. This scenario is expected to drive further large-scale investment and technological innovation in ABF carrier board production capacity, remaining a crucial factor in supporting the evolution of AI chips and the construction of AI infrastructure. For researchers, engineers, and investors, this sector will continue to be a significant point of interest.

Source: <https://kgvv.com/tweets/posts/2026-07-15/ima-daily5min-0715-46-fa182f298e/>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#22 Rapidus and Cadence Partner on Agentic AI for Advanced SoC Design, Driving System-Level Co-Optimization

Published July 17, 2026 Las Vegas Sun USA



RAPIDUS and Cadence
partner for advanced SoC Design for
Agentic AI, promoting system-level
level optimization
July 17, 2026, America

OVERVIEW

Japan's Rapidus announced a partnership with Cadence to drive system-level co-optimization for Agentic AI-enabled advanced SoC (System-on-Chip) design. This collaboration emphasizes tight integration across semiconductor design, manufacturing, packaging, and systems, crucial for next-generation SoCs required by AI infrastructure and physical AI-powered systems. Rapidus is also expanding its Raads lineup with new tools to enhance quality assurance and assist designers in resolving design issues.

Key Findings

Rapidus, the Japanese initiative aiming for advanced semiconductor manufacturing, has announced a strategic partnership with Cadence, a global leader in Electronic Design Automation (EDA) tools. This collaboration is set to drive system-level, tight co-optimization for advanced System-on-Chip (SoC) design targeting Agentic AI (autonomous AI). This strategic cooperation is intended to accelerate the development of next-generation SoCs critical for AI infrastructure and physical AI-powered systems.

Technical and Clinical Details

This partnership focuses on comprehensive optimization across all stages of semiconductor design, manufacturing processes, packaging, and the entire system. Agentic AI, characterized by high levels of autonomy and learning capabilities, demands extremely complex and high-performance SoCs that are challenging to achieve with conventional chip design methods. Rapidus and Cadence will enhance co-design methodologies, leveraging digital twin technology and AI-driven design automation tools from the early design phases through manufacturing, to meet chip performance, power consumption, and area (PPA) targets. By combining Cadence's expertise with Rapidus' 2nm (nanometer) process technology and advanced packaging capabilities, they will efficiently address complex packaging challenges such as chiplet integration, High Bandwidth Memory (HBM) stacking, and heterogeneous integration. Rapidus is also expanding its 'Raads' lineup of tools to enhance quality assurance and assist designers in quickly identifying and resolving design issues.

Background and Industry Context

The evolution of AI presents unprecedented challenges to semiconductor chip design and manufacturing. Agentic AI, in particular, demands real-time processing, ultra-low power consumption, and high reliability, which are difficult to achieve with traditional chip design approaches. Consequently, a 'system-level co-design' approach, which optimizes not only the chip manufacturing process but also the chip, package, and entire system as an integrated whole, has become indispensable. Rapidus, a national project supported by the Japanese government to establish 2nm process technology domestically, recognizes that strong partnerships with EDA industry leaders like Cadence are crucial for its success. This collaboration will foster the resurgence of Japan's semiconductor industry and contribute to strengthening the global supply chain resilience.

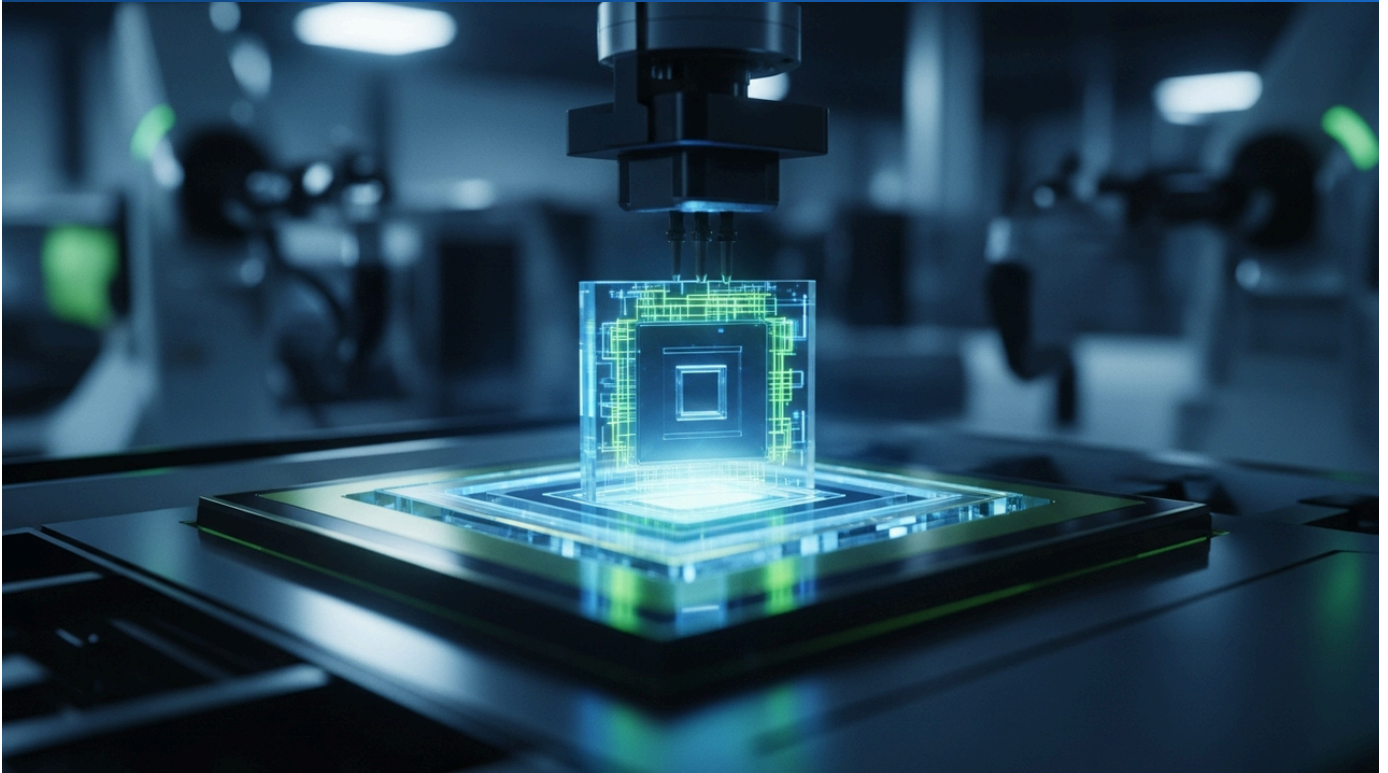
Strategic Significance and Outlook

The partnership between Rapidus and Cadence is poised to enable significant breakthroughs in the design and manufacturing of advanced SoCs for Agentic AI. The system-level co-optimization approach will maximize AI chip performance and efficiency, accelerating the development of a wide range of AI applications, from edge AI devices to large-scale data centers. The full operation of Rapidus' 2nm process and the utilization of Cadence's AI-driven design tools will build a strong foundation for Japan's semiconductor industry to once again play a leading role in the world's cutting-edge technology arena. Researchers, engineers, and investors should monitor the impact of this collaboration on the future of AI chip design and manufacturing, evaluating it as a new trend towards realizing next-generation AI infrastructure.

Source: <https://lasvegassun.com/news/2026/jul/16/rapidus-and-cadence-partner-on-agentic-ai-for-adva/>

#23 Kuo Ming-Chi Reveals TSMC's 'Glass Killer' Technology: Glass Core Substrate Development with NVIDIA to Revolutionize AI Chip Manufacturing by 2028

Published July 15, 2026 三立新聞網SETN.COM Taiwan



OVERVIEW

Renowned analyst Kuo Ming-Chi reveals TSMC's secretive development of 'glass core substrates' in collaboration with NVIDIA, poised to be a game-changer for next-generation AI chip manufacturing. This innovative technology is critical for mitigating chip warpage, enhancing power integrity, and significantly boosting AI computing power. With partners like Innolux and Ibiden, TSMC aims for practical application of these substrates to drive AI chip innovation from 2028 onwards.

Background

The escalating complexity of AI models and the exponential growth of data are pushing semiconductor chips to their computational and efficiency limits, rapidly exposing the inherent shortcomings of conventional organic substrates. Large-scale AI chips, in particular, face significant challenges with warpage and thermal management during advanced packaging, which increasingly bottleneck performance and manufacturing yield. Glass core substrate technology is emerging as a pivotal strategic solution to address these issues and unlock performance enhancements beyond traditional Moore's Law scaling. NVIDIA's deep involvement with TSMC in this joint development underscores the critical role of advanced packaging, particularly substrate innovation, as a key differentiator in the fierce competition for AI chip supremacy.

Key Findings

According to a report by TF International Securities analyst Kuo Ming-Chi, TSMC is engaged in a confidential, collaborative development with NVIDIA on a 'glass core substrate' technology, hailed as a potential 'game-changer' for next-generation AI chip manufacturing. This groundbreaking innovation promises to dramatically mitigate chip warpage, significantly improve power integrity, and consequently, substantially boost AI computing power.

Glass core substrates represent a fundamental shift in semiconductor packaging materials, offering superior physical and electrical characteristics compared to conventional organic alternatives. Its primary advantages include:

- **Exceptional Flatness and Thermal Stability:** The extremely high flatness and low coefficient of thermal expansion of glass effectively suppress chip warpage during the fabrication of large-scale AI chips. This dramatically improves manufacturing yield and enhances reliability for multi-layer stacking and fine interconnections in advanced packaging.
- **Enhanced Power Integrity:** The superior dielectric properties of glass significantly bolster power delivery stability, ensuring efficient supply of the high currents demanded by AI accelerators while minimizing critical signal loss.

- **Higher Interconnect Density:** A glass base facilitates much finer wiring (lower L/S ratio) and higher-density Through-Silicon Via (TSV) formation. This capability is crucial for dramatically increasing data transmission bandwidth between chiplets, essential for high-performance AI processors.

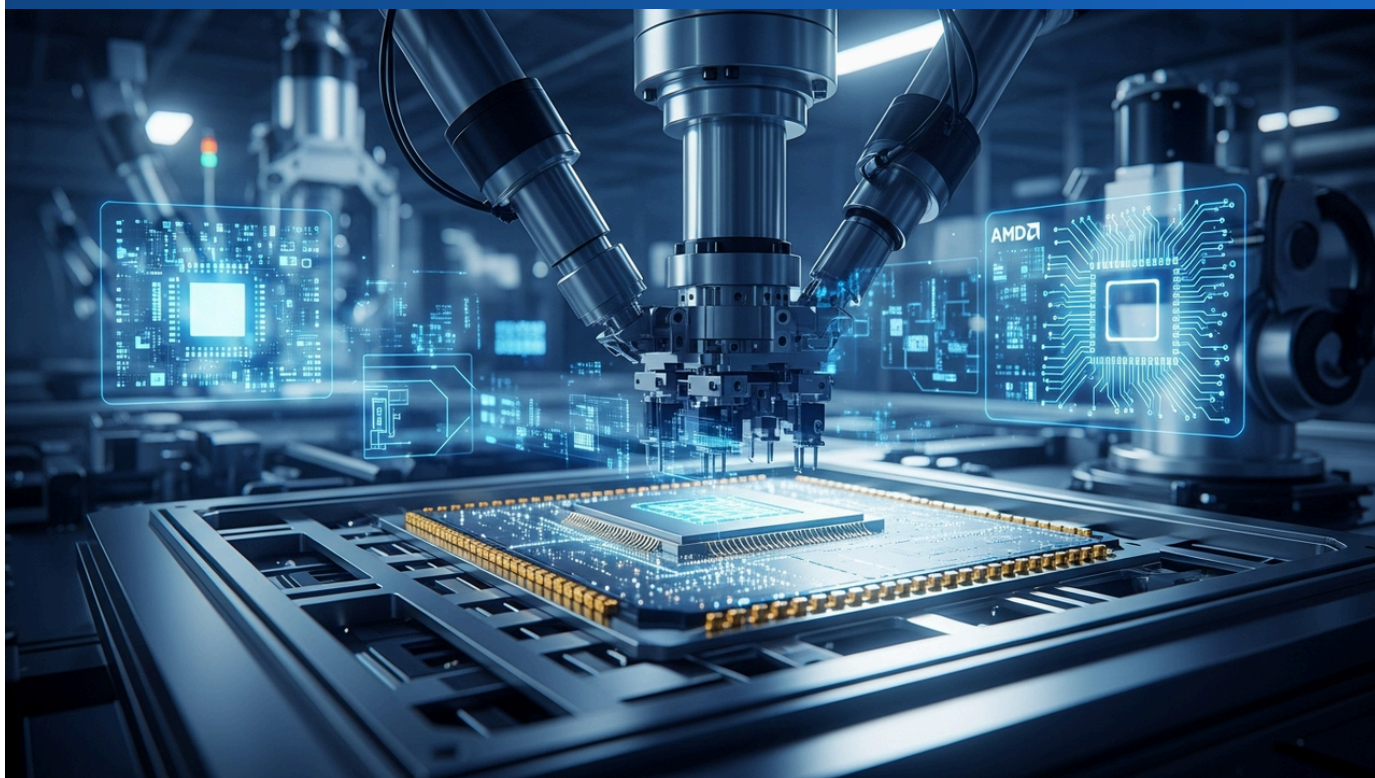
TSMC is actively pushing for the practical application of this technology, collaborating with display panel manufacturer Innolux and Japan's leading ABF substrate producer, Ibiden. Industry experts anticipate a high likelihood of adoption in NVIDIA's cutting-edge AI chips from 2028 onwards.

This glass core substrate technology is set to revolutionize AI chip manufacturing, elevating the performance of NVIDIA's future AI accelerators to unprecedented levels. Its widespread adoption will also profoundly impact the ABF substrate market, potentially creating new growth opportunities for major suppliers such as Ibiden and AT&S as providers of these advanced glass core substrates. The availability of such high-precision, reliable packaging materials is indispensable for the development of advanced Agentic AI. This 'glass killer' technology is expected to have a transformative effect on the entire semiconductor ecosystem in the AI era, warranting close monitoring by researchers, engineers, and investors alike for its long-term implications in shaping the future of artificial intelligence.

Source: <https://www.setn.com/klist/998>

#24 NVIDIA's 2027 CoWoS Supply Forecast Raised 69% to 1.1 Million Interposers; AMD to See Over 50% Growth: KeyBanc Asia Supply Chain Checks Reveal Strong Demand

Published July 16, 2026 TipRanks USA



OVERVIEW

KeyBanc analyst John Vinh's Asia supply chain checks reveal strong, persistent demand across the semiconductor ecosystem. NVIDIA's 2027 CoWoS supply forecast for Rubin and Rubin Ultra was raised 69% to 1.1 million interposers. AMD anticipates over 50% unit growth next year driven by server CPU capacity, with its CoWoS supply projected to increase from 80,000-90,000 units this year to 130,000 next year. This clearly indicates robust, sustained demand for advanced packaging.

Key Findings

Recent Asia supply chain checks conducted by KeyBanc analyst John Vinh confirm persistent, strong demand for AI chips across the entire semiconductor ecosystem. NVIDIA's 2027 CoWoS (Chip-on-Wafer-on-Substrate) supply forecast for its Rubin and Rubin Ultra GPUs has been significantly raised by 69% to 1.1 million interposers year-over-year. Concurrently, AMD is projected to achieve over 50% unit growth next year, driven by expanding server CPU capacity, with its CoWoS supply expected to increase from 80,000-90,000 units this year to 130,000 units next year. These figures unequivocally highlight the sustained high demand for advanced packaging.

Technical and Clinical Details

CoWoS is a 2.5D/3D packaging technology that integrates GPU dies and HBM (High Bandwidth Memory) stacks onto a silicon interposer, delivering the ultra-high bandwidth and power efficiency essential for AI accelerators. NVIDIA's Rubin and Rubin Ultra GPUs, as next-generation AI chips, heavily rely on this CoWoS technology to provide larger-scale data processing and faster inference capabilities. KeyBanc's analysis suggests that despite significant expansion in TSMC's CoWoS capacity, NVIDIA is securing the majority of it. The increase in CoWoS supply for AMD's server CPUs signifies that its "Venice" CPUs are enhancing their ability to process AI workloads more directly, bolstering their competitiveness in the high-performance computing market. This expanding demand underscores the lengthy lead times (7-9 months) for CoWoS manufacturing equipment and the ongoing need for continuous capital investment in capacity expansion.

Background and Industry Context

The evolution of AI is fundamentally transforming the semiconductor industry, with high-speed data transfer between chips and power efficiency becoming new performance bottlenecks beyond mere computational power increases. To address these challenges, advanced packaging, especially technologies like CoWoS, has become indispensable. TSMC is a dominant player in the CoWoS market, and its capacity directly influences the production plans of AI chip manufacturers. The intense competition between NVIDIA and AMD for CoWoS supply clearly demonstrates that advanced packaging capacity is a key differentiator and success factor in the AI chip market. Efforts to secure long-term CoWoS supply agreements and strengthen vertically integrated manufacturing capabilities are also accelerating.

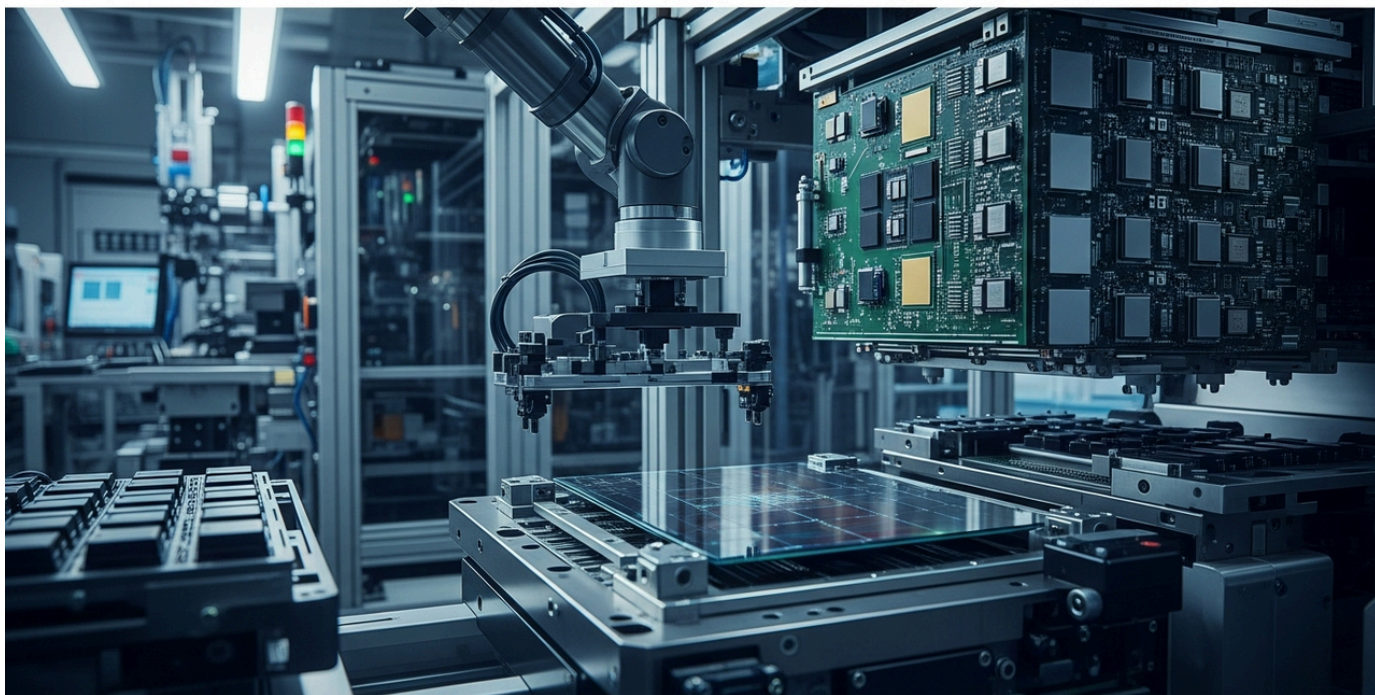
Strategic Significance and Outlook

The upward revision of CoWoS supply for NVIDIA and AMD suggests that the AI market's robust growth will continue. Particularly, as NVIDIA's Rubin series further drives the AI chip market, the stabilization of its supply will accelerate the adoption of AI technologies. The expansion of CoWoS demand in AMD's server CPU business means the company will increase its presence not only in AI accelerators but also in the broader data center market. However, the supply-demand balance for CoWoS remains tight, necessitating continuous expansion of supply capacity and technological innovation. For investors, advanced packaging technologies and associated capital expenditures will continue to be a significant growth theme across the entire semiconductor ecosystem.

Source: <https://www.tipranks.com/news/nvda-mu-amd-keybanc-raises-price-targets-after-asia-supply-chain-checks>

#25 NVIDIA's AI Chip Supply Bottleneck Stems from TSMC's Booked CoWoS Capacity, Intel EMIB Emerges as Alternative

Published July 14, 2026 BingX International



OVERVIEW

TSMC's CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity is fully booked through 2026, with 52-78 week lead times, posing a severe supply bottleneck for NVIDIA. While NVIDIA reportedly secures 60% of CoWoS capacity, AMD holds only 11%. This constraint, exacerbated by the multi-year acquisition and installation time for packaging equipment, is unlikely to ease quickly, prompting NVIDIA to potentially consider alternative packaging technologies like Intel's EMIB.

Key Findings

TSMC's CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity is fully booked through 2026, with lead times for manufacturing equipment stretching between 52 and 78 weeks. This presents a severe supply bottleneck for NVIDIA, a critical factor driving the company to consider alternative packaging technologies, such as Intel's EMIB (Embedded Multi-die Interconnect Bridge).

Technical and Clinical Details

CoWoS is a cutting-edge 2.5D/3D packaging technology that integrates Graphics Processing Units (GPUs), High Bandwidth Memory (HBM), and multiple chiplets onto a silicon interposer, enabling extremely high bandwidth and low latency essential for NVIDIA's high-performance AI chips. Although NVIDIA is estimated to secure approximately 60% of TSMC's CoWoS capacity, this allocation is insufficient to meet the surging demand for AI chips. In contrast, AMD's CoWoS capacity accounts for only about 11% of the total, and the company must allocate this limited supply between its Venice EPYC CPUs and MI400 GPUs, further exacerbating supply constraints. The specialized equipment required for CoWoS manufacturing takes several years from order to delivery, installation, and ramp-up, making short-term supply improvement challenging.

Background and Industry Context

The increasing complexity of AI models and the explosive growth in data volume push the performance limits of semiconductor chips, significantly elevating the importance of advanced packaging technologies. CoWoS has become key to achieving performance enhancements through chiplet technology and 3D stacking, particularly as the pace of Moore's Law slows. While TSMC is a leader in CoWoS technology, its production capacity cannot keep up with the explosive demand for AI chips. This supply shortage leads to increased costs and delayed market entry for AI chips, impacting the overall growth of the semiconductor industry. NVIDIA's consideration of competitive technologies like Intel's EMIB signals diversification of its supply chain and intensifying competition in the advanced packaging market.

Strategic Significance and Outlook

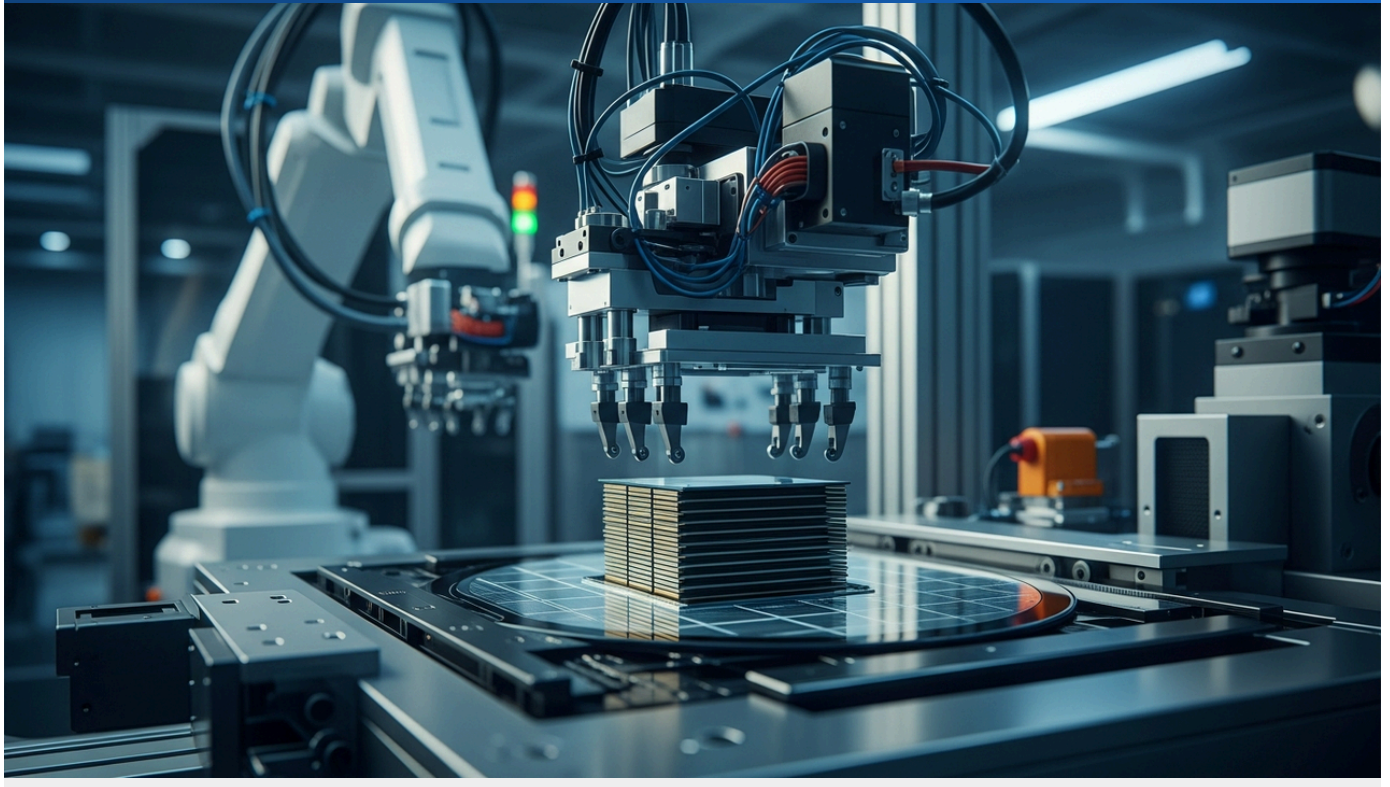
TSMC's CoWoS capacity constraints will directly impact NVIDIA's AI GPU shipment capabilities and will also pose a product supply bottleneck for competitors like AMD. This situation creates an opportunity for Intel to offer its proprietary advanced packaging technology, EMIB, to other companies, potentially diversifying the entire semiconductor ecosystem. Given the long lead times for CoWoS manufacturing equipment, the advanced packaging supply shortage is projected to persist beyond 2026, remaining a critical factor influencing the growth rate of the AI chip market. NVIDIA will need to accelerate its strategy to secure multiple suppliers and technological options for long-term supply stability.

Source: <https://bingx.com/en/news/post/will-tsmc-s-capacity-crunch-derail-the-amd-stock-rally>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#26 CoWoS Identified as Core Bottleneck for AI GPU Shipments, Distinct from HBM Shortage

Published July 13, 2026 BiyaPay Blog International



OVERVIEW

CoWoS (Chip-on-Wafer-on-Substrate) is an advanced packaging technology integrating GPUs, HBM, and chiplets; its limited capacity forms a critical manufacturing integration bottleneck for AI GPU shipments. While an HBM shortage refers to the memory itself, a CoWoS shortage signifies a constraint in the packaging capability that integrates these components. Both are crucial, and a deficit in either impedes final AI GPU delivery.

Key Findings

CoWoS (Chip-on-Wafer-on-Substrate), an advanced packaging technology that integrates GPUs, High Bandwidth Memory (HBM), and chiplets with high density, is currently functioning as a manufacturing integration bottleneck for AI GPU shipments due to its limited production capacity. This CoWoS shortage represents a more fundamental constraint on the AI chip supply chain, distinct from a mere HBM memory shortage.

Technical and Clinical Details

CoWoS technology involves horizontally arranging multiple logic and memory dies (HBM stacks) on a silicon interposer, which are then integrated onto a final organic substrate. This process significantly shortens data transmission distances between chips, achieving ultra-high bandwidth and low latency. These attributes are indispensable for handling the immense data processing volumes and high computational capabilities required by AI models. CoWoS manufacturing demands extremely precise wafer-level processes, sophisticated bonding techniques, and advanced inspection, making these steps far more complex than traditional packaging and requiring substantial capital investment and long lead times. Consequently, rapid expansion of CoWoS production capacity is challenging. In contrast, an HBM shortage refers to a supply deficit of the memory chips themselves, stemming from issues in DRAM wafer production capacity or HBM stack assembly. A CoWoS shortage implies a situation where, even if sufficient HBM is available, AI GPUs cannot be manufactured due to a lack of packaging capacity to integrate the components.

Background and Industry Context

The explosive growth of AI has propelled demand for high-performance AI chips to unprecedented levels. AI GPUs developed by companies like NVIDIA maximize their performance by seamlessly integrating GPUs and HBM through advanced packaging technologies such as CoWoS. However, CoWoS technology can only be manufactured by a few foundries and OSAT (Outsourced Semiconductor Assembly and Test) providers, such as TSMC, and their production capacity has not kept pace with the increasing demand for AI chips. This bottleneck leads to delayed market entry and increased costs for AI chips, affecting the overall pace of AI infrastructure development. The industry faces a dual challenge of HBM and CoWoS shortages, and resolving both is crucial for the sustainable growth of the AI industry.

Strategic Significance and Outlook

The constraints in CoWoS manufacturing capacity will continue to significantly impact the supply of AI GPUs. Overcoming this bottleneck will require continuous, large-scale capital investment and technological innovation from TSMC and its OSAT partners. Moreover, AI chip design companies like NVIDIA may consider diversifying CoWoS supply or adopting alternative packaging technologies such as Intel's EMIB. Since a supply shortage in either HBM or CoWoS will impede the final delivery of AI GPUs, a balanced strengthening of the entire supply chain is necessary. Overcoming this challenge will be a critical key to enabling and widespread adoption of next-generation AI computing.

Source: <https://www.biyapay.com/en/blogdetail/4358-what-is-cowos-why-does-it-limit-nvidia-gpu-shipmen>

#27 Taiwan's TGV Glass Substrate Supply Chain Advances: E&R Engineering Ships Laser Modification Equipment to US Client, Accelerating Mass Production

Published July 09, 2026 Taiwan News Taiwan



OVERVIEW

Driven by escalating HPC demand, glass substrates are emerging as a next-generation advanced packaging solution, leading to the formation of a robust Through-Glass Via (TGV) supply chain in Taiwan. E&R Engineering has successfully developed laser modification technology for TGV manufacturing, completing equipment validation and shipments to a US customer. Numerous Taiwanese firms are targeting pilot production lines and yield testing within the year, while TGV-related equipment suppliers are actively securing orders.

Key Findings

Amidst the surging demand for High-Performance Computing (HPC) and AI, glass substrates are gaining prominence as a next-generation advanced semiconductor packaging technology, accelerating the formation of a robust Through-Glass Via (TGV) supply chain in Taiwan. E&R Engineering has successfully developed critical laser modification technology for TGV manufacturing, with concrete steps towards commercialization demonstrated by completed equipment validation and shipments to a U.S. customer. Multiple Taiwanese companies are aiming for pilot production lines and yield testing within the current year, indicating rapid market momentum, and related equipment suppliers are actively securing orders.

Technical & Business Details

- **Advantages of Glass Substrates:** Glass substrates offer several significant advantages over traditional silicon interposers, including larger sizes, superior mechanical stability, a lower coefficient of thermal expansion (CTE), and improved high-frequency electrical characteristics. These properties enable higher I/O density and enhanced power delivery, crucial for large-scale AI chips and high-performance processors, thereby improving overall system performance and reliability.
- **Significance of TGV Technology:** TGV is a pivotal technology for next-generation packaging, enabling electrical connections through the thickness of the glass substrate. E&R Engineering's developed laser modification technology facilitates precise and efficient TGV formation, paving the way for the mass production of glass substrates. This technology addresses previous challenges in micro-drilling and subsequent metallization processes.
- **Materializing Supply Chain:** In Taiwan, a comprehensive TGV glass substrate supply chain is coalescing, involving material suppliers, equipment manufacturers, and OSAT (Outsourced Semiconductor Assembly and Test) companies. Suppliers of equipment for all essential TGV manufacturing steps, including drilling, thermal treatment, wet processes, and inspection systems, have already begun receiving customer orders, signaling rapid market adoption.

Background & Context

The evolution of AI is pushing the boundaries of semiconductor packaging technology. For AI accelerators, high-speed data transfer and power efficiency between chips are paramount, and current organic substrates and silicon interposers are nearing their physical limits. Glass substrates are seen as an innovative solution to these challenges, with major players like TSMC, Intel, and Samsung incorporating them into their next-generation roadmaps. For instance, TSMC is planning mass production of glass substrates with its CoPoS (Co-Packaging Optical System) solution by 2028, with Nvidia confirmed as its initial customer.

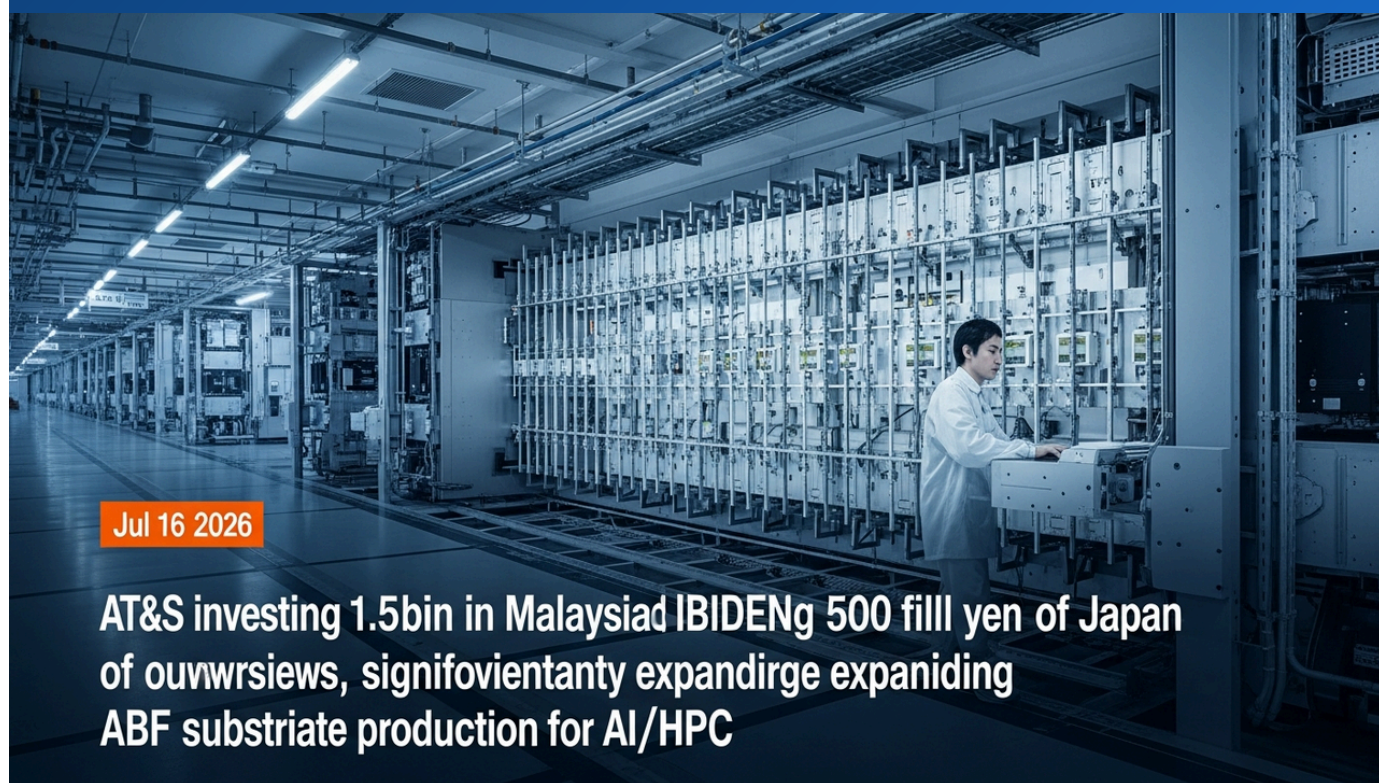
Strategic Significance & Outlook

The establishment of Taiwan's TGV supply chain represents a crucial step in accelerating the commercialization of glass-based advanced packaging technology. This will enable further leaps in AI semiconductor performance, making even more powerful AI systems possible. Sigmaintell Consulting forecasts the global glass-core packaging market to grow rapidly from approximately \$240 million in 2026 to \$8.5 billion in 2028 and \$27.6 billion by 2030, indicating that investment in this sector is set to intensify significantly over the coming years. Taiwan is poised to establish itself as a dominant player in this nascent, high-growth market.

Source: <https://www.taiwannews.com.tw/en/news/6397144>

#28 AT&S to Invest €1.5-2 Billion in Malaysian ABF Capacity, While IBIDEN Allocates ¥500 Billion for AI/HPC Substrate Expansion in Japan & Overseas

Published July 16, 2026 Sector Signals China



Jul 16 2026

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ABF substriate production for AI/HPC

OVERVIEW

AT&S has agreed with AMD and another major tech firm to expand high-end IC substrate capacity for AI/HPC, planning a €1.5-2 billion investment in its Kulim, Malaysia plant, fully supported by long-term customer commitments. Concurrently, Japan's IBIDEN approved a ¥500 billion capital expenditure plan from FY2026-2028 to significantly boost IC package substrate capacity for AI and high-performance servers, targeting existing and overseas facilities, with ¥220 billion specifically for its Gama plant's Cell6. These massive investments address the global ABF substrate shortage driven by surging AI demand.

Key Findings

In response to the escalating demand for semiconductors in AI and High-Performance Computing (HPC), leading IC substrate manufacturers AT&S and IBIDEN have announced significant production capacity expansion investments. AT&S plans to inject approximately €1.5-2 billion into its Malaysian facility, while IBIDEN has approved a capital expenditure plan of around ¥500 billion from fiscal years 2026 to 2028. These investments are strategic and essential moves to meet market demand, especially amidst the worsening global shortage of ABF (Ajinomoto Build-up Film) substrates.

Technical & Business Details

- **AT&S's Malaysian Investment:** Austrian firm AT&S, backed by long-term commitments from AMD and another undisclosed major technology company, intends to invest approximately €1.5-2 billion (equivalent to ¥250-330 billion) in utilizing its existing Kulim, Malaysia facility and a previously idled second factory building. This investment is geared towards substantially increasing the production capacity of high-end IC substrates for AI and HPC applications, demonstrating strong customer endorsement for this expansion.
- **IBIDEN's Domestic and International Fortification:** Japan's IBIDEN has approved a total capital expenditure plan of approximately ¥500 billion for fiscal years 2026 to 2028. This investment is aimed at expanding the production capacity of IC package substrates for AI and high-performance servers, primarily targeting its existing facilities in Gifu Prefecture and overseas plants. Notably, about ¥220 billion will be allocated to Cell6 of its Gama plant, focusing on the introduction of advanced technologies and enhancement of production efficiency.
- **Criticality of ABF Substrates:** ABF substrates are an indispensable material for multi-layer packaging substrates that interconnect high-performance semiconductors like CPUs, GPUs, and HBM. As AI chips become more complex and larger, the demand for bigger and higher-definition ABF substrates has exploded, making their supply capacity a critical bottleneck for the entire AI semiconductor market.

Background & Context

The advancement of AI is driving structural changes across the semiconductor industry. With exponentially growing demands for computational power and data bandwidth, advanced packaging technologies have become key to maximizing chip performance. In 2.5D/3D packaging solutions like CoWoS, ABF substrates are a crucial component that dictates overall performance. Consequently, the supply-demand balance of ABF substrates directly impacts the availability of AI chips and, by extension, the deployment speed of AI infrastructure. The substantial investments by AT&S and IBIDEN represent a necessary strategic response to stabilize the supply of this critical material and capture the growth opportunities of the burgeoning AI era.

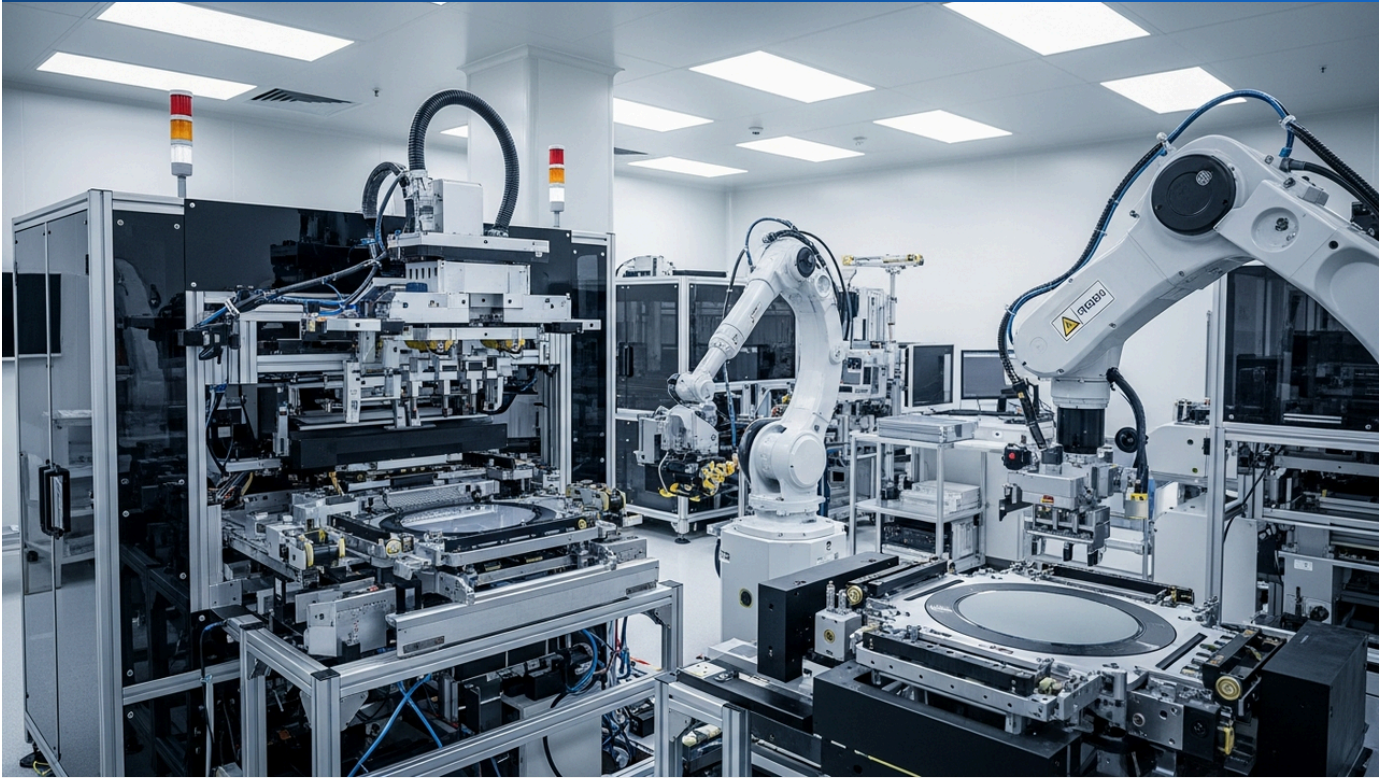
Strategic Significance & Outlook

The large-scale ABF substrate production capacity expansions by AT&S and IBIDEN will significantly contribute to stabilizing the AI semiconductor supply chain. Crucially, increased investment from multiple suppliers will reduce dependency risks on specific regions or companies, enhancing overall supply chain resilience. This will enable AI chip manufacturers to procure high-performance substrates more consistently, fostering further development and widespread adoption of AI technologies. These investments underscore the vital role that the semiconductor back-end industry plays in the AI era.

Source: <https://sector-signals.net/zh/themes/advanced-packaging/articles/abf-substrate-capacity-ats-ibiden-2026>

#29 Malaysia Launches RM92 Million Government-Backed Initiative to Develop HBM4 Advanced Packaging Pilot Line, Targeting Higher Semiconductor Value Chain

Published July 14, 2026 Business News Malaysia



OVERVIEW

Malaysia is aggressively pursuing a strategy to elevate its position in the semiconductor value chain by focusing on IC design and advanced packaging. The Malaysia Advanced Packaging Consortium (MAPC), established in May 2026, has secured RM92 million (\$19.5 million) in government funding and RM93 million (\$19.7 million) from industry partners to develop a pilot HBM4 advanced packaging line within the next two years. This initiative marks a significant step for Malaysia to evolve beyond its traditional role as an OSAT hub towards becoming a higher-value semiconductor manufacturing nation.

Key Findings

Malaysia is intensifying its focus on IC design and advanced packaging to climb higher in the semiconductor value chain. The Malaysia Advanced Packaging Consortium (MAPC), launched in May 2026, has secured RM92 million (approximately \$19.5 million USD) in government funding, complemented by RM93 million (approximately \$19.7 million USD) from industry partners. This substantial investment is earmarked for developing a pilot HBM4 advanced packaging line within the next two years, signaling Malaysia's strategic ambition to transition from a conventional Outsourced Semiconductor Assembly and Test (OSAT) provider to a high-value manufacturing and design hub.

Technical & Business Details

- **HBM4 Advanced Packaging:** MAPC is concentrating its efforts on developing advanced packaging technology for HBM4 (High Bandwidth Memory 4), the next generation of AI memory. HBM4 is crucial for AI accelerators and High-Performance Computing (HPC) systems, offering superior bandwidth and lower power consumption. Investing in this technology signifies Malaysia's commitment to enhancing its technological contribution to the global semiconductor supply chain.
- **Government-Industry Collaboration:** This initiative is a collaborative effort between the Malaysian government and private sector companies. The combined funding of RM92 million from the government and RM93 million from industry partners demonstrates a strong commitment to fostering domestic industry and bolstering international competitiveness. This public-private partnership aims to mitigate risks associated with advanced technology development and accelerate progress.
- **Pilot Line Objectives:** MAPC aims to establish a pilot HBM4 advanced packaging line within two years. This objective is crucial for validating the technology, gaining practical experience in advanced packaging, and laying the groundwork for future large-scale production. It represents a vital step for Malaysia to build expertise and capacity in a cutting-edge domain.

Background & Context

For decades, Malaysia has been a critical global hub for semiconductor back-end (OSAT) services. However, the advent of the AI era has intensified competition in the semiconductor industry, demanding a shift towards higher-value IC design and advanced packaging technologies. As Taiwan and South Korea lead in advanced packaging with technologies like CoWoS, Malaysia is strategically positioning itself to catch up, making the upgrading of its semiconductor ecosystem a national priority. Acquiring state-of-the-art memory packaging capabilities, such as HBM4, is essential for the country to secure a more strategic position in the global semiconductor supply chain.

Strategic Significance & Outlook

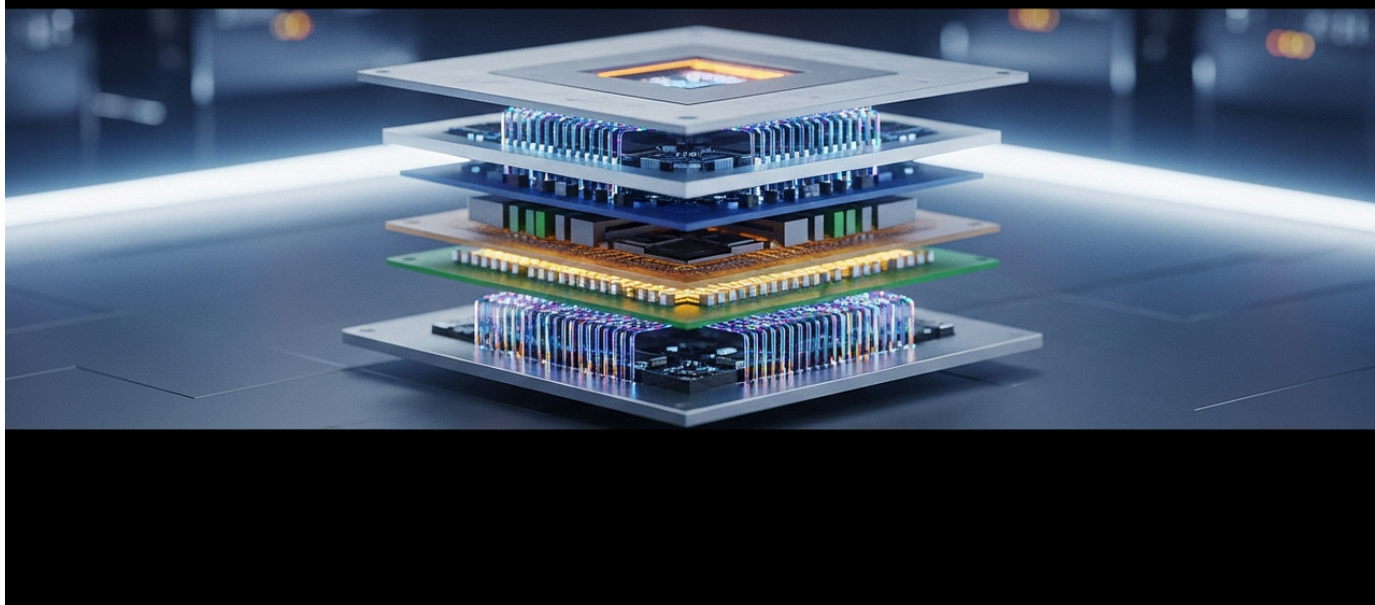
Malaysia's push into advanced packaging has the potential to significantly transform its semiconductor industry structure. The successful development of an HBM4 pilot line could attract further high-tech investments and create skilled employment opportunities, contributing to overall national economic growth. From a geopolitical perspective, this initiative also contributes to the diversification and resilience of the semiconductor supply chain, positioning Malaysia as an important node in supporting global AI infrastructure development. This move is part of a broader trend among Southeast Asian nations to take on more significant roles beyond traditional assembly and testing within the semiconductor ecosystem.

Source: <https://businessnews.com.my/malaysia-targets-higher-semiconductor-value/>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#30 Samsung Electronics Advances "2.xD" Packaging Integrating HBM, Logic, and Optical Tech to Resolve AI Power and Heat Bottlenecks

Published July 10, 2026 BigGo Finance South Korea



OVERVIEW

Samsung Electronics is developing "2.xD" next-generation packaging technology that integrates High Bandwidth Memory (HBM), logic chips, and silicon photonics (SiPh) into a single package to address critical power consumption and heat issues in AI data centers. This innovation aims to transcend the limitations of current silicon interposer-based packaging by utilizing a panel-based Redistribution Layer (RDL) interposer, allowing for comprehensive system integration. This approach promises significantly enhanced data transfer speeds and substantial reductions in power consumption and heat generation, fundamentally improving AI infrastructure performance and efficiency.

Key Findings: Samsung Tackles AI Power and Heat with "2.xD" Packaging

Samsung Electronics is aggressively pursuing the development of its groundbreaking "2.xD" next-generation packaging technology, designed to directly address the escalating power consumption and thermal management challenges faced by AI data centers. This innovative approach aims to integrate High Bandwidth Memory (HBM), high-performance logic chips, and silicon photonics (SiPh) into a single, advanced package.

Technical Details: Panel-Based RDL Interposers and Hybrid Bonding

- The "2.xD" packaging technology endeavors to surpass the limitations of conventional 2.5D packaging, which typically relies on silicon interposers. Samsung's strategy involves adopting a larger, more cost-effective panel-based Redistribution Layer (RDL) interposer to seamlessly integrate HBM, logic chips, and SiPh components within the same package. This will dramatically increase data transfer density while minimizing inter-chip communication latency and energy consumption.
- Furthermore, Samsung is advancing the development of custom HBM solutions and hybrid bonding techniques. Custom HBM will offer memory performance optimized for specific AI workloads, while hybrid bonding is crucial for achieving ultra-high-density and efficient chip-to-chip connections, enhancing overall package performance and reliability. The convergence of these technologies is expected to significantly boost AI processor capabilities and substantially improve the operational efficiency of AI data centers.

Background & Industry Context: AI Data Centers' New Bottlenecks

The proliferation of generative AI and large language models has led to an explosion in demand for AI data centers. However, this growth is increasingly constrained by physical bottlenecks: limitations in inter-chip data transfer speeds, massive power consumption, and the resulting excessive heat generation. Traditional packaging technologies are proving insufficient to meet these demands, necessitating new solutions that can more intimately integrate diverse components such as HBM, logic, and SiPh. Samsung's "2.xD" stands as a direct response to these challenges, marking a significant step towards elevating AI chip performance to the next frontier.

Strategic Significance & Outlook: Driving AI Infrastructure Efficiency and Sustainability

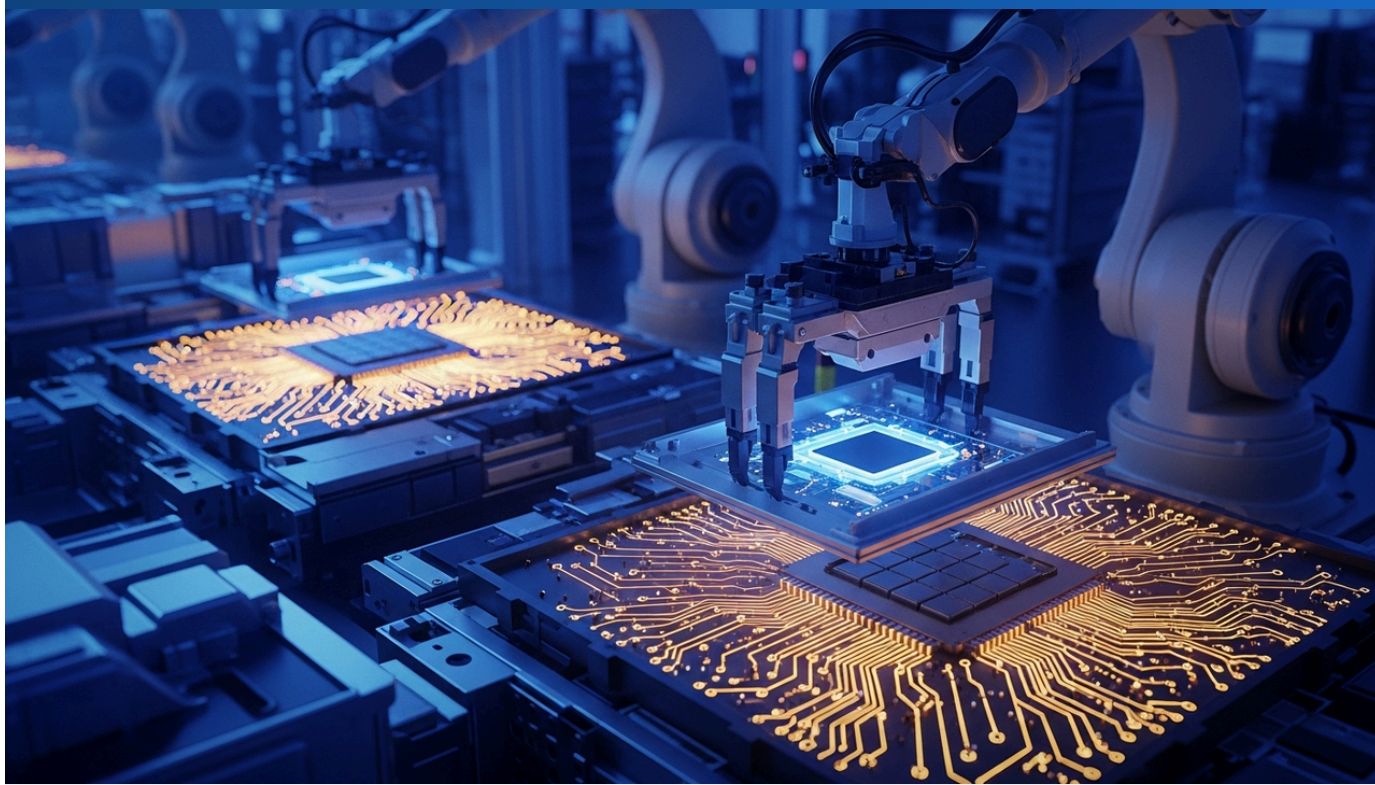
The commercialization of "2.xD" packaging technology is poised to dramatically enhance the energy efficiency of AI data centers, contributing to reduced operational costs. Moreover, its high-speed, low-latency data transfer capabilities will enable the realization of more complex and larger-scale AI models, accelerating the further evolution of AI technology. The integration of silicon photonics, bringing optical communication to the package level, has the potential to break through the limits of electrical interconnections, enabling terabit-scale data transfer rates. This represents a pivotal advancement towards building sustainable AI infrastructure and is expected to further solidify Samsung's leadership in the semiconductor industry.

Source: <https://finance.biggo.com/news/92953789-b58b-4119-9c90-072ce5429b45>

Collected: July 17, 2026 | Automated Research System (Gemini API)

#31 Applied Materials Fortifies AI Advanced Packaging with 10-Year TSMC Pact and NEXX Acquisition

Published July 16, 2026 Simply Wall St News USA



OVERVIEW

Applied Materials significantly expanded its presence in AI advanced packaging by securing a 10-year strategic partnership with TSMC for AI-focused packaging and completing the acquisition of NEXX. These moves, coupled with new DRAM and packaging tool introductions, position Applied Materials to align its equipment roadmap directly with TSMC's multi-year AI infrastructure build-out, securing future tool demand from the world's largest AI foundry.

Key Findings: Applied Materials Positions for AI Packaging Dominance with TSMC Alliance and NEXX Acquisition

Applied Materials is aggressively expanding its footprint in the burgeoning AI advanced packaging market. The company has announced a significant 10-year strategic partnership with industry giant TSMC, specifically focusing on AI packaging technologies. This alliance coincides with Applied Materials' introduction of new DRAM and packaging tools and the completion of its acquisition of NEXX, all part of a concerted effort to bolster its AI-centric product portfolio.

Technical & Business Details: Aligning Roadmaps with Foundry Leaders

- While maintaining its long-term collaboration with EssilorLuxottica on AR/AI glasses, Applied Materials' pivotal strategic move is its alliance with TSMC, the world's largest AI foundry. This decade-long agreement signifies a direct integration of Applied Materials' equipment roadmap with TSMC's multi-year AI infrastructure development plans. This firmly establishes Applied Materials as a primary supplier for TSMC's future advanced packaging equipment needs.
- The acquisition of NEXX enhances Applied Materials' portfolio, particularly in electrochemical deposition (ECD) and electroless plating (ELC) technologies. These capabilities are crucial for achieving the high-density interconnections required in 3D-stacked HBM and other advanced packages, which are fundamental to next-generation AI processors.
- These strategic investments are a direct response to the increasing demand for packaging technologies that enable finer pitches, faster data transfer rates, and superior power efficiency, all essential for maximizing the performance and efficiency of AI processors.

Background & Industry Context: Packaging as the New Frontier in AI Performance

The continuous improvement of AI chip performance is increasingly reliant not just on traditional front-end scaling (smaller transistors) but also on back-end processes, particularly advanced packaging technologies. Solutions like 2.5D/3D packaging that integrate HBM with logic chips, and combinations with silicon photonics, are critical for overcoming data transfer bottlenecks and power consumption challenges. Applied Materials' strategic shifts clearly indicate a pivot in the semiconductor equipment industry's focus from predominantly front-end (wafer fabrication) to significantly emphasizing back-end (packaging) advancements.

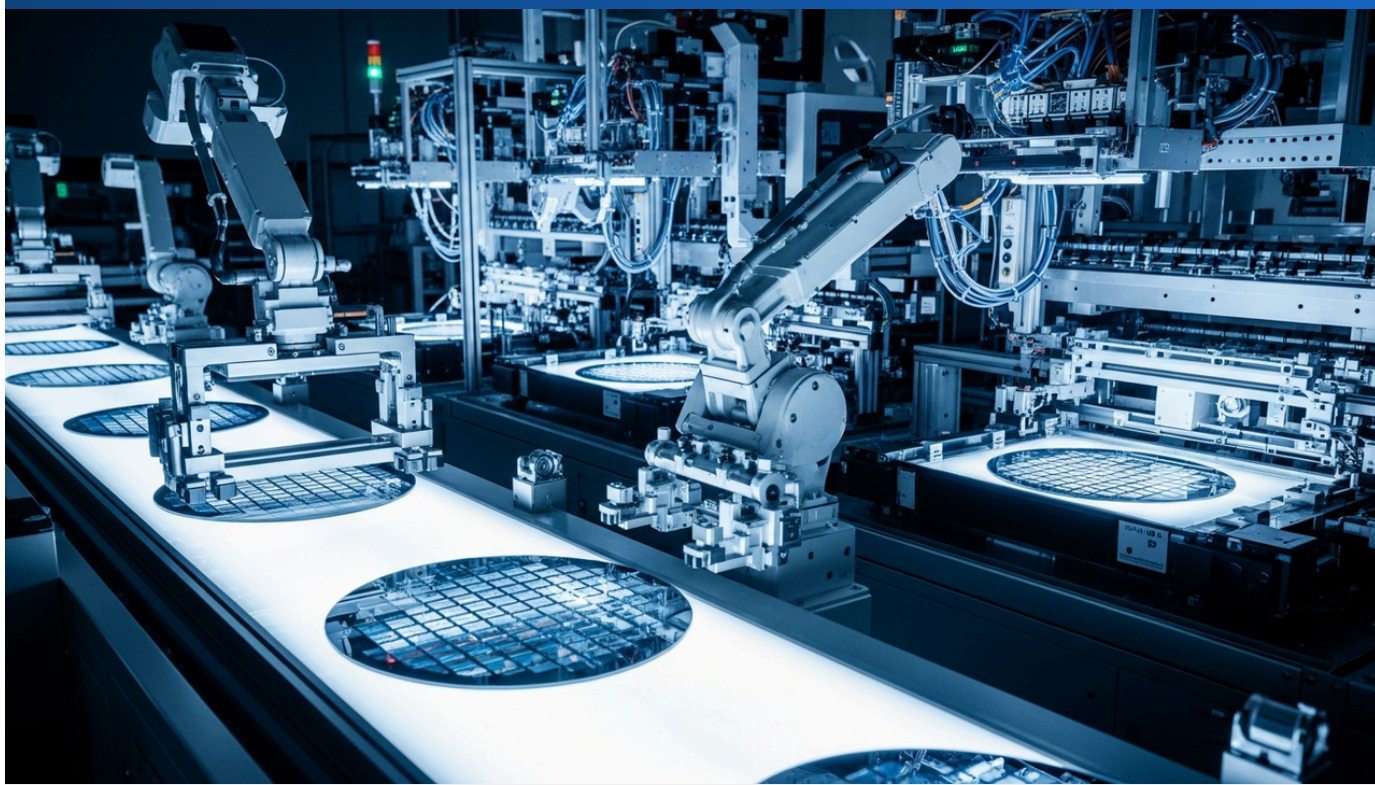
Strategic Significance & Outlook: Capitalizing on the AI Era's Growth

The long-term contract with TSMC assures Applied Materials a stable revenue stream and significant opportunities for technological development in the AI sector. This is paramount as advanced packaging increasingly becomes the bottleneck for AI chip manufacturing, reinforcing the company's market leadership. As investment in AI infrastructure continues to expand globally, Applied Materials is well-positioned to capitalize on this growth trend through its extensive equipment portfolio and strategic partnerships with key customers. Projections indicate that the share of capital expenditure dedicated to advanced packaging within the overall semiconductor industry will significantly increase over the coming years, further fueling Applied Materials' business expansion.

Source: <https://simplywall.st/stocks/us/semiconductors/nasdaq-amat/applied-materials/news/does-applied-materials-expanded-ai-packaging-push-with-tsmc>

#32 Micron Invests \$500M in GlobalWafers Texas Plant, Targets 40% US DRAM Production by 2035

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OVERVIEW

Micron Technology has committed \$500 million to GlobalWafers' Texas wafer plant, aligning with its ambitious goal to manufacture 40% of its DRAM in the United States by 2035, part of a broader \$250 billion US spending initiative. While HBM packaging facilities are underway in Singapore for a 2026 launch, US-based HBM packaging is anticipated to ramp up around 2028, following investments by SK hynix and Amkor Technology in advanced packaging capabilities in Indiana and Arizona, respectively.

Key Findings: Micron Pledges \$500M for US Wafer Plant, Aiming for 40% Domestic DRAM by 2035

Micron Technology has announced a \$500 million investment in GlobalWafers' silicon wafer manufacturing plant currently under construction in Texas. This strategic commitment is a cornerstone of Micron's audacious goal to produce 40% of its DRAM in the United States by 2035, underscoring a significant increase in its overall U.S. spending, which now totals \$250 billion. The move highlights a concerted effort to strengthen domestic semiconductor supply chains.

Technical & Investment Details: Global and Domestic HBM Packaging Strategies

- Micron is concurrently investing heavily in High Bandwidth Memory (HBM) packaging capabilities, critical for high-performance AI chips. A substantial \$7 billion HBM packaging facility is under construction in Singapore, slated to commence operations in 2026. This international expansion addresses the immediate and surging global demand for HBM.
- Domestically, HBM packaging capacity in the U.S. is projected to accelerate around 2028. Competitors such as SK hynix are already proceeding with plans for a 2.5D advanced packaging plant in Indiana, and Amkor Technology is expanding its Arizona campus with a \$7 billion investment, targeting production commencement in early 2028. These initiatives are significantly influenced by U.S. government incentives, such as the CHIPS Act, fostering a resurgence in domestic semiconductor manufacturing.
- The investment in GlobalWafers aims to bolster vertical integration within the U.S. semiconductor ecosystem, from upstream wafer supply to downstream packaging, thereby enhancing supply chain resilience.

Background & Industry Context: Geopolitical Imperatives and Supply Chain Reshaping

The semiconductor industry has recently experienced heightened geopolitical tensions and supply chain disruptions, notably during the COVID-19 pandemic. In response, governments worldwide are aggressively promoting the strengthening of domestic semiconductor manufacturing capabilities. The U.S. CHIPS Act is a prime example, offering substantial subsidies and tax incentives to chip manufacturers for domestic facility investments. Micron's announcement aligns with these global trends and policy incentives, aiming to secure its competitive edge in memory and packaging technologies, which are gaining increasing importance in the era of AI.

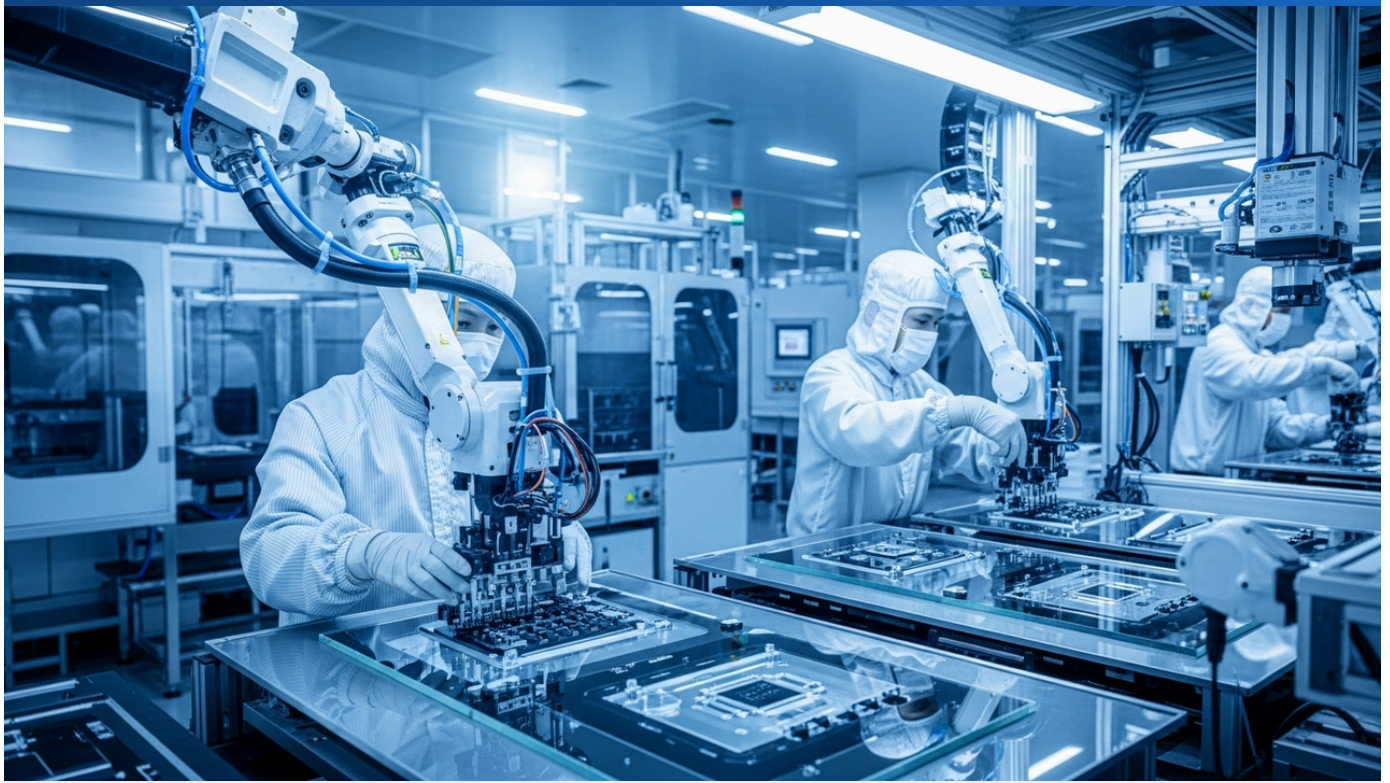
Strategic Significance & Outlook: Fortifying the US Ecosystem and Future Competitiveness

Micron's substantial investment is expected to invigorate the entire U.S. semiconductor ecosystem, fostering future innovation and job creation. The target of producing 40% of its DRAM domestically by 2035 presents new challenges in terms of manufacturing costs, technology transfer, and supply chain management. Still, it also promises significant benefits, including a more stable supply network and insulation from geopolitical risks. Establishing domestic HBM packaging capabilities is paramount for enhancing U.S. competitiveness in the AI semiconductor sector, with Micron emerging as a key player alongside SK hynix and Amkor in this crucial strategic shift.

Source: <https://www.tomshardware.com/tech-industry/semiconductors/micron-commits-500-million-to-globalwafers-texas-wafer-plant-as-it-raises-us-spending-to-250-billion>

#33 Samsung Electro-Mechanics Challenges Ibiden in AI Server Package Substrates with FC-BGA and Glass Substrate Push

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OVERVIEW

Samsung Electro-Mechanics is aggressively challenging Ibiden's dominant market share in AI package substrates by enhancing its Flip-Chip Ball Grid Array (FC-BGA) and next-generation glass substrate technologies for AI servers, leveraging its expertise in embedded component solutions. Ibiden, in response to surging AI demand, plans to invest 500 billion yen (approximately \$3.4 billion) by 2028 to expand its IC package substrate capacity. This sets the stage for intensified technological competition between the two industry leaders.

Key Findings: Samsung Electro-Mechanics Intensifies Challenge to Ibiden in AI Substrate Market

Samsung Electro-Mechanics is making aggressive inroads into the package substrate market, a critical determinant of AI semiconductor performance, directly challenging the long-standing dominance of Japan's Ibiden. Samsung Electro-Mechanics is primarily focusing on bolstering its Flip-Chip Ball Grid Array (FC-BGA) offerings for AI servers and accelerating the development and mass production capabilities for revolutionary next-generation glass substrate technologies.

Technical & Market Details: Embedded Technologies and Massive Investment Race

- Samsung Electro-Mechanics possesses a unique strength in "embedding" technology, which involves integrating passive components such as Multi-Layer Ceramic Capacitors (MLCCs) and silicon capacitors directly within the substrate for high-end AI server applications. This technique significantly enhances power delivery stability and improves signal integrity, thereby contributing to the higher performance of AI chips.
- Meanwhile, Ibiden, the current market leader, is also pursuing an aggressive investment strategy to meet the escalating AI demand. The company has announced plans to invest a colossal 500 billion yen (approximately \$3.4 billion USD) by 2028 to substantially expand its production capacity for AI server IC package substrates, aiming to secure a stable supply of high-density and reliable substrates.
- Glass substrates, emerging as a prominent next-generation technology, offer significant advantages over traditional organic substrates, including the potential for larger sizes, superior thermal stability, and enabling finer wiring patterns. This technology is key to further enhancing the integration density and performance of AI chips, and both companies are vying for leadership in this critical area.

Background & Industry Context: Intensified Back-End Competition in the AI Era

As semiconductor miniaturization approaches its physical limits, the "back-end" processes, particularly package substrates that handle inter-chip connections, have seen their importance skyrocket in driving AI chip performance. AI processors provide complex circuit designs for massive data processing and integration with HBM, making high-performance package substrates indispensable for realizing their full potential. Against this backdrop, competition among leading suppliers for advanced technologies like FC-BGA and glass substrates is expected to intensify further.

Strategic Significance & Outlook: Market Reshaping and Accelerated Innovation

The fierce competition between Samsung Electro-Mechanics and Ibiden is poised to accelerate technological innovation across the entire AI semiconductor market. Samsung's embedded technology paves the way for smaller, more efficient packaging solutions, while Ibiden's scale expansion strategy contributes to stabilizing supply to meet AI demand. In the long term, glass substrate technology holds the potential to become the next-generation platform, replacing current organic substrates, making technological leadership in this domain a decisive factor for future market share. The investments and technological rivalry between these two companies unequivocally underscore the growing importance of back-end processes in the AI-driven semiconductor industry.

Source: <https://www.mk.co.kr/en/business/12101116>