

Semiconductor_BackEnd

Weekly Intelligence Report

2026-08-02 | 13 articles | 6 countries

troy-technical.jp

This Week's Keyword

AI Advanced Packaging

Capacity surge & supply chain shifts

13

articles

Total Articles Analyzed

6

countries

Source Countries

128.8

%

Besi Hybrid Bonding Growth

29

%

ABF Substrate Shortage by 2028

All 13 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	Besi Record Hybrid Bonding	Corporate Strategy						Besi reports record Q2 2026 orders, 128.8% growth in hybrid bonding driven by AI demand.
#02	Malaysia HBM4 Investment	Corporate Strategy						Malaysia invests \$45M in advanced packaging, targeting HBM4 PoC within two years to boost domestic capabilities.
#03	Intel EMIB vs TSMC CoWoS	Technology Comparison						Intel's EMIB gains traction with Google; TSMC develops similar tech amidst CoWoS capacity constraints.
#04	ASE Ups 2026 Capex	Corporate Strategy						ASE Technology increases 2026 capex to \$10.5B, driven by surging AI packaging demand for LEAP capabilities.
#05	ABF Substrate Shortage	Market Analysis						HBM integration in AI chips to cause 29% ABF substrate shortage by 2028 despite \$19.1B expansion plans.
#06	Intel US AI Packaging	Corporate Strategy						Intel accelerates next-gen AI semiconductor development in US fabs using Foveros and enhanced EMIB-T packaging.
#07	SEMICON West to Phoenix	Industry Event						SEMICON West relocates to Phoenix, Arizona, solidifying the state as a major US semiconductor hub with TSMC's \$100B fab plans.
#08	2.5D Pkg & HBM Accel.	Technology Comparison						TSMC CoWoS and Samsung I-CubeS drive HBM-integrated 2.5D packaging, expanding reticle sizes for AI accelerators.
#09	TSMC CoPoS Glass Sub.	Research						TSMC pilots CoPoS with 310x310mm glass substrates, aiming for 2028-2029 mass production to overcome CoWoS bottlenecks.
#10	Amkor AZ Fab & SiP Shift	Corporate Strategy						Amkor builds \$7B advanced packaging fab in Arizona (2028), shifting Korean SiP production to Vietnam for AI focus.
#11	ASE Ups Capex & FOPLP	Corporate Strategy						ASE raises 2026 capex to \$10.5B, targets doubling LEAP revenue by 2027, with FOPLP mass production in Q1 2027.
#12	SiC Power Module Pkg	Research						Advanced packaging for SiC power modules (AMB, embedded die) improves thermal management for EV/AI data centers.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#13	ASMPT Record AP Sales	Corporate Strategy						ASMPT's Advanced Packaging business achieves record H1 2026 sales, driven by AI demand and strategic push for PLP.

High Med-High Med Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI supply chain exposed to ABF substrate shortages?

The projected 29% ABF substrate deficit by 2028, driven by HBM integration in AI chips, poses a critical bottleneck. US/EU procurement must assess supplier resilience and explore alternative materials or packaging designs now.

❷ How will Intel's EMIB-T and TSMC's CoPoS reshape AI packaging?

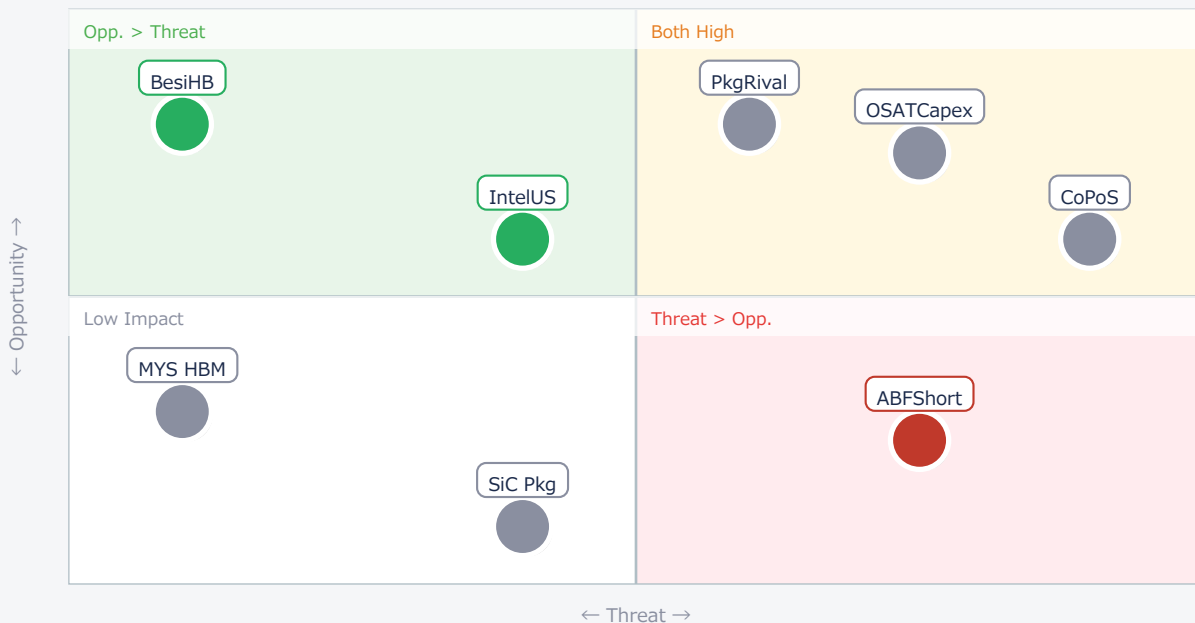
Intel's EMIB-T is gaining traction with Google, while TSMC's CoPoS (2028-2029 mass production) aims to break CoWoS bottlenecks. US/EU OEMs must evaluate which platform offers the best long-term performance, cost, and supply security for next-gen AI accelerators.

❸ Are your advanced packaging investments competitive globally?

Asian OSATs like ASE are pouring billions into LEAP and FOPLP, while Malaysia targets HBM4. US/EU companies must ensure their R&D; and manufacturing strategies match this pace to avoid falling behind in critical AI packaging capabilities.

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
● BesiHB	Opp.	EU supplier gains	—
● IntelUS	Opp.	US domestic capacity	—
● PkgRival	Critical	Diverse tech options	Intense competition
● CoPoS	Critical	Future capacity	New tech disruption
● OSATCapex	Critical	Increased capacity	Bottleneck persists
● ABFShort	Threat	—	Supply chain risk
● MYS HBM	Ref.	Supply chain diversity	Emerging competition

● SiC Pkg	Ref.	Niche market growth	—
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Deep Dive ① — Besi's Hybrid Bonding Dominance in AI

#01 | 2026/07/23 | ET Electronics News | Tech Novelty●●●○○ Proximity●●●●● Market Impact●●●●○ Data Reliability●●●●○ US/EU Relevance●●●●●

Dutch equipment maker Besi achieved record €292.9M orders in Q2 2026, a 128.8% YoY increase, driven by surging AI demand and its hybrid bonding technology. Customer base expanded from 15 to 21, underscoring broad industry adoption.

Hybrid bonding offers superior density, performance, and power efficiency for advanced packaging (HBM, logic, CPO), crucial for AI accelerators. Besi's strong performance solidifies its role as a key enabler for high-performance computing.

► Strategic Analyst's Perspective

Strategic Analyst's Perspective: Besi's reported growth is realistic, reflecting the critical need for advanced packaging in AI. The primary technical barrier is scaling hybrid bonding for even larger, more complex chiplet designs and ensuring yield. [Opportunity] for US/EU OEMs to leverage Besi's mature hybrid bonding solutions for next-gen AI products, gaining performance and power efficiency. [Threat] for competing equipment suppliers who lag in hybrid bonding technology. Next actions: [Procurement] Evaluate Besi's hybrid bonding roadmap and capacity for 2027-2028 AI projects. [R&D;] Investigate integration challenges and design-for-hybrid-bonding principles.

Deep Dive ② — Intel's US-Based Advanced Packaging Push

#06 | 2026/07/29 | Intel | Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●○ Data Reliability●●●●○ US/EU Relevance●●●●●

Intel is aggressively advancing next-gen AI semiconductor development in its US fabs using Foveros stacking, EMIB silicon bridges, and enhanced EMIB-T packaging. EMIB-T integrates power delivery channels (TSVs) directly within the bridge.

This innovation significantly boosts power delivery efficiency and optimizes signal routing, crucial for HBM technology and heterogeneous integration. This strengthens the US semiconductor supply chain and Intel's leadership in AI/HPC.

► Strategic Analyst's Perspective

Strategic Analyst's Perspective: Intel's focus on US-based advanced packaging, particularly EMIB-T, is a realistic and strategic move aligned with national security and supply chain resilience. Technical barriers include scaling EMIB-T for ultra-large dies and ensuring cost-competitiveness against Asian foundries. [Opportunity] for US/EU OEMs to secure high-performance AI chips with a robust, geographically diversified supply chain. [Threat] for non-US/EU foundries and OSATs if Intel's domestic capabilities become a preferred option for US customers. Next actions: [Strategy] Assess Intel's foundry roadmap for advanced packaging and its implications for long-term sourcing. [R&D;] Explore co-design opportunities with Intel for future AI platforms.

Deep Dive ③ — Intel vs. TSMC: The AI Packaging Battle

#03 | 2026/07/31 | Benzinga | Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●○ Data Reliability●●●○○ US/EU Relevance●●●●●

Intel's EMIB technology is gaining a significant edge in AI packaging, notably with Google adopting EMIB-T for its 9th-gen TPUs. This puts pressure on TSMC, whose CoWoS capacity is fully booked until 2025.

TSMC is reportedly developing an EMIB-like solution and plans to integrate 10 compute dies and 20 HBM stacks in a 14-reticle package by 2028. This intensifies the advanced packaging arms race for AI chips.

► Strategic Analyst's Perspective

Strategic Analyst's Perspective: The Intel-TSMC packaging rivalry is very real and will drive rapid innovation. Google's adoption of EMIB-T validates Intel's approach. TSMC's ambitious 2028 plans are technically challenging but achievable given their track record. [Opportunity] for US/EU OEMs to benefit from diverse, high-performance packaging options and competitive pricing. [Threat] for companies locked into a single packaging vendor, risking capacity constraints or slower innovation. Next actions: [Procurement] Diversify advanced packaging sourcing strategies. [R&D;] Monitor both Intel's and TSMC's packaging roadmaps to inform future chip architectures and design choices.

Other Notable Articles

AI Chip HBM Integration to Drive 29% ABF Substrate Shortage by 2028 (Taiwan)

Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●●

Critical supply chain bottleneck for AI chips; assess your ABF substrate exposure and supplier diversification.

SEMICON West Relocates to Phoenix, Arizona, Bolstering U.S. Semiconductor Hub (USA)

Tech Novelty●○○○○ Proximity●●●●● Market Impact●●●○○

Phoenix is rapidly becoming a major US semiconductor hub; consider regional presence and talent acquisition strategies.

ASE Technology、2026年設備投資を過去最高の105億ドルに増額、先進パッケージング事業の2027年倍増を目指す (Taiwan)

Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●○

ASE's massive capex and FOPLP plans highlight the scale of investment needed for AI packaging; expect capacity relief by 2027.

ASMPT's Advanced Packaging Business Achieves Record Sales in H1 2026, Driven by Surging AI Demand (Singapore)

Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●○

ASMPT's record sales and PLP push confirm strong market demand for advanced packaging equipment; evaluate their PLP readiness.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

■ Immediate (this week)

- [Procurement] Conduct an urgent risk assessment of ABF substrate supply chain exposure for all AI/HPC product lines.
- [Strategy] Initiate competitive analysis of Intel's EMIB-T vs. TSMC's CoWoS/CoPoS for next-gen AI packaging roadmaps.
- [Executive] Review current advanced packaging investment strategy against global OSAT capex and regional initiatives.

■ Short-term (1 month)

- [R&D;] Evaluate the technical feasibility and cost-benefit of integrating hybrid bonding solutions (e.g., Bési's) into future product designs.
- [Business Dev] Explore potential partnerships or joint ventures with advanced packaging equipment suppliers and OSATs to secure future capacity.
- [Procurement] Begin discussions with ABF substrate suppliers on long-term supply agreements and explore alternative material qualifications.

■ Medium-long term (quarter+)

- [Strategy] Develop a multi-year advanced packaging manufacturing strategy, considering domestic (US/EU) capacity expansion and global diversification.
- [Legal/IP] Review intellectual property landscape in panel-level packaging (PLP) and glass substrates, identifying potential licensing opportunities or threats.
- [R&D;] Invest in internal capabilities for advanced packaging design, simulation, and characterization to reduce reliance on external expertise.

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Semiconductor_BackEnd — Selected Articles

Date: 2026-08-02

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#01 Besi Achieves Record €292.9M Orders in Q2 2026, Driven by AI Demand and 128.8% Growth in Hybrid Bonding Technology

Published July 23, 2026 ET Electronics News Netherlands



OVERVIEW

BE Semiconductor Industries (Besi) reported record Q2 2026 orders of €292.9 million, a 128.8% increase year-over-year, primarily fueled by robust AI-related demand and the surging adoption of its hybrid bonding technology. Net profit reached €89 million on €249.9 million in revenue, while its hybrid bonding customer base expanded from 15 to 21 companies. This strong performance underscores Besi's critical role in enabling advanced semiconductor packaging solutions for high-performance computing and AI applications.

Key Findings

Dutch semiconductor equipment manufacturer BE Semiconductor Industries (Besi) achieved a record €292.9 million in orders during the second quarter of 2026, representing a remarkable 128.8% increase year-over-year. This unprecedented growth was predominantly driven by the escalating demand for artificial intelligence (AI) related applications and the accelerating adoption of Besi's advanced hybrid bonding technology.

Technical and Business Details

Besi's success is largely attributed to its pioneering work in hybrid bonding, a crucial next-generation semiconductor packaging technique. The number of customers utilizing Besi's hybrid bonding solutions grew significantly from 15 to 21 within a year, indicating broad industry acceptance. Hybrid bonding offers superior density, performance, and power efficiency compared to traditional wire or flip-chip bonding by directly joining individual dies. This makes it ideal for diverse applications, including high-performance logic, advanced memory (such as HBM), co-packaged optics (CPO), and consumer electronics. For Q2 2026, the company reported a revenue of €249.9 million and a net profit of €89 million, demonstrating year-over-year increases of 32.0% and 58.0%, respectively.

Background and Industry Context

The semiconductor industry is experiencing a transformative period, largely propelled by the exponential expansion of AI, data centers, and high-performance computing (HPC). These segments demand increasingly integrated, power-efficient, and high-bandwidth chip solutions, making advanced packaging technologies like hybrid bonding indispensable. Besi's technology is a key enabler for achieving the necessary levels of integration and performance for complex chiplet architectures and advanced HBM stacks, which are at the heart of modern AI accelerators.

Strategic Significance and Outlook

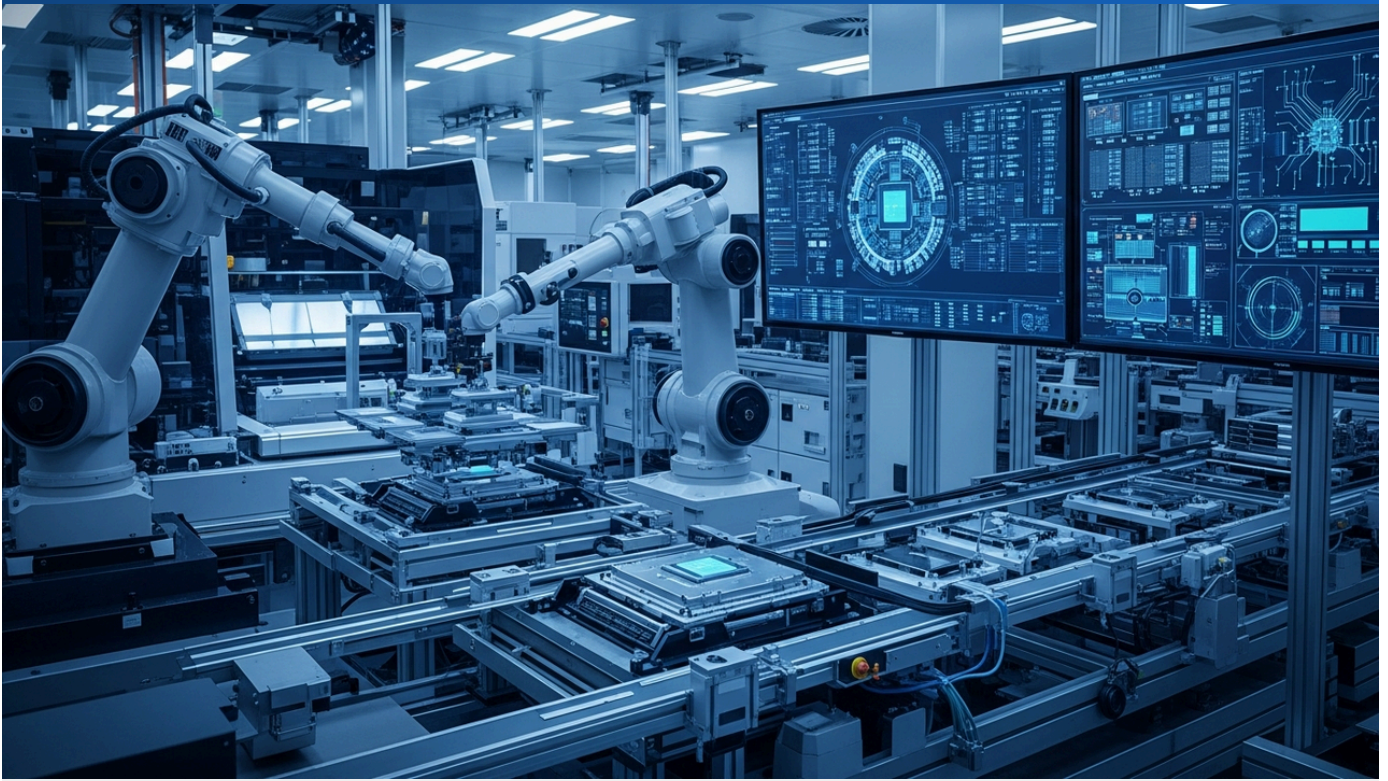
Besi plans to continue its aggressive research and development investments in hybrid bonding to further expand its customer base and market penetration. As the AI market continues its rapid ascent, Besi's technologies are poised to play a pivotal role in enhancing semiconductor performance and cost-efficiency, thereby accelerating innovation across the industry. The company's robust order book and technological leadership position it for sustained growth in the foreseeable future, solidifying its status as a critical enabler of the AI revolution.

Source: <https://electronics.economictimes.indiatimes.com/news/semiconductors/besi-reports-record-orders-driven-by-ai-and-hybrid-bonding-technology/132575561>

Collected: July 31, 2026 | Automated Research System (Gemini API)

#02 Malaysia Invests US\$45 Million to Propel Advanced Chip Packaging, Targeting HBM4 Domestic Proof-of-Concept

Published July 30, 2026 Asia News Network Malaysia



OVERVIEW

Malaysia announced a 185 million ringgit (approx. US\$45 million) investment into semiconductor projects to boost its advanced chip packaging capabilities for AI, data centers, and high-performance computing. The Malaysia Advanced Packaging Consortium (MAPC), involving five local companies, aims to commercialize a domestic proof-of-concept for HBM4 test chips within two years. This strategic move solidifies Malaysia's role as a high-value back-end hub in the global semiconductor supply chain, reducing external dependency.

Key Findings

The Malaysian government has unveiled a significant investment plan of 185 million ringgit (approximately US\$45 million) to substantially enhance its domestic advanced chip packaging capabilities. This strategic funding is directed towards accelerating the manufacturing of next-generation semiconductors essential for artificial intelligence (AI), data centers, and high-performance computing (HPC) applications.

Technical and Business Details

At the core of this initiative is the Malaysia Advanced Packaging Consortium (MAPC), spearheaded by the Ministry of Science, Technology and Innovation. The MAPC brings together five leading local companies with the ambitious goal of developing a domestic proof-of-concept (PoC) for HBM4 test chips, representing the next standard in High Bandwidth Memory. The project aims to commercialize these advanced packaging technologies within a two-year timeframe, positioning Malaysia as a critical back-end hub for AI chip manufacturing. This effort is particularly crucial as demand for highly integrated and high-performance semiconductor products continues to surge globally.

Background and Industry Context

As Moore's Law faces increasing physical limits, advancements in chip performance are increasingly reliant on innovative advanced packaging technologies rather than just miniaturization. The explosive growth of AI applications, in particular, has driven a sharp increase in demand for high-density packaging solutions like 2.5D/3D stacking and chiplets. Malaysia has long been a global leader in the Outsourced Semiconductor Assembly and Test (OSAT) sector. This new investment signifies an accelerated shift towards higher-value advanced packaging, further elevating Malaysia's strategic importance within the global semiconductor supply chain.

Strategic Significance and Outlook

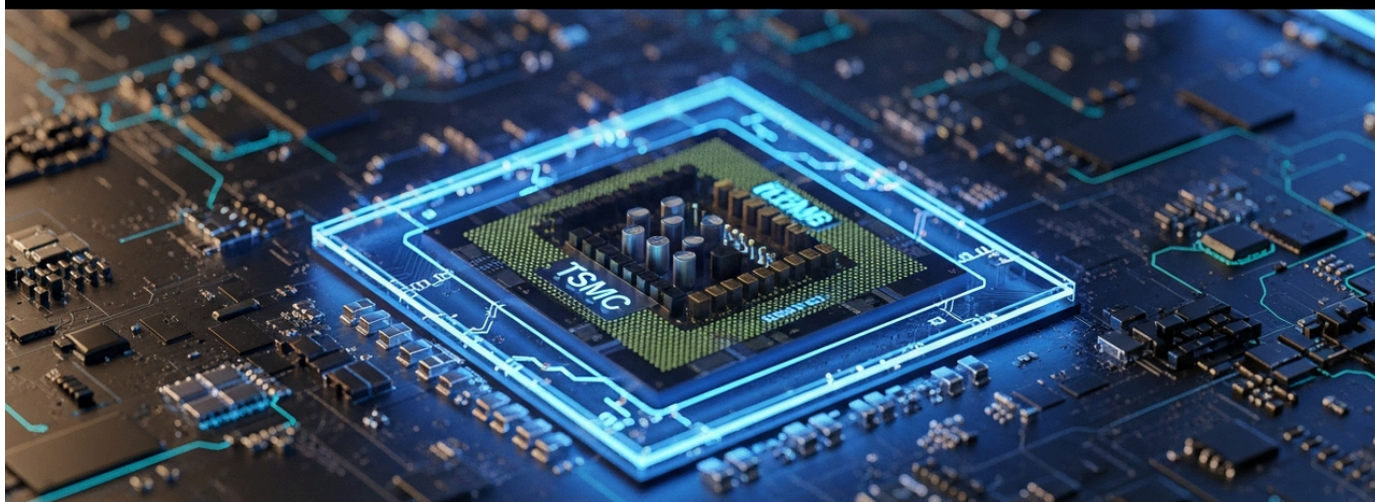
This Malaysian investment is not only about bolstering domestic industry but also contributes significantly to the resilience and diversification of the global semiconductor supply chain. Localizing cutting-edge technologies like HBM4 can mitigate supply risks and stimulate the regional innovation ecosystem. If successful, this initiative will establish Malaysia as a prominent global center for advanced semiconductor packaging in the age of AI.

Source: <https://asianews.network/malaysia-invests-over-us45mil-to-drive-advanced-chip-packaging/>

Collected: July 31, 2026 | Automated Research System (Gemini API)

#03 Intel's EMIB Dominates AI Packaging with Google Adoption, Prompting TSMC to Develop Similar Tech Amidst CoWoS Constraints

Published July 31, 2026 Benzinga USA



OVERVIEW

Intel's EMIB technology is establishing a significant competitive advantage in advanced chip packaging for AI workloads, exemplified by Google's adoption of EMIB-T in its 9th-generation TPUs. Facing CoWoS capacity fully booked until 2025, TSMC is reportedly developing an EMIB-like packaging solution and plans to integrate 10 large compute dies and 20 HBM stacks in a 14-reticle package by 2028. This intensifying competition highlights the critical demand for diverse high-density integration solutions in the rapidly evolving AI chip market.

Key Findings

Intel's Embedded Multi-die Interconnect Bridge (EMIB) technology is demonstrating a clear competitive edge in the advanced chip packaging market, particularly for AI workloads. In response to its CoWoS capacity being fully booked until 2025, TSMC is reportedly developing a packaging technology similar to Intel's EMIB, intensifying the advanced packaging arms race within the AI semiconductor industry.

Technical and Business Details

Intel's EMIB facilitates high-density interconnection of multiple dies (chipselets), potentially manufactured on different process nodes, through a silicon bridge. This architecture delivers high bandwidth, low latency, and superior power efficiency, enabling the creation of complex System-on-Packages (SoPs) vital for AI accelerators and high-performance CPUs. Google has adopted the enhanced EMIB-T packaging for its 9th-generation TPUs, which improves power delivery and signal routing by integrating channels directly into the bridge. Other major clients, including Amazon, Cisco, SpaceX, and Tesla, also leverage Intel's packaging solutions. Meanwhile, TSMC's popular CoWoS (Chip-on-Wafer-on-Substrate) technology faces significant demand-supply imbalances, with production capacity fully reserved until 2025. To address these constraints and maintain its market position, TSMC is rumored to be developing an EMIB-like packaging solution. Furthermore, TSMC has unveiled ambitious plans to integrate 10 large compute dies with 20 High Bandwidth Memory (HBM) stacks within a 14-reticle package by 2028, signaling its intent to develop ultra-high-density packaging capabilities that rival or surpass current offerings.

Background and Industry Context

The rapid evolution of AI is driving a paradigm shift in semiconductor design and manufacturing. The limitations of monolithic dies—in terms of cost, yield, and design complexity—have made advanced packaging of multiple smaller dies (chipselets) crucial for achieving performance gains and cost efficiencies. The competition between Intel and TSMC signifies not just a technological rivalry but a strategic battle for dominance in the next-generation AI infrastructure. The fact that companies like MediaTek are committing to support both TSMC CoWoS and Intel EMIB underscores the industry's need for diverse and robust advanced packaging options.

Strategic Significance and Outlook

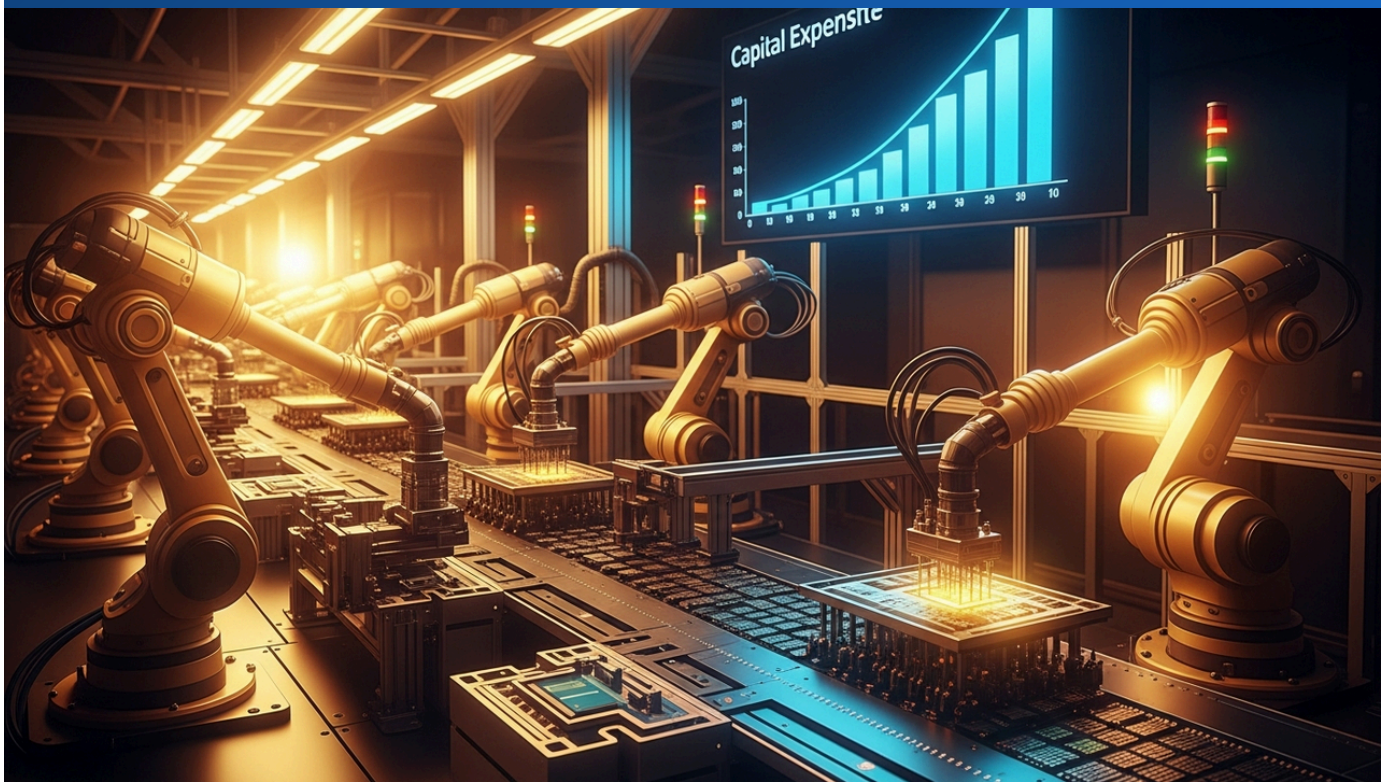
Advanced packaging will remain a primary area of innovation in the semiconductor industry for years to come. The fierce competition between Intel and TSMC, and their respective efforts to leverage or emulate advanced technologies, is expected to drive significant improvements in AI chip performance. This rivalry will spur the development of more innovative and efficient packaging solutions, accelerating the growth and capabilities of critical markets such as AI, HPC, and data centers. Enhancements in power efficiency and integration density will be key determinants of future AI accelerator performance.

Source: <https://www.benzinga.com/markets/tech/26/07/60829355/tsmc-is-reportedly-developing-advanced-chip-packaging-tech-to-challenge-intels-dominance>

Collected: July 31, 2026 | Automated Research System (Gemini API)

#04 ASE Technology Ups 2026 Capex to Record \$10.5 Billion, a 23.5% Increase, Driven by Surging AI Packaging Demand

Published July 31, 2026 Digitimes Taiwan



OVERVIEW

ASE Technology Holding, the world's largest semiconductor packaging and test provider, increased its 2026 capital expenditure plan by 23.5% to a record \$10.5 billion from an initial \$8.5 billion, responding to soaring demand for AI-related advanced packaging. The majority of this additional investment is targeted at expanding its LEAP (Leading-edge Advanced Packaging) capabilities and other mainstream advanced packaging and testing capacity. LEAP revenues are projected to exceed \$3.5 billion in 2026 and double in 2027, signaling ASE's strategic commitment to addressing critical bottlenecks in high-performance semiconductor manufacturing for the AI era.

Key Findings

ASE Technology Holding, the world's largest provider of semiconductor packaging and test services, has significantly revised its 2026 capital expenditure plan upwards, raising it to a record \$10.5 billion. This represents a 23.5% increase from the initial \$8.5 billion projection and marks the third such upward adjustment this year, driven by the escalating demand for advanced packaging, particularly in the artificial intelligence (AI) sector.

Technical and Business Details

The bulk of this unprecedented capital injection will be allocated to expanding ASE's "LEAP" (Leading-edge Advanced Packaging) capabilities. Specifically, out of the additional \$2 billion, approximately \$1 billion is earmarked for new facilities and the remaining \$1 billion for advanced equipment. LEAP technologies encompass next-generation high-density integration techniques such as chiplets, 2.5D/3D stacking, and hybrid bonding, which are crucial for meeting the complex requirements of AI chips and high-performance computing (HPC) semiconductors. ASE projects its LEAP business revenue to exceed \$3.5 billion in 2026 and anticipates a doubling of this revenue in 2027. This forecast underscores the industry's increasing reliance on packaging advancements for performance gains in AI chips and solidifies ASE's leadership in this pivotal domain.

Background and Industry Context

The semiconductor industry is currently navigating an unprecedented surge in demand for AI chips, with advanced packaging emerging as a critical bottleneck. Graphic Processing Units (GPUs) and AI accelerators demand high-bandwidth memory (HBM) integration and efficient multi-die connectivity, making sophisticated packaging solutions indispensable. The fact that TSMC's CoWoS packaging technology is reportedly booked out for several years highlights the severe capacity crunch. ASE's substantial investment is therefore crucial in alleviating this bottleneck and supporting the semiconductor supply chain in the AI era.

Strategic Significance and Outlook

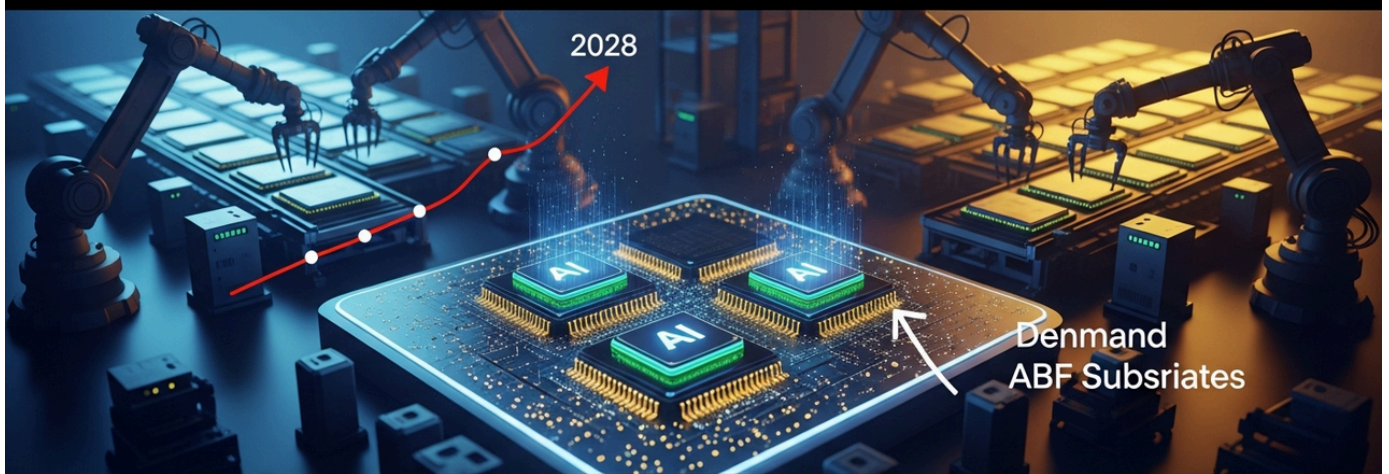
ASE's aggressive capital expenditure signals the continuing and increasing importance of advanced packaging in the global semiconductor industry. By expanding its LEAP capabilities, ASE will enable customers to bring higher-performance, more power-efficient AI chips to market faster. This directly translates into accelerating AI innovation, improving data center efficiency, and enabling new high-performance computing applications. ASE's strategy is not just about market share expansion but about providing foundational technology that underpins the entire AI revolution, significantly impacting the industry as a whole.

Source: <https://www.digitimes.com/news/a20260731PD223/ase-2026-data-revenue-2027.html>

Collected: July 31, 2026 | Automated Research System (Gemini API)

#05 AI Chip HBM Integration to Drive 29% ABF Substrate Shortage by 2028; \$19.1B Expansion Unlikely to Offer Short-Term Relief

Published July 26, 2026 [不明] Taiwan



OVERVIEW

The rapid integration of High Bandwidth Memory (HBM) into AI chips is set to drive a 39% Compound Annual Growth Rate (CAGR) in ABF substrate demand between 2025 and 2028. This surge is projected to create a supply deficit by 2027, potentially reaching a critical 29% gap by 2028. While leading manufacturers have committed \$19.1 billion to capacity expansion, these investments are unlikely to offer immediate relief, threatening to bottleneck next-generation AI and high-performance computing development and pushing up prices for key suppliers.

Background

As the traditional scaling benefits of Moore's Law diminish, advanced packaging technologies have emerged as a critical frontier for enhancing semiconductor performance. In the rapidly evolving sectors of Artificial Intelligence (AI) and High-Performance Computing (HPC), the proliferation of chiplet architectures and heterogeneous integration necessitates increasingly complex and larger packages. Ajinomoto Build-up Film (ABF) substrates are indispensable components in these advanced systems, serving as the foundation for flip-chip ball grid array (FCBGA) packages used in high-performance CPUs, GPUs, and AI accelerators. While ABF substrate shortages have occurred during previous industry booms, the current AI revolution is driving demand at an unprecedented scale and pace, profoundly impacting the entire semiconductor supply chain.

Key Findings

The demand for ABF substrates is projected to surge dramatically, with a Compound Annual Growth Rate (CAGR) of 39% from 2025 to 2028. This accelerated growth is primarily driven by the intensified integration of High Bandwidth Memory (HBM) into AI chips. The trend towards integrating more HBM stacks, coupled with the widespread adoption of 2.5D/3D packaging techniques, necessitates significantly larger and higher-layer-count ABF substrates. For example, AI server chips frequently incorporate 8 to 12 HBMs per GPU, escalating the physical size and complexity requirements for their underlying ABF substrates.

This rapid demand increase is expected to lead to a significant supply deficit, commencing as early as 2027 and potentially expanding to a critical 29% gap by 2028. In response to this robust demand, leading global substrate manufacturers, including Unimicron, Nan Ya PCB, and Kinsus, have initiated substantial expansion plans totaling \$19.1 billion. However, due to lengthy lead times for manufacturing equipment installation and the subsequent production ramp-up, these significant investments are not expected to fully alleviate the imminent short-term supply crunch.

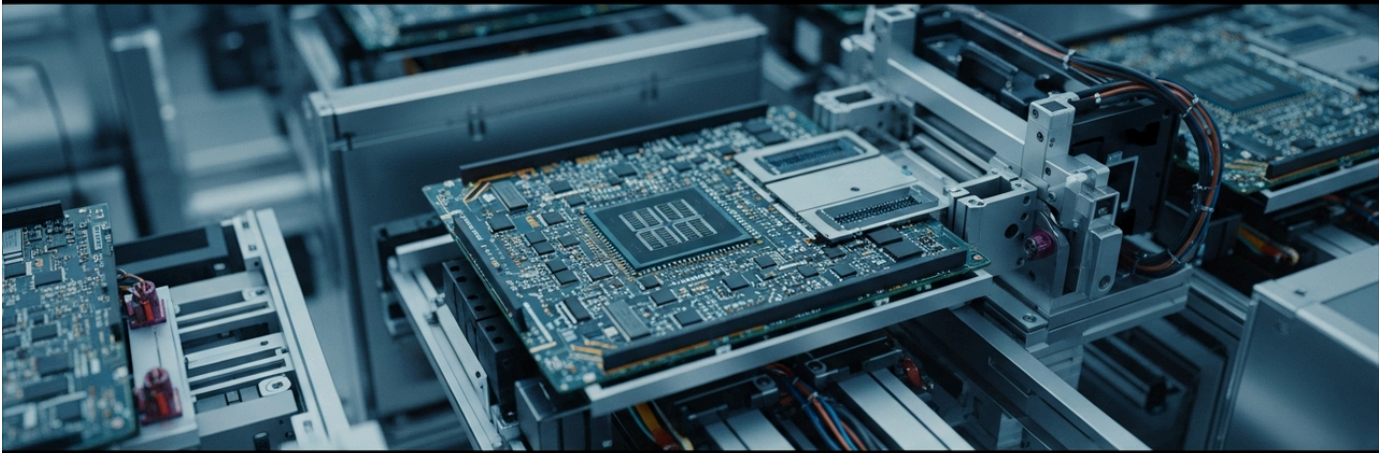
The looming ABF substrate shortage poses a significant bottleneck for semiconductor manufacturers aiming to bring next-generation AI and HPC products to market, directly impacting AI chip production schedules and potentially limiting the overall growth rate of the AI industry. While presenting a considerable business opportunity for ABF substrate manufacturers, this situation also underscores the urgent need for manufacturing technology innovation and supply chain strengthening. Long-term solutions will require not only continuous capacity expansion but also advancements in material science and the development of alternative substrate technologies. This supply deficit is poised to remain a critical concern for the semiconductor industry for the foreseeable future.

Source: <https://finance.biggo.com/news/4978b0ef-fc31-4d7d-9de1-c14abbafc97b>

Collected: July 31, 2026 | Automated Research System (Gemini API)

#06 Intel Accelerates Next-Gen AI Semiconductor Development in U.S. Fabs with Foveros and Enhanced EMIB-T Packaging

Published July 29, 2026 Intel USA



OVERVIEW

Intel is aggressively advancing next-generation AI semiconductor development in its U.S. fabs by leveraging cutting-edge advanced packaging technologies such as Foveros stacking, EMIB silicon bridges, and particularly EMIB-T. EMIB-T significantly improves power efficiency and signal routing by integrating power delivery channels directly within the bridge, specifically addressing the stringent requirements of HBM technology. This initiative strengthens the U.S. semiconductor supply chain and solidifies Intel's technological leadership in enabling high-performance computing for the AI era.

Key Findings

Intel is accelerating the development of next-generation AI semiconductors by utilizing its state-of-the-art U.S. fabrication facilities to advance innovative packaging technologies, including Foveros stacking, EMIB silicon bridges, and the enhanced EMIB-T. This strategic focus aims to deliver AI accelerators that achieve both high performance and superior power efficiency.

Technical and Business Details

At the core of Intel's advanced packaging strategy are Foveros, which enables vertical stacking of multiple dies, and EMIB (Embedded Multi-die Interconnect Bridge), facilitating horizontal connectivity between dies. EMIB-T (EMIB with Through-silicon vias for power delivery) represents a further evolution of EMIB. By incorporating direct power delivery channels (TSVs) within the silicon bridge, EMIB-T dramatically boosts power delivery efficiency to the chips while simultaneously optimizing signal routing. This advancement is crucial for meeting the demanding power and data transmission requirements of High Bandwidth Memory (HBM) technology, effectively resolving power delivery challenges when HBM and compute dies are placed adjacently. Intel is developing and producing these technologies within its U.S. manufacturing sites, ensuring a robust and secure supply chain by integrating design, manufacturing, and packaging processes.

Background and Industry Context

The progression of AI and high-performance computing (HPC) mandates semiconductor chips with increasing core counts, higher data throughput, and lower power consumption. However, achieving all these attributes with a single, massive monolithic die has become increasingly challenging due to manufacturing costs and yield considerations. Consequently, "heterogeneous integration," which combines multiple smaller chiplets using advanced packaging, has emerged as a key strategy for enhancing performance and efficiency. Intel's Foveros and EMIB-T are at the forefront of this heterogeneous integration strategy, offering solutions that maximize overall system performance while increasing chip design flexibility.

Strategic Significance and Outlook

Intel's strengthening of advanced packaging development and production within the U.S. aligns with the U.S. government's initiative to bring semiconductor manufacturing back onshore, contributing to geopolitical risk mitigation. Technological innovations like EMIB-T directly lead to improved performance in next-generation AI accelerators, accelerating the realization of diverse AI applications in data centers, edge AI, and autonomous driving. Intel is expected to further solidify its leadership in the semiconductor market through continuous investment and innovation in this domain during the AI era.

Source: <https://newsroom.intel.com/intel-foundry/intels-us-advanced-packaging-enables-next-generation-ai-semiconductors>

Collected: July 31, 2026 | Automated Research System (Gemini API)

#07 SEMICON West Relocates to Phoenix, Arizona, Bolstering U.S. Semiconductor Hub with TSMC's \$100 Billion Advanced Fab Plans

Published July 30, 2026 Arizona Commerce Authority USA



OVERVIEW

SEMI announced the permanent relocation of SEMICON West to Phoenix, Arizona, adopting an annual spring schedule from March 30 – April 1, 2027. This move reflects Arizona's rapid expansion as a semiconductor ecosystem, including TSMC's plan for an additional \$100 billion investment in four new 2nm-and-beyond advanced fabs in the state. The relocation solidifies Arizona's position as a critical hub for U.S. semiconductor manufacturing and innovation, fostering increased industry collaboration and talent development.

Key Findings

SEMI has announced that SEMICON West, the premier international exhibition for semiconductor manufacturing, will permanently relocate its annual event to Phoenix, Arizona, adopting a spring schedule from March 30 – April 1, 2027. This decision highlights Arizona's remarkable growth and strategic importance in the semiconductor ecosystem, including Taiwan Semiconductor Manufacturing Company's (TSMC) plans to invest an additional \$100 billion in four new advanced fabs, utilizing 2nm and below process nodes, within the state.

Business and Regional Details

The relocation of SEMICON West signifies Arizona's rapid emergence as a "new Silicon Valley" within the semiconductor industry. TSMC's monumental investment is not merely an expansion of manufacturing capacity; it brings state-of-the-art technology nodes (2nm and below) to the U.S. mainland, thereby strengthening the resilience and technological leadership of the American semiconductor supply chain. This will accelerate the development of a comprehensive semiconductor ecosystem in Arizona, spanning materials supply, equipment manufacturing, design, packaging, and research and development. The move of SEMICON West is expected to generate new business opportunities and foster collaboration, creating a central gathering point for semiconductor professionals, researchers, and companies.

Background and Industry Context

In recent years, the geopolitical significance of semiconductor supply chains has intensified, leading governments worldwide to prioritize strengthening domestic manufacturing capabilities. The U.S. government, through initiatives like the CHIPS Act, has actively supported investments in advanced domestic semiconductor manufacturing, with Arizona being one of the primary beneficiaries. The combined investments from TSMC, Intel, and other semiconductor-related companies have rapidly elevated Arizona to a new hub for the U.S. semiconductor industry. The SEMICON West relocation perfectly aligns with these macro trends and is poised to play a vital role in facilitating industry-wide growth.

Strategic Significance and Outlook

The establishment of SEMICON West in Arizona and TSMC's ongoing investments signify that the state will remain a crucial center for global semiconductor technology innovation for decades to come. This development will significantly contribute to job creation, technological advancement, and economic growth within the semiconductor sector, while also holding strategic importance for enhancing U.S. national security and technological independence. Arizona is set to play an increasingly critical role in shaping the future of the semiconductor industry.

Source: <https://www.azcommerce.com/news-events/news/2026/7/semicon-west/>

Collected: July 31, 2026 | Automated Research System (Gemini API)

#08 AIアクセラレーター向け2.5DパッケージングとHBM統合が加速：TSMC CoWoSとSamsung I-CubeSが技術を牽引、2026年までに5.5倍のレティクルサイズへ

Published July 27, 2026 Econ Market Research Global



OVERVIEW

The adoption of HBM-integrated 2.5D packaging for AI accelerators is rapidly expanding, with TSMC and Samsung spearheading the technological advancements. TSMC's CoWoS platform now supports silicon interposers up to 3.5 times the standard reticle size in volume production, with plans to reach 5.5 times by 2026, while Samsung's I-CubeS platform supports 6 HBM2E stacks and is developing 8 HBM3 configurations. This evolution is critical for meeting the complex system demands of AI, HPC, and data center processors, significantly boosting next-generation semiconductor performance and efficiency.

Background

The exponential growth of AI workloads presents both significant challenges and opportunities for the semiconductor industry. Historically, data transfer speed and memory bandwidth limitations have emerged as major bottlenecks restricting chip performance. 2.5D packaging offers a critical solution by allowing multiple dies—such as High Bandwidth Memory (HBM) and logic processors—to be placed side-by-side on a silicon interposer. This technique facilitates shorter, denser electrical connections compared to traditional wire bonding or flip-chip methods, which in turn leads to a significant reduction in signal latency and power consumption. Advanced packaging solutions, including 2.5D, are now widely adopted in cutting-edge AI accelerators, High-Performance Computing (HPC) systems, and data center processors, as highlighted by reports such as one from Econ Market Research.

Key Findings

The adoption of HBM-integrated 2.5D packaging for AI accelerators is rapidly gaining momentum, with industry leaders TSMC and Samsung spearheading the technological innovation. TSMC's CoWoS-S platform currently supports silicon interposers approximately 3.3 times the conventional reticle area, while its CoWoS-L variant is already in volume production at 3.5 times, with ambitious plans for further expansion to 5.5 times by 2026. Concurrently, Samsung's I-CubeS platform supports configurations utilizing 6 HBM2E stacks and is actively developing solutions for 8-HBM3 arrangements, marking significant strides in high-performance computing capabilities.

Further technical advancements include:

- **TSMC CoWoS Evolution:** TSMC's CoWoS-S (Chip-on-Wafer-on-Substrate) platform has demonstrated the integration of silicon interposers up to approximately 3.3 times the standard reticle size. This capability is paramount for establishing high-density connections between 4-8 HBM stacks and logic devices, a fundamental requirement for demanding AI training accelerators. The CoWoS-L platform has already achieved volume production at roughly 3.5 times the reticle size, with strategic plans to further expand to approximately 5.5 times by 2026. These significant expansions are vital, as escalating AI chip performance requirements necessitate progressively larger interposer areas and increased HBM capacity.

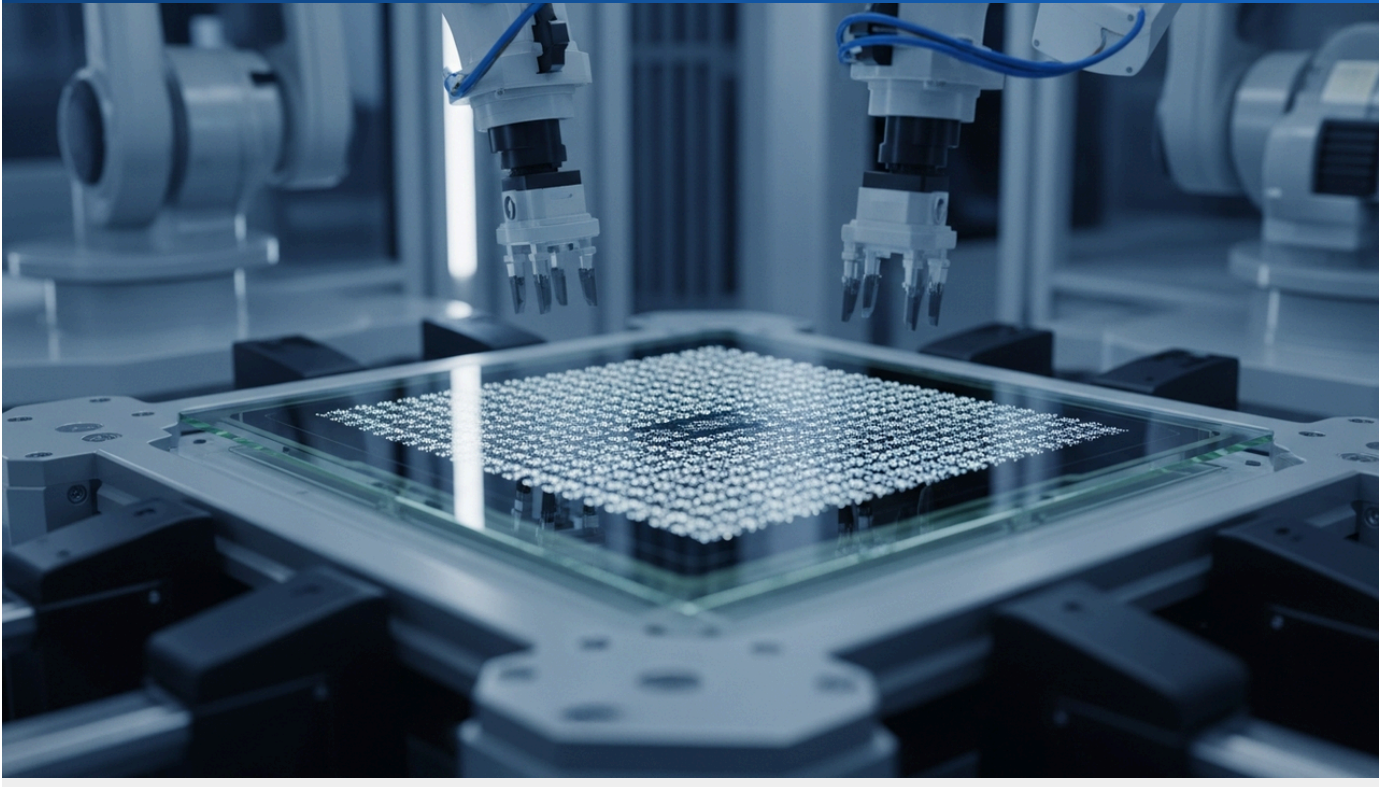
- **Samsung I-CubeS Deployment:** Samsung's advanced packaging platform, I-CubeS, is a key contributor to this rapidly evolving domain. Current I-CubeS configurations are engineered to support 6 HBM2E stacks, with ongoing development for future architectures accommodating 8-HBM3 arrangements. Samsung has also successfully qualified interposer-based packages roughly 3.3 times the reticle size, thereby addressing the critical demands for high-bandwidth and large-memory integration in contemporary AI chips.
- **HBM Criticality:** The high-speed data transfer and massive processing capabilities required by modern AI, HPC, and data center processors inherently necessitate the use of 4-8 HBM stacks. These HBM stacks interface with logic devices through sophisticated silicon interposers or high-density redistribution layers (RDLs). This approach delivers superior bandwidth and enhanced power efficiency when compared to conventional packaging methods, making it indispensable for mitigating performance bottlenecks prevalent in intensive AI workloads.

Looking ahead, the ongoing evolution of 2.5D packaging and HBM integration by industry leaders TSMC and Samsung is set to propel AI chip performance to unprecedented levels. The drive towards larger reticle sizes and an increased number of HBM stacks is fundamental for addressing the colossal computational and data bandwidth demands anticipated from future AI models. Moreover, the growing adoption of open chiplet interconnect standards, such as UCle 3.0, will further unlock new possibilities for integrating multi-vendor chiplets. This will enable the creation of even more complex, modular, and high-performing AI systems, pushing the frontiers of semiconductor manufacturing and fundamentally redefining computing for the AI era.

Source: <https://www.econmarketresearch.com/blog/top-companies-in-advanced-semiconductor-packaging>

#09 TSMCが310x310mmガラス基板CoPoSでCoWoS容量ボトルネックを打破、2028-2029年量産へ

Published July 29, 2026 36氦 / 半导体行业观察, AI Weekly Taiwan



OVERVIEW

TSMC has launched a pilot line for its CoPoS (Chip-on-Panel-on-Substrate) advanced packaging at Taiwan's VisEra, aiming to alleviate the critical CoWoS capacity bottleneck for AI chips. Utilizing 310x310mm rectangular glass panels, this platform targets mass production by late 2028-2029. CoPoS is designed to transcend the limitations of 12-inch wafers, significantly boosting output by repurposing existing display panel lines and enabling efficient tiling of large AI dies with panel-level lithography and glass substrates.

Background

The exponential growth of artificial intelligence has created unprecedented demand in the semiconductor industry. AI accelerators, in particular, require more cores, High-Bandwidth Memory (HBM) stacks, and larger package sizes, pushing existing packaging technologies to their limits. CoWoS (Chip-on-Wafer-on-Substrate), while a de facto standard for advanced packaging, faces limitations in terms of production efficiency and cost for very large dies due to its wafer-based nature. Against this backdrop, Panel-Level Packaging (PLP) is gaining traction as a next-generation solution for integrating large accelerators with chiplet architectures and HBM stacks.

Key Findings

TSMC has initiated a pilot line for its innovative CoPoS (Chip-on-Panel-on-Substrate) advanced packaging technology at VisEra's Longtan plant in Taiwan. This strategic move directly addresses the critical CoWoS production capacity bottlenecks currently impacting AI chip availability. The new CoPoS platform, leveraging 310x310mm rectangular glass panels, is slated for mass production between late 2028 and 2029.

Current CoWoS technology is fundamentally limited by the 12-inch wafer form factor, which restricts overall output and wafer-level packaging equipment capacity—a significant bottleneck for burgeoning AI chip demand. TSMC's CoWoS capacity is reportedly fully booked through 2027 by major customers like Nvidia, AMD, and Google, underscoring the urgent need for alternative high-volume solutions.

CoPoS transcends these 12-inch wafer limitations by employing Panel-Level Packaging (PLP), which offers significantly higher output per unit area. It capitalizes on existing display panel production lines, enabling rapid capacity expansion. Technically, CoPoS utilizes glass substrates, Physical Vapor Deposition (PVD), and high-precision panel-level lithography to achieve micron-level circuit accuracy. Its warpage-controlled, low-stress plastic packaging further facilitates the efficient tiling of large dies and high-density integration, crucial for demanding High-Performance Computing (HPC), 5G/6G, and AI applications. This approach becomes particularly advantageous for chip packaging areas exceeding 3.3 times the mask size, providing a pathway to overcome performance and cost bottlenecks.

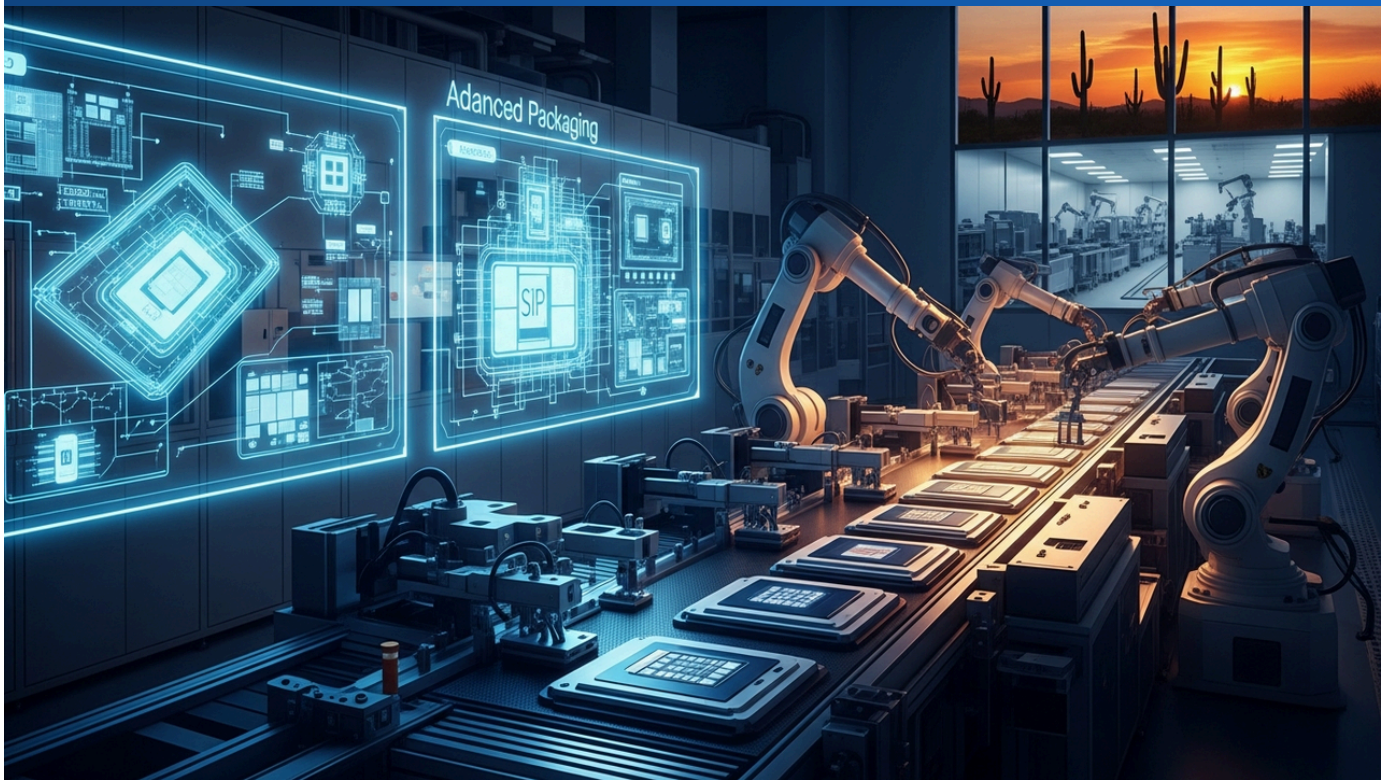
TSMC's CoPoS strategy aims to more efficiently tile larger AI dies, directly challenging competing technologies like Intel's Embedded Multi-die Interconnect Bridge (EMIB). The introduction of CoPoS is expected to significantly change the AI chip manufacturing ecosystem by alleviating CoWoS supply constraints and potentially increasing AI chip availability in the market. The broader industry trend, evidenced by Intel's collaboration with China's Lens Technology on glass substrate-based advanced packaging (targeting 2H 2027 mass production), suggests that PLP with glass substrates is becoming a major competitive battleground. This technology is positioned to set new industry benchmarks for performance, cost, and production efficiency in the AI era, intensifying market competition. Furthermore, Taiwan's supply chain, including companies like Innolux, AUO, and TPK-KY, is actively developing Fan-Out Panel-Level Packaging (FOPLP) using square glass substrates and Through-Glass Via (TGV) technology, signaling readiness for widespread CoPoS adoption.

Source: <https://eu.36kr.com/en/p/3916013244558981>

Collected: July 31, 2026 | Automated Research System (Gemini API)

#11 Amkor Technology、AI需要に対応しアリゾナに2028年稼働の先進パッケージング工場を建設、韓国SiP生産はベトナムへ移管

Published July 24, 2026 Seeking Alpha USA



OVERVIEW

Amkor Technology is making a monumental \$7 billion investment to construct an advanced packaging and test campus in Arizona, slated for production by early 2028, to address the escalating demand for AI chips. This strategic expansion also involves reallocating its System-in-Package (SiP) production from Korea to Vietnam, thereby dedicating existing Korean cleanroom capacity to advanced AI packaging. This initiative is designed to bolster domestic packaging for HPC, communications, and automotive semiconductors, create 2,000 manufacturing jobs, and solidify Amkor's leadership in proprietary packaging platforms for AI, chiplets, and co-packaged optics.

Background

The rapid proliferation of artificial intelligence introduces significant geopolitical and technological challenges for the semiconductor industry. In the United States, national strategies prioritize reshoring domestic manufacturing and enhancing supply chain resilience, with government initiatives like the CHIPS Act actively stimulating investments in advanced packaging. Outsourced Semiconductor Assembly and Test (OSAT) companies, such as Amkor, are central to these efforts, playing a critical role in the development and high-volume deployment of cutting-edge packaging solutions essential for AI chips. The substantial investment in Arizona directly reflects this reshoring imperative, while the strategic production shift to Vietnam represents a pragmatic business decision aimed at optimizing Amkor's global manufacturing footprint to meet escalating AI demand.

Key Findings

Amkor Technology is implementing an aggressive investment strategy in next-generation packaging to address the exploding demand for AI chips. This includes the construction of a 104-acre advanced packaging and test campus in Arizona, representing an investment of approximately \$7 billion. The new facility, slated for production in early 2028, will bolster domestic packaging capabilities for high-performance computing (HPC), communications, and automotive semiconductors, generating approximately 2,000 manufacturing jobs. Complementing this expansion, Amkor is reallocating System-in-Package (SiP) production to Vietnam, thereby freeing up space to expand AI-related advanced packaging capabilities at its existing Korean facilities.

Technical Details

- **Arizona New Facility:** Amkor's Arizona campus will host a comprehensive advanced packaging portfolio, encompassing technologies such as flip-chip ball-grid arrays, wafer-level fan-out, 2.5D and 3D integration, SWIFT, S-SWIFT, high-density system-in-package (SiP) platforms, as well as bumping, wafer probing, and final testing. This facility is poised to significantly strengthen the U.S. domestic semiconductor supply chain and secure strategically vital advanced packaging capabilities.

- **Production Shift to Vietnam:** To optimize cleanroom resources in Korea for burgeoning AI-related advanced packaging demands, Amkor is strategically relocating a portion of its SiP production to Vietnam. This move underscores the industry's intensified focus on advanced packaging capacity, which is increasingly dictating capital expenditure decisions across the semiconductor supply chain, driven by AI chip proliferation. This manufacturing footprint optimization seeks to achieve an optimal balance of cost-efficiency, capacity utilization, and proximity to customers for both established and next-generation package types.
- **Addressing AI Bottlenecks:** Acknowledging its pivotal role as a potential bottleneck in AI chip manufacturing, Amkor is channeling substantial investments into proprietary packaging platforms tailored for AI, chiplets, and co-packaged optics (CPO). This initiative signifies a strategic evolution for Amkor, transcending its traditional role as a cyclical Outsourced Semiconductor Assembly and Test (OSAT) provider, towards a model focused on sustainable margin expansion and long-term growth.

Strategic Significance & Outlook

Amkor's strategic investments and comprehensive reorganization of its manufacturing footprint represent critical moves to solidify its leadership in semiconductor packaging for the burgeoning AI era. The new Arizona facility is poised to significantly augment domestic production capacity for AI, HPC, and automotive chips, thereby fortifying the U.S. semiconductor ecosystem. Concurrently, the transfer of SiP production to Vietnam will enhance global manufacturing efficiency, enabling Korean facilities to concentrate on higher-value AI-centric advanced packaging. These initiatives are expected to mitigate potential bottlenecks in AI chip manufacturing and propel technological innovation, fostering growth across the broader semiconductor industry.

Source: <https://seekingalpha.com/article/4925158-amkors-correction-handed-patient-investors-a-second-look>

#12 ASE Technology、2026年設備投資を過去最高の105億ドルに増額、先進パッケージング事業の2027年倍増を目指す

Published July 31, 2026 TrendForce Taiwan



OVERVIEW

ASE Technology Holding is significantly increasing its 2026 capital expenditure to a record \$10.5 billion, aiming to double the revenue of its leading-edge advanced packaging (LEAP) business by 2027. This ambitious investment is driven by surging demand for AI chips, which has already led to over 20% price increases for advanced packaging technologies like CoWoS. The company's strategic roadmap includes commencing mass production of its 310x310mm fully automated Fan-Out Panel-Level Packaging (FOPLP) line in Q1 2027, bolstering its position in the rapidly expanding AI semiconductor market.

Background

The semiconductor industry is transitioning into the 'Foundry 2.0' era due to the rise of AI, demanding deep integration of wafer fabrication, advanced packaging, and testing. In the Chinese market, there is a shortage of domestic advanced packaging and testing capacity for AI computing chips, with an approximate 10% supply-demand gap for CoWoS. OSAT (Outsourced Semiconductor Assembly and Test) providers like ASE are indispensable in alleviating bottlenecks in AI chip design and manufacturing.

Headquartered in Taiwan, ASE has been a global leader in semiconductor assembly and test since its founding in 1984, employing approximately 48,000 people across over 50 smart factories, offering a wide range of turnkey solutions from package design to wafer-level processing, system-in-package integration, and testing.

Key Findings

ASE Technology Holding has increased its 2026 capital expenditure to a record US\$10.5 billion, announcing an ambitious goal to double the revenue of its leading-edge advanced packaging (LEAP) business by 2027. This strategic move addresses the explosive growth in AI chip demand and the corresponding strong need for advanced packaging capabilities. The company's robust performance, with Q2 2026 consolidated net revenues reaching NT\$126,148 million (approx. US\$3.92 billion), a 36.3% year-over-year increase, underpins this accelerated investment, with packaging operations accounting for approximately 52% of total revenues.

Technical Details

- **Growth of LEAP Business:** ASE's LEAP business is outperforming previous forecasts, driven by strong demand from AI-driven new applications, hardware, and industrial, power, connectivity, and storage devices. To meet this demand, ASE has raised prices for various advanced packaging technologies, including CoWoS and FoCoS, by over 20%, reflecting increased raw material costs and capital expenditures.

- **Mass Production of FOPLP:** Central to ASE's advanced packaging strategy is its 310x310mm fully automated Fan-Out Panel-Level Packaging (FOPLP) production line, expected to commence mass production in Q1 2027. Panel-level manufacturing enables larger-scale and more cost-efficient packaging than traditional wafer-level processes, making FOPLP a critical technology for integrating large chiplets, especially for AI and High-Performance Computing (HPC).
- **Outlook for CPO and Glass Substrates:** Initial low-volume deployment for Co-Packaged Optics (CPO) is anticipated by the end of 2026. However, mass production of glass substrate technology is not expected within the next 12 months. ASE's VIPack platform is built upon six technology pillars, including fan-out, embedded integration, 2.5D and 3D architectures, Through-Silicon Vias (TSV), and CPO, providing comprehensive solutions for next-generation semiconductors.

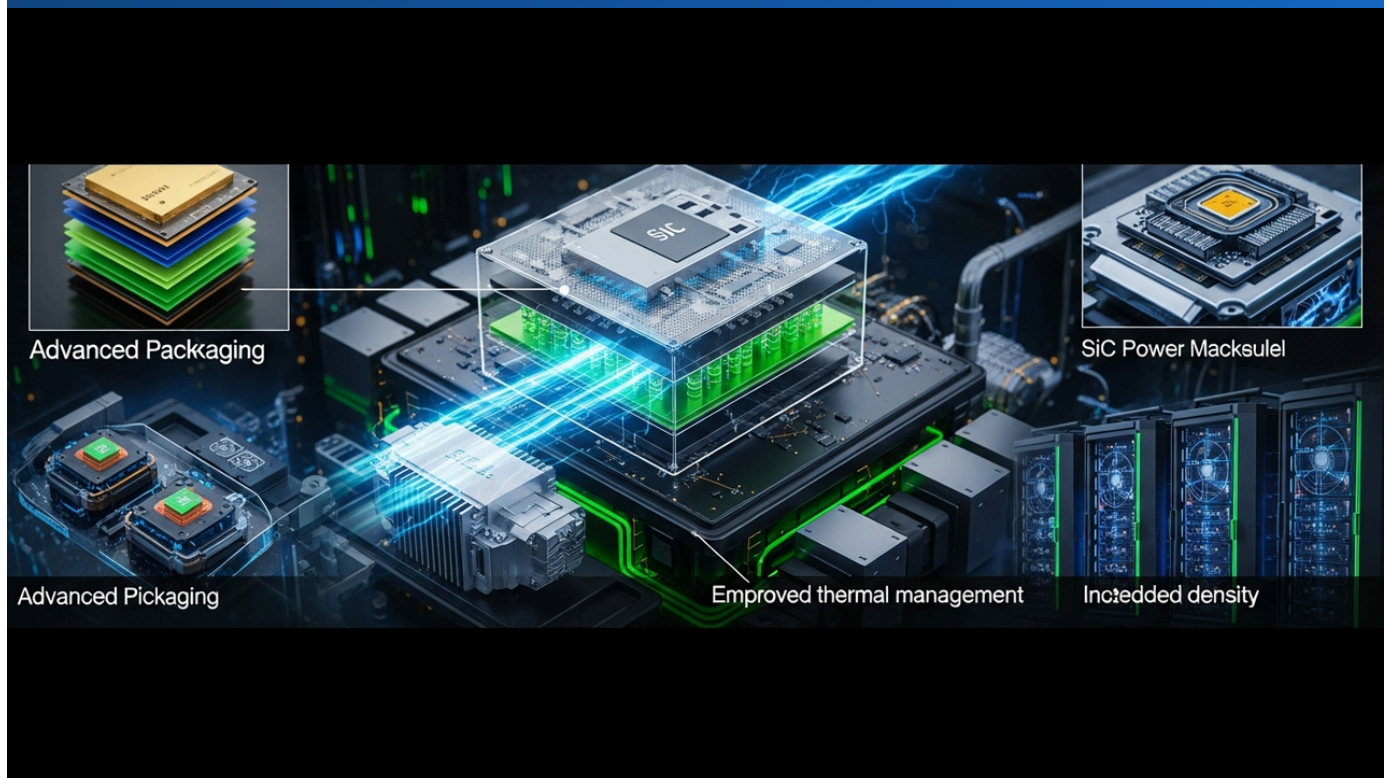
Strategic Significance & Outlook

ASE's record capital expenditure and aggressive expansion strategy for its LEAP business will strengthen its leadership in the AI era. The mass production of FOPLP will enhance the efficiency and scalability of AI chip manufacturing, contributing to alleviating market supply shortages. Furthermore, the early adoption of innovative technologies like CPO underscores the importance of optical interconnects in future AI and HPC infrastructures. ASE's comprehensive technology portfolio and substantial investments are expected to drive innovation in back-end semiconductor processes and play a central role in accelerating the development of AI technology.

Source: <https://www.trendforce.com/news/2026/07/31/news-ase-again-raises-2026-capex-to-record-us10-5b-eyes-2x-leading-edge-advanced-packaging-revenue-by-2027/>

#13 SiCパワーモジュール向け先進パッケージングがEVとAIデータセンターを変革：AMBと埋め込みダイ技術が熱管理と電力密度を向上

Published July 31, 2026 [Industry Publication/Research] Global



OVERVIEW

Advanced packaging technologies for Silicon Carbide (SiC) power modules are dramatically improving thermal management and power density in electric vehicle (EV) inverters and AI data center power systems. Fraunhofer IZM and Mitsubishi Heavy Industries recently showcased a 500 kW/L SiC inverter utilizing Active Metal Brazing (AMB) chip embedding, drawing significant attention from outsourced semiconductor assembly and test (OSAT) providers. This innovation integrates AMB substrates (Si₃N₄, AlN), high-temperature encapsulation materials, and embedded die packaging to withstand operational environments up to 200°C.

Background

The proliferation of electric vehicles and increasing power consumption in AI data centers demand more efficient, compact, and reliable power modules. SiC, with its wide bandgap, excellent thermal conductivity, and high breakdown field strength compared to conventional silicon, is an optimal semiconductor material for these applications. However, realizing the full potential of SiC devices requires overcoming thermal management and packaging challenges. Traditional wire bonding and packaging methods are insufficient for handling SiC's high-temperature and high-power operation, making advanced technologies like AMB indispensable.

Key Findings

Advanced packaging technologies for SiC (Silicon Carbide) power modules are revolutionizing electric vehicle (EV) inverters and AI data center power systems, significantly enhancing thermal management and power density. Fraunhofer IZM and Mitsubishi Heavy Industries, in June 2026, unveiled a 500 kW-per-liter SiC inverter built on Active Metal Brazing (AMB) chip embedding technology, drawing considerable interest from OSATs (Outsourced Semiconductor Assembly and Test providers).

Technical Details

- **AMB Substrates and Enhanced Thermal Cycling Resistance:** For SiC power modules, Active Metal Brazing (AMB) substrates using silicon nitride (Si₃N₄) or aluminum nitride (AlN) provide superior thermal cycling resistance and high thermal conductivity, contributing to extended device lifespan and improved reliability. This is crucial for stable operation of SiC devices, especially in high-temperature environments.
- **High-Temperature Encapsulation Materials:** For SiC devices operating at 175-200°C, specialized high-temperature silicone gels and rigid, highly-filled epoxy molding compounds (EMC) are used for encapsulation. These materials offer high resistance to thermal stress, protecting devices from external environments and maintaining long-term performance.

- **Embedded Die (PCB) Packaging:** Embedded die (PCB) packaging, which integrates bare SiC dies directly into PCB layers with plated microvias, shortens electrical paths and reduces parasitic inductance. This improves the switching performance and efficiency of SiC power modules, minimizing power loss. ASE subsidiary USI has also demonstrated embedding SiC dies in multilayer ABF (Ajinomoto Build-up Film) substrates for EV inverters and AI data center power, highlighting growing OSAT interest.
- **Supplier and Research Trends:** Substrate suppliers like Rogers are globally expanding AMB capacity. Research programs like PVA TePla and Fraunhofer IISB are working on aluminum nitride crystal growth, aiming for further innovation in fundamental material technologies for SiC power modules.

Strategic Significance & Outlook

The evolution of AMB and embedded die packaging will dramatically enhance the performance of SiC power modules, significantly contributing to extended EV range, faster charging, and improved energy efficiency in AI data centers. This technology is expected to accelerate the adoption of SiC semiconductors in a wide range of applications requiring high power density, low loss, and high reliability. Through continuous collaboration between suppliers and research institutions, further innovations in thermal management materials and packaging processes will advance, establishing SiC power modules as a new standard in power conversion technology.

Source: <https://news.pcim.mesago.com/beyond-wire-bonds-the-advanced-packaging-revolution-inside-power-modules-a-2f306efa2da0300884cd10470f93f50a/>

#16 ASMPT's Advanced Packaging Business Achieves Record Sales in H1 2026, Driven by Surging AI Demand

Published July 28, 2026 ASMPT Singapore

ASMPT

Technology NEWS



ASMPT achieves record sales in its advanced package packaging business All demand reporting strong performance in the first half 2026

OVERVIEW

ASMPT reported robust financial results for the first half of 2026, with its Advanced Packaging (AP) business achieving record sales, significantly propelled by escalating AI demand. Key contributors included Thermo-Compression Bonding (TCB), photonics, and high-precision SMT solutions. The company is strategically pushing Panel-Level Packaging (PLP) as a core growth driver, already shipping new chip-on-panel tools for customer qualification.

Key Findings

ASMPT has announced strong performance for the first half of 2026, with its Advanced Packaging (AP) business unit recording unprecedented sales, largely fueled by a surge in demand from the artificial intelligence (AI) sector. The company's Thermo-Compression Bonding (TCB), photonics, and high-precision Surface Mount Technology (SMT) solutions were cited as major contributors to this growth. Demonstrating a clear strategic direction, ASMPT is actively pursuing Panel-Level Packaging (PLP) as a critical future growth driver, evidenced by the shipment of new chip-on-panel tools for customer qualification.

Technical Details

- **Thermo-Compression Bonding (TCB):** TCB is a vital advanced packaging technique enabling high-density integration and fine-pitch interconnects, essential for 3D stacking in High Bandwidth Memory (HBM) and High-Performance Computing (HPC) chips. ASMPT's TCB solutions facilitate the efficient manufacturing of these complex structures with superior precision and throughput.
- **Photonics Solutions:** The increasing demand from AI and data centers highlights the growing importance of optical interconnects. ASMPT provides high-precision solutions for the assembly and packaging of optoelectronic devices, contributing to faster data transmission rates and reduced power consumption crucial for next-generation AI accelerators.
- **High-Precision SMT Solutions:** SMT is a foundational technology for accurately placing components on substrates in increasingly miniaturized and high-density electronic devices. ASMPT's SMT capabilities enable highly precise integration for complex systems like AI chip modules, enhancing product reliability and performance.
- **Panel-Level Packaging (PLP):** PLP is gaining traction as a cost-effective alternative to traditional wafer-level packaging. By leveraging existing display panel manufacturing infrastructure, PLP allows for the simultaneous processing of significantly more chips on larger substrates, potentially reducing per-unit costs and improving production throughput compared to wafer-level methods. ASMPT's push into PLP, with tools already out for customer qualification, positions it to capture significant market share in the rapidly expanding AI chip market.

Background & Context

The semiconductor industry is experiencing unprecedented demand, particularly from high-growth markets such as AI, HPC, 5G, and data centers. Advanced packaging technologies have emerged as a critical bottleneck in meeting this demand. Enhancing AI chip performance necessitates the efficient and high-density integration of multiple dies, requiring innovative packaging techniques like CoWoS, InFO, EMIB, and hybrid bonding. ASMPT's strong financial performance underscores its position at the forefront of this technological shift, with strategic investments paying off in addressing the escalating complexity and market demands for AI chips.

Strategic Significance & Outlook

ASMPT aims to further solidify its position within the AI ecosystem through its innovative advanced packaging solutions. The investment in Panel-Level Packaging and the deployment of chip-on-panel tools represent a crucial step towards capturing future market growth. As AI and HPC applications continue their widespread adoption, the demand for high-precision bonding, integrated photonics, and cost-efficient packaging methods is expected to surge. ASMPT's technologies are poised to play an indispensable role in overcoming these technical challenges and enabling the realization of next-generation semiconductor products globally.

Source: <https://www.asmpt.com/en/investor-relations/news-events/asmpt-announces-2026-interim-results/>