Semiconductor packaging

Weekly Intelligence Report

2026-08-09 | 12 articles | 6 countries

troy-technical.jp

This Week's Keyword

Advanced Packaging Crisis

AI chip bottlenecks, glass substrates, OSATs

12	6	130,000	US$10.5B
articles	countries	wafers/month	CapEx
Total Articles Analyzed	Source Countries/Regions	TSMC CoWoS Target	ASE 2026 Investment

All 12 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	SEMI Europe APC 2026	Market Overview	●○○○○	●●●○○	●●●○○	●●○○○	●●●●	SEMI Europe's 2026 conference highlights advanced packaging, chiplets, and power delivery for AI/HPC, emphasizing supply chain and sustainability.
#02	ACM Research Panel ECP	New Product	●●●○○	●●●●	●●●●	●●●●	●●●●	ACM Research secures orders for its 600x600mm horizontal panel electroplating tool, boosting efficiency for advanced packaging.
#03	IMAPS DPC 2026 PDCs	Market Overview	●○○○○	●●●○○	●●●○○	●●○○○	●●●●	IMAPS 2026 PDCs detailed chiplets, heterogeneous integration, and hybrid bonding, crucial for AI/HPC performance.
#04	Glass Substrates Race	Trend Analysis	●●●●	●●●○○	●●●●	●●●○○	●●●●	China and Japan race to mass-produce glass substrates for AI packaging, a game-changer offering superior performance but facing yield challenges.
#05	ASPS 2026 Korea	Market Overview	●○○○○	●●●○○	●●●○○	●●○○○	●●●○○	ASPS 2026 in Korea showcases advanced packaging, chiplets, and HBM for AI/HPC, highlighting Korean industry trends.
#06	TSMC Outsourcing CoWoS	Corporate Strategy	●●○○○	●●●●	●●●●	●●●○○	●●●●	TSMC outsources CoWoS front-end to OSATs to ease AI chip bottlenecks, boosting OSATs like Amkor and ASE.
#07	ASE Raises CapEx	Corporate Strategy	●●○○○	●●●●	●●●●	●●●○○	●●●●	ASE plans record $10.5B CapEx for 2026 to double advanced packaging revenue by 2027, focusing on CoWoS and HBM.
#08	SK Adv Pkg Plan	Government Policy	●●○○○	●●●○○	●●●●	●●●○○	●●●●	South Korea invests heavily in advanced packaging R&D;, talent, and infrastructure to secure leadership in AI/HPC semiconductors.
#09	China Glass Substrate	Trend Analysis	●●●●	●●●○○	●●●●	●●●○○	●●●●	18 Chinese firms accelerate development of glass core substrates for advanced packaging, aiming for supply chain autonomy.
#10	Supercomputing Adv Pkg	Analysis	●○○○○	●●●●	●●●○○	●●○○○	●●●●	Advanced packaging like CoWoS, EMIB, and T-AI are crucial for AI accelerator performance, overcoming data transfer bottlenecks.
#11	Silicon Box 500M Shipments	Corporate Announcement	●●●○○	●●●●	●●●●	●●○○○	●●●●	Silicon Box shipped over 500 million chiplet packages, validating high-volume manufacturing for AI/HPC applications.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#12	TSMC CoWoS Bottleneck	Market Analysis	●●○○○	●●●●●	●●●●●	●●●○○	●●●●●	TSMC's CoWoS capacity is sold out through 2026, creating a critical bottleneck for AI chip supply, exacerbated by ABF substrate shortage.

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI product roadmap exposed to CoWoS bottlenecks?

TSMC's CoWoS capacity is sold out through 2026, severely impacting AI chip supply. Does your product strategy account for this constraint, and have you diversified packaging partners beyond TSMC?

❷ How will glass substrates reshape your supply chain?

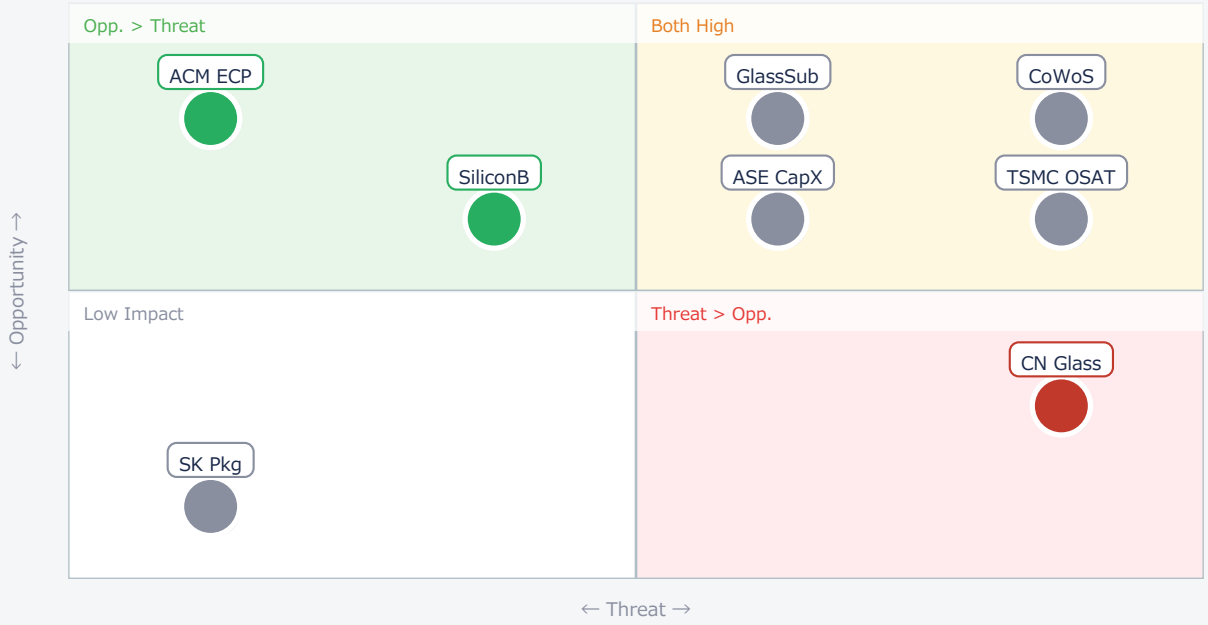
Glass core substrates are emerging as a game-changer for AI packaging, with China and Japan racing for mass production. Are you evaluating this technology for future designs and assessing new material supplier risks/opportunities?

❸ Are your OSAT partnerships robust enough for AI demand?

TSMC is outsourcing CoWoS front-end to OSATs, and ASE is investing $10.5B to double advanced packaging revenue. Are your current OSAT relationships sufficient to secure capacity for your next-gen AI/HPC products?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
CoWoS	Critical	OSATs gain	AI chip supply
GlassSub	Critical	New platform	Yield race
TSMC OSAT	Critical	OSAT growth	Supply reliance
ASE CapX	Critical	Capacity boost	Asian OSATs
ACM ECP	Opp.	US equip. lead	—
SiliconB	Opp.	Chiplet scale	—
CN Glass	Threat	—	Supply shift
SK Pkg	Ref.	R&D; collabs	Competitivenes

Deep Dive ① — ACM Research's Panel Electroplating Tool

#02 | 2026/08/07 | GlobeNewswire | Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●○ Data Reliability●●●●○ US/EU Relevance●●●●●

ACM Research has secured production and evaluation orders for its Ultra ECP ap-p horizontal panel-level electroplating tool. This tool supports large panel formats up to 600x600mm for Cu, Ni, SnAg, Au plating, crucial for advanced packaging.

The proprietary horizontal electroplating technology significantly improves film thickness uniformity and process stability across large panels, reducing defects and increasing yields compared to conventional vertical plating. This is key for high-density RDLs and bump formation.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: ACM Research's tool addresses a critical need for high-volume, cost-effective panel-level packaging. The stated performance improvements in uniformity and stability are realistic given the horizontal design advantages. Technical barriers include scaling throughput and ensuring compatibility with diverse substrate materials beyond current specs. [Opportunity] for US/EU OEMs and device manufacturers to leverage this technology for more efficient and higher-yield advanced packaging, potentially reducing costs. [Threat] is limited, but non-adopters risk falling behind in packaging efficiency. Next actions: [Procurement] Evaluate tool capabilities and engage ACM for pilot programs by Q4 2026. [R&D;] Assess integration with existing advanced packaging lines and material sets by Q1 2027.

Deep Dive ② — China's Push in Glass Core Substrates

#09 | 2026/08/07 | TrendForce | Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●●

TrendForce reports 18 Chinese companies are rapidly advancing in glass core substrates for advanced packaging, driven by a national strategy for supply chain autonomy amidst US-China tech competition.

Glass substrates offer superior electrical properties, thermal stability, and finer line capabilities (L/S < 1/1μm) compared to organic or silicon interposers. Chinese firms focus on laser processing, thin-film deposition, and glass TSV to improve production maturity.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The rapid entry of 18 Chinese firms into glass core substrates is a significant geopolitical and technological development. While glass substrates offer clear performance advantages for AI/HPC, achieving stable yield at scale remains a major technical barrier globally. China's aggressive push could lead to rapid cost reduction and localized supply. [Opportunity] for US/EU materials and equipment suppliers to partner with or compete against these emerging players, or for IP holders to license technology. [Threat] is significant for US/EU OEMs and device manufacturers, risking reliance on a Chinese-dominated supply chain for a critical next-gen material, potentially impacting cost and access. Next actions: [Strategy] Conduct a detailed supply chain risk assessment for glass substrates by Q4 2026. [R&D;] Accelerate internal R&D; or seek partnerships for glass substrate technology to avoid future dependence by Q1 2027.

Deep Dive ③ — TSMC CoWoS: The AI Chip Bottleneck

#12 | 2026/07/30 | Tech Times | Tech Novelty●●○○○ Proximity●●●●● Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●●

TSMC's CoWoS advanced packaging capacity is the critical bottleneck for AI chip supply, fully booked through 2026. This is exacerbated by a severe shortage of ABF substrate materials, extending lead times significantly.

TSMC plans to nearly quadruple CoWoS production to 130,000 wafers/month by late 2026, but demand, with NVIDIA consuming ~60%, is projected to still outstrip supply. This forces a structural shift in the supply chain.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The CoWoS bottleneck is a stark reality, and the numbers (130k wafers/month, 60% NVIDIA consumption) appear realistic given current market dynamics. The primary technical barrier is scaling complex 2.5D/3D integration processes and securing critical materials like ABF. [Opportunity] for US/EU OSATs (e.g., Amkor) and materials/equipment suppliers to expand capacity and offer alternative advanced packaging solutions. [Threat] is immense for US/EU OEMs and device manufacturers reliant on CoWoS for AI accelerators, facing delayed product launches and competitive disadvantage. Procurement managers must urgently diversify packaging strategies. Next actions: [Procurement] Initiate immediate discussions with multiple OSATs and ABF suppliers for long-term contracts by end of Q3 2026. [Strategy] Evaluate alternative packaging technologies (e.g., Intel's EMIB, Silicon Box's chiplets) for future AI product generations by Q4 2026.

Other Notable Articles

#01 SEMI Europe's Advanced Packaging Conference 2026 (SEMI Europe)
Tech Novelty●○○○○ Proximity●●●○○ Market Impact●●●○○

Highlights key trends in advanced packaging for AI/HPC, including power delivery and interconnects, relevant for EU strategy.

#06 IMAPS Device Packaging Conference 2026 PDCs Focus on Advanced Packaging for Chiplets and Heterogeneous Integration, Highlighting Hybrid Bonding (IMAPS)
Tech Novelty●○○○○ Proximity●●●○○ Market Impact●●●○○

Provides foundational understanding of chiplets, heterogeneous integration, and hybrid bonding, critical for R&D; teams.

#13 Supercomputing News Emphasizes Critical Role of Advanced Packaging (CoWoS, EMIB, T-AI) in AI Accelerators (Supercomputing News)
Tech Novelty●○○○○ Proximity●●●●○ Market Impact●●●○○

Reinforces the strategic importance of advanced packaging (CoWoS, EMIB) for overcoming AI accelerator bottlenecks.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Conduct urgent supply chain risk assessment for CoWoS and ABF substrates, identifying alternative sources and potential lead time impacts.
- [Executive] Schedule a cross-functional meeting (R&D;, Procurement, Strategy) to review AI product roadmaps against current advanced packaging capacity constraints.

Short-term (1 month)

- [R&D;] Begin preliminary evaluation of glass core substrates as a next-generation packaging material, assessing its potential and technical challenges for your product lines.
- [Business Dev] Engage with leading OSATs (e.g., ASE, Amkor, Silicon Box) to understand their expanded capacity plans and secure future advanced packaging allocations.
- [Strategy] Monitor Chinese advancements in glass core substrates and assess potential geopolitical impacts on future material sourcing and competitive landscape.

Medium-long term (quarter+)

- [R&D;] Invest in internal R&D; for advanced packaging technologies, including hybrid bonding, chiplets, and heterogeneous integration, to reduce reliance on external foundries.
- [Legal/IP] Develop a robust IP strategy around advanced packaging materials and processes, considering both defensive and offensive patenting opportunities.
- [Talent] Develop a long-term talent acquisition and training program for advanced packaging engineers and material scientists to address future skill gaps.

Semiconductor_BackEnd — Selected Articles

Date: 2026-08-09

Articles: 12

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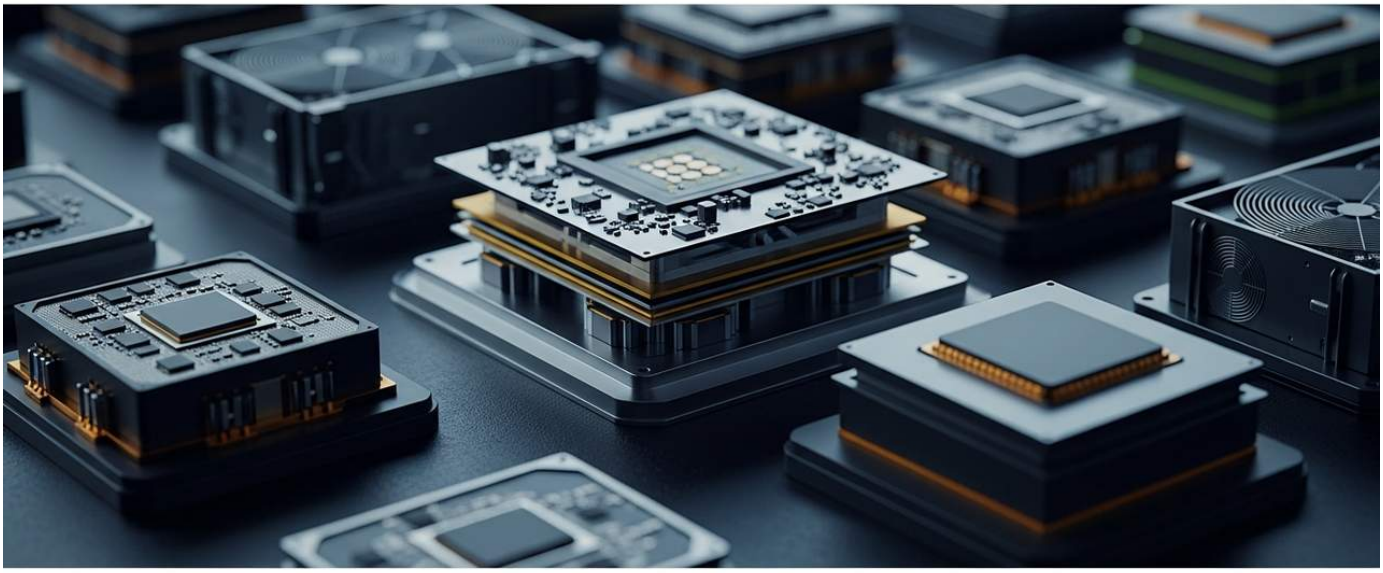
#01 SEMI Europe's Advanced Packaging Conference 2026 to Highlight Power and Interconnect Innovations for AI System Performance

Published Published November 11, 2026　SEMI Europe　ヨーロッパ



OVERVIEW

SEMI Europe's 2026 Advanced Packaging Conference (APC) will spotlight 'Power and Interconnects Innovations Enabling AI System Performance,' emphasizing advanced packaging (AP) and test as crucial for scaling next-generation AI systems. The conference will delve into 2.5D/3D integration, chiplet architectures, heterogeneous integration, and advanced substrates vital for HPC, AI, automotive, and 5G/6G, alongside critical discussions on sustainability, supply chain resilience, and chip–package–system co-design. These topics underscore advanced packaging's strategic role in overcoming the power and memory walls challenging modern AI and high-performance computing.

IN DEPTH

Background

The relentless demand from AI workloads and an explosion in data volumes are pushing the boundaries of semiconductor design and manufacturing. As traditional transistor scaling, once the bedrock of Moore's Law, faces diminishing returns, the industry confronts significant 'power wall' and 'memory wall' challenges. In response, advanced packaging and testing technologies are rapidly emerging as pivotal frontiers for realizing substantial system-level performance gains beyond what front-end scaling alone can provide.

Key Findings

The 2026 Advanced Packaging Conference (APC) will prominently feature innovations in power delivery and interconnect technologies as central to enabling the dramatic performance improvements required by AI systems. Advanced packaging techniques such as 2.5D/3D integration, chiplet architectures, and heterogeneous integration are highlighted as pivotal for sustaining system-level performance scaling across next-generation applications in HPC, AI, automotive, and 5G/6G.

Central to these advancements are **2.5D/3D integration** and **chiplet architectures**. These techniques enable the horizontal or vertical stacking of multiple dies, dramatically increasing bandwidth and reducing latency. Chiplets, in particular, offer a modular approach, allowing for independent manufacturing of specialized components that are then integrated in the backend, thereby enhancing design flexibility and improving manufacturing yield.

The conference will further delve into **heterogeneous integration**, exploring how diverse chips—such as CPUs, GPUs, memory, and I/O—fabricated on different process nodes can be seamlessly combined into a single, high-performance package. Supporting this are innovations in **advanced substrates**, including next-generation glass and improved organic materials, which promise higher routing density, superior electrical characteristics, and enhanced thermal performance crucial for future AI accelerators.

A key focus for performance enhancement lies in **power and interconnect innovations**. Technologies like **Backside Power Delivery Networks (BSPDN)** will be highlighted, offering shorter power delivery paths and significantly reduced voltage drop, directly translating to improved chip performance and energy efficiency. Complementing this, fine-pitch interconnects, exemplified by **hybrid bonding**, are enabling unprecedented stacking densities and accelerating data transfer speeds between chips, critical for overcoming the memory wall.

Beyond these core technological breakthroughs, APC 2026 will also address broader industry imperatives, including **supply chain resilience**, **sustainability initiatives**, and the development of **novel materials**. A holistic **chip-package-system co-design** approach will be emphasized as indispensable for achieving optimal system performance and cost efficiency, integrating packaging considerations from the earliest design stages. The conference aims to equip industry stakeholders with critical insights into the opportunities and challenges of advanced semiconductor packaging in the AI era, informing strategic planning for the coming decade.

Source: https://www.semiconeuropa.org/APC

#02 ACM Research Secures Production and Evaluation Orders for Ultra ECP ap-p Horizontal Panel Electroplating Tool, Supporting 600x600mm Panels

Published August 07, 2026 GlobeNewswire USA

OVERVIEW

ACM Research announced securing production and evaluation orders from two advanced packaging customers for its Ultra ECP ap-p horizontal panel-level electroplating tool. This innovative tool supports large panel formats up to 600 × 600 mm and various plating processes (Cu, Ni, SnAg, Au), featuring proprietary horizontal electroplating technology for improved uniformity and process stability. This development marks a significant step towards volume production of large-panel horizontal electroplating for advanced packaging applications.

IN DEPTH

Key Findings

ACM Research has announced that it has received production and evaluation orders from two advanced packaging customers for its self-developed Ultra ECP ap-p horizontal panel-level electroplating tool. This technology is characterized by its unique horizontal electroplating process, which significantly improves uniformity and process stability for various plating processes, including copper, nickel, tin-silver, and gold, on large panel formats up to 600 × 600 mm. This achievement represents a crucial step towards the high-volume manufacturing adoption of large-panel horizontal electroplating in advanced packaging.

Technical / Clinical Details

- **Large Panel Compatibility:** The Ultra ECP ap-p tool supports large panel formats up to 600 × 600 mm. This capability allows for the processing of a significantly greater number of chips simultaneously compared to traditional wafer-level processes, leading to substantial improvements in production efficiency and cost-effectiveness, particularly beneficial for the manufacturing of large packages and System-in-Package (SiP) modules.
- **Horizontal Electroplating Technology:** The proprietary horizontal electroplating technology ensures highly uniform film thickness and excellent material distribution across the entire panel surface. This leads to reduced defect rates and higher production yields. Furthermore, it mitigates issues such as liquid stagnation and bubble formation, which have been challenges in conventional vertical plating equipment, thereby enhancing process stability.
- **Versatile Plating Processes:** The tool is compatible with key plating materials widely used in advanced packaging, including copper (Cu), nickel (Ni), tin-silver (SnAg), and gold (Au). This versatility offers customers flexibility in selecting processes to meet diverse application requirements.

Background & Context

Driven by advancements in AI, High-Performance Computing (HPC), 5G communication, and autonomous driving, semiconductor devices are trending towards higher integration, increased functionality, and larger form factors. To address these demands, packaging technologies are evolving from wafer-level to panel-level processing, necessitating reductions in production costs and increases in capacity. ACM Research's Ultra ECP ap-p tool is designed to meet this trend, with its performance particularly anticipated for high-density Redistribution Layers (RDLs) and bump formation in advanced packaging.

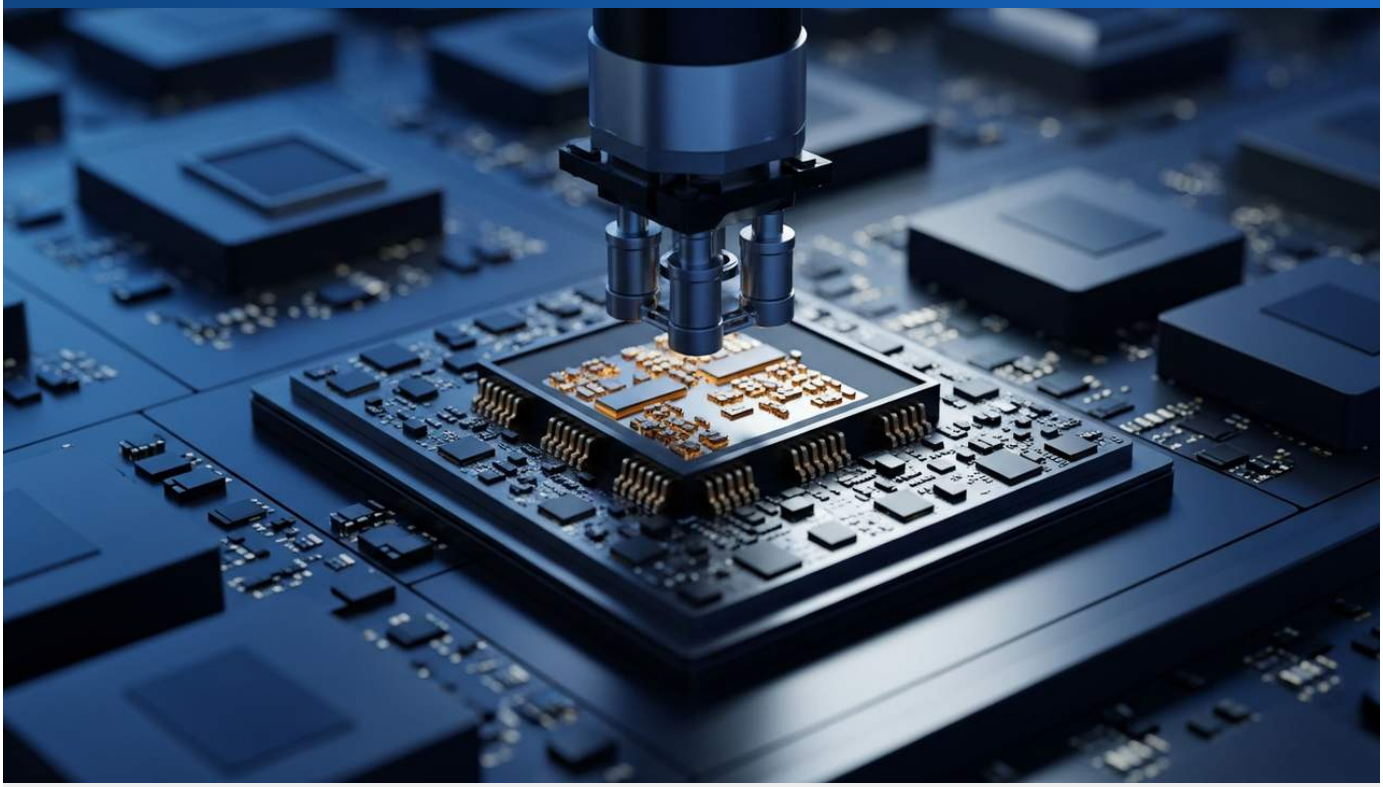
Strategic Significance & Outlook

Securing production and evaluation orders for the Ultra ECP ap-p horizontal panel electroplating tool marks a significant milestone for ACM Research in establishing its position as a leading equipment provider in the advanced packaging market. The widespread adoption of this technology is expected to enhance the efficiency and quality of panel-level packaging, contributing to the accelerated mass production of next-generation semiconductor devices. This will, in turn, further facilitate the market introduction of high-performance devices, such as AI chips and HPC semiconductors, globally.

Source: https://www.globenewswire.com/news-release/2026/08/07/3340949/0/en/acm-research-s-ultra-ecp-ap-p-horizontal-panel-electroplating-tool-receives-first-production-order-and-evaluation-order-from-customers.html

#06 IMAPS Device Packaging Conference 2026 PDCs Focus on Advanced Packaging for Chiplets and Heterogeneous Integration, Highlighting Hybrid Bonding

Published Date unknown IMAPS USA



OVERVIEW

IMAPS Device Packaging Conference 2026 Professional Development Courses (PDCs) extensively covered "Advanced Packaging for Chiplets and Heterogeneous Integration." The courses defined various 2D to 3.5D IC integrations based on interconnect density and electrical performance. Discussions included chiplet communication via bridges embedded in build-up package substrates and fan-out epoxy molding compounds with Redistribution Layers (RDLs). Fundamentals of hybrid bonding and high-volume products utilizing this technology were also presented, consolidating the latest trends in advanced packaging.

IN DEPTH

Key Findings

The Professional Development Courses (PDCs) at the IMAPS Device Packaging Conference 2026 provided an in-depth exploration of "Advanced Packaging for Chiplets and Heterogeneous Integration," underscoring this as one of the industry's most critical technological trends. The courses distinctly defined various IC integration approaches, from 2D to 3.5D, based on interconnect density and electrical performance, with a specific focus on advancements in chiplet communication and hybrid bonding.

Technical / Clinical Details

- **Defining Chiplets and Heterogeneous Integration:** The PDCs detailed various forms of IC integration, ranging from 2D packaging to 2.5D with high-density interposers, 3D involving direct die-to-wafer connections, and 3.5D combining build-up packages with bridge technologies. These were explained from the perspective of interconnect density and electrical performance, offering clear guidance for designers to select optimal integration approaches based on specific application requirements.
- **Innovations in Chiplet Communication:** Communication between chiplets is achieved through bridges, made of silicon or organic materials, embedded within build-up package substrates, or via fan-out epoxy molding compounds (EMCs) equipped with high-density Redistribution Layers (RDLs). These technologies enable high-speed and efficient data transfer between chiplets, thereby enhancing overall system performance.
- **Fundamentals and Applications of Hybrid Bonding:** The basic principles of hybrid bonding were elaborated, explaining how this technology achieves ultra-fine pitch (sub-micron) die-to-wafer or die-to-die connections. Furthermore, concrete high-volume products leveraging this technology, such as smartphone processors and High Bandwidth Memory (HBM), were showcased, emphasizing its practical utility.

Background & Context

The demands of next-generation applications like AI, High-Performance Computing (HPC), and 5G/6G communications necessitate exponential increases in semiconductor chip complexity and performance. Traditional monolithic chip design faces limitations in manufacturing cost, yield, and design flexibility, leading chiplets and heterogeneous integration to emerge as primary industry solutions. These technologies enable performance improvements and cost optimization beyond Moore's Law by manufacturing different functionalities as separate chiplets and then efficiently integrating them in the backend.

Strategic Significance & Outlook

The IMAPS Device Packaging Conference PDCs offered a valuable opportunity for researchers, engineers, and industry professionals to gain a deep understanding of the latest trends in chiplets and heterogeneous integration and to apply this knowledge to their product development. The proliferation of advanced connection technologies like hybrid bonding will further accelerate the evolution of high-density, high-performance applications, such as AI chips and HPC modules. Moving forward, these technologies are expected to become mainstream in semiconductor packaging, driving innovation across the entire electronics industry.

Source: https://imaps.org/page/DPC-26-PDCs

Collected: August 07, 2026 | Automated Research System (Gemini API)

#07 Glass Substrates Emerge as AI Packaging Game-Changer, Igniting Global Race Towards Mass Production as China and Japan Intensify Competition for Yield Stabilization

Published Date unknown The Economy South Korea

OVERVIEW

As AI semiconductor competition shifts from process-node miniaturization to advanced packaging, China and Japan are intensifying efforts to lead the glass core substrate market, a cornerstone for next-generation semiconductor packaging. Companies are accelerating investments in manufacturing facilities and supply chain development, viewing glass substrates as crucial for AI semiconductor scalability. Industry experts state that yield stabilization and overcoming fundamental technological barriers are critical for market leadership in this rapidly evolving sector.

IN DEPTH

Key Findings

As the focus of AI semiconductor competition transitions from traditional process node miniaturization to advanced packaging, China and Japan are intensifying their race for leadership in the mass production of glass core substrates, a foundational technology for next-generation semiconductor packaging. Glass substrates are positioned as a "game-changer" enabling the performance scalability of AI semiconductors, with companies in both nations accelerating massive investments in manufacturing facilities and supply chain development.

Technical / Clinical Details

- **Technical Superiority of Glass Substrates:** Compared to traditional organic substrates, glass substrates offer superior dimensional stability, a low coefficient of thermal expansion (CTE), and low dielectric loss. These properties enable the creation of finer Redistribution Layers (RDLs) and higher-density interconnections, reducing signal delay and power loss, thereby enhancing the overall performance and power efficiency of AI chips.
- **Challenges in Yield Stabilization:** The mass production of glass substrates faces several technical challenges, including the inherent brittleness of glass materials, difficulties in micro-fabrication techniques, and warpage control in large panels. Overcoming these challenges and achieving stable yield for product supply will be a decisive factor in establishing market leadership.
- **Manufacturing Investments and Supply Chain Development:** Chinese and Japanese companies are investing heavily in constructing new factories and expanding existing facilities to establish glass substrate production capabilities. Furthermore, strengthening the entire supply chain, from raw material supply to final product, is crucial for gaining competitive advantage and ensuring stable supply.

Background & Context

The sophistication of AI applications demands enormous data processing capabilities and high bandwidth from semiconductor chips. With the limitations of conventional process miniaturization becoming apparent, advanced packaging has emerged as the new primary means of enhancing chip performance. Glass substrates are drawing attention as an ideal platform for efficiently integrating AI processors with high-speed memory like HBM (High Bandwidth Memory), leading to the belief that whoever masters this technology will dominate the next-generation AI semiconductor market.

Strategic Significance & Outlook

The fierce competition between China and Japan is expected to drive the rapid development and widespread adoption of glass core substrate technology. As yield stabilization and overcoming technical challenges progress, glass substrates are anticipated to be broadly adopted not only for AI chips but also for a wide range of high-performance applications such as HPC (High-Performance Computing), data centers, and automotive electronics. The outcome of this competition will significantly reshape the global semiconductor supply chain landscape and be a crucial factor in determining the pace of future AI technology evolution.

Source: https://economy.ac/news/2026/06/202606289308

#08 Advanced Semiconductor Packaging & Chiplet Show (ASPS) 2026 in Suwon, Korea, to Cover Advanced Packaging, Chiplets, and HBM

Published August 26, 2026 Advanced Semiconductor Packaging & Chiplet Show (ASPS) South Korea

OVERVIEW

The Advanced Semiconductor Packaging & Chiplet Show (ASPS) will take place from August 26-28, 2026, at the Suwon Convention Center in South Korea. This B2B exhibition is focused on semiconductor manufacturers in South Korea, specifically addressing the packaging process in semiconductor manufacturing. Key themes include advanced semiconductor packaging, chiplets, and HBM, providing insights into the latest technological trends and business opportunities in the Korean semiconductor industry.

IN DEPTH

Key Findings

The Advanced Semiconductor Packaging & Chiplet Show (ASPS) will be held from August 26-28, 2026, at the Suwon Convention Center in South Korea. This exhibition will focus on advanced semiconductor packaging technologies, chiplet architectures, and High Bandwidth Memory (HBM), presenting critical technology trends and business opportunities that will shape the future of the Korean semiconductor industry. Particular emphasis will be placed on the latest packaging solutions essential for enhancing the performance and efficiency of AI chips.

Technical / Clinical Details

- **Advanced Semiconductor Packaging:** A wide range of advanced packaging technologies will be showcased, including 2.5D/3D stacking, fan-out packaging, and Co-Packaged Optics (CPO), targeting applications such as AI, High-Performance Computing (HPC), automotive, and 5G/6G communications that demand high integration, miniaturization, and high efficiency.
- **Chiplet Architectures:** The latest trends in chiplet technology will be presented, demonstrating how combining multiple chiplets with different functionalities can increase design flexibility, reduce manufacturing costs, and improve overall system performance. This is a crucial approach to extend beyond the limits of Moore's Law.
- **High Bandwidth Memory (HBM):** HBM technology, essential for breaking the "memory wall" in AI processors, utilizes Through-Silicon Vias (TSVs) to stack multiple DRAM dies, enabling ultra-fast data transfer with the processor. The exhibition will focus on the latest generations of HBM and their manufacturing technologies.

Background & Context

The explosive growth of AI demands unprecedented innovation in semiconductor packaging technology. South Korea, home to global memory and foundry giants like Samsung Electronics and SK Hynix, is at the forefront of advanced packaging technology development. ASPS serves as a platform for the entire Korean semiconductor ecosystem to converge and further enhance its importance in the global supply chain.

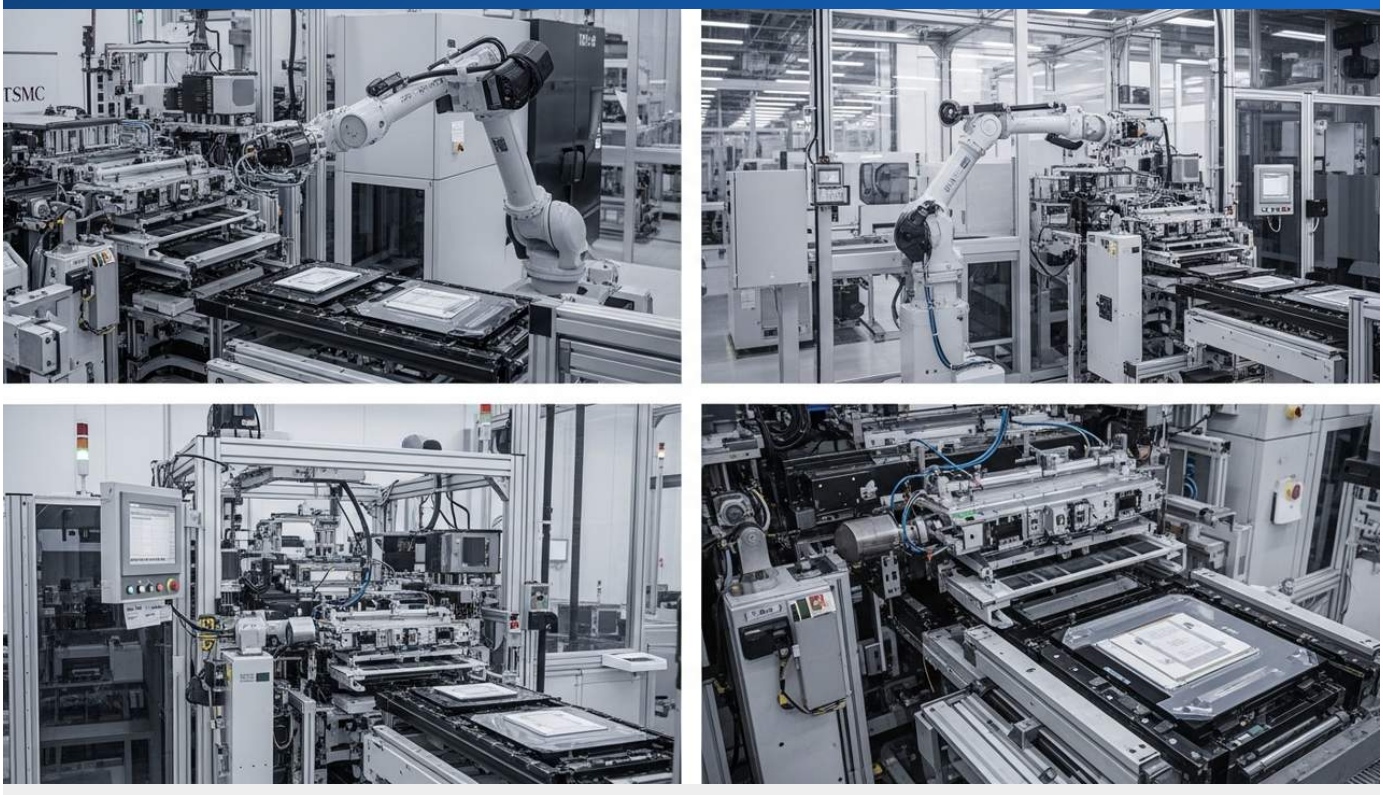
Strategic Significance & Outlook

ASPS 2026 provides an excellent opportunity for Korean semiconductor manufacturers to showcase their latest packaging technologies and solutions to the world. The exhibited technologies are expected to elevate AI chip performance to the next level and accelerate the widespread adoption of AI in various fields, including data centers, autonomous driving, and high-performance mobile devices. This event is also anticipated to contribute to the standardization of advanced packaging and chiplet technologies, strengthening the supply chain, and fostering new business collaborations, thereby supporting the sustainable growth of the entire semiconductor industry.

Source: https://www.semipkgshow.com/en

#09 TrendForce Reports TSMC Expanding CoWoS Front-End Outsourcing to OSATs Amid Surging NVIDIA ASIC Demand

Published August 05, 2026 TrendForce Taiwan



OVERVIEW

TrendForce reports that TSMC is reportedly expanding the outsourcing of key front-end processes for its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging to OSATs (Outsourced Semiconductor Assembly and Test service providers). This move aims to alleviate advanced packaging bottlenecks and rapidly increase the supply capacity of AI accelerators, driven by surging demand for NVIDIA ASICs. Key OSAT players are expected to benefit from this expanded outsourcing.

IN DEPTH

Key Findings

According to TrendForce's latest report, Taiwan Semiconductor Manufacturing Company (TSMC) is reportedly expanding the outsourcing of certain critical front-end processes for its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging technology to Outsourced Semiconductor Assembly and Test (OSAT) service providers. This strategic move aims to rapidly increase the supply capacity of AI accelerators and mitigate market bottlenecks amidst surging demand for NVIDIA's Application-Specific Integrated Circuits (ASICs).

Technical Details

- CoWoS technology is a 2.5D packaging solution that integrates multiple logic chips and High Bandwidth Memory (HBM) onto a silicon interposer, which is then mounted onto a substrate. It is essential for meeting the high-performance requirements of AI/HPC chips.
- The processes being outsourced to OSATs are speculated to be some of the complex 'front-end' steps of CoWoS, such as silicon interposer manufacturing, Redistribution Layer (RDL) formation, and micro-bump formation. These steps demand extremely high precision and technical expertise.
- This expanded outsourcing will enable TSMC to concentrate its production resources on higher-value, more advanced processes, while OSATs gain an opportunity to enhance their presence in the advanced packaging sector.

Background & Context

NVIDIA's Graphics Processing Units (GPUs) have become the de facto standard for AI model training and inference, with demand growing at a pace far exceeding forecasts. Advanced packaging like CoWoS is indispensable for maximizing the performance of AI accelerators, but its manufacturing process is complex and time-consuming, creating a bottleneck across the entire supply chain. TSMC's expansion of outsourcing to OSATs represents a pragmatic solution to alleviate this bottleneck and enable faster market supply.

Strategic Significance & Outlook

This strategic move by TSMC is likely to further elevate the importance of OSATs in the advanced packaging market and potentially trigger a restructuring of the industry's supply chain. Major OSAT players, such as ASE Technology Holding and Amkor Technology, have been expanding their CoWoS-related production capacities, and this increased outsourcing from TSMC will further accelerate their growth. This is expected to stabilize the supply of AI semiconductors and foster the further proliferation and development of AI technologies.

Source: https://www.trendforce.com/news/2026/08/05/news-tsmc-reportedly-expands-outsourcing-of-key-cowos-front-end-step-to-osats-amid-rising-nvidia-asic-demand/

Collected: August 07, 2026 | Automated Research System (Gemini API)

#10 ASE Technology Raises 2026 CapEx to Record US$10.5 Billion, Targets 2x Advanced Packaging Revenue by 2027

Published July 31, 2026 TrendForce Taiwan

OVERVIEW

TrendForce reports that ASE Technology Holding, the world's largest OSAT company, plans to raise its 2026 capital expenditure (CapEx) to a record US$10.5 billion. The company aims to double its revenue from advanced packaging by 2027, driven by increasing demand for AI and high-performance computing (HPC) semiconductors. This massive investment further solidifies ASE's position in the industry's supply chain.

IN DEPTH

Key Findings

According to TrendForce's report, ASE Technology Holding, the world's largest outsourced semiconductor assembly and test (OSAT) service provider, has announced plans to increase its capital expenditure (CapEx) for 2026 to a record US$10.5 billion. Through this significant investment, the company has set an ambitious goal to double its revenue from cutting-edge advanced packaging by 2027.

Technical Details

- The majority of this CapEx will be allocated towards expanding production capacity for advanced technologies such as CoWoS (Chip-on-Wafer-on-Substrate) and fan-out packaging, which are essential for AI accelerators and high-performance computing (HPC) semiconductors.
- Particular emphasis will be placed on developing and mass-producing solutions for High Bandwidth Memory (HBM) integration, chiplet technology, and heterogeneous integration packaging. These technologies aim to enhance data transfer speeds and optimize power efficiency.
- ASE plans to invest in new automation equipment, inspection systems, and advancements in material science to support these complex packaging processes, ensuring yield improvement and stringent quality control.

Background & Context

The rapid advancement of AI is creating unprecedented demand in the semiconductor industry, specifically for advanced packaging technologies capable of high efficiency and density. OSAT companies like ASE play a crucial role in meeting this demand by collaborating with foundries and Integrated Device Manufacturers (IDMs). This record-breaking capital expenditure is a strategic move to alleviate bottlenecks in the AI chip supply chain and accelerate market growth.

Strategic Significance & Outlook

ASE Technology's substantial CapEx and its plan to double advanced packaging revenue signal a clear intention to solidify its leadership within the AI-era semiconductor ecosystem. This initiative is expected to stabilize the supply of AI chips, ultimately fostering further proliferation of AI applications and technological innovation. Moreover, it is likely to encourage similar investments from other OSAT companies and suppliers, thereby accelerating the overall growth of the advanced packaging market.

Source: https://www.trendforce.com/news/2026/07/31/news-ase-again-raises-2026-capex-to-record-us10-5b-eyes-2x-leading-edge-advanced-packaging-revenue-by-2027/

Collected: August 07, 2026 | Automated Research System (Gemini API)

#11 South Korea Unveils Major Investment Plan to Boost National Competitiveness in Advanced Packaging

Published August 01, 2026 Maeil Business Newspaper (MK.co.kr) South Korea

OVERVIEW

The South Korean government announced a large-scale investment plan to enhance national competitiveness in advanced packaging. This strategy aims to meet surging demand for AI and high-performance computing (HPC) semiconductors and solidify Korea's leadership in the global supply chain. The plan emphasizes R&D funding, talent development, and infrastructure improvements.

IN DEPTH

Key Findings

The South Korean government has unveiled a massive investment plan targeting the advanced packaging sector to bolster its national competitiveness in semiconductor back-end processes. This national strategy aims to address the growing demand for AI and high-performance computing (HPC) semiconductors, thereby cementing South Korea's technological leadership in the global semiconductor supply chain.

Technical Details

- The investment plan specifically prioritizes research and development in cutting-edge packaging technologies, including heterogeneous integration, 3D stacking, chiplet technology, and High Bandwidth Memory (HBM) integration.
- The government intends to strengthen industry-academia collaboration, supporting the development of next-generation packaging materials, the localization of high-precision manufacturing equipment, and the establishment of advanced inspection and testing technologies.
- This initiative will enable South Korea to accelerate the development of ultra-high-density and highly efficient packaging solutions required for future high-end markets, such as AI processors and semiconductors for autonomous vehicles.

Background & Context

Semiconductors are a cornerstone of the Korean economy, with companies like Samsung Electronics and SK Hynix leading the global market. However, concerns over geopolitical tensions and supply chain vulnerabilities have prompted nations worldwide to pursue domestic semiconductor manufacturing and strengthening. Amidst this trend, South Korea is focusing on advanced packaging, where it holds a technological advantage, to secure its future competitiveness. This is part of a broader strategy to balance national security with economic self-reliance.

Strategic Significance & Outlook

This substantial government investment will provide a powerful impetus for South Korea's semiconductor industry to remain at the forefront of the advanced packaging sector globally. By integrating R&D funding, talent development, and infrastructure improvements, the creation and industrialization of new technologies will accelerate, positively impacting the entire global semiconductor ecosystem. This will further strengthen South Korea's position as a central hub for semiconductor innovation in the AI era.

Source: https://www.mk.co.kr/en/business/12119467

#12 TrendForce Analyzes: 18 Chinese Enterprises Accelerate Positions in Glass Core Substrate Market

Published August 07, 2026 TrendForce Taiwan

OVERVIEW

TrendForce reported that 18 Chinese companies are rapidly enhancing their presence in the glass core substrate market for advanced packaging. This movement is part of China's strategy to achieve supply chain autonomy amidst intensifying US-China tech competition. These enterprises are accelerating R&D and production capacity investments to acquire foundational technologies supporting next-generation AI and HPC chips.

IN DEPTH

Key Findings

According to TrendForce's latest analysis, as many as 18 Chinese enterprises are rapidly establishing and strengthening their positions in the glass core substrate market for advanced packaging. This move is seen as part of a national strategy aimed at enhancing China's self-reliance in the global semiconductor supply chain and securing access to cutting-edge technologies.

Technical Details

- Glass core substrates offer superior electrical properties (low dielectric loss), thermal stability, and the ability to form finer lines (L/S < 1/1μm) compared to traditional organic substrates and silicon interposers. These advantages enable high-density integration for AI accelerators and high-performance computing (HPC) chips.
- Chinese companies are focusing on developing key manufacturing process technologies, including laser processing, precision thin-film deposition, and Through-Silicon Via (TSV) formation in glass, thereby improving the maturity of their production techniques.
- These technological advancements contribute to improved signal integrity and reduced power consumption in chiplet integration, heterogeneous stacking, and High Bandwidth Memory (HBM) interconnections.

Background & Context

The technological competition between the US and China in the semiconductor industry is escalating, with China accelerating the localization of advanced packaging materials and equipment. Glass core substrates are garnering attention as a next-generation material that can alleviate bottlenecks in high-performance semiconductors, and the Chinese government is supporting this as a strategic priority. The increasing entry of domestic companies reflects China's strong determination to stabilize its supply chain and ensure technological independence.

Strategic Significance & Outlook

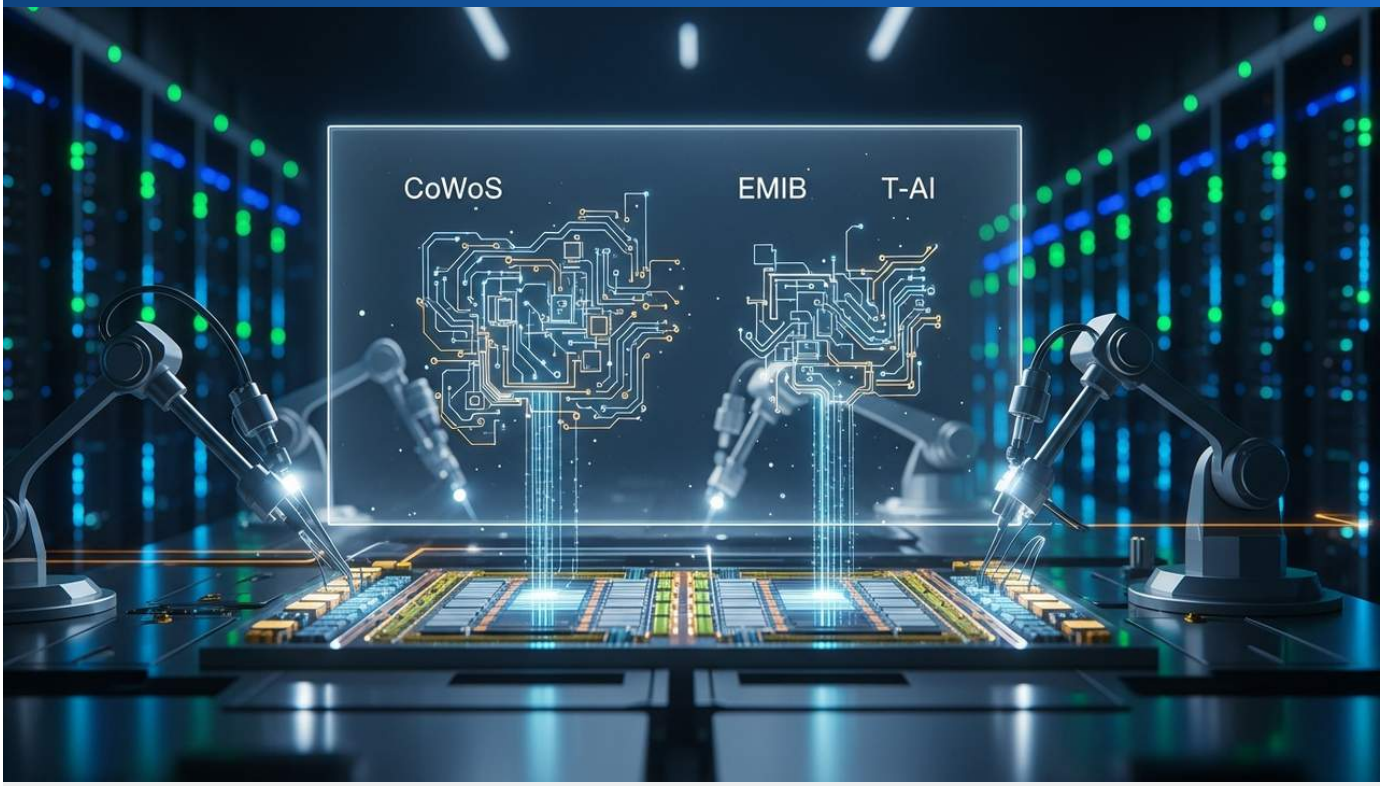
The strengthening presence of Chinese enterprises in the glass core substrate market could significantly impact the global advanced packaging supply chain. This may lead to intensified cost competition and further acceleration of technological innovation in glass core substrates in the future. Moreover, this marks an important step for China in building its own technological ecosystem in the AI-era semiconductor field. This movement has the potential to alter the long-term balance of power in the global semiconductor industry.

Source: https://www.trendforce.com/news/2026/08/07/news-18-chinese-enterprises-accelerate-positions-in-glass-core-substrate-market/

Collected: August 07, 2026 | Automated Research System (Gemini API)

#13 Supercomputing News Emphasizes Critical Role of Advanced Packaging (CoWoS, EMIB, T-AI) in AI Accelerators

Published August 06, 2026 Supercomputing News Global



OVERVIEW

Supercomputing News published an analytical article emphasizing the critical role of advanced packaging technologies like CoWoS, EMIB, and T-AI in enhancing AI accelerator performance. These technologies resolve data transfer bottlenecks between processors and memory, dramatically improving AI workload efficiency. The article highlights advanced packaging as a primary means to achieve performance gains beyond Moore's Law.

IN DEPTH

Key Findings

Supercomputing News has published a detailed analytical article underscoring the indispensable role of advanced packaging technologies such as CoWoS, EMIB, and T-AI in overcoming performance bottlenecks for Artificial Intelligence (AI) accelerators. These technologies are proving to be crucial enablers for extending computing capabilities beyond the conventional limits of Moore's Law.

Technical Details

- **CoWoS (Chip-on-Wafer-on-Substrate):** Developed by TSMC, this 2.5D packaging technology integrates multiple logic dies and High Bandwidth Memory (HBM) onto a silicon interposer, achieving high-density interconnects. This dramatically increases data transfer speeds between the processor and memory.
- **EMIB (Embedded Multi-die Interconnect Bridge):** An Intel-developed technology that embeds small silicon bridges within the package substrate, enabling high-speed connections between different dies. This eliminates the need for a full interposer, offering high bandwidth while reducing cost and complexity.
- **T-AI (Through-put AI):** This term generally refers to a comprehensive packaging and system integration approach optimized for AI workloads, rather than a specific packaging technology. It signifies a combination of design philosophies and technologies aimed at maximizing the processing efficiency of AI accelerators.
- These technologies deliver the immense data transfer capabilities and low latency required for AI model training and inference, providing performance gains at levels unattainable with conventional packaging.

Background & Context

As AI model sizes grow and data center computing demands surge, the performance of AI accelerators often becomes the system's bottleneck. Specifically, the data transfer speed between the CPU or GPU and HBM is a primary limiting factor for overall performance. Advanced packaging technologies address this bottleneck by tightly integrating multiple chips, allowing them to function effectively as a 'single super-chip.' This represents the forefront of semiconductor innovation in the AI era.

Strategic Significance & Outlook

Advanced packaging technologies like CoWoS, EMIB, and T-AI will be pivotal in shaping the future evolution of AI accelerators. Further maturation and cost-efficiency improvements in these technologies will accelerate the proliferation of more powerful and energy-efficient AI systems. Semiconductor manufacturers are mandated to increase investments in these packaging solutions to drive the next generation of AI innovation. This will be a decisive differentiator in the global technology race.

Source: https://www.supercomputing.news/emerging/advanced-packaging-cowos-emib-t-ai-accelerator-bottleneck

Collected: August 07, 2026 | Automated Research System (Gemini API)

#14 Silicon Box Ships Over 500 Million Chiplet Packages from Singapore, Scaling Manufacturing Output

Published August 07, 2026 Digital Journal (PR-Zen) Singapore

OVERVIEW

Singapore-based advanced packaging company Silicon Box announced it has shipped over 500 million chiplet packages. This marks a significant milestone demonstrating the company's manufacturing capability and the maturity of its advanced packaging technology. Serving key markets like AI, HPC, automotive, and consumer electronics, Silicon Box is accelerating the proliferation of the chiplet ecosystem.

IN DEPTH

Key Findings

Silicon Box, an advanced packaging company headquartered in Singapore, has announced that it has shipped over 500 million chiplet packages. This achievement clearly demonstrates the company's capability to deliver chiplet-based solutions at scale and the maturity of its manufacturing technology.

Technical Details

- Silicon Box has developed proprietary lithography, bonding, and redistribution layer (RDL) technologies that enable ultra-fine pitch connections between chiplets. This allows for high-density integration of multiple functional chiplets into a single package.
- The company's solutions are optimized for applications demanding high I/O density and low power consumption, particularly in AI accelerators, high-performance computing (HPC) processors, high-performance mobile System-on-Chips (SoCs), and automotive semiconductors.
- Shipping over 500 million units validates the robustness of their manufacturing process and their ability to achieve high-volume production while meeting stringent quality standards. This is a crucial accomplishment for enhancing the overall reliability of the chiplet ecosystem.

Background & Context

Facing the limits of Moore's Law, the semiconductor industry is rapidly shifting towards a chiplet strategy. Chiplets enable higher performance, lower power consumption, and flexible designs by integrating multiple functional blocks (chiplets) manufactured on different process nodes. Silicon Box has emerged as a key OSAT (Outsourced Semiconductor Assembly and Test service provider) in this new paradigm, and its large-scale production capacity is accelerating the widespread adoption of chiplets.

Strategic Significance & Outlook

Silicon Box's milestone of shipping 500 million units symbolizes the transition of chiplet technology from a mere research phase to a commercially viable, large-scale production solution. The company's growth will strengthen the supply capacity for high-performance semiconductors, essential for the future development of data-intensive applications such as AI, data centers, and autonomous vehicles. Silicon Box, while based in Singapore, is expected to further solidify its position as a strategic player in the global semiconductor supply chain.

Source: https://www.digitaljournal.com/pr/news/pr-zen/silicon-box-ships-500m-units-1843816404.html

Collected: August 07, 2026 | Automated Research System (Gemini API)

#15 TSMC CoWoS Advanced Packaging Becomes Critical Bottleneck in AI Chip Supply, Sold Out Through 2026

Published July 30, 2026 Tech Times USA

OVERVIEW

The bottleneck in AI chip production has shifted from silicon manufacturing to advanced packaging, specifically TSMC's CoWoS technology, with capacity fully booked until the end of 2026. A severe shortage of ABF substrate materials is significantly extending lead times, compelling a structural shift in the supply chain. TSMC plans to nearly quadruple CoWoS production to 130,000 wafers per month by late 2026, with Nvidia projected to consume approximately 60% of this expanded capacity.

IN DEPTH

Key Findings

The manufacturing bottleneck in the artificial intelligence (AI) chip supply chain has decisively shifted from front-end silicon wafer fabrication to advanced back-end packaging, particularly TSMC's Chip-on-Wafer-on-Substrate (CoWoS) technology. Demand for this highly integrated packaging has surged to such an extent that TSMC's CoWoS capacity is completely sold out through the end of 2026, severely constraining the supply of high-performance AI accelerators.

Technical / Clinical Details

CoWoS is a sophisticated 2.5D/3D packaging solution that integrates multiple logic dies and High Bandwidth Memory (HBM) on a single silicon interposer, delivering superior bandwidth and power efficiency crucial for AI, high-performance computing (HPC), and data center applications. Key AI chip developers, like NVIDIA, heavily rely on CoWoS for their cutting-edge designs. However, the complexity and extended cycle times of CoWoS manufacturing, coupled with a critical shortage of essential materials such as Ajinomoto Build-up Film (ABF) substrates, are primary impediments to capacity expansion. According to analysis from AT&S CEO, TSMC aims to expand its monthly CoWoS production capacity from its current levels to 130,000 wafers by late 2026, a nearly fourfold increase. Despite this ambitious expansion, market demand is projected to outstrip supply, with Nvidia alone estimated to consume about 60% of this significantly boosted capacity. This supply-demand imbalance is resulting in significantly longer lead times for advanced packaging.

Background & Context

The rapid advancement of AI technologies has created unprecedented demand for high-performance AI accelerators. These accelerators require highly integrated semiconductor packaging to efficiently process vast amounts of data at high speeds. As traditional semiconductor manufacturing approaches the physical limits of Moore's Law, advanced packaging techniques like CoWoS have emerged as the new frontier for performance gains. Consequently, the back-end process, once a secondary concern, has become the rate-limiting step for overall chip throughput, forcing the semiconductor industry to re-evaluate its investment strategies to include substantial allocation for advanced packaging infrastructure, not just front-end fabrication.

Strategic Significance & Outlook

The acute CoWoS capacity crunch has far-reaching implications across the entire semiconductor supply chain. Manufacturers heavily reliant on CoWoS are exploring alternative packaging technologies and strengthening partnerships with Outsourced Semiconductor Assembly and Test (OSAT) providers to diversify their options. Furthermore, there is an accelerating trend towards increased investment in material suppliers, such as those for ABF substrates, and the establishment of multi-year, long-term supply agreements. While this scenario presents significant growth opportunities for the advanced packaging market, including related materials, equipment manufacturers, and OSAT companies, it also underscores persistent challenges in ensuring a stable supply of AI chips in the foreseeable future.

Source: https://www.semicoregroup.com/news/540004