Semiconductor_BackEnd

Weekly Intelligence Report

2026-08-16 | 35 articles | 9 countries

troy-technical.jp

This Week's Keyword

AI Packaging Bottlenecks

HBM, ABF, and advanced packaging capacity strain AI chip su

35	9	>98	240
articles	countries	%	B USD
Total Articles Analyzed	Source Countries	TSMC CoWoS Yield	2026 Global CapEx

All 35 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	TSMC CoWoS Yield, ABF	Corporate Strategy	●●●○○	●●●●○	●●●●●	●●●●○	●●●●○	TSMC achieves >98% CoWoS yield, but ABF substrates are now the primary bottleneck for AI chip expansion.
#02	NVIDIA Feynman, TSMC SoIC	Corporate Strategy	●●●○○	●●●●○	●●●●○	●●●○○	●●●●○	NVIDIA's Feynman platform accelerates, pushing TSMC to boost SoIC capacity to 50K wafers/month by 2027.
#03	AI Strains CoWoS/SoIC	Market Analysis	●●○○○	●●●●○	●●●●●	●●●○○	●●●●●	Global CoWoS demand to double by 2027, facing 10-20% shortfall, making advanced packaging a critical bottleneck.
#04	Ibiden ¥500B ABF Substrates	Corporate Strategy	●●○○○	●●●●○	●●●●●	●●●●○	●●●●○	Ibiden invests ¥500B in ABF substrates for AI servers, anticipating supply crunch beyond 2028.
#05	KLA $1.1B AP Revenue	Corporate Strategy	●●○○○	●●●●○	●●●○○	●●●●○	●●●●●	KLA forecasts $1.1B in advanced packaging revenue for 2026, driven by AI and HBM demand.
#06	Applied Materials Q3 Rev	Corporate Performance	●●○○○	●●●●○	●●●●○	●●●●○	●●●●●	Applied Materials reports $9.12B Q3 2026 revenue, plans to double semiconductor systems output by 2028.
#07	JEDEC Relaxes HBM4 Height	Standard Update	●●●●○	●●●○○	●●●●○	●●●●○	●●●●○	JEDEC relaxes HBM4 package height to 775 µm, enabling 12-Hi/16-Hi stacks without immediate Cu-Cu hybrid bonding.
#08	TSMC CoWoS/SoIC Bottleneck	Market Analysis	●●○○○	●●●●○	●●●●●	●●●○○	●●●●●	TSMC's CoWoS/SoIC are primary AI chip bottlenecks, forecasting 10-20% global supply shortfall by 2027.
#09	Samsung Unveils zHBM	Research	●●●●●	●●○○○	●●●●●	●●●●○	●●●●○	Samsung unveils zHBM, a 3D logic-memory integrated AI architecture, alongside HBM4E/HBM5 roadmap at FMS 2026.
#10	TSMC/Samsung AP Comp.	Corporate Strategy	●●●○○	●●●●○	●●●●●	●●●○○	●●●●●	TSMC doubles AP capacity but still lags AI demand; Samsung expands 2nm & AP collaboration with Broadcom.
#11	TSMC CoWoS Yield 98-99%	Corporate Strategy	●●●○○	●●●●○	●●●●●	●●●●○	●●●●○	TSMC achieves 98-99% yield for CoWoS 5.5x AI products, targeting 14x reticle size expansion by 2029.
#12	Micron Mass Prod. HBM4	New Product	●●●●○	●●●●●	●●●●●	●●●●○	●●●●●	Micron begins mass production of 36GB 12-layer HBM4 for NVIDIA Vera Rubin, investing $250B in US.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#13	Samsung HBM4 Market Share	Corporate Strategy	●●●○	●●●●	●●●●	●●●○	●●●●	Samsung aggressively invests in HBM4, targeting top market share next year, attracting NVIDIA and AMD interest.
#14	ECTC 2026 Glass/FOPLP	Research	●●●●	●●○○	●●●●	●●●○	●●●●	ECTC 2026 highlights glass substrates and FOPLP as key for next-gen high-density packaging in HPC/AI.
#15	SEMI Europe APC 2026	Market Overview	●●●○	●●●○	●●●●	●●●○	●●●●	SEMI Europe APC 2026 emphasizes 2.5D/3D integration, chiplets, and heterogeneous integration for AI system performance.
#16	SK Hynix HBM4 Price Hike	Corporate Strategy	●●●○	●●●●	●●●●	●●●○	●●●●	SK Hynix raises HBM4 prices by 70%, invests ~$7B in US/Korea packaging to meet AI demand.
#17	AI Shifts to PLP/Glass	Research	●●●●	●●○○	●●●●	●●●○	●●●●	AI demand accelerates shift to Panel Level Packaging (PLP) and glass core substrates for next-gen packaging.
#18	Samsung HBM4 Yield 80%	Corporate Strategy	●●●○	●●●●	●●●●	●●●○	●●●●	Samsung HBM4 yield improves to 80%, intensifying AI memory race as SK Hynix labor talks stall.
#19	2026 Chip Crisis Wake-Up	Market Overview	○○○○	●●●●	●●●●	●●○○	●●●●	The 2026 chip crisis highlights supply chain reliance on semiconductors, with AI demand reshaping requirements.
#20	HBM Supply Crisis to 2027	Market Analysis	○○○○	●●●●	●●●●	●●●○	●●●●	HBM supply crisis to persist until 2027, driven by surging AI demand and equipment backlogs, bottlenecking AI hardware.
#21	3D/2.5D Packaging UCIe	Market Report	●●●○	●●●○	●●●○	●●●○	●●●○	Global 3D/2.5D IC packaging market accelerates with UCIe standard, integrating logic, memory, analog, and RF dies.
#22	IDTechEx 2.5D/3D Trends	Market Analysis	●●●●	●●○○	●●●●	●●●○	●●●●	IDTechEx highlights glass interposers and hybrid bonding as critical emerging trends in 2.5D/3D packaging.
#23	IMAPS DPC 2026 Advances	Market Overview	●●●○	●●●○	●●●●	●●●○	●●●●	IMAPS DPC 2026 details 3D/2.5D packaging advances like FOPLP and hybrid bonding driving demand in key sectors.
#24	HBM Bonding Equip. Crunch	Market Analysis	○○○○	●●●●	●●●●	●●●○	●●●●	HBM supply crunch persists until 2027 due to long backlogs for bonding equipment and low yields.
#25	Samsung EM Glass Substrate	Corporate Strategy	●●●●	●●●○	●●●●	●●○○	●●●○	Samsung Electro-Mechanics accelerates glass substrate bid for AI chips, targeting 2028 mass production.
#26	Samsung EM Util. Rate Soars	Corporate Performance	●●○○	●●●●	●●●○	●●○○	●●●○	Samsung Electro-Mechanics' package substrate utilization rate soars to 89%, driven by AI data center demand.
#27	Applied Mat. AP Forecast	Corporate Strategy	●●○○	●●●●	●●●●	●●●○	●●●●	Applied Materials boosts 2026 advanced packaging revenue growth forecast to over 70% amid AI chip investment.
#28	US Commerce $874M Invest	Policy/Investment	●●○○	●●●●	●●●●	●●●●	●●●●	U.S. Commerce Dept. invests up to $874M in seven semiconductor companies for AI, advanced packaging, and supply chain security.
#29	Samsung EM Vietnam Cap.	Corporate Strategy	●●○○	●●●●	●●●○	●●○○	●●●○	Samsung Electro-Mechanics to more than double advanced packaging substrate capacity for AI semiconductors in Vietnam.
#30	ASMPT Record H1 Sales	Corporate Performance	●●●○	●●●●	●●●○	●●●●	●●●○	ASMPT's advanced packaging business achieves record H1 2026 sales driven by AI demand, with PLP as key future driver.
#31	Intel Foveros/EMIB-T	Corporate Strategy	●●●●	●●●●	●●●●	●●●○	●●●●	Intel Foundry boosts AI data center compute with Foveros and EMIB, planning EMIB-T launch in 2026 for power efficiency.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#32	Global CapEx Surge 2026	Market Analysis	●○○○	●●●●	●●●●	●●●○	●●●●	Global semiconductor capital investment to surge 30% to $240B in 2026, driven by AI inference demand and advanced packaging.
#33	NXP Malaysia Capacity	Corporate Strategy	●●○○	●●●●	●●●○	●●○○	●●●●	NXP Semiconductors doubles Malaysia backend production capacity by Q1 2028; Resonac reports 46% growth for AI backend materials.
#34	Global Sales Soar, TSMC	Market Overview	●●●○	●●●●	●●●●	●●●○	●●●●	Global semiconductor sales soar 2.2x in June 2026; TSMC achieves >99% CoWoS yield but flags HBM and ABF substrate bottlenecks.
#35	TSMC System-Level Valid.	Corporate Strategy	●●●○	●●●●	●●●●	●●●○	●●●●	TSMC declares AI advanced packaging competition shifts to system-level reliability and validation, highlighting 3DIC importance.

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI chip supply chain exposed to ABF substrate shortages?

TSMC and Ibiden highlight ABF substrates as the next major bottleneck for AI chip expansion beyond 2028. With Ajinomoto planning capacity increases through 2030, are your procurement teams securing long-term contracts and exploring alternative materials or suppliers to mitigate this critical risk?

❷ How will HBM4's 70% price hike impact your AI hardware costs?

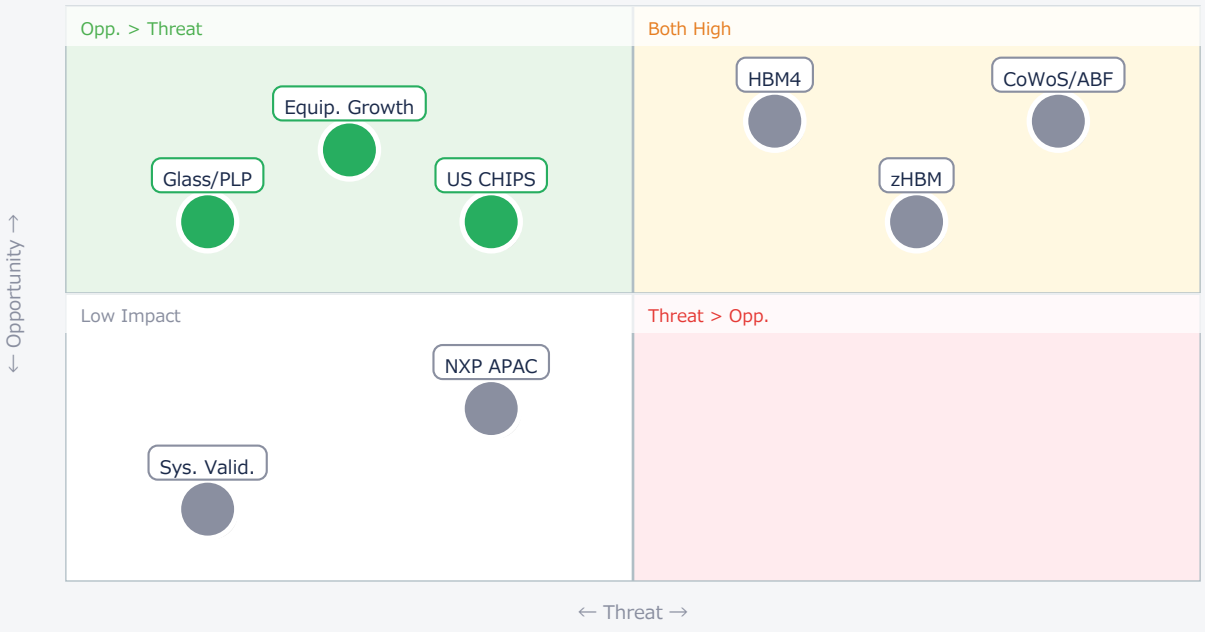
SK Hynix projects a 70% price increase for HBM4, while Micron begins mass production for NVIDIA's Vera Rubin. Given the persistent HBM supply crisis until at least 2027, have your strategic planners modeled the impact of these costs on your AI product roadmap and profitability?

❸ Are you investing in next-gen packaging like glass substrates and PLP?

ECTC and IDTechEx highlight glass substrates and Panel Level Packaging (PLP) as key for future high-density AI/HPC. Samsung Electro-Mechanics targets 2028 mass production. Are your R&D; and Business Development teams actively exploring these technologies for competitive advantage or risk mitigation?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
CoWoS/ABF	Critical	New material sales	AI chip supply risk
HBM4	Critical	Memory market gain	AI system cost hike
zHBM	Critical	Future IP licensing	Competitor lead
Glass/PLP	Opp.	New material market	Incumbent tech shift
US CHIPS	Opp.	Domestic growth	Geo-political risk
Equip. Growth	Opp.	Tool sales boom	Capacity limits
Sys. Valid.	Ref.	Enhanced reliability	Complex design flow

● NXP APAC	Ref.	Regional supply	Increased competition

Deep Dive ① — Micron's HBM4 Mass Production for NVIDIA

#12 | 2026/08/13 | openPR.com | Tech Novelty●●●●○ Proximity●●●●● Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●●

Micron Technology has commenced mass production of its 36GB 12-layer HBM4 memory, shipping to NVIDIA for its Vera Rubin platform. This marks a significant leap in high-bandwidth memory, crucial for next-gen AI accelerators.

The move underscores the rapid shift towards higher-capacity, higher-bandwidth memory, with Micron planning over $250 billion in US semiconductor manufacturing and R&D; investment by 2035 to meet AI-driven demand.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: Micron's HBM4 mass production is a critical development, validating the market's rapid shift to higher-density HBM. While the 36GB 12-layer HBM4 is a significant performance boost, the $250B US investment by 2035 is a long-term play, and immediate HBM supply constraints will persist. [Opportunity] for US/EU OEMs to secure advanced memory supply from a domestic vendor, enhancing supply chain resilience. [Threat] for non-HBM memory suppliers and for OEMs reliant on competitors' HBM. Next Actions: [Procurement] Engage Micron immediately to understand HBM4 allocation and pricing. [R&D;] Begin designing next-gen AI platforms around HBM4 capabilities, by Q4 2026.

Deep Dive ② — Samsung Unveils zHBM: 3D Logic-Memory AI

#09 | 2026/08/12 | Samsung Semiconductor | Tech Novelty●●●●● Proximity●●○○○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●○

Samsung unveiled zHBM, a novel 3D logic-memory integrated AI architecture, alongside its HBM4E/HBM5 roadmap at FMS 2026. This solution integrates logic and memory in three dimensions, drastically shortening data movement distances.

zHBM aims to mitigate traditional data transfer bottlenecks, promising significant enhancements in AI processing efficiency. This breakthrough positions Samsung as a leader in future AI memory solutions, impacting fundamental AI chip design.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: Samsung's zHBM concept represents a significant academic breakthrough in memory architecture, potentially redefining AI chip design. While its proximity to market is low (likely 5+ years for commercialization), the published vision is highly ambitious and technically sound for addressing the memory wall. [Opportunity] for US/EU IP holders and R&D; firms to explore similar 3D logic-memory integration concepts or collaborate with Samsung. [Threat] for US/EU AI chip designers if Samsung gains a proprietary, unmatchable lead in integrated AI memory. Next Actions: [R&D;] Form a task force to evaluate zHBM's architectural implications and competitive landscape by Q1 2027. [Strategy] Assess potential licensing or partnership opportunities with Samsung or other 3D integration leaders.

Deep Dive ③ — ABF Substrates: The Next AI Bottleneck

#01 | 2026/08/12 | Xenospectrum | Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●●○ US/EU Relevance●●●●○

TSMC announced its advanced CoWoS packaging technology consistently achieves yields exceeding 98% for 5.5x reticle AI chip products. However, the primary supply chain bottleneck is shifting from HBM memory to ABF substrates.

This highlights a critical material constraint for future AI chip expansion. Ajinomoto plans significant ABF capacity increases through 2030, but demand continues to outpace supply, impacting global AI chip production.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: TSMC's high CoWoS yield is realistic, reflecting mature process control, but the shift to ABF as the primary bottleneck is a critical, near-term concern. The technical barrier is scaling production of increasingly large and complex ABF substrates reliably. [Opportunity] for US/EU materials and chemical suppliers to innovate and expand production of alternative high-performance substrates or ABF-like films. [Threat] for US/EU OEMs and device manufacturers facing potential delays and increased costs for AI accelerators due to ABF shortages. Next Actions: [Procurement] Conduct an immediate audit of ABF substrate exposure in AI product lines. [R&D;] Initiate research into alternative substrate materials or design modifications to reduce ABF reliance, by Q4 2026.

Other Notable Articles

Applied Materials Reports $9.12 Billion in Q3 2026 Revenue (GlobeNewswire)
Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●○

Applied Materials' strong Q3 revenue and plan to double output by 2028 signal robust equipment demand for AI.

JEDEC Relaxes HBM4 Package Height to 775 µm (Exponential Industry)
Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○

JEDEC's HBM4 height relaxation enables higher stacks without immediate hybrid bonding, offering design flexibility.

2026 Chip Crisis Sounds Hardware Wake-Up Call (Trax Technologies)
Tech Novelty●○○○○ Proximity●●●●● Market Impact●●●●●

The 2026 chip crisis underscores AI's profound impact on supply chains, demanding resilience and diversification.

Intel Foundry Boosts AI Data Center Compute with Foveros and EMIB (ET Datacenters)
Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●○

Intel's Foveros and EMIB-T (2026) advance AI data center compute, improving power efficiency and HBM support.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Conduct an emergency audit of ABF substrate and HBM supply chain exposure for all AI-related product lines.
- [R&D;] Initiate a rapid assessment of alternative advanced packaging materials and architectures (e.g., glass substrates) for future designs.

Short-term (1 month)

- [Strategy] Review and update AI chip sourcing strategies to diversify suppliers and mitigate risks from HBM price hikes and packaging bottlenecks.
- [Business Dev] Explore strategic partnerships with advanced packaging equipment and material suppliers to secure future capacity and technology access.
- [Executive] Mandate cross-functional teams (R&D;, Procurement, Strategy) to develop a comprehensive AI supply chain resilience plan.

Medium-long term (quarter+)

- [R&D;] Invest in domestic or regional advanced packaging R&D; and manufacturing capabilities, potentially leveraging CHIPS Act incentives.
- [Legal/IP] Monitor competitor advancements in 3D logic-memory integration (e.g., Samsung's zHBM) for potential IP licensing or defensive strategies.
- [Procurement] Establish long-term, multi-vendor contracts for critical packaging materials and HBM to ensure supply stability beyond 2027.

Semiconductor_BackEnd — Selected Articles

Date: 2026-08-16

Articles: 35

Table of Contents

#17 AI Accelerates Shift to Panel Level Packaging (PLP) and Glass Core Substrates, Positioning Them as Pillars of Next-Gen Packaging

#18 Samsung HBM4 Yield Dramatically Improves from Under 60% to 80%; SK Hynix Labor Talks Stall, Intensifying AI Memory Race

#19 2026 Chip Crisis Sounds Hardware Wake-Up Call: AI Demand Reshaping Semiconductor Supply Chains

#20 HBM Supply Crisis of 2026 Projected to Persist Until 2027, Redefining AI Hardware Deployment Bottleneck

#21 Bonafide Research: Global 3D/2.5D IC Packaging Market Accelerates with UCIe Standard, Forecasts Growth Through 2031

#22 IDTechEx Analyzes New 2.5D/3D Semiconductor Packaging Trends: Glass Interposers and Hybrid Bonding Drive Evolution

#23 IMAPS Device Packaging Conference 2026 Details 3D/2.5D Packaging Advances: FOPLP, Hybrid Bonding Drive Demand

#24 HBM Supply Crunch: Long Backlogs for Bonding Equipment and Low Yields Create Bottleneck, Constraining AI Demand Until 2027

#25 Samsung Electro-Mechanics Accelerates Glass Substrate Bid for AI Chips, Targets 2028 Mass Production Against Japanese Rival

#26 Samsung Electro-Mechanics Sees Semiconductor Package Substrate Utilization Rate Soar to 89%, Driven by AI Data Center Demand

#27 Applied Materials Boosts 2026 Advanced Packaging Revenue Growth Forecast to Over 70% Amid Expanding AI Chip Investment in HBM and Multi-Layer Packaging

#28 U.S. Commerce Department to Invest Up to $874 Million in Seven Semiconductor Companies Across AI, Advanced Packaging, and Supply Chain Security

#29 Samsung Electro-Mechanics to More Than Double Advanced Packaging Substrate Capacity for AI Semiconductors at Vietnam Plant

#30 ASMPT's Advanced Packaging Business Achieves Record H1 2026 Sales Driven by Surging AI Demand; Panel-Level Packaging Positioned as Key Future Growth Driver

#31 Intel Foundry Boosts AI Data Center Compute with Foveros and EMIB Advanced Packaging, EMIB-T Launch Planned for 2026

#32 Global Semiconductor Capital Investment to Surge 30% to $240 Billion in 2026, Driven by AI Inference Demand; Advanced Packaging Fuels Multi-Year Double-Digit Growth

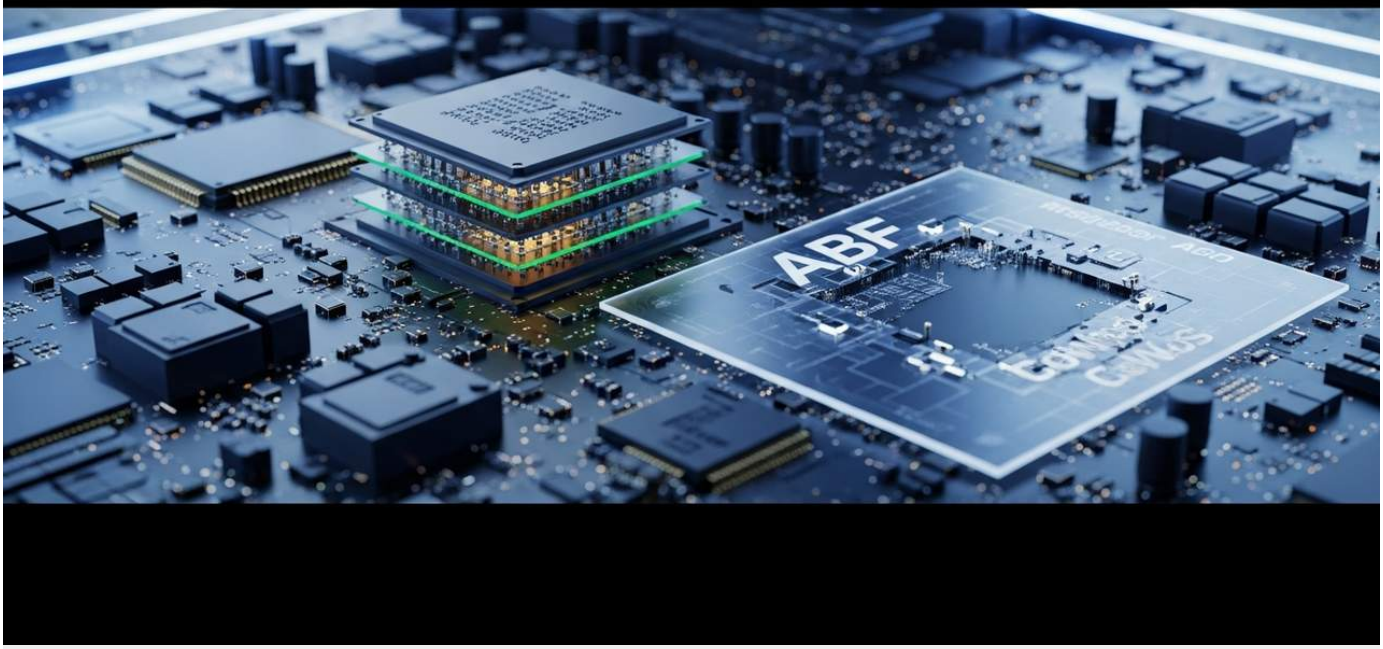
#33 NXP Semiconductors Doubles Malaysia Backend Production Capacity, Targeting Q1 2028 Operation; Resonac Reports 46% Revenue Growth for AI Backend Materials

#34 Global Semiconductor Sales Soar 2.2x to Record $134.5 Billion in June 2026; TSMC Achieves Over 99% CoWoS Yield But Flags HBM and ABF Substrate Bottlenecks

#35 TSMC Declares AI Advanced Packaging Competition Shifts to System-Level Reliability and Validation, Highlighting 3DIC Importance at OCP APAC 2026

#01 TSMC Achieves Over 98% CoWoS Yield; ABF Substrates Emerge as Next Bottleneck for AI Chip Expansion

Published August 12, 2026 Xenospectrum Taiwan



OVERVIEW

TSMC has announced that its advanced CoWoS packaging technology, particularly for 5.5x reticle AI chip products, consistently achieves yields exceeding 98%. While CoWoS capacity has doubled annually for three consecutive years, nearly meeting demand, the primary supply chain bottleneck is shifting from HBM memory to ABF substrates. The company's SoIC technology, with 6-micron hybrid bonding pitches already in mass production, targets a further reduction to 4.5 microns by 2029. This shift highlights a critical material constraint for future AI chip expansion, prompting suppliers like Ajinomoto to plan significant ABF capacity increases through 2030 and beyond.

IN DEPTH

Key Findings

TSMC has publicly confirmed that its advanced CoWoS packaging technology, specifically for 5.5x reticle-sized AI-related products, has achieved stable yields of over 98%. This high yield is critical as CoWoS capacity has doubled annually for the past three years, bringing it "very close" to meeting current demand. However, a new critical bottleneck is emerging within the semiconductor supply chain: ABF (Ajinomoto Build-up Film) substrates, which are now identified as the next major constraint for the expansion of AI chip production, surpassing previous concerns regarding High Bandwidth Memory (HBM) supply.

Technical / Clinical Details

According to Jun He, TSMC's Vice President of Advanced Packaging Technology and Services, the company's CoWoS technology demonstrates exceptional production efficiency for high-performance AI chips. Furthermore, TSMC's SoIC (System-on-Integrated-Chips) technology is entering a high-growth phase, with 6-micron hybrid bonding pitches already in mass production. Plans are underway to shrink this pitch to 4.5 microns by 2029, enabling even denser 3D stacking. The CoWoS roadmap includes scaling to 14x reticle sizes by 2029, facilitating the integration of larger and more complex AI accelerators.

Background & Context

The burgeoning demand for artificial intelligence has dramatically increased the requirements for advanced chip packaging. Technologies like CoWoS and SoIC, which enable 2.5D and 3D integration of various dies (logic, memory), are essential for achieving higher data transfer rates and lower power consumption. While HBM supply has been a previous point of concern, industry efforts have largely addressed this, leading to improved availability. The focus has now shifted to ABF substrates, a crucial insulating material for high-performance IC package substrates. The increasing complexity and size of AI processors necessitate larger and more advanced ABF substrates, making their constrained supply a significant impediment to the industry's growth.

Strategic Significance & Outlook

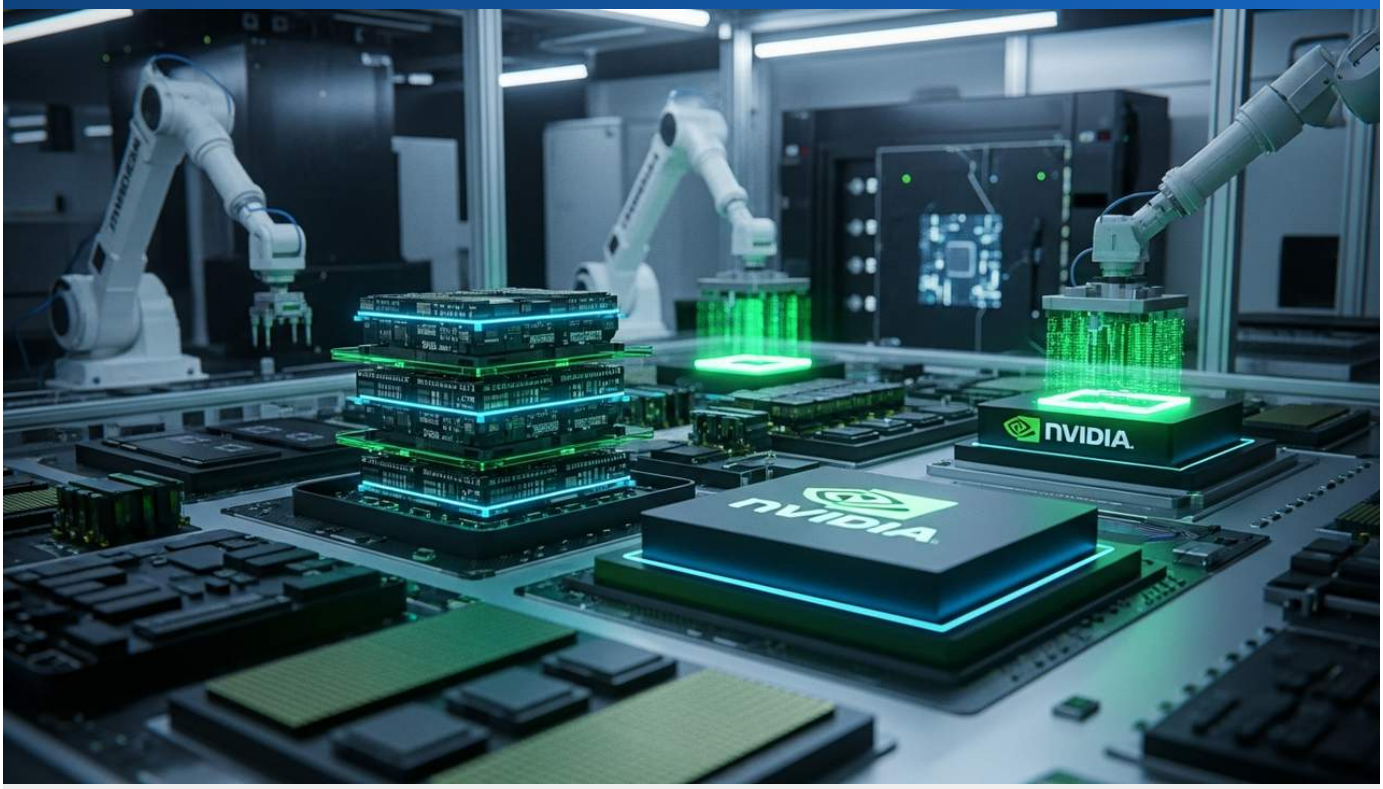
To mitigate the ABF substrate shortage, Ajinomoto, a leading global supplier, is planning to progressively expand its production capacity at facilities including its Gunma plant through 2030. Additionally, the company is considering a third factory to meet demand beyond 2030, aiming for long-term supply stability. TSMC's advancements in SoIC and CoWoS expansion plans are foundational for future AI and High-Performance Computing (HPC) chip performance. However, the overall balance of the supply chain, particularly the stable supply of critical materials like ABF, will be a decisive factor in the continued growth and innovation within the semiconductor industry.

Source: https://xenospectrum.com/en/tsmc-cowos-memory-abf-bottlenecks/

Collected: August 14, 2026 | Automated Research System (Gemini API)

#02 NVIDIA Accelerates Feynman AI Platform; TSMC Ramps SoIC Capacity to 50K Wafers/Month by 2027

Published August 14, 2026 Benzinga Taiwan



OVERVIEW

NVIDIA is expediting the roadmap for its next-generation Feynman AI platform, prompting TSMC to significantly boost its advanced packaging capabilities. TSMC is rapidly expanding its SoIC technology production, accelerating construction of AP7 in Chiayi and AP8 in Southern Taiwan Science Park. Supply chain sources indicate SoIC monthly production capacity is projected to increase from 20,000 wafers to 50,000 wafers by the end of 2027, supporting NVIDIA's adoption of the A16 process, SoIC 3D stacking, and co-packaged optics (CPO) integration.

IN DEPTH

Key Findings

NVIDIA is accelerating the deployment roadmap for its next-generation Feynman AI platform, targeting a debut in late 2028. In response, TSMC is aggressively expanding its advanced packaging capacity, particularly for SoIC (System-on-Integrated-Chips) technology. Construction of the AP7 facility in Chiayi and AP8 in the Southern Taiwan Science Park is being expedited, with TSMC's monthly SoIC production capacity projected to increase to approximately 50,000 wafers by the end of 2027.

Technical / Clinical Details

NVIDIA's Feynman platform is designed to directly utilize TSMC's cutting-edge A16 process and significantly increase the integration of SoIC 3D stacking and Co-Packaged Optics (CPO) technologies. SoIC represents TSMC's advanced 3D chiplet technology, which involves vertically stacking multiple chiplets to substantially improve data transfer efficiency and power efficiency. CPO, by integrating optical interconnects directly within the package, dramatically enhances inter-chip communication speeds. These technologies are crucial for elevating AI chip performance to the next generation, and TSMC's capacity expansion is a powerful enabler for NVIDIA's innovative AI product launches.

Background & Context

The explosive growth in AI demand has created an unprecedented need for advanced packaging capacity within the semiconductor industry. AI accelerators, which require high-speed processing of vast amounts of data, are highly dependent on advanced packaging technologies like CoWoS (Chip-on-Wafer-on-Substrate) and SoIC. NVIDIA's acceleration of the Feynman platform reflects intense competition in the AI market and the urgent need for more powerful AI infrastructure. TSMC's capacity expansion is a strategic move to meet these market pressures and solidify its leadership in the AI semiconductor supply chain.

Strategic Significance & Outlook

TSMC is preparing capacity for a diverse range of advanced packaging solutions, including SoIC, CoWoS-L, and the next-generation CoPoS (Chip-on-Package-on-Substrate) technologies. The plan to increase SoIC monthly production capacity from 20,000 wafers by the end of 2026 to 50,000 wafers by the end of 2027 will significantly contribute to stabilizing the supply and enhancing the performance of future AI chips. This aggressive investment and technological development are expected to accelerate innovation in semiconductor back-end processes and potentially set new benchmarks for computing power in the AI era.

Source: https://www.benzinga.com/markets/tech/26/08/61201714/nvidias-next-gen-feynman-ai-platform-is-ramping-up-forcing-tsmc-to-race-ahead-report

Collected: August 14, 2026 | Automated Research System (Gemini API)

#03 AI Demand Strains CoWoS and SoIC Supply: Global Demand to Double to Over 2.5M Wafers by 2027, Facing 10-20% Shortfall

Published August 11, 2026 Exponential Industry USA

OVERVIEW

TSMC's CoWoS and SoIC advanced packaging technologies are now the primary physical constraints for AI GPU and accelerator production. Global CoWoS demand is projected to double from 1.3-1.4 million wafers in 2026 to 2.5-2.7 million wafers by 2027, with supply still anticipated to fall short by 10-20%. While TSMC is constructing additional advanced packaging facilities in Chiayi and OSAT partners like ASE/SPIL and Amkor are expanding capacity, the supply-demand gap persists.

IN DEPTH

Key Findings

TSMC's advanced packaging technologies, CoWoS and SoIC, represent the most significant physical bottlenecks in the production of AI GPUs and accelerators today. Global demand for CoWoS is projected to almost double from 1.3-1.4 million wafers in 2026 to an estimated 2.5-2.7 million wafers by 2027. Despite significant investments in capacity expansion by TSMC and its partners, the supply of advanced packaging is still anticipated to be 10-20% short of demand, posing a critical challenge for the rapidly expanding AI sector.

Technical / Clinical Details

CoWoS (Chip-on-Wafer-on-Substrate) is a leading 2.5D packaging technology that horizontally integrates multiple chips, such as High Bandwidth Memory (HBM), onto an interposer. SoIC (System-on-Integrated-Chips), on the other hand, is TSMC's proprietary 3D packaging technology that vertically stacks chiplets, enabling higher integration density and shorter interconnect paths. As AI applications demand ever-increasing performance, these technologies are vital for maximizing the processing power and efficiency of AI processors. Specifically, AI GPUs and accelerators require memory bandwidths reaching hundreds of gigabytes per second to terabytes per second, a feat largely enabled by CoWoS integration of HBM.

Background & Context

The escalating complexity and scale of AI models have pushed traditional 2D packaging to its performance limits, accelerating the transition to advanced packaging technologies. The expansion of AI workloads in data centers and cloud infrastructure is driving the demand for high-performance AI chips, leading to unprecedented requirements for CoWoS and SoIC packaging capacity. TSMC is responding with massive investments, including the construction of new advanced packaging facilities in Chiayi. Major OSAT (Outsourced Semiconductor Assembly and Test) providers like ASE/SPIL and Amkor are also collaborating to boost capacity. However, the growth in demand continues to outpace these supply-side augmentations.

Strategic Significance & Outlook

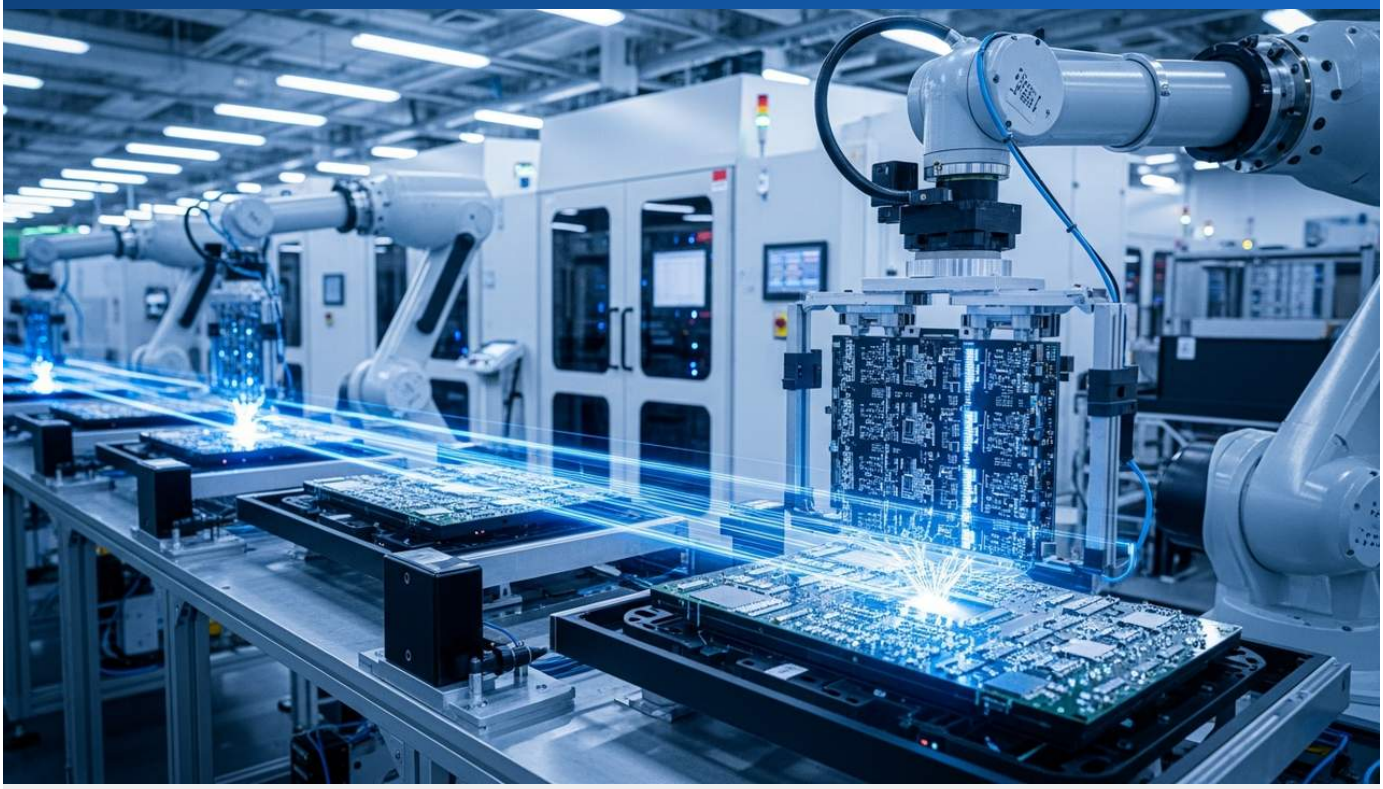
The persistent supply-demand gap in advanced packaging could impact the volume and market expansion of AI chips in the short term. This situation not only compels TSMC and OSAT companies to make further investments but also intensifies the competition in developing new packaging materials and equipment. Furthermore, customer companies may explore strengthening relationships with multiple suppliers or investing in their own in-house packaging technology development to diversify supply chain risks. In the long run, this bottleneck is expected to accelerate further innovation in packaging technologies and the establishment of more efficient production processes, ultimately shaping the future trajectory of the semiconductor industry.

Source: https://exponentialindustry.com/blog/2026-08-10-tsmc-cowos-soic-ai-advanced-packaging-bottleneck/

Collected: August 14, 2026 | Automated Research System (Gemini API)

#04 Ibiden Commits ¥500 Billion to ABF Substrates for AI Servers, Anticipating Supply Crunch Beyond 2028

Published August 06, 2026 MK Japan



OVERVIEW

Ibiden, the world's leading AI substrate manufacturer, announced a ¥500 billion investment from this year to 2028 to expand production capacity for IC package substrates for AI and high-performance servers. Despite long-term contracts securing ABF substrates until 2028, customers are pushing for accelerated capacity expansion and joint investments, fearing shortages in 2029 and 2030. Strong ABF demand has also led to a surge in orders for vacuum laminate equipment, impacting related companies like Eternal Precision Mechanics.

IN DEPTH

Key Findings

Ibiden, the world's leading manufacturer of AI substrates, has unveiled plans for a substantial investment of ¥500 billion (approximately $3.2 billion USD) from this year through 2028. This capital injection is dedicated to significantly expanding its production capacity for IC package substrates tailored for AI and high-performance servers, directly addressing the critical supply shortage of ABF (Ajinomoto Build-up Film) substrates driven by the exponential growth in AI demand.

Technical / Clinical Details

ABF substrates are indispensable as insulating materials in high-performance semiconductor packages, enabling numerous wiring layers and intricate circuit formation, particularly for AI chips and high-performance CPUs/GPUs. Modern high-performance semiconductors demand more cores and higher I/O densities, necessitating larger and more complex ABF substrates. Ibiden’s investment aims to bolster production lines for these advanced ABF substrates to meet surging demand. Despite customers securing ABF substrates through long-term contracts until 2028, concerns about supply tightness in 2029 and 2030 are driving them to actively request further accelerated capacity expansion and, in some cases, joint capital expenditures from substrate manufacturers, including Ibiden.

Background & Context

The evolution of AI is profoundly impacting the entire semiconductor industry, especially increasing the importance of back-end packaging technologies and their associated materials. ABF substrates are a critical component for 2.5D/3D packaging solutions like TSMC’s CoWoS, and their potential as a bottleneck to maximizing AI chip performance has been widely noted. This robust demand has also led to a surge in orders for vacuum laminate equipment used in ABF substrate manufacturing, creating significant business opportunities for related equipment manufacturers such as Eternal Precision Mechanics, a subsidiary of Eternal Materials. Furthermore, TSMC executives have consistently highlighted ABF, alongside HBM memory, as one of the most severe shortages in the semiconductor industry, confirming Ibiden’s pivotal role as a major beneficiary in this landscape.

Strategic Significance & Outlook

Ibiden's substantial investment is crucial for supporting the ongoing development of AI infrastructure. While this investment is expected to stabilize supply by 2028, AI demand is anticipated to remain robust beyond 2029, necessitating continued collaboration and investment across the industry. Key suppliers like Ajinomoto are also making efforts to stabilize supply, with plans to progressively expand ABF capacity by 2030 and a third factory under consideration for post-2030 demand. The stable supply of ABF substrates will be a decisive factor in the development and mass production of next-generation AI chips and is essential for enhancing the overall resilience of the semiconductor supply chain.

Source: https://www.mk.co.kr/en/business/12119467

Collected: August 14, 2026 | Automated Research System (Gemini API)

#05 KLA Forecasts $1.1 Billion in Advanced Packaging Revenue for 2026, Driven by Surging AI and HBM Demand

Published August 10, 2026 Quartz USA

OVERVIEW

KLA Corporation anticipates its advanced packaging business revenue will reach approximately $1.1 billion in 2026, representing over 70% year-over-year growth, fueled by increasing AI infrastructure investments and semiconductor complexity. Strong demand across CoWoS and emerging SoIC packaging technologies is driving the need for more sophisticated inspection and metrology tools to support hybrid bonding and nanometer-level precision requirements. AI expenditures, HBM, and advanced packaging are expected to continue driving KLA's robust growth through 2027.

IN DEPTH

Key Findings

KLA Corporation projects significant growth in its advanced packaging business, with revenue from its semiconductor process control portfolio in this segment expected to climb from approximately $635 million in 2025 to roughly $1.1 billion in 2026. This represents a robust year-over-year growth exceeding 70%, underpinned by accelerating AI infrastructure investments and the increasing complexity of semiconductor devices.

Technical / Clinical Details

KLA's growth is primarily driven by strong demand for cutting-edge packaging technologies like TSMC's CoWoS and the rapidly emerging SoIC. These advanced methods necessitate hybrid bonding between dies and demand extremely high precision in alignment, inspection, and metrology at the nanometer level. KLA's process control systems are indispensable for meeting these stringent requirements, playing a critical role in defect detection and measurement at every stage of the packaging process. As semiconductor devices increase in integration and value, the structural importance of advanced process control for maximizing production yields grows, directly benefiting KLA.

Background & Context

With the explosive expansion of demand for AI and High-Performance Computing (HPC), advancements in semiconductor chip performance are now heavily reliant not only on miniaturization but also on the evolution of advanced packaging technologies. The increasing adoption of HBM (High Bandwidth Memory) and the proliferation of chiplet architectures escalate packaging complexity, thus requiring more sophisticated inspection and metrology solutions. KLA offers a comprehensive suite of process control solutions, spanning from early semiconductor manufacturing stages to back-end packaging, and has demonstrated agile responsiveness to these market shifts. Compared to competitors, KLA's broad portfolio and technological advantages solidify its leadership in the rapidly growing advanced packaging market.

Strategic Significance & Outlook

KLA expects AI-related capital expenditures, rising HBM demand, and the expansion of the advanced packaging market to continue driving its strong revenue growth through 2027. The structural changes within the semiconductor industry, characterized by increasing device complexity and value, will permanently elevate the importance of process control. KLA's strategy involves sustained investment in research and development to deliver solutions that address the new challenges posed by next-generation packaging technologies, thereby maintaining long-term growth. This approach is anticipated to further strengthen its dominant position in the advanced packaging market.

Source: https://qz.com/can-kla-s-advanced-packaging-strength-support-1b-revenue-target

Collected: August 14, 2026 | Automated Research System (Gemini API)

#06 Applied Materials Reports $9.12 Billion in Q3 2026 Revenue, Plans to Double Semiconductor Systems Output by 2028 Amid Surging Demand

Published August 13, 2026 GlobeNewswire USA

OVERVIEW

Applied Materials announced Q3 2026 revenue of $9.12 billion, marking a 25% year-over-year increase and slightly exceeding market expectations. The company maintains strong leadership and a pipeline of innovative next-generation solutions in DRAM, leading-edge foundry logic, and advanced packaging, projecting robust revenue and margin growth beyond 2027. Driven by expanding AI computing infrastructure, Applied Materials plans to double its quarterly semiconductor systems output by 2028 to meet increasing demand.

IN DEPTH

Key Findings

Applied Materials reported its Q3 2026 results (through July), achieving revenues of $9.12 billion, a 25% increase year-over-year, slightly surpassing market expectations. This growth is primarily driven by the expansion of AI computing infrastructure, which is boosting demand for equipment in DRAM, leading-edge foundry logic, and advanced packaging. In response to this escalating demand, the company announced an ambitious plan to double its quarterly output of semiconductor systems from current levels by 2028.

Technical / Clinical Details

As a leading semiconductor equipment manufacturer, Applied Materials provides industry-leading, innovative solutions across DRAM, advanced logic processes, and advanced packaging. Sophisticated packaging technologies, such as TSMC's CoWoS and SoIC 2.5D/3D integration, necessitate precise thin-film deposition, etching, and inspection processes, for which Applied Materials supplies high-precision tools. The company's technologies are fundamental to supporting the performance enhancement and mass production of next-generation AI chips, addressing the complex requirements of back-end processes like HBM stacking and chiplet integration.

Background & Context

The global acceleration of investments in AI, High-Performance Computing (HPC), and data center infrastructure is propelling the semiconductor industry into a period of historic growth. AI accelerators, in particular, require not only advanced processing capabilities but also highly sophisticated packaging technologies to handle vast amounts of data at high speeds and efficiency. Applied Materials' strong performance is a testament to its strategic response to these market trends, through both technological innovation and capacity expansion. Leveraging its extensive technical expertise and broad customer base, the company plays a crucial role across the entire semiconductor supply chain.

Strategic Significance & Outlook

Applied Materials emphasized its strong leadership position and pipeline of innovative next-generation solutions in the DRAM, leading-edge foundry logic, and advanced packaging markets, projecting robust revenue and margin growth beyond 2027. The plan for additional manufacturing capacity, aiming to double quarterly output by 2028, signifies a long-term commitment to meeting the sustained semiconductor demand in the AI era. This strategic expansion suggests that Applied Materials will continue to drive growth within the semiconductor industry and contribute to the proliferation of advanced technologies.

Source: https://ir.appliedmaterials.com/news-releases/news-release-details/applied-materials-announces-third-quarter-2026-results

#07 JEDEC Relaxes HBM4 Package Height to 775 µm, Enabling 12-Hi/16-Hi Stacks Without Immediate Cu-Cu Hybrid Bonding

Published August 12, 2026 Exponential Industry USA

OVERVIEW

JEDEC has relaxed the HBM4 package height specification from 720 µm to 775 µm, allowing for 12-Hi and 16-Hi stack HBM modules without immediate reliance on Cu-Cu hybrid bonding. HBM utilizes 3D stacked DRAM dies connected via TSVs and microbumps, interfacing with accelerators through 2.5D interposers like TSMC CoWoS. Vendor-specific bonding methods include SK Hynix's MR-MUF and Samsung/Micron's TCB-NCF.

IN DEPTH

Key Findings

JEDEC (Joint Electron Device Engineering Council) has made a significant decision to relax the HBM4 (High Bandwidth Memory 4) package height specification, increasing it from the previous 720 µm to 775 µm. This modification is a crucial step toward enabling 12-Hi and 16-Hi stack HBM modules without the immediate necessity of adopting the more complex copper-to-copper (Cu-Cu) hybrid bonding technology. This provides manufacturers with greater flexibility to increase HBM capacity and performance.

Technical / Clinical Details

HBM is an advanced memory technology that involves vertically stacking multiple DRAM dies through TSVs (Through-Silicon Vias) and microbumps. These stacked HBM dies are then connected to logic chips, such as GPUs and AI accelerators, via a 2.5D interposer, exemplified by TSMC's CoWoS (Chip-on-Wafer-on-Substrate) technology. This architecture delivers extremely high memory bandwidth and low power consumption. JEDEC's package height relaxation facilitates HBM manufacturers in stacking more dies while temporarily mitigating the increase in packaging complexity and cost, thereby achieving higher capacities. Current HBM production employs vendor-specific bonding methods; for instance, SK Hynix uses MR-MUF (Mass Reflow-Molded Underfill), while Samsung and Micron utilize TCB-NCF (Thermo-Compression Bonding with Non-Conductive Film). These techniques are optimized to ensure high connection reliability at fine bump pitches.

Background & Context

The rapid advancements in high-performance computing fields such as AI, HPC, and data centers have exponentially increased the demand for memory bandwidth and capacity. HBM, with its superior performance, has become the de facto standard for meeting these requirements. JEDEC's specification relaxation aims to foster further HBM evolution, establishing an environment for future AI accelerators to process larger models more efficiently. Furthermore, with the accelerated adoption of chiplet architectures, heterogeneous integration of multiple dies within a single package is becoming commonplace, driving demand for interconnect precision below 5 microns. This trend further underscores the critical importance of HBM and advanced packaging technologies.

Strategic Significance & Outlook

The relaxation of HBM4 package height temporarily reduces a technical barrier for HBM manufacturers in developing and mass-producing higher-capacity HBM products. This could accelerate the market introduction cycle for HBM and further drive innovation in the AI and HPC sectors. While a transition to more advanced connection technologies like Cu-Cu hybrid bonding is inevitable in the long term, this relaxation serves as a technological bridge during the interim period. The evolution of HBM is expected to continue stimulating innovation in back-end packaging technologies, material development, and equipment advancement, playing an indispensable role in enhancing the performance of next-generation AI infrastructure.

Source: https://exponentialindustry.com/blog/2026-08-11-hbm-stacking-architecture-packaging-market-guide/

Collected: August 14, 2026 | Automated Research System (Gemini API)

#08 TSMC CoWoS & SoIC Packaging Become Primary AI Chip Bottleneck, Forecasting 10-20% Global Supply Shortfall by 2027 Amidst Doubling Demand

Published August 11, 2026 Exponential Industry Taiwan

OVERVIEW

TSMC's CoWoS and SoIC packaging technologies are identified as the primary physical constraints in AI GPU and accelerator production. Global CoWoS demand is projected to double from 1.3-1.4 million wafers in 2026 to 2.5-2.7 million in 2027. Despite capacity expansions by TSMC and OSAT partners, the industry faces a significant 10-20% supply deficit by 2027, severely impacting AI hardware deployment.

IN DEPTH

Key Findings

TSMC's advanced packaging technologies, specifically CoWoS (Chip-on-Wafer-on-Substrate) and SoIC (System-on-Integrated-Chips), have emerged as the paramount physical constraints in the production of AI GPUs and accelerators. Global demand for CoWoS packaging alone is projected to nearly double from an estimated 1.3-1.4 million wafers in 2026 to 2.5-2.7 million wafers in 2027. Despite aggressive capacity expansions by TSMC and its OSAT (Outsourced Semiconductor Assembly and Test) partners, the industry is anticipated to face a substantial 10-20% supply shortfall by 2027, indicating a persistent bottleneck that will significantly impact the rollout of AI hardware.

Technical / Clinical Details

CoWoS is a sophisticated 2.5D packaging technique that utilizes micro-bump flip-chip bonding to integrate High Bandwidth Memory (HBM) stacks with logic dies, such as GPUs, onto a silicon interposer. This architecture is crucial for achieving the high bandwidth and low latency required for intensive AI workloads. SoIC, an even more advanced 3D stacking technology, employs sub-micron pitch direct copper-to-copper hybrid bonding, allowing for ultra-fine vertical interconnects between dies. This direct bonding approach maximizes data transfer efficiency and dramatically boosts overall system performance. Both CoWoS and SoIC are at the forefront of heterogeneous integration, enabling the complex, high-performance computing required for advanced AI models.

Background & Context

The burgeoning AI industry has created an unprecedented surge in demand for high-performance AI semiconductors. GPUs and accelerators from companies like NVIDIA rely heavily on advanced packaging solutions like TSMC's CoWoS and SoIC to deliver their full computational power. However, these complex packaging processes demand specialized equipment, highly skilled labor, and extended manufacturing lead times, making rapid capacity scaling a significant challenge. While TSMC dominates the advanced packaging market, even its substantial investments are struggling to keep pace with the exponential growth in AI demand. OSAT partners are also increasing their investments, but the technical hurdles of these advanced processes prevent quick closures of the supply gap.

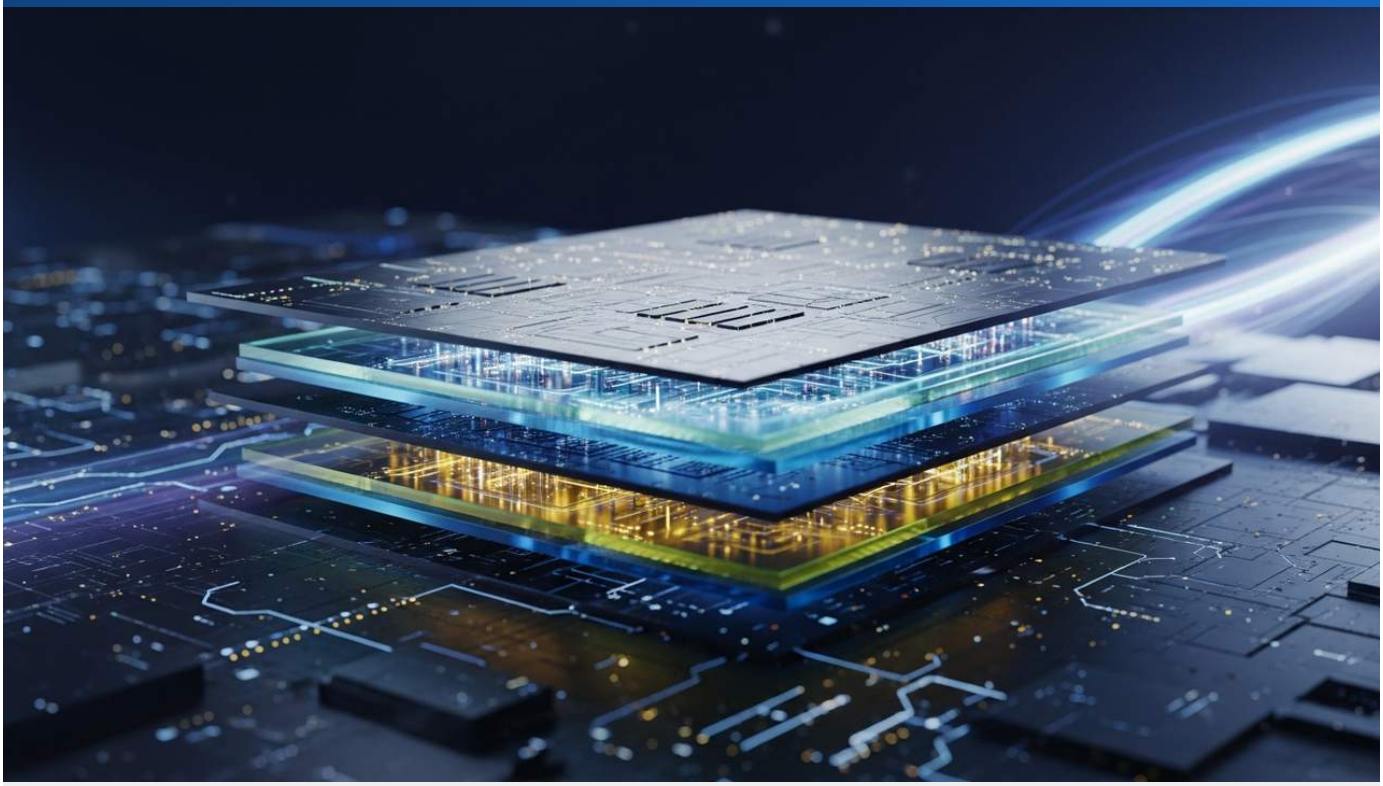
Strategic Significance & Outlook

The persistent supply crunch in CoWoS and SoIC packaging represents a critical challenge for the AI industry in the short to medium term. This bottleneck is expected to drive up AI chip prices, delay product deliveries, and potentially slow down investments in AI infrastructure. While TSMC and OSATs are committed to further capacity expansions, demand is likely to continue outstripping supply beyond 2027. The industry must explore new packaging architectures, diversify supply chains, and optimize resource allocation to mitigate this constraint. Ultimately, the development of even higher-integration, more efficient next-generation packaging solutions will be key to unlocking the full potential of AI.

Source: https://vertexaisearch.cloud.google.com/grounding-api-redirect/AUZIYQHodwvDy4xioEjjl05wjHfgv-dEWDJY0EXhk8MV65O07YQMBVwmxz-Ij1-6Ok8EZ3zzPzxudrgHpv3md76_TRMN1xq9z32-NCw5RNhwDTHB_1wVsOw6xvSMvUNn7MOPM4-PrJB4eJISMLCDiNR0pi1wwjxlxNxUQMqHqIgXqrNnzUCziAIAWg5xKMnTzCUd5qFzl2NdI9-Rw1OdqA==

#09 Samsung Unveils zHBM, a 3D Logic-Memory Integrated AI Architecture, Alongside HBM4E/HBM5 Roadmap at FMS 2026

Published August 12, 2026 Samsung Semiconductor South Korea



OVERVIEW

Samsung presented its vision for next-generation AI infrastructure at FMS 2026, unveiling its HBM roadmap, including HBM4E and HBM5, and a novel 3D memory architecture called zHBM. This zHBM solution integrates logic and memory in three dimensions, drastically shortening data movement distances and mitigating traditional data transfer bottlenecks. This breakthrough promises to significantly enhance AI processing efficiency and positions Samsung as a leader in future AI memory solutions.

IN DEPTH

Key Findings

Samsung unveiled an ambitious vision for future AI infrastructure at the Flash Memory Summit (FMS) 2026, introducing a next-generation HBM roadmap encompassing HBM4E and HBM5, and a groundbreaking AI memory architecture dubbed 'zHBM.' This zHBM concept aims to revolutionize AI processing by integrating logic and memory in a true 3D fashion, significantly reducing the physical distance for data movement. The solution is specifically designed to alleviate the persistent data transfer bottlenecks observed in conventional systems, promising a dramatic leap in AI computational efficiency.

Technical / Clinical Details

The zHBM architecture moves beyond traditional HBM stacks, which primarily consist of vertically stacked DRAM dies connected to a logic die. Instead, zHBM envisions direct 3D integration of specific logic functionalities either within the HBM stack itself or in its immediate vicinity. This tight integration minimizes the physical distance and latency of data transfer between DRAM and the main processor, a critical factor for AI workloads. While current HBM technologies connect through silicon interposers, zHBM's closer integration promises to drastically increase effective data bandwidth and improve power efficiency. The forthcoming HBM4E and HBM5 iterations will further enhance bandwidth through increased data channel counts and faster interface speeds, meeting the escalating performance demands of AI accelerators. These advancements are poised to fundamentally address the compute-memory data transfer bottleneck, especially critical for training large language models (LLMs) and complex neural networks.

Background & Context

As AI workloads, particularly deep learning models, continue to scale in computational complexity, the speed of data transfer between processors and memory (memory bandwidth) has become a primary limiting factor for overall system performance. HBM technology was developed precisely to alleviate this bottleneck and has seen widespread adoption in AI GPUs and High-Performance Computing (HPC) applications. However, even with the advent of HBM3E, the relentless pace of AI innovation demands even greater bandwidth and efficiency. Samsung's initiatives with zHBM and next-generation HBM are a direct response to these market requirements, forming a strategic pillar to bolster its competitiveness in the AI semiconductor market. Rival companies are also actively pursuing advanced memory and 3D integration solutions, making this a crucial battleground in the semiconductor industry.

Strategic Significance & Outlook

3D integrated memory architectures like zHBM are set to become indispensable components in future AI system designs. Resolving data movement bottlenecks directly translates to shorter AI model training times, improved inference efficiency, and the feasibility of building larger, more complex AI models. Samsung aims to solidify its leadership in the AI era by offering comprehensive turnkey solutions that integrate its foundry, memory, and advanced packaging expertise. The industry will closely watch how zHBM is implemented in AI accelerators and its real-world performance validation. This technology holds the potential to revolutionize not only AI but also a broad spectrum of applications including HPC and edge AI devices.

Source: https://semiconductor.samsung.com/news-events/tech-blog/samsung-presents-its-vision-for-next-generation-ai-infrastructure-with-3d-memory-architecture-at-fms-2026/

Collected: August 16, 2026 | Automated Research System (Gemini API)

#10 TSMC Doubles Advanced Packaging Capacity Over Three Years; Samsung Expands 2nm & Advanced Packaging Collaboration with Broadcom

Published August 13, 2026 BigGo Finance Taiwan

OVERVIEW

TSMC revealed it has doubled its advanced packaging capacity annually for the past three years but still lags behind surging AI chip demand, operating 10 dedicated facilities globally. Meanwhile, Samsung Electronics is intensifying its collaboration with Broadcom, focusing on 2nm-and-below foundry processes and advanced packaging alongside HBM supply. Samsung is accelerating 2nm mass production infrastructure at its Taylor, Texas plant, aiming to reclaim market share in the fiercely competitive AI chip arena.

IN DEPTH

Key Findings

TSMC has announced that it has doubled its advanced packaging capacity annually over the past three years in response to the explosive demand for AI semiconductors. However, the company acknowledged that it still cannot fully meet the escalating AI chip demand, indicating ongoing supply constraints. In contrast, Samsung Electronics is expanding its strategic collaboration with Broadcom, aiming to provide comprehensive semiconductor solutions that include not only High Bandwidth Memory (HBM) supply but also cutting-edge 2nm-and-below foundry processes combined with advanced packaging. Samsung is particularly accelerating the establishment of 2nm mass production infrastructure at its Taylor, Texas facility, signaling a clear intent to strengthen its competitive position in the next-generation AI chip market.

Technical / Clinical Details

TSMC's advanced packaging capabilities are primarily concentrated on 2.5D/3D integration technologies like CoWoS (Chip-on-Wafer-on-Substrate) and SoIC (System-on-Integrated-Chips), which are critical for enhancing the performance of AI GPUs and accelerators. The 10 dedicated packaging facilities operated globally by TSMC represent substantial investments and profound technical expertise required for these complex processes. Samsung's strategy, on the other hand, is built on a 'turnkey solution' approach that integrates its memory, foundry, and packaging divisions. The expanded collaboration with Broadcom aims to deliver optimal 2nm process technology for high-performance AI chip designs, coupled with advanced HBM and packaging solutions (e.g., interposer-based packaging like I-Cube, and future 3D stacking). This integrated offering seeks to provide customers with a one-stop solution for advanced AI. The investment in the Taylor, Texas plant is a crucial step to secure the mass production of this 2nm technology, notably featuring Gate-All-Around (GAA) transistor technology.

Background & Context

The explosive growth of AI is driving significant structural changes in the semiconductor industry. Beyond traditional processor performance, factors such as high-performance memory like HBM and the advanced packaging technologies that integrate them are now critical determinants of AI chip performance and supply. TSMC has long been the leader in advanced packaging, but the rapid surge in demand has highlighted supply limitations. Samsung, leveraging its synergistic strengths in memory, foundry, and packaging, is aggressively investing and forming strategic alliances to challenge TSMC's dominance. Broadcom, a leading player in high-performance networking chips and AI accelerators, extending its partnership with Samsung, could significantly influence the entire AI chip ecosystem. The 2nm process technology is particularly vital for next-generation AI chips due to its performance and power efficiency advantages, making securing mass production capability in this node a decisive competitive factor.

Strategic Significance & Outlook

The fierce competition between TSMC and Samsung in advanced packaging and process technology is expected to intensify further in the coming years. While TSMC continues to scale its existing CoWoS/SoIC capabilities, addressing new supply chain bottlenecks like ABF substrates remains a challenge. Samsung aims to expand its market share in AI semiconductors through early mass production of 2nm technology and strengthening collaborations with key customers like Broadcom. This competition will accelerate the performance improvement and cost efficiency of AI chips, ultimately fostering the broader adoption of AI applications. The capital expenditure race between these two giants will also create significant business opportunities for semiconductor equipment manufacturers and material suppliers worldwide.

Source: https://finance.biggo.com/news/d0aa8655-6d69-45dd-8169-1be4da3c1792

#11 TSMC Achieves 98-99% Yield for AI Products on CoWoS 5.5x Process, Targets 14x Reticle Size Expansion by 2029

Published August 12, 2026 Wccftech Taiwan

OVERVIEW

TSMC Vice President Ho Chun announced remarkable 98% to 99% yields for multiple AI-related products assembled using the CoWoS 5.5x process. This exceptional achievement highlights TSMC's manufacturing prowess in highly complex advanced packaging. He further revealed TSMC's plan to significantly scale CoWoS technology to a 14x reticle size by 2029, a strategic move to accommodate the increasing performance demands of future AI chips.

IN DEPTH

Key Findings

TSMC Vice President Ho Chun publicly announced that multiple AI-related products, assembled using the company's CoWoS (Chip-on-Wafer-on-Substrate) 5.5x reticle size process, are achieving an impressive yield rate of 98% to 99%. This figure unequivocally demonstrates TSMC's superior manufacturing efficiency and quality in the highly intricate field of heterogeneous integration packaging for AI chips. Furthermore, Vice President Ho unveiled an ambitious roadmap to significantly expand CoWoS technology from its current 5.5x to a 14x reticle size by 2029.

Technical / Clinical Details

CoWoS is a critical 2.5D packaging technology essential for maximizing the performance of AI accelerators by integrating high-performance logic dies with HBM (High Bandwidth Memory) on a silicon interposer. Achieving 98-99% yield in this technology signifies TSMC's mature process control capabilities and advanced automation in micro-bump flip-chip bonding, silicon interposer fabrication, and subsequent packaging stages. Challenges associated with scaling packaging capabilities to over three times the photomask size include managing warpage in large interposers, ensuring the integrity of multi-layer structures, and addressing the complexities of thermal management. TSMC's planned expansion to a 14x reticle size is crucial for integrating even more AI chiplets and HBM stacks within a single package, thereby meeting the massive computational power and memory bandwidth demands of next-generation AI models. This scale-up necessitates further innovations in manufacturing equipment, materials, and process technology.

Background & Context

The rapid evolution of AI, particularly generative AI, has fueled an explosive demand for high-performance AI semiconductors. For these AI chips, not only computational power but also memory bandwidth and efficiency are paramount, making advanced packaging technologies like CoWoS a critical bottleneck. TSMC's achievement of high yields demonstrates its capacity to meet these challenging market requirements and contributes to stabilizing the supply of AI chips. While competitors are also accelerating investments in advanced packaging, TSMC's CoWoS technology maintains its position as an industry benchmark. This announcement reassures investors and customers of TSMC's long-term strategy to address future AI demand, bringing stability to the entire semiconductor supply chain.

Strategic Significance & Outlook

The continuous evolution of TSMC's CoWoS technology, especially its expansion to a 14x reticle size by 2029, will elevate AI chip performance and integration density to new levels. This will enable the training and inference of larger and more complex AI models, further broadening the application scope of AI. However, the advancement of such large-scale packaging technologies simultaneously requires innovations in substrate materials, cooling solutions, and testing methodologies. TSMC's CoWoS strategy will not only solidify its leadership in the AI era but also profoundly influence the overall technology roadmap and competitive landscape of the semiconductor industry.

Source: https://wccftech.com/tsmc-exec-makes-big-announcement-confirms-98-yield-for-cowos-packaged-ai-chips/

#12 Micron Initiates Mass Production of 36GB 12-Layer HBM4 for NVIDIA Vera Rubin, Boosts US Semiconductor Investment Over $250 Billion

Published August 13, 2026 openPR.com USA

OVERVIEW

Micron Technology commenced mass production of its advanced 36GB 12-layer HBM4 memory in March 2026, shipping to NVIDIA for its Vera Rubin platform. This move underscores the market's rapid shift towards higher-capacity, higher-bandwidth memory driven by escalating AI computational loads. Micron also announced plans to increase its US semiconductor manufacturing and R&D investment to over $250 billion by 2035 to meet AI-driven demand, reinforcing its leadership in next-generation AI infrastructure.

IN DEPTH

Key Findings

Micron Technology announced the commencement of mass production for its innovative 36GB 12-layer HBM4 memory in March 2026, with shipments already underway to NVIDIA for its next-generation AI platform, Vera Rubin. This significant milestone highlights Micron's robust position in the AI accelerator market and the rapid evolution of high-bandwidth memory technology. Furthermore, Micron revealed plans to substantially increase its total semiconductor manufacturing and technology R&D investments in the United States to over $250 billion by 2035, aiming to address the accelerating demand for advanced memory driven by AI.

Technical / Clinical Details

HBM4 offers significantly higher bandwidth compared to its predecessor, HBM3E, through an increased number of data channels and improved interface speeds. Micron's 36GB 12-layer HBM4 achieves its high density and performance by vertically stacking 12 DRAM dies, integrated using Through Silicon Via (TSV) technology and micro-bump bonding. This high-density, high-performance memory is indispensable for supporting the immense data processing capabilities required by state-of-the-art AI GPUs and accelerators like NVIDIA's Vera Rubin. HBM4 dramatically enhances computational speed and efficiency in data-intensive AI workloads, including large language model (LLM) training and inference, High-Performance Computing (HPC), and data center applications. The adoption of HBM4 not only boosts the overall performance of AI systems but also contributes to improved power efficiency, fostering the development of more sustainable AI infrastructure.

Background & Context

The increasing complexity and scale of AI models have led to the 'memory wall' problem, where the data transfer rate between the processor and memory becomes a bottleneck for overall system performance. HBM technology was developed to address this issue and has become a de facto standard in the AI semiconductor industry. While HBM3E is expected to remain a crucial technology in 2026, the transition to HBM4 is an inevitable trend, with major memory manufacturers accelerating production and qualification. Micron's mass production of HBM4 and shipments to NVIDIA will intensify competition with rivals like SK Hynix and Samsung in the HBM market. The substantial investment plan in the United States aligns with government initiatives like the CHIPS Act, aiming to strengthen domestic semiconductor manufacturing capabilities and enhance supply chain resilience.

Strategic Significance & Outlook

Micron's initiation of HBM4 mass production and its supply to the NVIDIA Vera Rubin platform marks a critical turning point in the evolution of the AI accelerator market. The widespread adoption of HBM4 is expected to dramatically enhance the performance of AI applications, enabling the development of more advanced AI models. Furthermore, the investment exceeding $250 billion in the United States reflects Micron's strong commitment to establishing long-term leadership not only in HBM but also across a broad spectrum of advanced semiconductor technologies. This strategy will allow the company to build a robust foundation for meeting the demands of next-generation AI infrastructure and further expand its influence in the global semiconductor supply chain. The coming period will see intensified competition in HBM4 market share and continued technological innovation.

Source: https://www.openpr.com/news/4602776/high-bandwidth-memory-market-2026-ai-accelerators-and-hbm4

Collected: August 16, 2026 | Automated Research System (Gemini API)

#13 Samsung's Aggressive HBM4 Investment Targets Top HBM Market Share Next Year, Attracting NVIDIA and AMD Interest

Published August 08, 2026 Sammy Fans South Korea

OVERVIEW

According to UBS forecasts, Samsung Electronics is poised to become the world's leading HBM memory manufacturer next year, driven by aggressive investments and expanded production in HBM4. The rapid surge in HBM demand, fueled by increasing data processing in AI systems, makes HBM4 adoption a key factor. HBM4 doubles data channels from 1,024 to 2,048, enabling ultra-fast data transfer between memory and AI chips. Samsung's intensified investment in manufacturing facilities and strong interest from major AI chip vendors like NVIDIA and AMD underscore its strategic push.

IN DEPTH

Key Findings

According to the latest forecasts from UBS, Samsung Electronics is strategically positioned to capture the top global market share in HBM memory next year, driven by its aggressive investments and enhanced production capacity for HBM4, the next generation of High Bandwidth Memory. This projection comes amidst an explosive increase in HBM demand, propelled by the escalating data processing requirements of AI systems. The early and large-scale transition to HBM4 technology is identified as a primary catalyst for Samsung's potential market leadership. Reports also indicate strong interest in Samsung's HBM4 technology from leading AI chip manufacturers such as NVIDIA and AMD.

Technical / Clinical Details

HBM4 is designed to deliver a significant leap in data transfer performance compared to previous HBM generations. One of its most crucial improvements is the doubling of data channels from the HBM3E standard of 1,024 bits to 2,048 bits. This dramatically expands the data bandwidth between memory and AI chips (GPUs, ASICs, etc.), enabling the ultra-fast data movement essential for training and inference of large-scale AI models. HBM4 achieves high density and efficient memory solutions by vertically stacking multiple DRAM dies using Through Silicon Via (TSV) technology and connecting them at ultra-fine pitches. Samsung is intensifying its investments in advanced manufacturing facilities to scale HBM4 production, focusing on yield improvement and cost efficiency. This technology is expected to play a vital role in resolving memory bottlenecks and maximizing overall system performance in sectors such as AI data centers, High-Performance Computing (HPC), and autonomous automotive systems.

Background & Context

The evolution of AI is transforming the semiconductor industry, making the supply of high-bandwidth memory like HBM a key determinant of AI chip performance, alongside processor computational power. Currently, SK Hynix leads the HBM market, but Samsung is pursuing a tripartite strategy encompassing memory, foundry, and packaging to regain market dominance. As HBM4 is poised to become a critical component of next-generation AI chips, its development and the establishment of mass production capabilities are strategically paramount for major memory manufacturers. The reported interest from leading AI chip companies like NVIDIA and AMD reflects high confidence in Samsung's technological capabilities and supply capacity, which is expected to further intensify the market share competition.

Strategic Significance & Outlook

Samsung's substantial commitment to HBM4 has the potential to significantly reshape the competitive landscape of the AI memory market. Should Samsung successfully achieve early mass production, ensure quality stability, and secure supply to key customers, it could rapidly bolster its presence in the HBM market. Capturing the top market share next year would be a crucial milestone in solidifying Samsung's leadership in the AI era. This heightened competition will accelerate technological innovation, ultimately leading to the introduction of more powerful and efficient AI systems to the market. The HBM4 generation competition will be a critical factor influencing the overall development of the AI industry.

Source: https://www.sammyfans.com/2026/08/08/samsungs-hbm4-push-could-help-it-take-the-top-spot-next-year/

Collected: August 16, 2026 | Automated Research System (Gemini API)

#14 ECTC 2026 Highlights Advanced Packaging Future: Glass Substrates and FOPLP at the Core of System Innovation

Published August 11, 2026 Advanced Packaging Magazine USA

OVERVIEW

ECTC 2026 emphasized a structural shift in semiconductor innovation, moving beyond transistor scaling to packaging and integration technologies. Noteworthy advancements in heterogeneous integration, hybrid bonding, advanced substrates, photonic packaging, and thermal management were highlighted. Glass substrates and Fan-Out Panel Level Packaging (FOPLP) were identified as key technologies with significant potential for next-generation high-density packaging platforms, crucial for HPC and AI applications.

IN DEPTH

Key Findings

The 2026 Electronic Components and Technology Conference (ECTC 2026) clearly underscored a significant paradigm shift in semiconductor innovation, moving from traditional transistor scaling to advanced packaging and integration technologies. The conference prominently featured the latest advancements in heterogeneous integration, hybrid bonding, innovative advanced substrates, photonic packaging, and sophisticated thermal management solutions. Particularly, glass substrates and Fan-Out Panel Level Packaging (FOPLP) garnered substantial attention as next-generation high-density packaging platforms, identified as essential technologies for enhancing the performance of High-Performance Computing (HPC) and AI applications.

Technical / Clinical Details

Heterogeneous integration involves combining multiple dies (chiplets) with different functionalities into a single package, thereby improving overall system performance, power efficiency, and functionality. Hybrid bonding is a key enabler, offering direct copper-to-copper bonding between chips at sub-micron pitches, drastically increasing interconnect density and data transfer speeds compared to traditional micro-bumps. At ECTC 2026, glass substrates were specifically discussed as a promising solution for next-generation high-density packaging. Compared to silicon interposers, glass substrates offer easier large-area scaling, superior electrical properties, enhanced mechanical stability, and the potential for more cost-effective manufacturing. Furthermore, Fan-Out Panel Level Packaging (FOPLP) is gaining traction as a technology that processes chips on larger panel sizes, allowing for more units per batch than wafer-level packaging, thus reducing manufacturing costs while achieving high integration density. These technologies are crucial for optimizing the balance of performance, power, and cost in complex systems integrating AI processors and HBM (High Bandwidth Memory).

Background & Context

With the perceived limits of Moore's Law, the semiconductor industry is finding it increasingly difficult to sustain performance improvements solely through transistor miniaturization. Consequently, packaging technology has emerged as a new frontier driving system-level innovation. The demand from compute-intensive applications like AI and HPC accelerates this trend, necessitating packaging solutions that offer higher performance, bandwidth, lower latency, and greater power efficiency. Emerging technologies such as glass substrates and FOPLP are vital for overcoming the limitations of conventional organic substrates and silicon interposers to meet these demands. The discussions at the conference signify that these technologies are transitioning from research phases towards practical implementation, charting the course for the industry's future direction.

Strategic Significance & Outlook

Glass substrates and FOPLP are expected to play pivotal roles in the future advanced packaging market. Their adoption is likely to accelerate in sectors requiring high-density and high-performance semiconductors, including AI accelerators, data centers, and automotive electronics. FOPLP, in particular, holds the potential to reduce the cost of high-performance packages through economies of scale in manufacturing. Over the next few years, further research and development, along with industry standardization, are anticipated to drive the commercialization of these technologies. The insights from ECTC 2026 suggest that these advancements will form the next wave of semiconductor innovation, establishing new paradigms for system performance.

Source: https://advancedpackaging.news/article/125052/Advanced_packaging_moves_to_the_center_of_system_innovat

Collected: August 16, 2026 | Automated Research System (Gemini API)

#15 SEMI Europe APC 2026 Discusses Power and Interconnect Innovations Driving AI System Performance: 2.5D/3D Integration, Chiplets, and Heterogeneous Integration as Key

Published Published August 15, 2026 SEMI Europe ヨーロッパ

OVERVIEW

The Advanced Packaging Conference (APC) 2026 convened to address the critical role of power delivery and interconnect innovations in driving AI system performance. As traditional device scaling approaches its limits, advanced packaging (AP) and test technologies, including 2.5D/3D integration, chiplets, and heterogeneous integration, are now indispensable for achieving next-generation compute power, bandwidth, and functionality while concurrently reducing power consumption.

IN DEPTH

Background

The relentless advancement of cutting-edge technologies—including Artificial Intelligence (AI), High-Performance Computing (HPC), autonomous vehicles, and 5G communications—is placing unprecedented demands on semiconductor chips across performance, power consumption, and form factor. As the rate of traditional CMOS scaling decelerates, the semiconductor industry is undergoing a profound paradigm shift, redefining packaging from a mere protective function to a primary enabler of system performance improvement and functional expansion. The discussions at SEMI Europe's APC 2026 underscored this industry-wide transformation, signaling advanced packaging's central role in innovation. Innovations in interconnects, enabling high-density power delivery and robust signal transmission, are especially critical for determining the power efficiency and throughput of modern AI accelerators.

Key Findings

The 2026 Advanced Packaging Conference (APC), organized by SEMI Europe, placed a central focus on innovations in power management and interconnect technologies—both indispensable for enabling high-performance AI systems. A key consensus emerged: as traditional device scaling, achieved through transistor miniaturization, approaches its physical and economic limits, advancements in advanced packaging (AP) and test technologies are now critical for sustaining system-level performance gains. Specifically, the conference highlighted 2.5D/3D integration, chiplet architectures, heterogeneous integration, and advanced substrate and interconnect technologies as pivotal for dramatically enhancing computing power, data bandwidth, and functionality, all while effectively reducing overall power consumption.

Technical Details

2.5D/3D integration technologies enable unprecedented integration density and performance by moving beyond the constraints of monolithic chips. This is achieved either by placing multiple semiconductor dies with diverse functionalities onto a silicon interposer (2.5D) or by stacking them vertically (3D). Chiplet architectures facilitate the construction of sophisticated System-on-Chips (SoCs) by assembling smaller, functionally specific 'chiplets,' thereby enhancing design flexibility, improving manufacturing yield, and reducing costs. Heterogeneous integration further optimizes system efficiency and performance by judiciously combining chiplets fabricated using disparate processes—such as logic, memory, analog, and RF components. These integrated approaches are vital for overcoming data movement bottlenecks and enhancing power efficiency in solutions like CoWoS (Chip-on-Wafer-on-Substrate), which integrates High Bandwidth Memory (HBM) directly with AI processors. Furthermore, advanced substrate technologies are instrumental in enabling fine-pitch wiring and low-loss signal transmission, which are critical for superior high-frequency characteristics and enhanced thermal management. Complementing these, precise interconnect technologies are paramount for ensuring signal integrity and long-term reliability within these increasingly complex packaging structures.

Strategic Significance & Outlook

Sustained innovation in advanced packaging and testing is an absolute imperative for future performance scaling in AI and HPC systems. Technologies such as 2.5D/3D integration, chiplets, and heterogeneous integration are poised for broader adoption and standardization in the coming years. This evolution will empower designers to efficiently construct increasingly complex and high-performance systems, thereby unlocking new applications and significant market opportunities. The strategic direction articulated at APC 2026 unequivocally signals the semiconductor industry's commitment to prioritizing innovation in packaging and interconnects, charting a course towards a more sustainable and high-performance computing future.

Source: https://www.semiconeuropa.org/APC

#16 SK Hynix Raises HBM4 Prices by 70% Amidst Over 60% HBM Market Share, Accelerates ~$7 Billion Packaging Investment in US and Korea

Published Published August 15, 2026 SK Hynix (Facebook関連アカウント) South Korea

OVERVIEW

SK Hynix, commanding over 60% of the high-bandwidth memory (HBM) market, projects a nearly 70% price increase for its next-generation HBM4, slated for 2026. To meet soaring AI demand, the company is committing approximately $7 billion, including a new $3.87 billion advanced packaging facility in Indiana, USA, and doubling wafer production capacity in Korea, to accelerate HBM4 market entry and alleviate memory bottlenecks with its high-speed 2048-bit interface.

IN DEPTH

Background

The rapid evolution of artificial intelligence is instigating a profound structural transformation within the semiconductor industry, where the demand for high-bandwidth memory (HBM) consistently outstrips existing supply. SK Hynix, recognized as a pioneer in HBM technology, has solidified its position as a critical supplier to leading AI chip manufacturers, including NVIDIA, thereby securing a dominant market share. While SK Hynix leads, formidable competitors such as Samsung and Micron are also vigorously pursuing HBM4 development and expanding their production capacities, intensifying the competitive landscape within the HBM market. SK Hynix's substantial investment in the U.S. aligns strategically with U.S. government initiatives promoting domestic semiconductor manufacturing, such as the CHIPS Act, aiming for geographical diversification of the supply chain and contributions to regional economic development.

Key Findings

SK Hynix, capitalizing on its commanding market share exceeding 60% in the High Bandwidth Memory (HBM) sector, has announced an anticipated price increase of approximately 70% for its forthcoming HBM4 generation, slated for 2026. This assertive pricing strategy underscores the exponential surge in AI demand and the prevailing tight supply of HBM. To meet the escalating need for AI memory, the company intends to double its wafer production capacity, which includes establishing a new manufacturing facility in Korea, alongside a significant $3.87 billion (approximately 550 billion KRW) investment in an advanced packaging plant in Indiana, USA. These substantial capital injections, totaling roughly $7 billion, are strategically designed to alleviate existing AI memory supply bottlenecks and accelerate the market introduction of HBM4.

Technical Details: HBM4 Architecture and Performance

HBM4 is engineered to deliver a substantial uplift in data bandwidth and efficiency over its predecessor, HBM3E. A pivotal feature of HBM4 is its 2048-bit interface width, which is projected to theoretically double the data transfer rate compared to HBM3E's 1024-bit interface. This expanded interface is crucial for optimizing data flow between AI processors and memory, thereby significantly mitigating computational bottlenecks prevalent in High-Performance Computing (HPC) applications. These applications include, but are not limited to, large language model (LLM) training, high-resolution image processing, and complex scientific simulations. SK Hynix's advanced packaging facilities will play a critical role in enhancing the miniaturization and reliability of HBM stacking technology, particularly through refined die-to-die connections utilizing Through Silicon Via (TSV) technology. The new Indiana plant is anticipated to not only significantly boost HBM4 production capacity but also forge a resilient supply chain foundation within the U.S., strategically addressing potential geopolitical supply risks. Furthermore, the plan to double wafer production capacity is an essential measure to secure the foundational DRAM chip supply required for HBM and establish a robust mass production system for HBM4.

Strategic Significance and Market Outlook

SK Hynix's dual strategy of aggressive HBM4 pricing and substantial global investments is set to profoundly reshape the dynamics of the AI memory market. The HBM4's 2048-bit interface is anticipated to deliver a dramatic performance uplift for AI and HPC applications, thereby enabling the conceptualization and deployment of vastly more complex and data-intensive AI models. The establishment of an advanced packaging facility in the U.S. will serve to fortify the global semiconductor supply chain and ensure a more stable supply of critical AI chips. Industry observers will closely scrutinize how SK Hynix capitalizes on its technological leadership in the HBM4 market to distinguish itself from its rivals. This strategic maneuver is also expected to catalyze new business opportunities for semiconductor equipment manufacturers and material suppliers, further accelerating the overall development of the semiconductor industry in the ongoing AI era.

Source: https://www.facebook.com/fb-answers/sk-hynix-hbm-ai-memory-outlook-2026/

#17 AI Accelerates Shift to Panel Level Packaging (PLP) and Glass Core Substrates, Positioning Them as Pillars of Next-Gen Packaging

Published August 15, 2026 IEEE / Presentation USA

OVERVIEW

Driven by soaring demand from AI, automotive electronics, and consumer devices, advanced packaging is a critical enabler for enhanced performance, higher integration, and miniaturization in semiconductors. Panel Level Packaging (PLP) and glass core substrates are emerging as key next-generation platforms shaping the industry's future. While PLP promises reduced manufacturing costs and large package scalability, challenges like warpage control and thermal robustness persist. These technologies are poised to deliver indispensable solutions for high-performance chips in the AI era.

IN DEPTH

Key Findings

With the surging demand from Artificial Intelligence (AI), automotive electronics, and consumer devices, advanced packaging is now recognized as the most critical driver for achieving enhanced chip performance, higher integration, and miniaturization in the semiconductor industry. Within this context, two innovative technologies, Panel Level Packaging (PLP) and glass core substrates, are emerging as pivotal platforms set to define the future direction of semiconductor packaging. PLP garners significant anticipation for its potential to reduce manufacturing costs and accommodate ultra-large packages, while glass core substrates are expected to offer high-density routing and superior electrical properties, playing an indispensable role in next-generation high-performance chips.

Technical / Clinical Details

Panel Level Packaging (PLP) involves manufacturing and packaging chips on larger square or rectangular panels instead of traditional circular wafers. This approach promises improved material utilization efficiency during manufacturing, potentially reducing final packaging costs by increasing the number of chips processed per unit area. PLP is particularly well-suited for large-scale heterogeneous integration, such as AI processors and HBM (High Bandwidth Memory), especially in fan-out packaging. However, PLP still faces technical challenges, including warpage control in large-area substrate manufacturing, high-precision lithography, and ensuring thermal robustness. On the other hand, glass core substrates, compared to conventional organic substrates, enable finer routing patterns, offer low dielectric loss, high mechanical strength, and excellent thermal stability. These characteristics improve high-frequency signal transmission quality, making them ideal platforms for AI chips and HPC applications requiring high-density interconnects. Glass also exhibits a lower coefficient of thermal expansion than organic materials, which is expected to reduce thermal stress between different materials and enhance package reliability.

Background & Context

As the slowdown of Moore's Law becomes increasingly evident, the semiconductor industry is seeking new approaches to achieve performance improvements beyond transistor miniaturization. Advanced packaging is one of the primary solutions to this challenge, with the explosive growth of AI accelerating its development and adoption. AI chips require high-performance processors, large-capacity and high-bandwidth memory, and efficient packaging technologies to integrate them for rapid data processing. PLP and glass core substrates are positioned as next-generation solutions that break through the limitations of conventional packaging technologies to meet these demands. The shift towards these technologies significantly impacts semiconductor equipment manufacturers, material suppliers, and the entire design flow, prompting a transformation across the entire supply chain.

Strategic Significance & Outlook

Panel Level Packaging and glass core substrates will become indispensable technologies for manufacturing high-performance semiconductors in the AI era. PLP offers unique strengths in manufacturing cost and economies of scale, while glass core substrates excel in electrical performance and reliability. Over the next few years, further advancements in warpage control, thermal design, and cost-effective mass production techniques for these technologies are anticipated. The maturation of these technologies will enable significant leaps in semiconductor performance across AI accelerators, data centers, edge AI devices, and autonomous vehicles, sparking a new wave of innovation. The industry as a whole must continue collaborative efforts to overcome the challenges these technologies face and maximize their potential.

Source: https://events.vtools.ieee.org/m/541765

Collected: August 16, 2026 | Automated Research System (Gemini API)

#18 Samsung HBM4 Yield Dramatically Improves from Under 60% to 80%; SK Hynix Labor Talks Stall, Intensifying AI Memory Race

Published August 10, 2026 TrendForce Taiwan

OVERVIEW

Samsung's HBM4 yield has dramatically improved from under 60% at launch to 80% within months, according to Seoul Economic Daily. This swift process enhancement by Samsung comes amid tight HBM supply, surpassing its year-end 2026 target of 80%. The over 80% yield for the 1c DRAM used in HBM4 significantly contributed to this overall improvement. Concurrently, SK Hynix's labor talks have reportedly broken down over bonus payments, adding a new dimension to the competitive HBM market.

IN DEPTH

Key Findings

According to reports from the Seoul Economic Daily, Samsung Electronics has dramatically improved the yield of its next-generation High Bandwidth Memory (HBM), HBM4, from under 60% at the start of mass production to an impressive 80% in just a few months. This demonstrates Samsung's exceptionally rapid process improvement amid a globally tight HBM supply, achieving its year-end 2026 target of 80% ahead of schedule. A significant contributor to the overall HBM4 yield improvement is the fact that the 1c DRAM chips, a key component, have also achieved over 80% yield. This move substantially strengthens Samsung's competitiveness in the HBM market. Meanwhile, reports indicate that labor talks at competitor SK Hynix have broken down, with negotiations over bonus payments proving difficult, introducing new concerns about the stability of the HBM supply chain.

Technical / Clinical Details

HBM4 is a complex packaging technology that vertically stacks multiple DRAM dies and connects them with tiny Through Silicon Vias (TSVs). This process demands extremely high precision and stringent quality control, leading to generally low yields at the initial stages. Samsung's achievement of 80% yield highlights the company's advanced technological maturity and optimization capabilities across the intricate HBM4 manufacturing process (including DRAM chip fabrication, bump formation, die stacking, and hybrid bonding). Specifically, the 1c DRAM used in HBM4 is produced with state-of-the-art 10nm-class process technology, and its high yield indicates stable quality of individual DRAM dies. This ensures the reliability and performance of the final HBM4 package after multi-layer stacking. Samsung is believed to have leveraged its 'turnkey system,' integrating memory design, foundry manufacturing, and advanced packaging departments, to achieve this rapid yield improvement. HBM4 is expected to be integrated into NVIDIA's next-generation AI chips, such as Vera Rubin, dramatically enhancing AI workload performance through increased data channels and expanded bandwidth.

Background & Context

The explosive growth of AI has created unprecedented demand for high-performance memory like HBM, leading to a structural supply shortage in the market. HBM is a crucial component that determines the performance of AI accelerators, and its supply capacity and yield are key factors influencing the growth of the entire AI industry. Samsung and SK Hynix are major competitors in the HBM market, engaged in fierce competition to establish leadership in the HBM4 generation. Samsung's rapid yield improvement signifies a strong tailwind for the company to expand its market share in HBM. Conversely, SK Hynix's labor dispute could potentially impact its production plans and market supply, posing a new risk factor for AI chip manufacturers. This situation underscores the importance of resilience in the overall HBM supply chain and securing multiple sources of supply.

Strategic Significance & Outlook

Samsung's significant improvement in HBM4 yield signals intensified competition in the AI memory market and the company's strong ambition to expand its market share. This is expected to stabilize HBM4 supply to major customers like NVIDIA, accelerating the deployment of next-generation AI chips. Should SK Hynix's labor issues be resolved, the HBM4 mass production race between the two companies will further intensify, accelerating technological innovation. AI demand is projected to continue rising, making HBM technology evolution and stable supply indispensable for the overall development of the AI industry. This competition will also create significant business opportunities for semiconductor equipment manufacturers and material suppliers, fostering further innovation in HBM technology.

Source: https://www.trendforce.com/news/2026/08/10/news-samsungs-hbm4-yield-reportedly-hits-80-as-race-to-supply-vera-rubin-heats-up-sk-hynix-labor-talks-add-a-twist/

#19 2026 Chip Crisis Sounds Hardware Wake-Up Call: AI Demand Reshaping Semiconductor Supply Chains

Published August 13, 2026 Trax Technologies USA

OVERVIEW

The 2026 chip crisis highlighted modern supply chains' deep reliance on semiconductor availability, where chip access dictates the viability and growth of AI accelerators, warehouse robots, autonomous vehicles, and IoT sensors. This crisis signals a structural shift across the entire semiconductor supply chain, as AI demand reshapes requirements for memory, GPUs, advanced packaging, and related infrastructure. The industry is compelled to build more resilient and predictable supply systems.

IN DEPTH

Key Findings

The chip crisis of 2026 unequivocally demonstrated the profound dependence of all modern hardware-dependent businesses, from AI accelerators to autonomous vehicles and IoT sensors, on semiconductor supply. This crisis is not merely a temporary shortage but underscores a structural shift occurring across the entire semiconductor supply chain, driven by the explosive demand for AI fundamentally reshaping requirements for memory, GPUs, advanced packaging, and related infrastructure. The availability of chips is now recognized as a critical factor directly impacting a company's operational efficiency and competitive edge.

Technical / Clinical Details

The evolution of AI necessitates high-performance computing capabilities and massive data processing, for which GPUs (Graphics Processing Units) and specialized AI accelerators are indispensable. These chips heavily rely on high-capacity, high-speed HBM (High Bandwidth Memory) and advanced packaging technologies like CoWoS (Chip-on-Wafer-on-Substrate) for efficient integration. The recent chip crisis reiterated that manufacturing these high-performance chips requires state-of-the-art foundry processes, sophisticated packaging equipment, and specialized materials and tools. Specifically, the complexity of HBM stacks, silicon interposers, and the micro-bump or hybrid bonding technologies connecting them leads to extended manufacturing lead times and yield challenges. Supply chain bottlenecks are not confined to single components but manifest across various aspects, including manufacturing equipment, specific chemical materials, and even a shortage of skilled technicians.

Background & Context

Over the past few decades, the semiconductor industry has embraced globalization and specialization, resulting in an extremely complex and interdependent supply chain structure. The current crisis highlighted the vulnerability of this structure to geopolitical risks and unexpected demand fluctuations, particularly given that a few companies dominate cutting-edge manufacturing capabilities or specific material production. AI demand, unlike traditional PC or smartphone markets, is characterized by its unpredictability and rapid scaling. This new demand pattern puts immense pressure on existing supply chain models, exacerbating shortages in specific areas such as memory, GPUs, and advanced packaging. Governments worldwide are also implementing policies, such as the U.S. CHIPS Act and the EU's European Chips Act, to encourage domestic manufacturing and enhance semiconductor supply chain resilience.

Strategic Significance & Outlook

The 2026 chip crisis served as a 'wake-up call' for the semiconductor industry and all dependent hardware industries, forcing a re-evaluation and restructuring of supply chains. Moving forward, companies are expected to shift towards enhancing supply chain transparency, securing diverse sources of supply, and strengthening regional manufacturing capabilities. Particularly for AI-related semiconductors, substantial investments will continue to be poured into increasing HBM and advanced packaging capacities. Furthermore, AI itself may be integrated into supply chain management to improve demand forecasting accuracy and optimize risk management. Overcoming this crisis is expected to foster a more robust and sustainable semiconductor ecosystem, ensuring the pace of technological innovation in the AI era.

Source: https://www.traxtech.com/ai-in-supply-chain/2026-chip-supply-chain-crisis-hardware-impact?hs_amp=true

Collected: August 16, 2026 | Automated Research System (Gemini API)

#20 HBM Supply Crisis of 2026 Projected to Persist Until 2027, Redefining AI Hardware Deployment Bottleneck

Published August 15, 2026 EnkiAI USA

OVERVIEW

Explosive growth in the AI sector has triggered a structural HBM supply crisis, making it the primary bottleneck for AI hardware deployment throughout 2026, projected to last until at least 2027. The market has shifted from supply-driven to extreme demand-driven, with major memory manufacturers sold out for years. Rapid increases in per-chip memory, like NVIDIA's Blackwell B200 GPU using 192GB HBM3E (a 140% increase from H100), are fueling this demand tsunami. Micron (US, $15B) and SK Hynix (Indiana, $3.87B) are investing heavily in advanced HBM packaging to mitigate the shortage.

IN DEPTH

Key Findings

The explosive growth of the AI sector has ignited a structural supply crisis for High Bandwidth Memory (HBM), positioning it as the most critical bottleneck for AI hardware deployment throughout 2026, with projections indicating it will persist until at least 2027. The HBM market has fundamentally shifted from a supply-driven environment to one defined by extreme over-demand, with major memory manufacturers reportedly sold out for years in advance. A primary driver of this demand surge is the rapid increase in per-chip memory allocation, exemplified by NVIDIA's Blackwell B200 GPU, which utilizes 192GB of HBM3E—a 140% increase over the H100's 80GB.

Technical / Clinical Details

The manufacturing of HBM stacks is a highly complex process, requiring tiny Through Silicon Vias (TSVs) and extremely high-precision bonding equipment. TSVs enable vertical stacking of DRAM dies, providing high-density data paths, but this technology is challenged by low yield tolerances. The scarcity of vendors capable of manufacturing these specialized tools, particularly multi-layer bonders, creates an equipment-specific bottleneck. For instance, HANMI (Hanmi Semiconductor), a leading bonder manufacturer, reportedly faces a 12-month backlog, significantly constraining HBM production capacity expansion. TSMC's CoWoS (Chip-on-Wafer-on-Substrate) production capacity is targeted to increase by 25% by the end of 2026; however, AI demand growth is outpacing this expansion, elevating advanced packaging as the most severe bottleneck. This confluence of technical challenges and equipment shortages exacerbates the HBM supply deficit.

Background & Context

The increasing complexity and scale of AI models necessitate not only greater computational power but also a dramatic increase in memory bandwidth to enable ultra-fast data transfer between processors and memory. HBM was developed to address this 'memory bottleneck' and has become an indispensable component for AI accelerators. However, HBM manufacturing is highly technology-intensive, involving numerous complex steps from DRAM chip fabrication and TSV formation to die stacking, micro-bump or hybrid bonding, and final packaging. Consequently, expanding production capacity requires massive capital expenditure and long lead times. Micron Technology is investing $15 billion in an advanced HBM packaging facility in the U.S., and SK Hynix plans to build a $3.87 billion packaging plant in Indiana, demonstrating significant investments by major memory manufacturers to alleviate the shortage. These investments also align with U.S. government policies (e.g., the CHIPS Act) to incentivize domestic semiconductor manufacturing.

Strategic Significance & Outlook

The HBM supply crisis will directly impact the growth trajectory and development pace of the entire AI industry. It is highly probable that supply will not meet demand until at least 2027, leading to elevated AI chip prices, delays in AI hardware delivery, and constraints on AI infrastructure investments. While large-scale capital investments by memory manufacturers and packaging providers will contribute to long-term supply capacity improvement, short-term bottlenecks are likely to persist. The industry as a whole must address this challenge through HBM technology optimization, the development of new packaging solutions, and collaborative supply chain optimization. Stable HBM supply remains an absolute prerequisite for AI to achieve its next breakthroughs.

Source: https://enkiai.com/data-center/hbm-supply-crisis-2026-the-bottleneck-redefining-ai/

Collected: August 16, 2026 | Automated Research System (Gemini API)

#21 Bonafide Research: Global 3D/2.5D IC Packaging Market Accelerates with UCIe Standard, Forecasts Growth Through 2031

Published August 08, 2026 Bonafide Research India

OVERVIEW

This article provides an overview of a market research report published by Bonafide Research. According to Bonafide Research's latest report, the global 3D IC and 2.5D IC packaging market is projected to accelerate due to the adoption of the open Universal Chiplet Interconnect Express (UCIe) standard, ensuring multi-vendor interoperability. This trend is driving the integration of logic, memory, analog, and RF dies within a single footprint, thereby increasing demand for advanced packaging solutions. However, challenges such as yield loss in TSV processes and high thermal management costs remain key production hurdles.

IN DEPTH

This article provides an overview of a market research report published by Bonafide Research.

Report Overview

Bonafide Research's 'Global 3D IC and 2.5D IC Packaging Market Outlook, 2031' report provides a comprehensive analysis of the future prospects and key trends in the 3D IC and 2.5D IC packaging market. The report offers detailed information on market size forecasts, growth drivers, technological challenges, and the strategic movements of key market players.

Key Findings

- The introduction of the open Universal Chiplet Interconnect Express (UCIe) standard is a major factor accelerating the growth of the 3D IC and 2.5D IC packaging market, as it ensures interoperability between chiplets in multi-vendor environments.
- Driven by the UCIe standard, there is an accelerating trend towards efficiently integrating dies with different functionalities, such as logic, memory, analog, and RF, within a single footprint. This is increasing demand for high-performance heterogeneous integration packaging solutions.
- Key growth drivers for the market include the rising demand for high-performance chips in applications such as AI, High-Performance Computing (HPC), data centers, autonomous vehicles, and 5G/6G communications.
- However, high yield losses in Through Silicon Via (TSV) processes and the high costs associated with thermal management in highly integrated packages remain significant challenges for improving productivity and cost efficiency.

About the Publisher

Bonafide Research is an India-based market research and consulting firm that provides detailed market analysis and forecasts across a wide range of industrial sectors. The company aims to provide clients with insights to make strategic decisions through comprehensive reports based on quantitative and qualitative data. Bonafide Research covers various sectors, including consumer electronics, automotive, IT, healthcare, and food & beverage.

Source: https://www.bonafideresearch.com/product/2608511401/global-3d-ic-and-twofived-ic-packaging-market

Collected: August 16, 2026 | Automated Research System (Gemini API)

#22 IDTechEx Analyzes New 2.5D/3D Semiconductor Packaging Trends: Glass Interposers and Hybrid Bonding Drive Evolution

Published August 15, 2026 IDTechEx UK

OVERVIEW

IDTechEx's analysis highlights glass interposers and hybrid bonding as critical emerging trends in semiconductor packaging. Glass interposers offer compatibility with panel-level packaging, promising cost-effective, high-density routing. Hybrid bonding (Cu-Cu) for HBM is crucial for ultra-fine pitch vertical interconnections between chips. The chiplet concept and heterogeneous integration are accelerating advanced packaging adoption, fueling demand in key markets like HPC, autonomous vehicles, and 5G.

IN DEPTH

Key Findings

The latest analysis from IDTechEx emphasizes glass interposers and hybrid bonding technologies as key emerging trends in the evolution of semiconductor packaging. Glass interposers, compatible with panel-level packaging (PLP), hold significant promise for achieving high-density routing at a more manageable cost. Concurrently, hybrid bonding (copper-to-copper) for HBM (High Bandwidth Memory) is identified as an indispensable technology for enabling ultra-fine pitch vertical interconnections between chips. These technologies are accelerating the adoption of the chiplet concept and heterogeneous integration, vigorously driving the demand for advanced packaging solutions in critical markets such as High-Performance Computing (HPC), autonomous vehicles, and 5G communications.

Technical / Clinical Details

Glass interposers offer several advantages over traditional silicon interposers, including easier large-area scaling, superior electrical properties (low dielectric loss), and greater mechanical strength. Their coefficient of thermal expansion is intermediate between organic substrates and silicon, which helps mitigate thermal stress between dissimilar materials and improves reliability. This enables higher-density routing layers at potentially lower costs while ensuring high-frequency signal transmission quality. Compatibility with Panel Level Packaging (PLP) further contributes to potential cost reductions through economies of scale in manufacturing. Hybrid bonding (Cu-Cu bonding) is a technology that directly connects chiplets at pitches far finer than micro-bumps (sub-micron level). This dramatically increases I/O density, maximizes data bandwidth, and improves power efficiency. Especially in the integration of HBM with logic dies, this technology is critical for alleviating data movement bottlenecks and significantly boosting the performance of high-performance chips like AI accelerators. Chiplets and heterogeneous integration enhance design flexibility, improve yield, and facilitate system customization by optimally integrating multiple chips with different functionalities.

Background & Context

The limitations of Moore's Law and the escalating demand from compute-intensive applications such as AI, HPC, and autonomous driving are compelling the semiconductor industry to explore new avenues for performance improvement. As transistor miniaturization alone becomes more challenging for performance gains, advanced packaging technologies have emerged as the primary means to drive system-level performance enhancements. Technologies like glass interposers and hybrid bonding are at the forefront of this paradigm shift, aimed at overcoming the limitations of conventional packaging. These advancements are spurring massive investments and technological development across the entire semiconductor supply chain, creating new business opportunities for material suppliers, manufacturing equipment vendors, and design service providers.

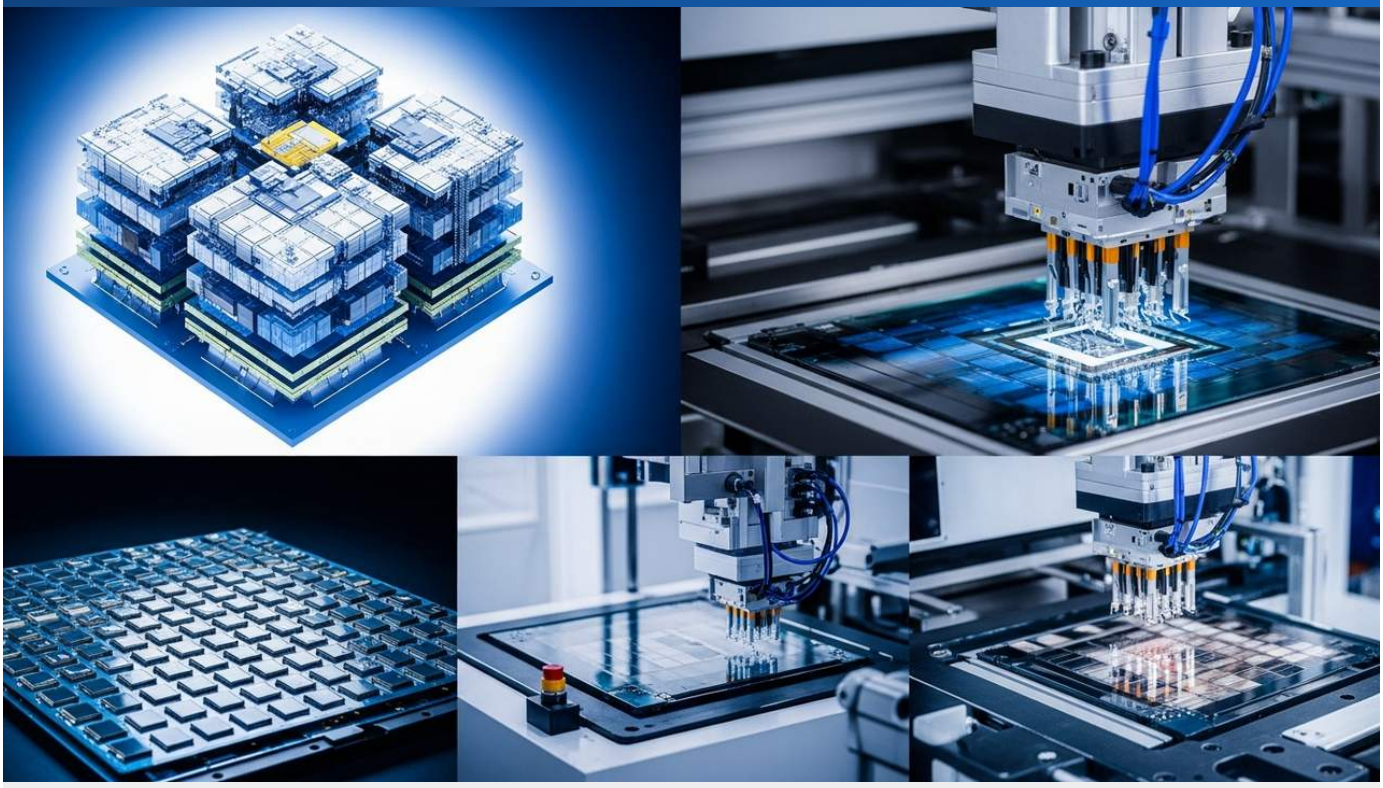
Strategic Significance & Outlook

Glass interposers and hybrid bonding are expected to play increasingly vital roles in the 2.5D/3D semiconductor packaging market over the next few years. The widespread adoption of these technologies will dramatically enhance the performance of AI accelerators, next-generation data centers, automotive AI platforms, and 5G/6G infrastructure. As mass production techniques for glass interposers mature and hybrid bonding becomes more standardized, more complex and higher-performance chiplet-based systems are anticipated to be developed and manufactured more cost-effectively. These trends will be central to reshaping the competitive landscape of the semiconductor industry and generating a new wave of technological innovation.

Source: https://www.idtechex.com/ja/research-article/emerging-trends-and-key-markets-in-2-5d-and-3d-semiconductor-packaging/31994

#23 IMAPS Device Packaging Conference 2026 Details 3D/2.5D Packaging Advances: FOPLP, Hybrid Bonding Drive Demand

Published August 15, 2026 IMAPS USA



OVERVIEW

Professional Development Courses at IMAPS Device Packaging Conference 2026 provided in-depth insights into current and future 3D/2.5D packaging processes and technologies. Key innovations like Fan-Out Panel Level Packaging (FOPLP), hybrid bonding, and copper pillar thermo-compression bonding were highlighted as drivers for 3D IC and wafer-level packaging demand in mobile, data center, automotive, and aerospace sectors. These technologies are crucial for next-generation applications demanding high performance and density.

IN DEPTH

Key Findings

The Professional Development Courses (PDCs) at the IMAPS (International Microelectronics Assembly and Packaging Society) Device Packaging Conference 2026 offered detailed insights into the forefront of current 3D IC and 2.5D IC packaging processes and technologies, as well as their future developmental trajectories. Particular attention was given to innovative techniques such as Fan-Out Panel Level Packaging (FOPLP), hybrid bonding, and copper pillar thermo-compression bonding. It was emphasized that these technologies are vigorously driving the demand for 3D IC and wafer-level packaging across diverse sectors, including mobile devices, high-performance data centers, automotive, and aerospace.

Technical / Clinical Details

3D IC and 2.5D IC packaging achieve integration density and performance beyond the limits of traditional 2D packaging by integrating multiple semiconductor dies vertically or horizontally. FOPLP (Fan-Out Panel Level Packaging) is a technology that packages chips on larger square or rectangular panels rather than circular wafers, enabling improved material efficiency and reduced manufacturing costs. This approach provides high throughput and cost-effectiveness for large and complex packaging solutions required by HPC (High-Performance Computing) and AI accelerators. Hybrid bonding directly connects chiplets at sub-micron pitches via copper-to-copper bonds, dramatically increasing I/O density, maximizing data bandwidth, and improving power efficiency. This is crucial for integrating HBM (High Bandwidth Memory) with logic dies or for ultra-high-speed communication between chiplets. Copper pillar thermo-compression bonding connects chips via fine copper pillars, offering excellent electrical and thermal characteristics. These technologies provide high-density, high-performance, low-power, and reliable packaging solutions required by various applications, including server processors for data centers, AI chips for autonomous vehicles, SoCs (System-on-Chip) for next-generation mobile devices, and robust high-performance systems in the aerospace sector.

Background & Context

The semiconductor industry faces the challenge of slowing Moore's Law, making it difficult to sustain performance improvements solely through transistor miniaturization. Consequently, packaging technology is being re-evaluated as a primary means to enhance system-level performance and functionality. Technological advancements in AI, 5G, IoT, and autonomous driving, in particular, are accelerating the development of chips that demand high integration, high performance, and low power consumption, thereby increasing the demand for advanced technologies like 3D/2.5D packaging, FOPLP, and hybrid bonding. Discussions at international forums like IMAPS indicate that these technologies are transitioning from research stages to practical implementation and are becoming established as industry standards.

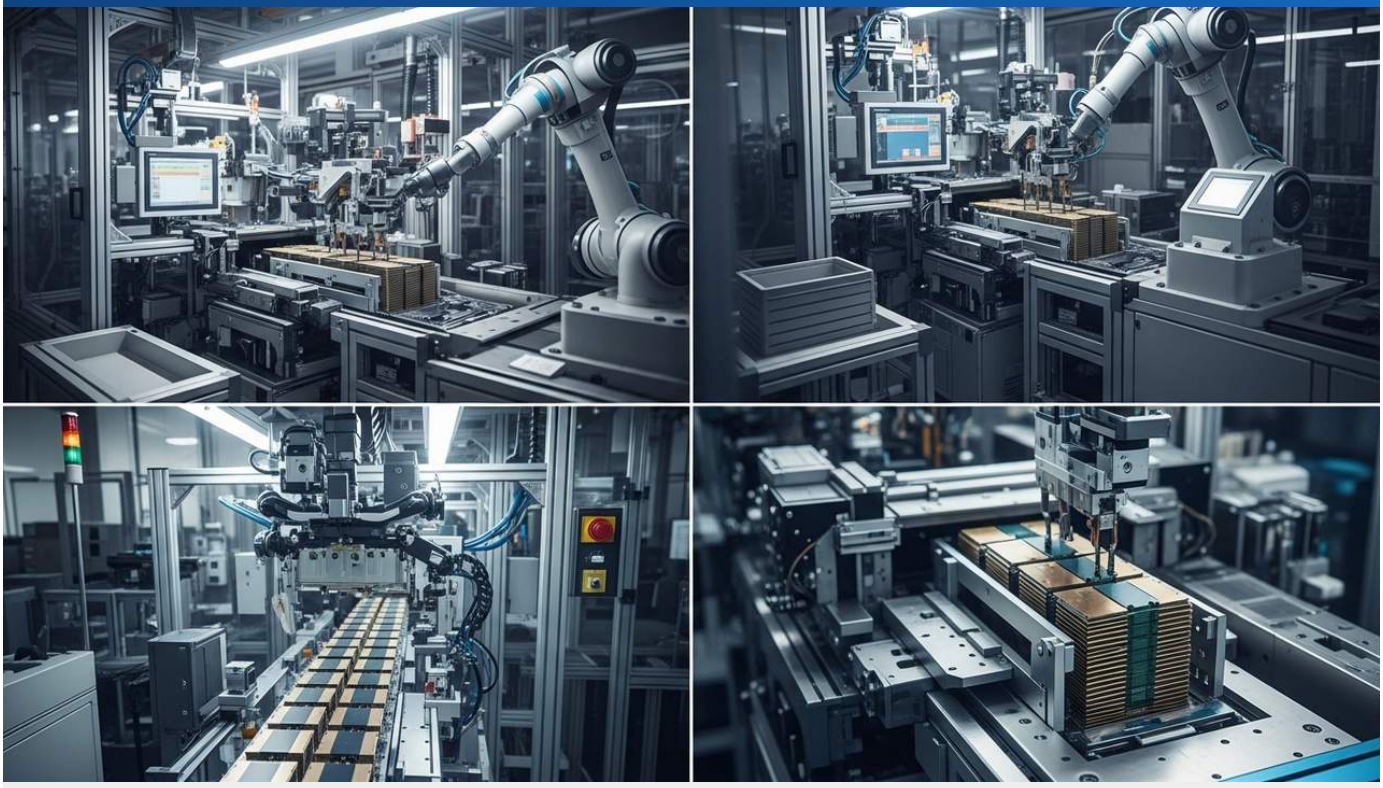
Strategic Significance & Outlook

The advanced packaging technologies highlighted at IMAPS DPC 2026 are expected to continue shaping the major trends in the semiconductor industry for years to come. FOPLP will drive the market with its improved manufacturing cost efficiency and large-area capability, while hybrid bonding will lead with ultra-high-density interconnects. The widespread adoption of these technologies will enable further performance enhancements in mobile devices, increased processing power in data centers, strengthened real-time AI processing in autonomous vehicles, and the development of compact, high-reliability systems in the aerospace sector. As these technologies mature and gain broader adoption, a new wave of innovation in semiconductor chip design and manufacturing is anticipated. The industry must collaborate to maximize the opportunities presented by these technologies while overcoming remaining technical challenges (e.g., thermal management, yield, reliability).

Source: https://imaps.org/page/DPC-26-PDCs

#24 HBM Supply Crunch: Long Backlogs for Bonding Equipment and Low Yields Create Bottleneck, Constraining AI Demand Until 2027

Published August 15, 2026 AI CERTs News USA



OVERVIEW

HBM stack manufacturing demands Through Silicon Vias (TSV) and high-precision bonding equipment, with low yield tolerance posing an industry challenge. Limited vendors for these specialized tools mean HANMI, a major multi-layer bonder supplier, faces a 12-month backlog, severely constraining HBM capacity expansion. Despite TSMC's CoWoS capacity targeting a 25% increase by late 2026, AI demand is growing faster, making packaging the most critical bottleneck. This complex scenario is the primary reason the HBM supply shortage is projected to last until 2027.

IN DEPTH

Key Findings

The persistent shortage of High Bandwidth Memory (HBM) required for the explosive growth of AI demand is primarily exacerbated by the technical complexities of HBM stack manufacturing and the constrained supply of specialized production equipment. Specifically, HBM stacks utilizing Through Silicon Vias (TSV) necessitate extremely high-precision bonding equipment, and the industry faces a significant challenge due to low yield tolerance. With only a limited number of vendors capable of manufacturing these specialized tools, particularly multi-layer bonders, leading supplier HANMI reportedly faces a prolonged 12-month backlog, severely impeding the expansion of HBM production capacity. Consequently, advanced packaging has emerged as the most critical bottleneck in the AI semiconductor supply chain, with HBM supply shortages projected to continue until at least 2027.

Technical / Clinical Details

HBM stacks are prime examples of 3D packaging technology, involving the vertical stacking of multiple DRAM dies and their electrical interconnection via TSVs. The TSV process includes highly precise steps such as creating minute holes in the dies and filling them with copper to form electrical pathways. Subsequent die-to-die bonding employs micro-bump or hybrid bonding techniques, which demand nanometer-level precision. Even minor misalignments in these stages can significantly impact overall yields, making process optimization and stringent quality control paramount throughout manufacturing. High-precision bonding equipment must accurately align multiple dies and simultaneously bond microscopic bumps. The development and manufacturing of such sophisticated equipment are time-consuming and costly, limiting the number of manufacturers capable of supplying the market. While TSMC's CoWoS (Chip-on-Wafer-on-Substrate) technology is crucial for HBM integration, even with a target of a 25% capacity increase by the end of 2026, AI demand growth is outpacing this expansion, creating bottlenecks at the final packaging stage.

Background & Context

The evolution of AI technology demands not only greater computational power from CPUs and GPUs but also a dramatic increase in memory bandwidth. HBM was developed to meet this demand, becoming an indispensable component for AI accelerators. However, HBM manufacturing relies on the fusion of multiple cutting-edge technologies—DRAM chip miniaturization, TSV technology, and advanced packaging—and this complexity is the fundamental cause of the supply shortage. Major memory manufacturers (SK Hynix, Samsung, Micron) are making massive investments in HBM production capacity expansion, but the shortage of specialized manufacturing equipment hinders overall scaling. The prolonged backlogs at equipment manufacturers mean that the benefits of memory manufacturers' investments appear only with a time lag, contributing to the prolonged HBM supply shortage.

Strategic Significance & Outlook

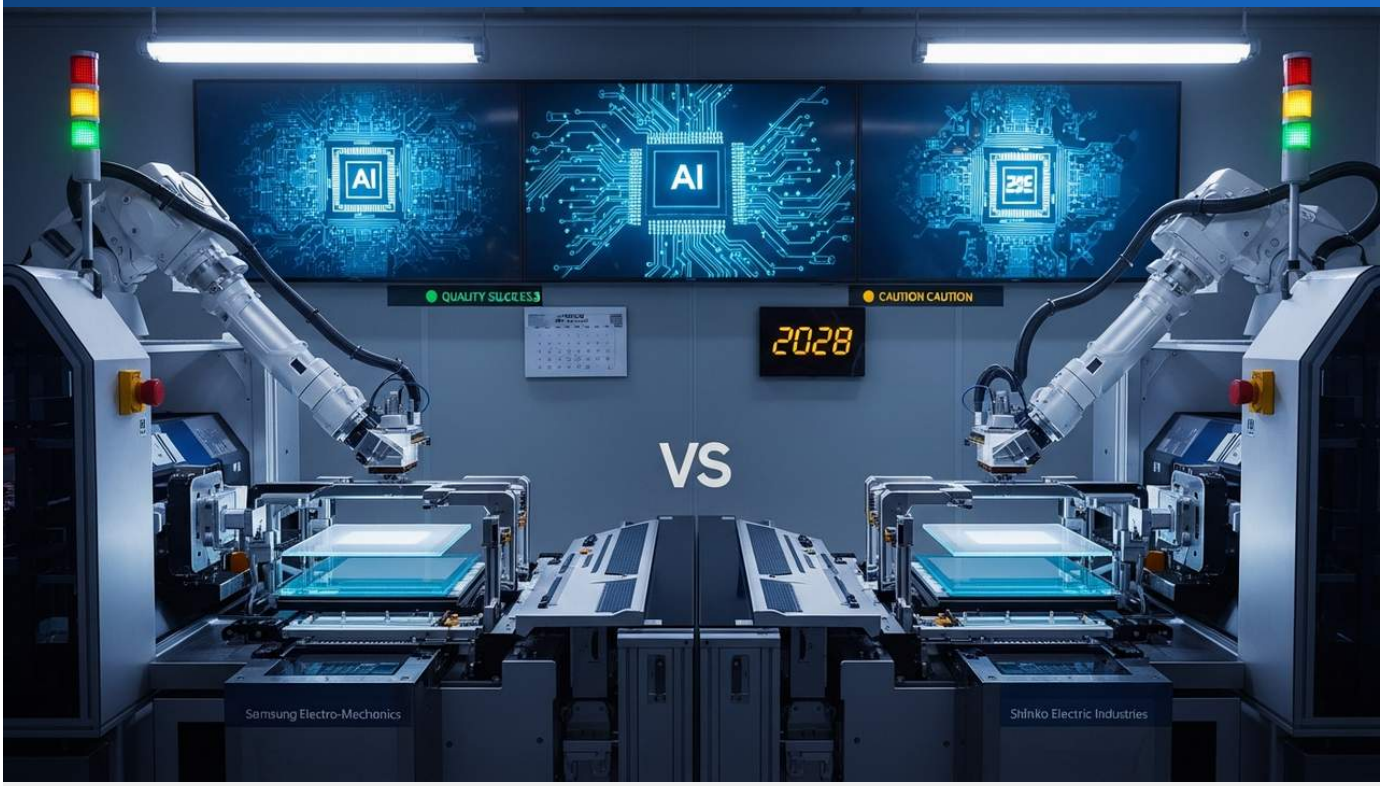
The HBM supply shortage is a critical issue that directly impacts the growth rate and technological innovation of the entire AI industry. Projections that supply will not meet demand until 2027 imply higher AI chip prices, delays in AI hardware deployment, and constraints on AI infrastructure investment plans. Addressing this challenge requires closer collaboration and investment coordination among memory manufacturers, packaging providers, and manufacturing equipment suppliers. Equipment manufacturers need to increase their production capacity, while memory manufacturers must focus on yield improvement and explore alternative technologies. Furthermore, AI chip designs may need to adopt approaches that optimize HBM dependence. Stabilizing HBM supply is an absolute prerequisite for AI to achieve its next breakthroughs and achieve widespread societal adoption.

Source: https://www.aicerts.ai/news/hbm-supply-crunch-why-ai-memory-shortage-lasts-until-2027/

Collected: August 16, 2026 | Automated Research System (Gemini API)

#25 Samsung Electro-Mechanics Accelerates Glass Substrate Bid for AI Chips, Targets 2028 Mass Production Against Japanese Rival

Published Published August 14, 2026 BusinessKorea (仮) South Korea



OVERVIEW

Samsung Electro-Mechanics (SEM) is accelerating its pursuit of glass substrates for AI chip packaging, targeting mass production by 2028 through its 'GlaSSEM' joint venture with Dongwoo Fine-Chem. This strategic move directly challenges Japanese incumbents like Shinko Electric Industries in a critical, high-stakes market. The company faces significant technical hurdles, including achieving customer quality certification and stable yields for these advanced substrates, which are vital for addressing warpage in increasingly complex AI chip packages.

IN DEPTH

Background

The relentless demand for superior performance in AI chips mandates continuous innovation in advanced packaging, specifically to enhance data transfer speeds and power efficiency between processors and memory. Glass substrates are emerging as a pivotal solution, offering low dielectric loss, exceptional thermal stability, and superior dimensional stability, which are expected to substantially improve data transmission integrity and overall package reliability. This technology holds particular significance for AI accelerators, where the increasing integration of High Bandwidth Memory (HBM) and logic chips positions glass as a potential de facto standard for next-generation designs.

Key Developments

Samsung Electro-Mechanics (SEM) is making aggressive strides towards the mass production of glass substrates for AI chip packaging, setting an ambitious target of 2028. This pursuit, however, is fraught with significant technical challenges, particularly in securing stringent customer quality certifications and achieving consistently stable production yields. To accelerate its efforts, SEM has formed 'GlaSSEM,' a joint venture with Dongwoo Fine-Chem, intensifying its direct competition with established Japanese players like Shinko Electric Industries within this critical and burgeoning advanced packaging segment.

Technical Analysis

- Glass substrates present a compelling alternative to conventional organic substrates, primarily by effectively mitigating warpage issues that become pronounced with increasing package area in high-performance AI chips. This intrinsic advantage is critical for enabling higher chip stacking densities and facilitating more complex 3D packaging architectures, thereby cementing glass's role as a pivotal technology for future AI semiconductors.

- Samsung Electro-Mechanics is committing substantial research and development resources to cultivate robust glass substrate technology, encompassing advancements from fundamental material science to sophisticated manufacturing processes. The technical challenges are considerable, notably in the fabrication of ultra-fine micro-vias and high-density metal lines on inherently brittle glass, requiring extraordinary precision and the deployment of novel techniques.
- Immediate priorities include securing rigorous quality certifications from tier-one customers and establishing a consistently high yield rate essential for scaling up to mass production. Successfully navigating these formidable technical barriers is imperative for SEM to achieve its ambitious 2028 mass production goal.

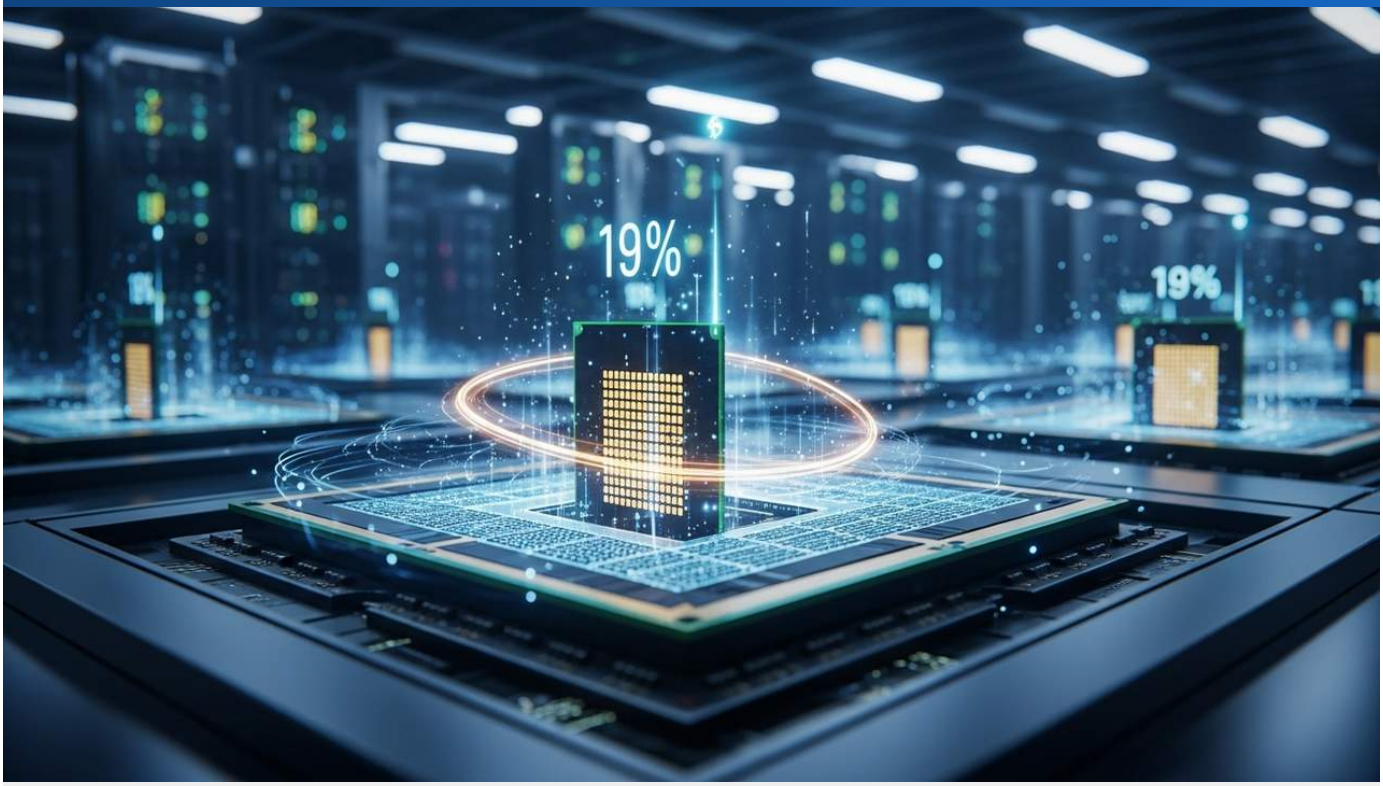
Strategic Outlook

The adoption of glass substrate technology is poised to be a determining factor in defining the performance benchmarks of future AI semiconductors. Should Samsung Electro-Mechanics successfully surmount these complex technical hurdles and commence mass production by 2028, it stands to significantly enhance its competitive posture within the advanced packaging market. Nevertheless, given the rapid advancements by rival companies, securing clear superiority in substrate quality, achieving cost-effectiveness, and ensuring robust supply chain stability will be paramount for sustained long-term success in this rapidly burgeoning and highly strategic sector.

Source: #

#26 Samsung Electro-Mechanics Sees Semiconductor Package Substrate Utilization Rate Soar to 89%, Driven by AI Data Center Demand

Published August 14, 2026 연합뉴스 (Yonhap News) South Korea



OVERVIEW

Samsung Electro-Mechanics reported a significant increase in its semiconductor package substrate utilization rate, reaching an average of 89% in the first half of the year—a 19 percentage point rise year-over-year. This surge is directly attributed to the escalating demand for high-value Flip-Chip Ball Grid Array (FCBGA) substrates, fueled by expanded AI data center investments from leading global tech giants. The heightened operational efficiency reflects a robust response to the accelerating build-out of AI infrastructure.

IN DEPTH

Key Findings

Samsung Electro-Mechanics has dramatically increased its average semiconductor package substrate utilization rate to 89% in the first half of this year, representing a substantial 19 percentage point jump year-over-year. This surge is primarily fueled by the exploding demand for AI data center infrastructure, with high-value Flip-Chip Ball Grid Array (FCBGA) substrates being a key driver for the company's package solution division.

Technical Details

- A utilization rate of 89% indicates that Samsung Electro-Mechanics' production lines are operating near full capacity, reflecting the tight supply conditions in the AI semiconductor market. FCBGA is a critical packaging technology used to connect high-performance logic chips like CPUs, GPUs, and AI accelerators with High Bandwidth Memory (HBM), growing in importance as AI workloads become more complex.
- This elevated operational efficiency underscores how investments in advanced packaging technology, crucial for maximizing AI semiconductor performance, are directly contributing to the company's revenue and market share. The quality and stable supply of FCBGA are paramount for AI data centers that demand massive data processing and extremely high data transfer speeds.

Background & Context

The rapid advancement and adoption of AI technologies have dramatically amplified the demand for computing power in data centers worldwide. This has led to an explosive increase in AI semiconductor chip demand, with HBM and the advanced packaging substrates required for its implementation becoming significant bottlenecks in the supply chain. Samsung Electro-Mechanics' soaring utilization rate is concrete evidence of the profound impact of this global AI boom across the entire semiconductor backend supply chain. As numerous global tech giants accelerate their AI strategies, a stable supply of high-performance package substrates is becoming a key competitive differentiator.

Strategic Significance & Outlook

Samsung Electro-Mechanics' high utilization rate signals robust future growth in the AI semiconductor market and positions the company to capitalize on this expansion. However, sustained high utilization also strains the broader supply chain, carrying potential risks of shortages and price increases. The company is expected to continue expanding its production capacity for high-value products through ongoing capital investments and technological innovation to reinforce its leadership in the AI era.

Source: #

Collected: August 16, 2026 | Automated Research System (Gemini API)

#27 Applied Materials Boosts 2026 Advanced Packaging Revenue Growth Forecast to Over 70% Amid Expanding AI Chip Investment in HBM and Multi-Layer Packaging

Published Published August 14, 2026 Xenospectrum (情報集約サイト) USA

OVERVIEW

Applied Materials has substantially elevated its 2026 advanced packaging revenue growth forecast to over 70%, a 20-point jump from its previous 50%+ projection. This revision reflects a critical expansion of AI semiconductor investment beyond traditional front-end scaling, now heavily focusing on High Bandwidth Memory (HBM) and sophisticated multi-layer packaging. While HBM stacking is a primary catalyst for backend equipment demand, the firm also notes that securing sufficient cleanroom space is emerging as a significant bottleneck for customer capital expenditure.

IN DEPTH

Background

The relentless evolution of artificial intelligence necessitates increasingly rapid and voluminous data processing, fueling an explosive demand for GPUs, AI accelerators, and their supporting High Bandwidth Memory (HBM). Historically, front-end miniaturization was the primary driver for performance gains in semiconductor manufacturing. However, this approach is now encountering significant technological limits and escalating costs. In response, advanced packaging – the efficient integration of multiple chips – has rapidly emerged as a crucial new frontier for enhancing performance and achieving cost reductions. This paradigm shift is dramatically elevating the importance of backend equipment investment within the broader semiconductor manufacturing ecosystem.

Key Findings

Applied Materials has announced a substantial upgrade to its 2026 advanced packaging business revenue growth forecast, elevating it from "over 50%" to "over 70%." This significant revision decisively signals a rapid expansion of AI semiconductor investments beyond traditional front-end process miniaturization, now extending into critical backend domains like High Bandwidth Memory (HBM) and complex multi-layer packaging. Advanced packaging is paramount for integrating multiple chips to achieve the higher performance and efficiency essential for next-generation AI capabilities.

Specifically, HBM stacking, which involves vertically integrating DRAM chips to dramatically boost bandwidth, necessitates sophisticated die bonding, thermo-compression bonding (TCB), and precision inspection equipment. Applied Materials' equipment provides key technologies essential for these complex stacking processes and heterogeneous integration, suggesting its deep integration within the mainstream advanced packaging technologies driving the AI era.

However, a critical new constraint on customer capital expenditure has emerged: securing adequate cleanroom space. This cleanroom bottleneck, alongside other infrastructure limitations, indicates that the scaling of AI semiconductor production is hindered not just by equipment supply but also by the need for significant infrastructure investment in advanced manufacturing environments, demanding a more balanced investment approach across the entire semiconductor ecosystem. Applied Materials' strong forecast underscores a sustained structural expansion of the AI semiconductor market, positioning the company to maximize benefits from its technological leadership, even as industry-wide infrastructure constraints require strategic investment and collaboration across the backend supply chain to meet future AI demands.

Source: https://xenospectrum.com/en/applied-materials-packaging-growth/

Collected: August 16, 2026 | Automated Research System (Gemini API)

#28 U.S. Commerce Department to Invest Up to $874 Million in Seven Semiconductor Companies Across AI, Advanced Packaging, and Supply Chain Security

Published August 10, 2026 AnySilicon USA

OVERVIEW

The U.S. Department of Commerce announced its intent to provide up to $874 million in incentives to seven semiconductor technology companies, targeting critical areas such as AI, advanced computing, semiconductor packaging, materials, and supply chain security. This substantial investment falls under the purview of the CHIPS and Science Act, aiming to bolster domestic semiconductor innovation and manufacturing capabilities while reducing reliance on foreign supply chains. The initiative marks a strategic move to enhance U.S. competitiveness and resilience across the entire semiconductor ecosystem.

IN DEPTH

Key Findings

The U.S. Department of Commerce has declared its intent to provide up to $874 million in incentives under the CHIPS and Science Act to seven semiconductor companies operating in critical areas such as AI, advanced computing, semiconductor packaging, materials, and supply chain security. This substantial investment signifies a robust commitment by the U.S. to bolster domestic semiconductor technology development and manufacturing capabilities, thereby reducing strategic reliance on foreign supply chains.

Technical Details

- The recipient companies are focusing on cutting-edge process technologies to accelerate the development of chips for AI and High-Performance Computing (HPC), as well as innovative packaging solutions that efficiently integrate multiple chips. Specifically, technologies like 3D stacking, heterogeneous integration, and wafer-level packaging are expected to be supported.
- Furthermore, the investment targets the development of specialized materials essential for semiconductor manufacturing and technologies that enhance the security and resilience of the entire supply chain. This indicates a comprehensive approach by the U.S. to build a robust foundation at every stage of the semiconductor ecosystem.
- This funding also aims to contribute to establishing "trusted foundry" capabilities, particularly for military and national security applications, ensuring a secure supply of chips for sensitive uses.

Background & Context

The CHIPS and Science Act represents a comprehensive strategic framework designed to maintain U.S. technological leadership and revitalize domestic semiconductor manufacturing. In recent years, global recognition of semiconductor supply chain vulnerabilities, coupled with escalating geopolitical tensions, has compelled the U.S. to strengthen its indigenous technological base. This latest round of incentives is intended to address the soaring demand for high-performance semiconductors driven by the rapid advancements in AI, aiming to boost international competitiveness by supporting R&D to mass production within the U.S.

Strategic Significance & Outlook

This $874 million investment is expected to vigorously support the research and development, capital expenditures, and workforce training of the targeted companies, thereby accelerating semiconductor innovation in the U.S. In the long term, it has the potential to foster the growth of an advanced semiconductor ecosystem domestically, contributing to new job creation and economic growth. Moreover, enhanced supply chain resilience is anticipated to mitigate future supply disruption risks, providing a crucial national security advantage. This positions the U.S. on a firmer footing in the technological competition of the AI era.

Source: https://anysilicon.com/news/u-s-plans-874-million-investment-in-seven-semiconductor-technology-companies/

Collected: August 16, 2026 | Automated Research System (Gemini API)

#29 Samsung Electro-Mechanics to More Than Double Advanced Packaging Substrate Capacity for AI Semiconductors at Vietnam Plant

Published Published August 08, 2026　ベトナムコリアタイムズ (Vietnam Korea Times)　ベトナム

OVERVIEW

Samsung Electro-Mechanics (SEMCO) is poised to significantly expand its production of advanced packaging substrates for AI semiconductors, with a reported 2.4-fold capacity increase at its Thai Nguyen, Vietnam factory. This strategic move underscores a broader shift in Samsung's Vietnam operations, transitioning from traditional finished product manufacturing to becoming a critical hub for high-performance Flip-Chip Ball Grid Array (FCBGA) substrates and other essential AI components. The expansion positions Vietnam as a key player in the global semiconductor backend supply chain, addressing the burgeoning demand for AI infrastructure.

IN DEPTH

Background

The accelerating pace of AI innovation is fueling an unprecedented demand for high-performance data centers, consequently driving an explosive increase in the need for AI-specific semiconductors. This surge in demand directly translates to advanced packaging technologies and their critical substrates, with growing concerns over potential shortages of high-density, high-speed communication substrates such as Flip-Chip Ball Grid Array (FCBGA). Samsung Electro-Mechanics (SEMCO)'s strategic investment in its Vietnam facility directly addresses this critical supply bottleneck, positioning the company to capitalize on the burgeoning market opportunities presented by the AI era. Vietnam, bolstered by its cost-effective and skilled workforce alongside robust government support, is rapidly solidifying its position as a nascent but significant hub for semiconductor backend processing.

Key Findings

Samsung Electro-Mechanics (SEMCO) has officially announced a substantial expansion of its advanced packaging substrate production capacity for AI semiconductors, reportedly a 2.4-fold increase, at its Thai Nguyen factory in Vietnam. This strategic move signals a significant broadening of the Samsung Group's operational footprint in Vietnam, extending beyond traditional finished product manufacturing into critical backend semiconductor processes and the production of essential AI components.

Technical Details

- The core of this expansion focuses on augmenting production lines for ultra-large Flip-Chip Ball Grid Array (FCBGA) substrates. FCBGA technology is indispensable for high-performance computing, serving as the critical interconnector for advanced logic chips such as CPUs and GPUs with High Bandwidth Memory (HBM), directly influencing the overall performance and efficiency of AI accelerators.

- A 2.4-fold increase in production capacity is projected to translate into a substantial boost in monthly substrate output, potentially reaching tens of thousands of units. This expansion will significantly fortify SEMCO's supply capabilities within the increasingly critical global AI semiconductor supply chain. Already home to some of Samsung Electronics' backend semiconductor lines, the Thai Nguyen facility is strategically positioned to evolve into a major production hub for AI-specific semiconductors.

Strategic Significance & Outlook

This substantial production capacity expansion is paramount for Samsung Electro-Mechanics to significantly bolster its competitive edge in the rapidly evolving AI semiconductor market. The projected 2.4-fold capacity increase is expected to not only contribute to global market share expansion for SEMCO but also to deepen Samsung's overall influence within the increasingly vital AI chip supply chain. Looking ahead, the Thai Nguyen factory in Vietnam is slated to play a central and indispensable role in Samsung's long-term AI semiconductor strategy, consistently supporting the foundational infrastructure of next-generation AI through sustained investment and technological innovation.

Source: #

Collected: August 16, 2026 | Automated Research System (Gemini API)

#30 ASMPT's Advanced Packaging Business Achieves Record H1 2026 Sales Driven by Surging AI Demand; Panel-Level Packaging Positioned as Key Future Growth Driver

Published August 11, 2026 ASMPT Corporate (Press Release) Hong Kong

OVERVIEW

ASMPT reported robust interim results for H1 2026, with its Advanced Packaging (AP) business achieving record sales, primarily fueled by the accelerating demand from the AI sector. The company's Thermo-Compression Bonding (TCB), photonics, and high-precision Surface Mount Technology (SMT) solutions were significant contributors to this strong performance. ASMPT is actively developing Panel-Level Packaging (PLP) as a critical future growth driver, already initiating shipments of new chip-on-panel tools to key customers, signifying a proactive stance in next-generation packaging.

IN DEPTH

Key Findings

ASMPT announced robust interim results for the first half of 2026, with its Advanced Packaging (AP) business achieving record sales, predominantly driven by the surging demand from the AI sector. The company's Thermo-Compression Bonding (TCB), photonics, and high-precision Surface Mount Technology (SMT) solutions were instrumental in this strong performance. ASMPT is also actively positioning Panel-Level Packaging (PLP) as a crucial future growth driver, having already commenced shipments of new chip-on-panel tools to customers.

Technical Details

- ASMPT's Thermo-Compression Bonding (TCB) technology is essential for stacking High Bandwidth Memory (HBM) and for advanced packaging schemes like CoWoS (Chip on Wafer on Substrate), which integrate multiple chips in close proximity. This enables high-density, high-speed interconnections, maximizing the performance of AI accelerators.
- The photonics solutions involve integrating optical communication technology into semiconductor packages, addressing the growing demand for high-speed data transmission within data centers and optical interconnects. High-precision SMT technology enhances the accuracy of mounting miniature components, improving the reliability of complex packaging structures.
- Panel-Level Packaging (PLP) holds significant promise for dramatically increasing production efficiency and cost-effectiveness by utilizing larger substrates (panels) than traditional wafer-level packaging. ASMPT's chip-on-panel tools represent a crucial step towards the commercialization and widespread adoption of PLP.

Background & Context

The evolution of technologies such as AI, high-performance computing, and 5G communication has not only demanded higher performance from semiconductor chips but has also dramatically elevated the importance of advanced packaging, which connects these chips. Particularly, the increasing demand for HBM in AI semiconductors and the heterogeneous integration of GPUs and logic chips require more sophisticated and efficient packaging solutions. ASMPT's record sales clearly demonstrate its central position in this technological trend and its ability to deliver solutions that meet market needs.

Strategic Significance & Outlook

ASMPT has established a strong foothold in the advanced packaging market, and with the continued expansion of AI demand, further growth is anticipated. The commercialization of Panel-Level Packaging technology, in particular, could lead to significant reductions in production costs and increases in throughput, accelerating its adoption across a wider range of applications. This strategic move is crucial for ASMPT to maintain its leadership in next-generation semiconductor manufacturing technologies and secure long-term revenue growth.

Source: https://troy-technical.com/2026/08/02/asmpts-advanced-packaging-business-achieves-record-sales-in-h1-2026-driven-by-surging-ai-demand/

Collected: August 16, 2026 | Automated Research System (Gemini API)

#31 Intel Foundry Boosts AI Data Center Compute with Foveros and EMIB Advanced Packaging, EMIB-T Launch Planned for 2026

Published August 10, 2026 ET Datacenters India

OVERVIEW

Intel Foundry is actively deploying advanced packaging technologies, including Foveros stacking and Embedded Multi-die Interconnect Bridge (EMIB) interconnects, to meet the escalating demands of AI workloads. These innovations enable the seamless integration of multiple specialized chips into powerful single units, effectively overcoming traditional scaling limitations and paving the way for next-generation AI semiconductors. In 2026, Intel plans to introduce EMIB-T, further enhancing power efficiency, signal routing, and High Bandwidth Memory (HBM) support through direct power delivery to the chips.

IN DEPTH

Key Findings

Intel Foundry is strategically leveraging advanced packaging technologies, including Foveros stacking and Embedded Multi-die Interconnect Bridge (EMIB) interconnects, to significantly enhance AI computing performance for data centers in response to escalating AI workload demands. These innovative approaches enable the seamless interconnection of multiple specialized chips into a single, powerful unit, effectively overcoming traditional semiconductor scaling limits and facilitating next-generation AI semiconductors. Notably, Intel plans to introduce EMIB-T in 2026, which will further improve power efficiency and signal routing by delivering power directly to the chips, bolstering support for High Bandwidth Memory (HBM) technology.

Technical Details

- Foveros is a 3D stacking technology that vertically integrates logic chips, allowing the combination of chips manufactured on different process nodes to achieve high performance and power efficiency within a compact footprint. This enables AI accelerators to deliver more computational power in a smaller area.
- EMIB is a 2.5D packaging technology that connects chiplets, potentially manufactured on different process nodes, side-by-side. It shortens interconnect distances compared to traditional interposers, enabling low-power, high-speed communication between chips. EMIB-T will apply PowerVia technology for direct power delivery to the chip, improving power delivery efficiency and signal integrity, contributing to further performance gains in AI chips.
- These technologies are essential for eliminating data transfer bottlenecks, particularly when integrating with high-bandwidth memories like HBM, and for dramatically accelerating AI model training and inference speeds.

Background & Context

With the advancement of AI, data centers require high-performance, power-efficient semiconductors capable of processing vast amounts of data at high speeds. Traditional monolithic chip designs face increasing manufacturing costs and physical limitations, making heterogeneous integration, which combines multiple chiplets, the new mainstream approach in the industry. Intel is leading this trend by developing its proprietary advanced packaging technologies like Foveros and EMIB, aiming to enhance its competitiveness in the AI semiconductor market. This strategy focuses on maximizing overall system performance and efficiency, not just individual chip performance.

Strategic Significance & Outlook

Foveros, EMIB, and the upcoming EMIB-T in 2026 will form a crucial technological foundation for Intel to establish leadership in the AI era. These advanced packaging technologies will provide Intel Foundry with the flexibility and scalability needed to support diverse customer AI semiconductor designs, further boosting the performance of next-generation AI accelerators, HPCs, and data center processors. Improvements in power efficiency and bandwidth are also expected to contribute to a reduction in the total cost of ownership (TCO) for AI systems, making a significant impact across the industry.

Source: https://datacenters.economictimes.indiatimes.com/news/ai-compute-infrastructure/intels-advanced-packaging-boosts-ai-compute-for-data-centers/133081675

Collected: August 16, 2026 | Automated Research System (Gemini API)

#32 Global Semiconductor Capital Investment to Surge 30% to $240 Billion in 2026, Driven by AI Inference Demand; Advanced Packaging Fuels Multi-Year Double-Digit Growth

Published August 10, 2026 Soka Technology Unknown

OVERVIEW

The global semiconductor industry is projected to enter an unprecedented capital investment supercycle in 2026, driven by a skyrocketing demand for AI inference capabilities. Industry forecasts estimate total semiconductor equipment capital expenditure to reach approximately $240 billion, marking a 30% year-over-year increase. This robust growth is primarily fueled by advanced packaging technologies and heterogeneous integration, which are critical for AI hardware performance, with investments in equipment, test, and specialized manufacturing tools expected to maintain double-digit growth for several years.

IN DEPTH

Key Findings

In 2026, the global semiconductor industry is predicted to enter an unprecedented capital investment supercycle, primarily driven by the exponential demand for AI inference capabilities. Industry forecasts indicate that total capital expenditure on semiconductor equipment will surge by 30% year-over-year, reaching approximately $240 billion. This robust growth is largely attributed to advanced packaging technologies and heterogeneous integration, which are deemed essential for enhancing AI hardware performance, with investments in equipment, test, and specialized manufacturing tools expected to sustain double-digit growth for several years.

Technical Details

- Improving AI chip performance necessitates not only computational power but also high-speed data transfer capabilities with memory, which are efficiently achieved through advanced packaging and heterogeneous integration. This includes technologies such as High Bandwidth Memory (HBM) stacking, chiplet integration, and 2.5D/3D packaging.
- These technologies overcome the limitations of traditional monolithic chip designs, enabling optimal combination of distinct functional chips to improve power efficiency, reduce costs, and dramatically enhance overall system performance.
- The capital investments are expected to focus heavily on die bonding, wafer bonding, inspection equipment, and post-packaging test solutions. These tools demand high precision and throughput, leading to vigorous R&D investment in these areas.

Background & Context

The proliferation and evolution of AI are stimulating demand for high-performance computing everywhere, from cloud infrastructure to edge devices. The emergence of large language models (LLMs) like ChatGPT, in particular, has drastically altered the type and volume of semiconductors required for AI inference. To meet this demand, semiconductor manufacturers are pursuing performance and efficiency not only through front-end miniaturization but also through innovation in back-end processes, with advanced packaging at its core. While the semiconductor industry has grappled with supply constraints in recent years, this investment boom is an inevitable step towards building the infrastructure that will power future AI societies.

Strategic Significance & Outlook

The projected surge in 2026 capital expenditure will significantly boost the overall capacity of the global semiconductor supply chain. This could alleviate AI semiconductor shortages and accelerate the broader adoption of AI technology. Continuous investment in advanced packaging technologies will redefine the competitive landscape of the semiconductor industry and serve as a driving force for new technological breakthroughs. This supercycle is anticipated to continue for several years, presenting substantial business opportunities for semiconductor equipment manufacturers while accelerating innovation in AI hardware.

Source: https://sokatec.com/blogs/news/semiconductor-capital-investment-growth-2026

Collected: August 16, 2026 | Automated Research System (Gemini API)

#33 NXP Semiconductors Doubles Malaysia Backend Production Capacity, Targeting Q1 2028 Operation; Resonac Reports 46% Revenue Growth for AI Backend Materials

Published Published August 12, 2026 note (個人ブログ/キュレーション) Japan

OVERVIEW

NXP Semiconductors has initiated construction of a new assembly and test (A&T) facility in Malaysia, projected to more than double the site's overall production capacity by Q1 2028 through advanced automation. Concurrently, Japan's Resonac reported a 46% year-over-year revenue increase for its AI-focused backend materials, underscoring the broad impact of AI demand across the semiconductor supply chain. This dual development highlights the industry's strategic response to the escalating needs of the AI era.

IN DEPTH

Background

The rapid evolution of AI is driving profound structural changes throughout the semiconductor industry. The escalating demand for high-performance AI chips is not only intensely pushing front-end chip manufacturing but also necessitating strengthened backend capabilities and technological innovation in assembly, testing, and advanced packaging. Malaysia serves as a pivotal hub for semiconductor backend processes in the Asia-Pacific region, and NXP's significant investment further solidifies its strategic presence there. Moreover, the robust performance of semiconductor material manufacturers underscores the intricate interconnectedness of the entire semiconductor ecosystem, all poised to benefit from the ongoing AI boom.

NXP's factory expansion in Malaysia represents a critical strategic move to enhance its competitiveness in the burgeoning AI and automotive markets and to address anticipated future demand growth. Doubling production capacity by 2028 is expected to significantly improve NXP's global supply chain resilience and boost profitability. Resonac's recent success, meanwhile, powerfully demonstrates the vital role of material innovation in pushing the performance limits of AI semiconductors, signaling continued active investment in backend processes from both equipment and materials perspectives. These collective developments are poised to support the broader adoption of AI technology and the sustained growth of the semiconductor industry.

Key Findings

NXP Semiconductors has commenced construction of a new assembly and test (A&T) factory in Malaysia, with ambitious plans to more than double the site's overall production capacity upon full operation by Q1 2028. This significant expansion aims to establish a state-of-the-art smart factory, integrating Automated Material Handling Systems (AMHS) and advanced quality control technologies. In parallel, Japan's chemical materials giant Resonac reported a remarkable 46% year-over-year increase in revenue for its AI-focused backend materials, unequivocally demonstrating the widespread positive impact of surging AI demand across both semiconductor device manufacturers and their critical backend material suppliers.

The new NXP facility will bolster assembly and testing processes for semiconductors destined for critical growth markets including AI, automotive, and industrial equipment. The strategic integration of AMHS is designed to significantly enhance production efficiency, mitigate human error, and minimize contamination risks within cleanroom environments. Furthermore, advanced quality control technologies are deemed indispensable for meeting the stringent reliability and performance standards demanded by high-reliability automotive semiconductors and other mission-critical applications.

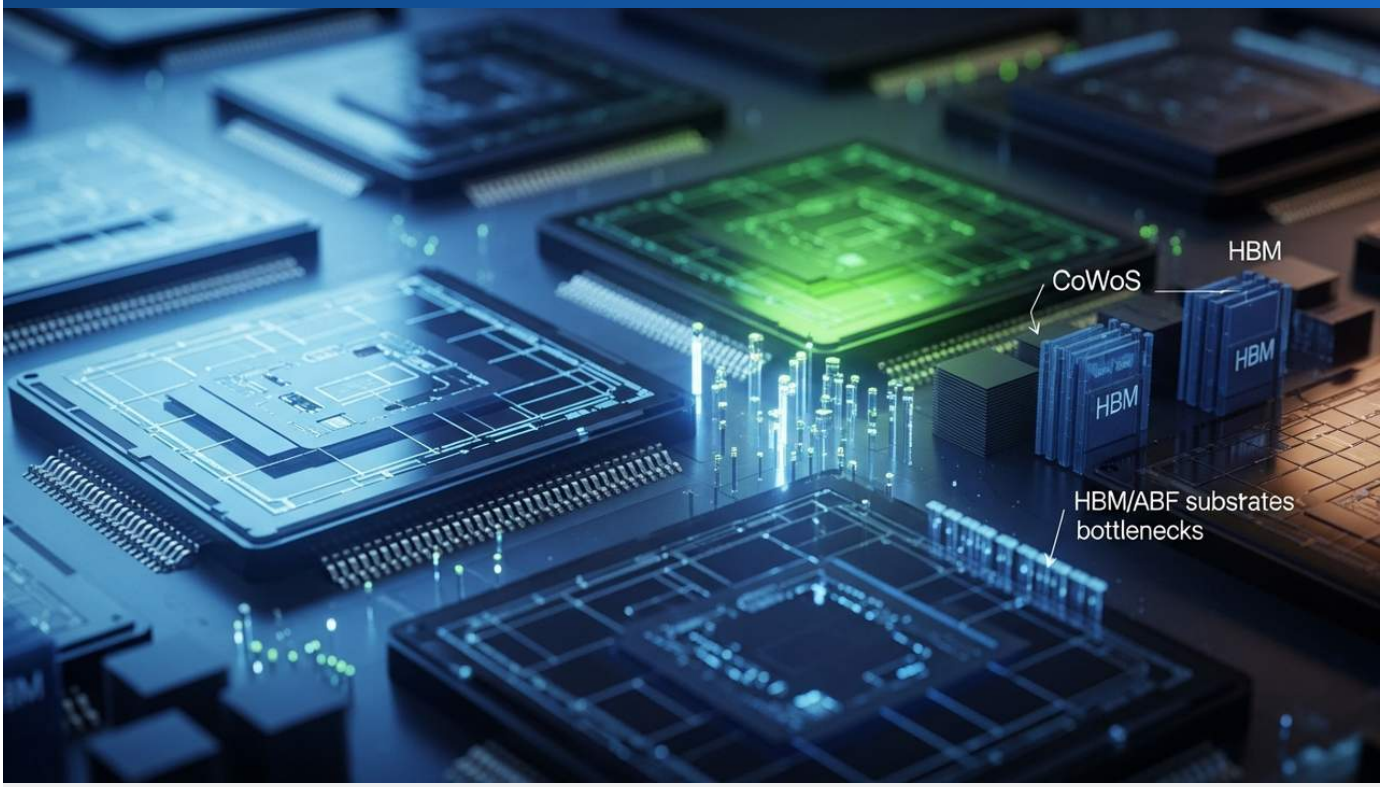
Resonac's strong performance in AI-focused backend materials points to a substantial surge in demand for specialized solutions such as advanced heat dissipation materials, encapsulants, and sophisticated package substrate materials—all crucial for the optimal functioning of high-performance AI chips. Considering the substantial thermal output of modern AI chips, achieving superior thermal conductivity and developing robust encapsulation technologies to safeguard complex package structures are paramount requirements for the industry.

Source: https://note.com/handotai14/n/ne20b0f717d81

Collected: August 16, 2026 | Automated Research System (Gemini API)

#34 Global Semiconductor Sales Soar 2.2x to Record $134.5 Billion in June 2026; TSMC Achieves Over 99% CoWoS Yield But Flags HBM and ABF Substrate Bottlenecks

Published August 11, 2026 Amiko Consulting Japan



OVERVIEW

Global semiconductor sales reached an unprecedented monthly high of $134.5 billion in June 2026, marking a 2.2-fold increase year-over-year, driven by a dramatic surge in AI data center investments across High Bandwidth Memory (HBM), logic, and advanced foundries. SK Hynix has committed to substantial investments to meet AI memory demand. Despite TSMC achieving over 99% yield for its 5.5-reticle size CoWoS advanced packaging, the company identified HBM and ABF substrates as persistent bottlenecks.

IN DEPTH

Key Findings

Global semiconductor sales in June 2026 reached an unprecedented monthly record of $134.5 billion, representing a 2.2-fold increase year-over-year. This historic growth is primarily attributed to the explosive expansion in demand for High Bandwidth Memory (HBM), logic chips, and advanced foundries, driven by massive investments in AI data centers. While SK Hynix has decided on significant investments to meet AI memory demand, TSMC achieved an impressive yield of over 99% for its 5.5-reticle size CoWoS packages, yet still points to memory supply and Ajinomoto Build-up Film (ABF) substrates as persistent bottlenecks in the overall semiconductor supply chain.

Technical Details

- HBM is a stacked DRAM technology that provides the high bandwidth critical for AI accelerator performance. The surging demand for HBM emphasizes not only its production capacity but also the importance of advanced packaging technologies like CoWoS to integrate it.
- TSMC's CoWoS (Chip on Wafer on Substrate) is a 2.5D packaging technology that integrates GPUs and HBM on a silicon interposer. Achieving over 99% yield signifies the maturity and high efficiency of this complex technology. However, this high yield, the ultimate product supply is constrained by the production capacity of HBM chips themselves and the shortage of ABF substrates, which are indispensable for CoWoS packages.
- ABF substrates are high-performance materials used in FC-BGA packaging, known for their excellent fine-line routing capabilities and thermal properties. However, their manufacturing requires sophisticated technology and equipment, and current supply struggles to keep pace with demand.

Background & Context

The rapid advancement of AI technology has pushed the demand for computing and memory in data centers to unprecedented levels. Particularly, the training and inference of large language models (LLMs) require vast quantities of HBM and high-performance logic chips. While the semiconductor industry is striving to expand production capacity to meet this surge, specific materials and components, especially HBM and ABF substrates, which are crucial elements of advanced backend processes, remain bottlenecks in the entire supply chain. This indicates that not just manufacturing chips, but also the ability to efficiently package and integrate them, determines competitive advantage in the AI era.

Strategic Significance & Outlook

The record-breaking increase in global semiconductor sales suggests that AI-driven market growth will continue. Aggressive investments by major memory manufacturers like SK Hynix will contribute to improving HBM supply, but the ABF substrate supply issue could constrain the growth rate of the AI semiconductor market in the short term. The industry as a whole will require concerted efforts across the supply chain to resolve bottlenecks and further investment in material manufacturers. While TSMC's high CoWoS yield demonstrates technological breakthroughs, building a balanced supply capacity across the entire ecosystem is crucial to unlock the market's true potential.

Source:
https://amiko.consulting/%E5%8D%8A%E5%B0%8E%E4%BD%93%E3%83%8B%E3%83%A5%E3%83%BC%E3%8
20260812/

#35 TSMC Declares AI Advanced Packaging Competition Shifts to System-Level Reliability and Validation, Highlighting 3DIC Importance at OCP APAC 2026

Published August 12, 2026 digitimes Taiwan

OVERVIEW

At the OCP APAC 2026 summit, TSMC Vice President of Advanced Packaging Technology & Service, Jun He, announced that the escalating AI computing demand is rapidly increasing chip integration complexity, shifting the advanced packaging competition beyond single-device performance to overall reliability and validation across package, board, system, and even rack levels. AI systems require unprecedented levels of quality, reliability, and development speed, necessitating comprehensive 3DIC (3D Integrated Circuit) validation that extends beyond conventional component-only certification.

IN DEPTH

Key Findings

During the OCP APAC 2026 summit, Jun He, TSMC's Vice President of Advanced Packaging Technology & Service, announced that the escalating demand for AI computing is dramatically increasing the complexity of chip integration. This shift means that competition in advanced packaging is no longer confined to single-device performance but has transitioned to overall reliability and validation at the package, board, system, and even rack levels. He emphasized that traditional component-only certification is insufficient for the unprecedented quality, reliability, and development speed required by AI systems, making comprehensive 3DIC (3D Integrated Circuit) validation essential.

Technical Details

- While traditional semiconductor development primarily focused on individual chip performance and reliability, the AI era is seeing complex 2.5D/3D packages (e.g., TSMC's CoWoS), integrating HBM (High Bandwidth Memory) with GPUs and CPUs, becoming the standard. In these systems, where numerous disparate chips operate cooperatively, not only individual chip performance but also comprehensive thermal management, power delivery, signal integrity, and long-term reliability of the entire integrated system become paramount.
- Jun He highlighted the critical importance of 3DIC validation. This involves not merely evaluating the electrical characteristics and physical structures of packaged chips but also simulating and validating their operation within the broader context of the board, system, and even the entire data center rack. This approach prevents unforeseen interactions and performance degradation, ensuring stable operation of AI systems.

Background & Context

The evolution of AI is driving a new paradigm shift in semiconductor design and manufacturing. Particularly, complex AI workloads like large language models (LLMs) demand massive data processing and ultra-high-speed communication between processors and memory. Consequently, advanced packaging, including chiplet technology and heterogeneous integration, has become a primary means of enhancing semiconductor performance. In this context, the expansion of foundry roles like TSMC, from mere manufacturing contractors to solution providers assisting customers with overall system design and validation, marks a significant turning point for the industry.

Strategic Significance & Outlook

TSMC's statement underscores that advanced packaging is at the forefront of technological competition in the AI era. The focus on system-level reliability and validation will lead to the provision of more reliable solutions for AI chip designers and data center operators. Moving forward, major foundries like TSMC are expected to collaborate more closely with customers, offering comprehensive services, including 3DIC validation, to accelerate the development speed of AI systems and reduce time-to-market. This approach is indispensable for supporting the further widespread adoption of AI technology and the sustained growth of the semiconductor industry.

Source: https://www.digitimes.com/news/a20260811PD258/packaging-tsmc-demand-design-development.html

Collected: August 16, 2026 | Automated Research System (Gemini API)