Semiconductor packaging

Weekly Intelligence Report

2026-08-30 | 19 articles | 8 countries

troy-technical.jp

This Week's Keyword

AI Chip Packaging

Supply chain diversification & yield boost

19	8	30	20
articles	countries	%	%
Total Articles Analyzed	Source Countries	Thermal Cond. Improve	FC-BGA Capacity Boost

All 19 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	Google TPUs Intel EMIB	Corporate Strategy	●●●○○	●●●●●	●●●●○	●●●○○	●●●●●	Google adopts Intel EMIB for next-gen TPUs, achieving yield targets in mass production, diversifying supply.
#02	Rapidus 600mm PLP 2030	Corporate Strategy	●●●●○	●●○○○	●●●●○	●●●○○	●●●●○	Rapidus targets 600mm panel-level packaging and 8-reticle interposers by 2030 for AI/HPC.
#03	ASMPT TCB/Hybrid Bonding	New Product	●●●○○	●●●●○	●●●○○	●●○○○	●●●○○	ASMPT to showcase advanced thermocompression and hybrid bonding for HPC/AI at SEMICON Taiwan 2026.
#04	Unimicron Thai ABF Plant	Corporate Strategy	●●○○○	●●●●●	●●●●○	●●●○○	●●●●○	Unimicron starts mass production at new Thai ABF plant to meet AI server demand, diversifying risk.
#05	SEMCO FC-BGA Capacity	Corporate Strategy	●●○○○	●●●●○	●●●○○	●●●○○	●●●○○	Samsung Electro-Mechanics boosts FC-BGA substrate capacity by 20% for AI/HPC, enhancing competitiveness.
#06	Ibiden ABF Yield Improve	Research	●●●●○	●●●○○	●●●●○	●●●○○	●●●●○	Ibiden improves AI chip ABF substrate yield with new process, stabilizing supply for high-performance chips.
#07	Shinko EU Auto/Industrial	Corporate Strategy	●●○○○	●●●●●	●●●○○	●●○○○	●●●●●	Shinko Electric expands high-density package substrate supply to European automotive/industrial clients.
#08	Resonac Thermal Materials	New Material	●●●●○	●●●○○	●●●●○	●●●●○	●●●●○	Resonac develops innovative thermal management materials, achieving 30% thermal conductivity improvement for AI/HPC.
#09	Ajinomoto ABF Film Expand	Corporate Strategy	●●○○○	●●●●○	●●●●○	●●●○○	●●●●○	Ajinomoto Fine-Techno expands ABF film capacity, anticipating easing AI chip supply shortages by early 2027.
#10	Japan Adv Pkg Subsidy	Corporate Strategy	●●○○○	●●●●●	●●●●●	●●●●○	●●●●●	Japan introduces new subsidy program for advanced packaging R&D;, focusing on heterogeneous integration.
#11	Applied Mat Hybrid Bond	New Product	●●●●○	●●●●○	●●●●○	●●●●○	●●●●●	Applied Materials unveils new hybrid bonding platform for high-volume 3D stacked chip manufacturing.
#12	KLA AI Defect Inspect	New Product	●●●●○	●●●●○	●●●●○	●●●●○	●●●●●	KLA unveils AI-powered high-speed, high-precision defect inspection solution to boost advanced package yield.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#13	Onto Metrology PLP	New Product	●●●●○	●●●●○	●●●○○	●●●●○	●●●●●	Onto Innovation unveils high-precision, high-speed metrology solution to accelerate Panel Level Packaging mass production.
#14	imec Glass Substrates	Research	●●●●●	●●○○○	●●●●○	●●●○○	●●●●●	imec announces breakthrough in 3D stacked packaging with glass substrates for AI/HPC.
#15	Fraunhofer FHS	Research	●●●●○	●●○○○	●●○○○	●●●○○	●●●●●	Fraunhofer IZM demonstrates high-density Flexible Hybrid Substrate (FHS) for wearables and IoT.
#16	AT&S; HPC Substrate	Corporate Strategy	●●○○○	●●●●○	●●●○○	●●○○○	●●●●●	Austrian AT&S; accelerates IC substrate capacity expansion for HPC, responding to data center demand.
#17	Infineon EU Chips Act	Corporate Strategy	●●○○○	●●●●●	●●●●○	●●●●○	●●●●●	Infineon strengthens advanced packaging collaboration in Europe under EU Chips Act.
#18	STMicro Auto SiP	New Product	●●●○○	●●●●○	●●●○○	●●●○○	●●●●●	STMicroelectronics unveils modular SiP solution for automotive AI, driving miniaturization and performance.
#19	Glass Substrate Mass Prod	Market Overview	●●●○○	●●●●○	●●●●○	●●●○○	●●●●○	Glass substrates in advanced packaging accelerate to mass production, key for HBM and chiplet integration.

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI/HPC supply chain diversified enough?

Google's adoption of Intel EMIB (#01) and Unimicron's new Thai plant (#04) highlight the urgent need to de-risk reliance on single-source advanced packaging and substrate suppliers. Are your procurement strategies robust against geopolitical shifts and capacity constraints?

❷ Are your next-gen packaging roadmaps ready for 3D-IC and glass substrates?

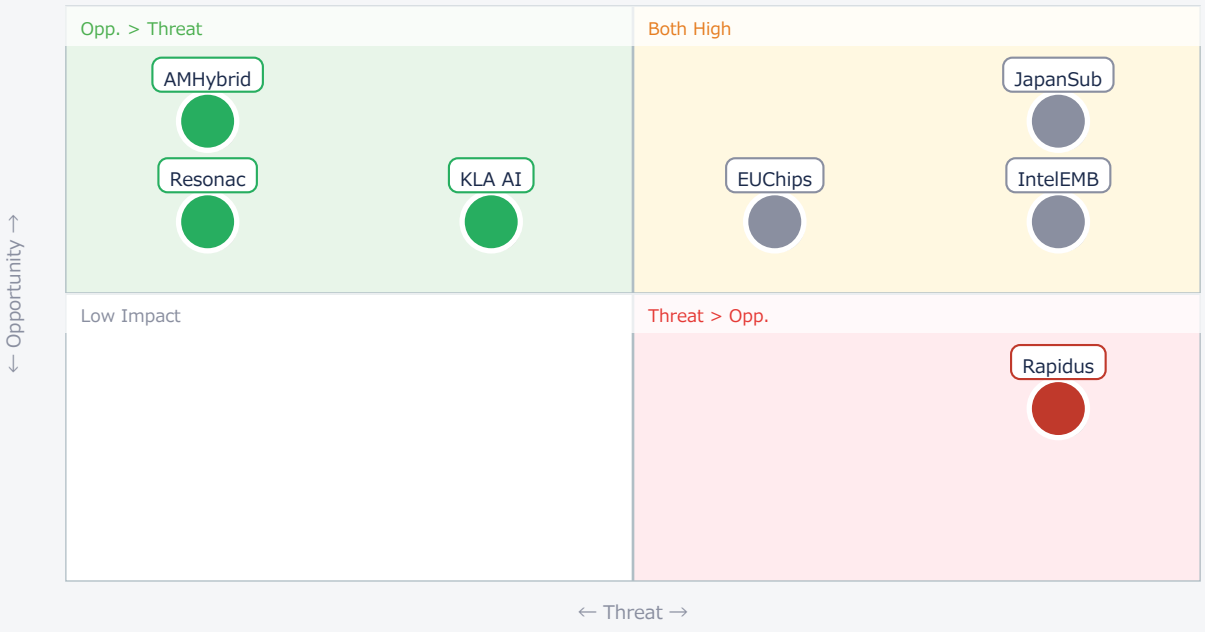
Applied Materials' new hybrid bonding platform (#11) and imec's glass substrate breakthrough (#14) signal a rapid shift towards high-volume 3D stacking. Does your R&D; have a clear strategy to leverage these technologies for future AI/HPC designs?

❸ How will Japan and EU's strategic investments impact your competitiveness?

Japan's new advanced packaging subsidy (#10) and Infineon's EU Chips Act collaboration (#17) are creating regional powerhouses. What is your strategy to compete or collaborate with these emerging, government-backed ecosystems?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
JapanSub	Critical	New market access	Increased competition
EUChips	Critical	EU internal growth	Regional competition
IntelEMB	Critical	Intel market gain	TSMC CoWoS threat
AMHybrid	Opp.	3D-IC mass production	—
KLA AI	Opp.	Yield improvement	—
Resonac	Opp.	Cooling solutions	—
Rapidus	Threat	—	Japan cost advantage

Deep Dive ① — Applied Materials' Hybrid Bonding Platform

#11 | 2026/08/28 | Business Wire | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●○ Data Reliability●●●●○ US/EU Relevance●●●●●

Applied Materials has unveiled a new hybrid bonding platform for high-volume manufacturing of 3D stacked chips, crucial for next-gen AI/HPC. This system achieves ultra-fine pitch, high-precision alignment, and high throughput, resolving bottlenecks.

Hybrid bonding directly joins chips at a molecular level, enabling higher connection density and shorter signal paths. This platform accelerates the commercialization of 3D-ICs, supporting HBM stacks, chiplet interconnections, and 3D-SoCs.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The published claims for high-precision, high-throughput hybrid bonding are realistic, building on years of R&D.; Technical barriers include managing thermal stress during bonding and ensuring defect-free interfaces at ultra-fine pitches in high-volume production. [Opportunity] for US/EU OEMs and device manufacturers to leverage this platform for advanced AI/HPC designs, enabling unprecedented performance. [Threat] for those reliant on older packaging methods, as this technology will become a standard. Next actions: [R&D;] Evaluate platform capabilities for next-gen product roadmaps by end of quarter. [Procurement] Engage Applied Materials for early access/evaluation units by next month.

Deep Dive ② — KLA's AI-Powered Defect Inspection

#12 | 2026/08/27 | SEMI Global | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●○ Data Reliability●●●●○ US/EU Relevance●●●●●

KLA introduced an AI-powered defect inspection solution for advanced semiconductor packaging, including CoWoS. It detects minute defects in high-density RDLs and 3D stacked structures with superior speed and precision, boosting yield.

Key features include AI-powered pattern recognition for subtle defects, high-speed scanning, 3D structural defect visualization, and real-time feedback for process control. This is vital for complex chiplet integration and HBM stacking.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: KLA's AI-powered inspection is a credible advancement, as AI is increasingly critical for complex pattern recognition. The challenge lies in integrating these systems seamlessly into existing high-volume lines and continuously updating AI models for new defect types. [Opportunity] for US/EU OEMs and device manufacturers to significantly improve yields and reduce costs in advanced packaging, especially for AI/HPC chips. [Threat] for competitors who lack such advanced inspection capabilities, leading to lower yields and slower time-to-market. Next actions: [Operations] Assess current inspection bottlenecks and plan for pilot integration of KLA's solution within 6 months. [R&D;] Collaborate with KLA to optimize defect detection for proprietary package designs.

Deep Dive ③ — imec's Glass Substrate Breakthrough

#14 | 2026/08/25 | EETimes | Tech Novelty●●●●● Proximity●●○○○ Market Impact●●●●○ Data Reliability●●●○○ US/EU Relevance●●●●●

imec, a Belgian research institute, announced a breakthrough in 3D stacked packaging using glass substrates as interposers. Glass offers superior flatness, low dielectric loss, and high thermal stability for AI/HPC applications.

The advancements include ultra-fine Through-Glass Via (TGV) technology, low-warpage processes for large substrates, and heterogeneous integration capabilities. imec aims for commercialization through joint research within the next few years.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: imec's breakthrough in TGV and low-warpage processes for glass substrates is a significant technical achievement, pushing the boundaries of advanced packaging. Realism is high given imec's track record, but commercialization still faces challenges in scaling to high-volume manufacturing and cost reduction. [Opportunity] for US/EU materials and component suppliers to develop compatible glass materials and processing equipment. [Threat] for companies heavily invested in silicon interposers, as glass offers superior performance metrics. Next actions: [R&D;] Initiate internal feasibility studies on glass substrate integration for future product generations by end of quarter. [Business Dev] Explore collaborative R&D; partnerships with imec and its partners immediately.

Other Notable Articles

Unimicron Initiates Mass Production at New Thai ABF Substrate Plant (DigiTimes Japan)
Tech Novelty●●○○○ Proximity●●●●● Market Impact●●●●○

Crucial for diversifying AI server ABF substrate supply chains and mitigating geopolitical risks.

Ibiden Announces Significant Yield Improvement in AI Chip ABF Substrates with New Process Technology, Stabilizing Supply (Nikkei Asia)
Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○

Yield improvements in critical ABF substrates are vital for easing AI chip production bottlenecks.

Ajinomoto Fine-Techno to Expand ABF Film Production Capacity, Anticipates Easing AI Chip Supply Shortages by Early 2027 (The Wall Street Journal)
Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●○

Raw material capacity expansion is a direct response to AI chip demand, easing supply by early 2027.

Austrian AT&S; Accelerates IC Substrate Capacity Expansion for High-Performance Computing (HPC), Responding to Data Center Demand (Business Journal)
Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●○○

European-based capacity expansion for HPC substrates strengthens regional supply for data centers.

STMicroelectronics Unveils Modular SiP Solution for Automotive AI Market, Driving Miniaturization and Performance in Autonomous Driving and ADAS (Electronics Weekly)
Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●○○

A modular SiP solution from a European vendor directly addresses the growing automotive AI market needs.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Review current advanced packaging and substrate supplier diversification strategies, especially for AI/HPC components, in light of Google's EMIB adoption and Asian capacity expansions.
- [Strategy] Initiate competitive intelligence deep dive on Japan's new advanced packaging subsidy program (#10) to identify potential collaboration or competitive threats.

Short-term (1 month)

- [R&D;] Task advanced packaging teams to evaluate Applied Materials' new hybrid bonding platform (#11) and imec's glass substrate breakthrough (#14) for integration into future product roadmaps.
- [Procurement] Engage with Unimicron (#04), Ajinomoto (#09), and Ibiden (#06) to understand their capacity expansion and yield improvement timelines for critical ABF substrates and films.
- [Business Dev] Explore potential partnerships with European entities like Infineon (#17), AT&S; (#16), and STMicroelectronics (#18) under the EU Chips Act for regional supply chain resilience.

Medium-long term (quarter+)

- [Executive] Develop a comprehensive regionalization strategy for advanced packaging, considering investments in US/EU manufacturing capabilities and strategic alliances to mitigate geopolitical risks.
- [R&D;] Establish a dedicated task force to explore the long-term potential of glass substrates and panel-level packaging (Rapidus #02, imec #14, Onto Innovation #13) for next-generation chip architectures beyond 2030.
- [Legal/IP] Conduct a landscape analysis of IP related to hybrid bonding, glass substrates, and advanced thermal management materials (Resonac #08) to identify licensing opportunities or potential infringement risks.

Semiconductor_BackEnd — Selected Articles

Date: 2026-08-30

Articles: 19

Table of Contents

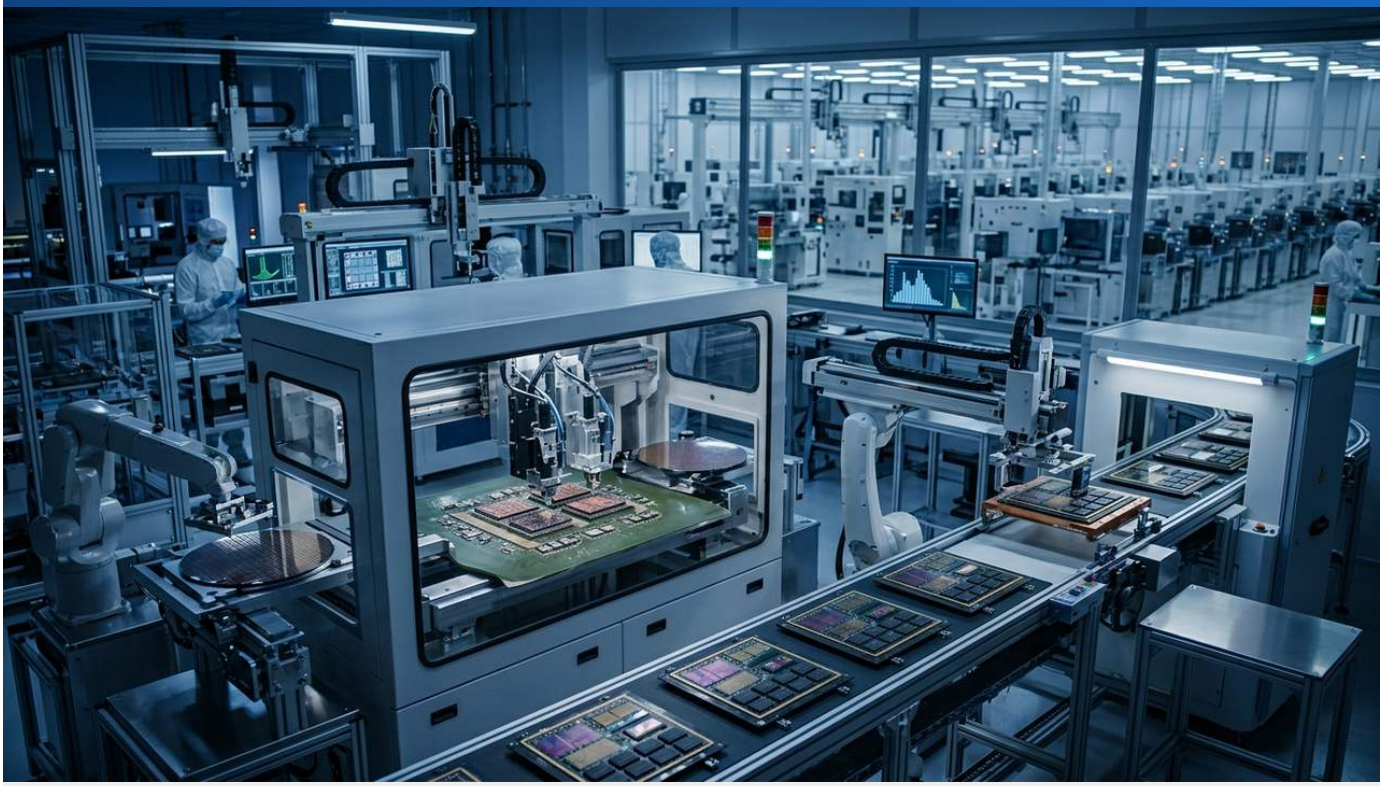
#18 Infineon Strengthens Advanced Packaging Collaboration in Europe under EU Chips Act, Building Chiplet and Heterogeneous Integration Supply Chain

#19 STMicroelectronics Unveils Modular SiP Solution for Automotive AI Market, Driving Miniaturization and Performance in Autonomous Driving and ADAS

#20 Glass Substrates in Advanced Packaging Accelerate from Prototype to Mass Production, Emerging as Key Technology for HBM and Chiplet Integration

#01 Google's Next-Gen TPUs Adopt Intel EMIB Packaging, Achieve Yield Targets in First Mass Production

Published August 27, 2026 digitimes Taiwan



OVERVIEW

Google has successfully implemented Intel's Embedded Multi-die Interconnect Bridge (EMIB) packaging technology for mass production of its next-generation TPUs, already achieving yield targets. This strategic move, in collaboration with MediaTek, addresses the increasing cost and capacity constraints of TSMC's CoWoS, diversifying Google's advanced packaging supply chain. The successful adoption is poised to open significant opportunities for Intel in the high-performance computing market, potentially leading to EMIB's sustained use in future TPU iterations.

IN DEPTH

Key Findings

Google has successfully adopted Intel's Embedded Multi-die Interconnect Bridge (EMIB) packaging technology for its next-generation Tensor Processing Units (TPUs) in mass production, already achieving critical yield targets. This adoption stems from EMIB meeting Google's stringent criteria across technical performance, cost-efficiency, and production capacity, positioning it as a viable alternative to TSMC's constrained CoWoS technology. This collaboration also sees MediaTek deepening its partnership with Google as an ASIC co-development partner.

Technical / Clinical Details

Intel's EMIB facilitates high-density interconnections between multiple semiconductor dies within a single package, bypassing the need for a full-size silicon interposer characteristic of TSMC's CoWoS (Chip-on-Wafer-on-Substrate). By utilizing localized silicon bridges, EMIB simplifies the manufacturing process, which can lead to lower costs and improved yields, especially for integrating AI accelerators and High Bandwidth Memory (HBM). TSMC's CoWoS has faced structural bottlenecks, including escalating costs, yield risks, and capacity limitations, making EMIB an attractive alternative. The reported achievement of yield targets in Google's initial EMIB-powered TPUs underscores the maturity and reliability of this advanced packaging solution.

Background & Context

The burgeoning demand for AI and High-Performance Computing (HPC) has exponentially increased the need for advanced semiconductor packaging. While TSMC's CoWoS has been a dominant solution due to its superior performance, its supply has been severely constrained, unable to fully meet market demand. In this context, major technology companies like Google are actively seeking to diversify their packaging supply chain and mitigate risks. The successful integration of EMIB by Google signifies a significant shift in the advanced packaging landscape. Furthermore, Taiwan's Powertech Technology (PTI) is also projected to commence mass production of its panel-level packaging (PiFO) by mid-2027, indicating a broader trend of innovation and increasing competition in the advanced packaging sector.

Strategic Significance & Outlook

Google's embrace of EMIB offers Intel a substantial opportunity to secure more customers in the advanced packaging domain. The strong likelihood of EMIB's continued use in future TPU generations suggests its potential to emerge as a new industry standard for AI hardware. This development is expected to have a profound impact on the semiconductor industry's supply chain strategies, reducing reliance on TSMC's CoWoS and fostering a more diversified and robust packaging ecosystem. Investors and industry observers will be closely monitoring the broader adoption of EMIB and its potential to reshape market dynamics.

Source: https://www.digitimes.com/news/a20260827PD212/google-mediatek-packaging-intel-tpu.html

Collected: August 28, 2026 | Automated Research System (Gemini API)

#02 Rapidus Targets 600mm Panel-Level Packaging and 8-Reticle Interposers by 2030 for Advanced AI/HPC Systems

Published August 21, 2026 TrendForce Japan

OVERVIEW

Rapidus announced an accelerated advanced packaging roadmap aiming for 600mm panel-level packaging and 8-reticle interposers by 2030. The company has fully activated its Rapidus Chiplet Solutions (RCS) pilot line to validate 2.xD and 3D packaging processes, focusing on high-density chiplet integration for next-generation AI and HPC systems. This strategic move includes a comprehensive portfolio of flip-chip BGA, 2.5D silicon interposers, panel-level RDL organic interposers, and 3D stacking via hybrid bonding, positioning Japan at the forefront of advanced semiconductor manufacturing.

IN DEPTH

Key Findings

The Japanese consortium Rapidus has unveiled an ambitious advanced packaging roadmap, targeting 600mm panel-level packaging and 8-reticle interposers by 2030 to enable high-density chiplet integration for next-generation AI and high-performance computing (HPC) systems. The company has already commenced validation of 2.xD and 3D packaging processes through the full activation of its Rapidus Chiplet Solutions (RCS) pilot line. This initiative represents a critical technological leap, potentially reshaping the landscape of advanced semiconductor manufacturing and strengthening Japan's competitive edge in the global supply chain for the AI era.

Technical Details

Rapidus's advanced packaging strategy centers on leveraging larger interposers and pioneering panel-level processing. The interposer roadmap outlines a phased expansion from current 4-reticle (3,320 mm^2) designs to 6-reticle (4,980 mm^2) by 2028, culminating in 8-reticle (6,640 mm^2) by 2030. A cornerstone of this plan is the development of a 600 x 600 mm panel-level packaging platform, which is projected to yield an organic substrate area of approximately 14,400 mm^2 by 2030. This shift from wafer-based to panel-based processing is expected to deliver significant cost reductions and yield improvements, crucial for high-volume manufacturing. The comprehensive packaging portfolio includes flip-chip BGA, 2.5D silicon interposers, panel-level RDL organic interposers, and advanced 3D stacking techniques via hybrid bonding, all essential for realizing ultra-high-density chiplet integration.

Background and Industry Context

The escalating demands of artificial intelligence and HPC have driven an urgent need for innovations not only in chip fabrication but also in packaging technologies. As the limits of traditional transistor scaling become apparent, heterogeneous integration—the sophisticated method of combining diverse chiplets into a single package—is seen as a key enabler for transcending the limitations of Moore's Law. Rapidus, with substantial backing from Japan's Ministry of Economy, Trade and Industry (METI), is concurrently pursuing 2nm process technology development, underscoring its commitment to re-establishing Japan's prominence in the global semiconductor ecosystem. This dual focus on leading-edge manufacturing and advanced packaging is vital for creating vertically integrated solutions that meet future market demands.

Strategic Significance and Outlook

Rapidus's aggressive roadmap is a strategic imperative alongside its 2nm process development, forming the core of its integrated semiconductor manufacturing vision. The 600mm panel-level packaging technology, by processing on significantly larger substrates than traditional wafers, promises revolutionary improvements in cost efficiency and throughput. By achieving these targets by 2030, Rapidus aims to establish high-volume production capabilities for next-generation high-performance semiconductors, potentially positioning itself as a key player in the fiercely competitive AI chip market and leading the resurgence of Japan's semiconductor industry. The move signifies a concerted effort to build a resilient and innovative domestic supply chain.

Source: https://www.trendforce.com/news/2026/08/21/news-rapidus-scales-up-advanced-packaging-targets-8-reticle-interposers-with-600mm-panels-by-2030/

Collected: August 28, 2026 | Automated Research System (Gemini API)

#04 ASMPT to Showcase Advanced Thermocompression and Hybrid Bonding Innovations for HPC and AI at SEMICON Taiwan 2026

Published August 26, 2026 ASMPT SEMI Solutions Taiwan

OVERVIEW

Global technology leader ASMPT announced it will showcase its advanced packaging portfolio at SEMICON Taiwan 2026, supporting HPC, AI accelerators, silicon photonics, and Co-Packaged Optics (CPO) applications. The company will highlight high-precision solutions like its MEGA multi-chip bonding system, leveraging thermocompression bonding (TCB) and hybrid bonding technologies. These innovations are crucial for high-density chiplet integration and enhanced data transfer rates, addressing critical manufacturing challenges for next-generation high-performance devices.

IN DEPTH

Key Findings

ASMPT, a global technology leader, announced its plan to showcase groundbreaking advanced packaging technologies at SEMICON Taiwan in September 2026. These innovations are designed to robustly support cutting-edge applications such as High-Performance Computing (HPC), AI accelerators, silicon photonics, and Co-Packaged Optics (CPO). The company will feature its expertise in critical techniques like Thermocompression Bonding (TCB) and Hybrid Bonding, presenting solutions that enable high-precision chiplet integration and high-speed data transfer. This exhibition underscores ASMPT's technological leadership in meeting the complex semiconductor packaging demands of the AI era.

Technical Details

Central to ASMPT's exhibit will be its MEGA multi-chip bonding solution, a system renowned for its exceptional chip placement and alignment accuracy. This solution integrates sophisticated dispensing, UV curing, and advanced inspection capabilities, facilitating ultra-fine pitch bonding essential for efficiently and reliably integrating numerous chiplets. Thermocompression Bonding (TCB) enables fine-pitch copper-to-copper interconnections, delivering high electrical performance and superior thermal management when combined with low coefficient of thermal expansion (CTE) materials. Hybrid bonding, offering even finer connection pitches and higher bond strengths, is a pivotal technology for die-to-wafer or die-to-die connections in 3D-ICs, crucial for next-generation chiplet architectures. These technologies collectively drive significant improvements in performance and power efficiency, particularly for AI processing units and High Bandwidth Memory (HBM) modules in data centers.

Background and Industry Context

The semiconductor industry faces unprecedented demands for speed, miniaturization, and higher integration driven by megatrends like AI, 5G, and autonomous driving. As the limits of traditional transistor scaling become apparent, heterogeneous integration—the strategy of segmenting functionalities into chiplets and integrating them using advanced packaging—has emerged as a vital path forward. Taiwan stands as a global hub for the semiconductor supply chain, and SEMICON Taiwan is one of the most significant semiconductor events in the Asia-Pacific region. Major suppliers like ASMPT unveiling their latest technologies here significantly impacts the entire semiconductor ecosystem in Taiwan and globally.

Strategic Significance and Outlook

ASMPT's advanced packaging technologies are poised to play an indispensable role in semiconductor manufacturing for the AI era. High-density chiplet integration and low-latency data transfer are paramount for achieving peak performance in HPC and AI accelerators. The company's solutions not only meet these immediate requirements but also pave the way for future technological frontiers such as Co-Packaged Optics (CPO). CPO, which integrates optical and electronic devices within a single package, promises to revolutionize data transfer by eliminating bottlenecks and drastically reducing power consumption in data centers, while boosting performance. ASMPT's continuous innovation is set to shape the future of semiconductor packaging and accelerate the evolution of digital society.

Source: https://semi.asmpt.com/en/news-center/press-releases/asmpt-at-semicon-southeast-asia-2026-from-advanced-packaging-to-intelligent-factories-11/

Collected: August 28, 2026 | Automated Research System (Gemini API)

#05 Unimicron Initiates Mass Production at New Thai ABF Substrate Plant to Meet Surging AI Server Demand, Diversifying Geopolitical Risk

Published August 27, 2026 DigiTimes Japan Taiwan

OVERVIEW

Unimicron has commenced mass production at its new facility in Thailand, addressing the escalating demand for Ajinomoto Build-up Film (ABF) substrates, especially for AI servers. This strategic expansion aims to diversify geopolitical risks and bolster supply capacity beyond its existing Taiwanese operations. The company plans to significantly increase its revenue share from AI-related products by late 2026, solidifying its position as a key supplier in the rapidly growing AI market.

IN DEPTH

Key Findings

Unimicron has officially begun mass production at its new ABF (Ajinomoto Build-up Film) substrate plant in Thailand, a critical move to satisfy the skyrocketing demand for high-performance substrates used in AI servers. This new facility is poised to alleviate the supply shortage of high-density, multi-layer ABF substrates, particularly those required for advanced AI accelerators integrating High Bandwidth Memory (HBM). The launch of this plant strategically diversifies Unimicron's production footprint, mitigating geopolitical risks associated with concentrated manufacturing in Taiwan, while simultaneously enhancing its global supply capabilities. Unimicron projects a substantial increase in AI-related revenue by the latter half of 2026, positioning this new plant as a cornerstone of its growth strategy in the burgeoning AI market.

Technical and Manufacturing Details

ABF substrates are indispensable components for packaging high-performance semiconductors such as CPUs and GPUs, with AI/HPC (High-Performance Computing) applications demanding increasingly complex multi-layer structures and finer line widths. Unimicron’s Thai plant incorporates the latest manufacturing technologies and advanced automation systems to achieve high-yield production of high-quality ABF substrates. This enables the company to meet the stringent specifications of next-generation AI processors that power data centers and cloud infrastructures. Specific technological advancements include uniform circuit pattern formation techniques for high-layer count substrates, precise processing of low-dielectric loss materials, and structural designs optimized for enhanced thermal management.

Background and Industry Context

In recent years, the strengthening of semiconductor supply chains and geographical diversification has become a global imperative, particularly concerning the concentration of advanced semiconductor manufacturing capabilities in Taiwan. Unimicron's investment in Thailand aligns with this global trend, offering crucial supply chain stability for its customers. The rapid evolution of AI has led to an explosive demand for ABF substrates, driving manufacturers worldwide to accelerate capacity expansion. The AI server market is projected for sustained high growth, making the stable supply of high-performance packaging substrates vital for the overall development of the AI industry.

Strategic Significance and Outlook

With the operational launch of its new Thai plant, Unimicron is set to further solidify its presence in the AI market and expand its customer base. The company remains committed to aggressive investment in R&D for next-generation ABF substrates, focusing on miniaturization, high-frequency compatibility, and low-thermal expansion technologies. This commitment aims to support the continuous evolution of AI semiconductor technology from the packaging perspective. By doing so, Unimicron expects to maintain its competitive edge in the global packaging substrate market, pursue sustainable growth, and establish a flexible production system capable of meeting diverse customer needs.

Source: #

#06 Samsung Electro-Mechanics Boosts FC-BGA Substrate Capacity by 20% for AI/HPC, Enhances Competitiveness with Fine-Pitch Wiring

Published August 26, 2026 The Korea Economic Daily South Korea

OVERVIEW

Samsung Electro-Mechanics (SEMCO) announced a 20% expansion of its high-end FC-BGA substrate production capacity in South Korea, driven by surging demand from AI/HPC applications. This strategic investment integrates advanced fine-pitch wiring technologies and low-dielectric materials to strengthen competitiveness. The move aims to maintain SEMCO's leadership in the global market, ensuring stable supply for next-generation AI processors and data centers.

IN DEPTH

Key Findings

Samsung Electro-Mechanics (SEMCO) has announced a significant 20% increase in its production capacity for high-end Flip-Chip Ball Grid Array (FC-BGA) substrates at its South Korean facilities. This substantial expansion is a direct response to the booming demand from the artificial intelligence (AI) and high-performance computing (HPC) markets, particularly for next-generation AI processors and data center chips. As a leading player in FC-BGA technology, SEMCO aims to solidify its competitive edge through this investment.

The capacity boost includes the integration of cutting-edge fine-pitch wiring technologies and advanced low-dielectric materials, which are crucial for high-frequency signal transmission. These enhancements will enable SEMCO to meet the increasingly complex packaging requirements of high-performance chips, contributing to improved signal integrity and reduced power consumption. FC-BGA substrates are a core interconnect technology for high-performance CPUs, GPUs, and AI accelerators, making their performance and stable supply critical for the overall advancement of the semiconductor industry.

Technical and Manufacturing Details

FC-BGA substrates are high-density packaging components designed to electrically connect chips to printed circuit boards, characterized by their multi-layer structure and fine interconnects. SEMCO focuses on developing sub-micron wiring technology, multi-layer stacking, and robust thermal management solutions. This expansion specifically addresses warpage control for increasingly thick substrates and incorporates new dielectric layer materials to achieve ultra-low dielectric loss. These advancements are vital for maximizing the power delivery and high-speed signal transmission capabilities demanded by AI/HPC chips.

Background and Industry Context

The proliferation of AI and the expansion of data centers are the primary drivers for the FC-BGA substrate market. Major semiconductor manufacturers like NVIDIA, AMD, and Intel are intensely competing to release high-performance AI chips, leading to a surge in demand for advanced packaging substrates. Particularly for AI accelerators integrated with High Bandwidth Memory (HBM), FC-BGA substrates serve as critical interposers, directly impacting AI chip production volumes. SEMCO's investment is a strategic decision that aligns with these market trends, aimed at ensuring long-term growth.

Strategic Significance and Outlook

SEMCO plans to continue expanding the frontiers of FC-BGA technology through ongoing R&D and capacity investments. Future efforts will focus on even finer pitch interconnections, higher layer counts, and improved cost efficiency, delivering next-generation packaging solutions to the market. By doing so, SEMCO aims to establish itself as a dominant supplier in the AI/HPC market, contributing significantly to the broader semiconductor ecosystem.

Source: #

#07 Ibiden Announces Significant Yield Improvement in AI Chip ABF Substrates with New Process Technology, Stabilizing Supply

Published August 24, 2026 Nikkei Asia Japan

OVERVIEW

Ibiden has reported a substantial improvement in manufacturing yield for Ajinomoto Build-up Film (ABF) substrates used in AI processors, driven by the introduction of a new process technology. This advancement ensures a more stable supply of high-performance ABF substrates to meet the surging AI chip demand. The company is also intensifying R&D efforts in miniaturization and warpage reduction, reinforcing its capabilities for next-generation AI chips.

IN DEPTH

Key Findings

Ibiden has announced a significant breakthrough in its manufacturing process for Ajinomoto Build-up Film (ABF) substrates, a critical interposer for AI processors, achieving a substantial improvement in yield. This technological innovation signifies that Ibiden has established a robust framework to provide a more stable supply of high-quality ABF substrates to meet the escalating demand for AI chips. As AI chip performance advances, ABF substrates are required to possess exceptionally high reliability and complex wiring structures. While maintaining yield has been a challenge with increasing miniaturization in conventional manufacturing processes, Ibiden's new technology overcomes this hurdle. This enables semiconductor manufacturers to more efficiently produce AI processors and is expected to significantly contribute to strengthening the entire AI industry's supply chain.

Technical and Manufacturing Details

The new process technology developed by Ibiden primarily focuses on the following aspects:

- **Optimization of Ultra-Fine Wiring Formation Technology:** Precise control over exposure and etching processes enables high-accuracy formation of sub-micron level wiring patterns, which were previously challenging.
- **Enhanced Interlayer Connection Reliability:** Improvements in interlayer adhesion and via formation techniques during multi-layer stacking lead to stabilized electrical properties and increased reliability.
- **Optimized Material Properties:** Reevaluation of material selection and processing techniques for low-dielectric loss and low-coefficient of thermal expansion (CTE) materials ensures both high-frequency compatibility and warpage suppression.
- **Strengthened Automated Inspection Systems:** Implementation of AI-powered inline inspection systems facilitates early defect detection and rapid process feedback.

These improvements have led to a dramatic increase in consistency and production efficiency, especially in the manufacturing of high-layer-count ABF substrates for AI chips. Ibiden plans to continue developing further miniaturization and low-warpage technologies to meet the future specifications of AI chips.

Background and Industry Context

The explosive proliferation of AI is driving significant transformation in the semiconductor industry. High-performance AI chips require complex package structures, often integrating High Bandwidth Memory (HBM) and multiple chiplets, to process vast amounts of data at high speeds. Consequently, ABF substrates, which connect chips and substrates, have become a bottleneck for AI chip production. With supply shortages and quality challenges becoming prominent, yield improvements by major suppliers like Ibiden are crucial for ensuring a stable supply of AI chips and accelerating the growth of the entire industry.

Strategic Significance and Outlook

Ibiden's recent announcement will further enhance the competitiveness of its ABF substrate business. The AI market is expected to continue its expansion, leading to even higher demand for high-performance ABF substrates. Leveraging this technological advantage, Ibiden aims to lead the packaging solutions for next-generation AI processors. Furthermore, the company plans to invest in the development of green process technologies to reduce environmental impact, contributing to sustainable semiconductor manufacturing.

Source: #

#08 Shinko Electric Industries Expands High-Density Package Substrate Supply to European Automotive and Industrial Clients, Targeting Automotive AI Demand

Published August 23, 2026 Japan Times Japan

OVERVIEW

Shinko Electric Industries announced an expanded supply of high-density package substrates to European automotive and industrial equipment manufacturers. The company’s robust and reliable packaging technology is highly valued amidst the proliferation of in-vehicle AI and edge AI devices. This strategic expansion is expected to bolster Shinko Electric Industries' presence in the global supply chain, addressing critical demand for advanced automotive electronics.

IN DEPTH

Key Findings

Shinko Electric Industries has decided to significantly expand its supply of high-density packaging substrates to automotive and industrial equipment manufacturers in the European market. This move reflects the accelerating adoption of in-vehicle AI and edge AI devices in areas such as autonomous driving, connected cars, industrial robots, and smart factories. These applications demand exceptionally robust and reliable packaging with superior heat dissipation capabilities due to harsh operating environments. Shinko Electric Industries' long-standing expertise in high-reliability packaging technology has garnered strong recognition from leading European manufacturers, leading to this supply expansion. This demonstrates the critical role Japanese substrate manufacturers play in the global semiconductor supply chain.

Technical and Product Details

The high-density packaging substrates that Shinko Electric Industries is expanding supply for feature the following:

- **High-Density Wiring Technology:** Fine line/space (L/S) capabilities enable connections for complex semiconductor chips with numerous I/Os.
- **High Heat Dissipation Materials and Structures:** Utilizes thermally conductive materials and optimized thermal dissipation path designs to efficiently dissipate large amounts of heat generated in automotive environments.
- **High Reliability and Robustness:** Material and structural designs capable of withstanding severe automotive and industrial conditions such as vibration, shock, and temperature variations. Particularly, high reliability of interlayer connections in multi-layer substrates.
- **Miniaturization and Thinning:** Technologies that minimize package footprint and thickness to meet the demand for smaller edge AI devices and automotive ECUs (Electronic Control Units).

Leveraging these technologies, the company meets the stringent quality standards and long-term supply requirements specific to the European market.

Background and Industry Context

Europe leads the global automotive and industrial equipment sectors, with AI technology rapidly being adopted in these areas in recent years. Advancements in autonomous driving levels and the proliferation of IoT devices in factories are driving up demand for high-performance, high-reliability semiconductors and the packaging technologies that support them. Furthermore, geopolitical considerations for supply chain diversification have made it a pressing issue for global corporations, increasing expectations for technically capable Japanese companies. Shinko Electric Industries' supply expansion is a strategic move that aligns with these market needs.

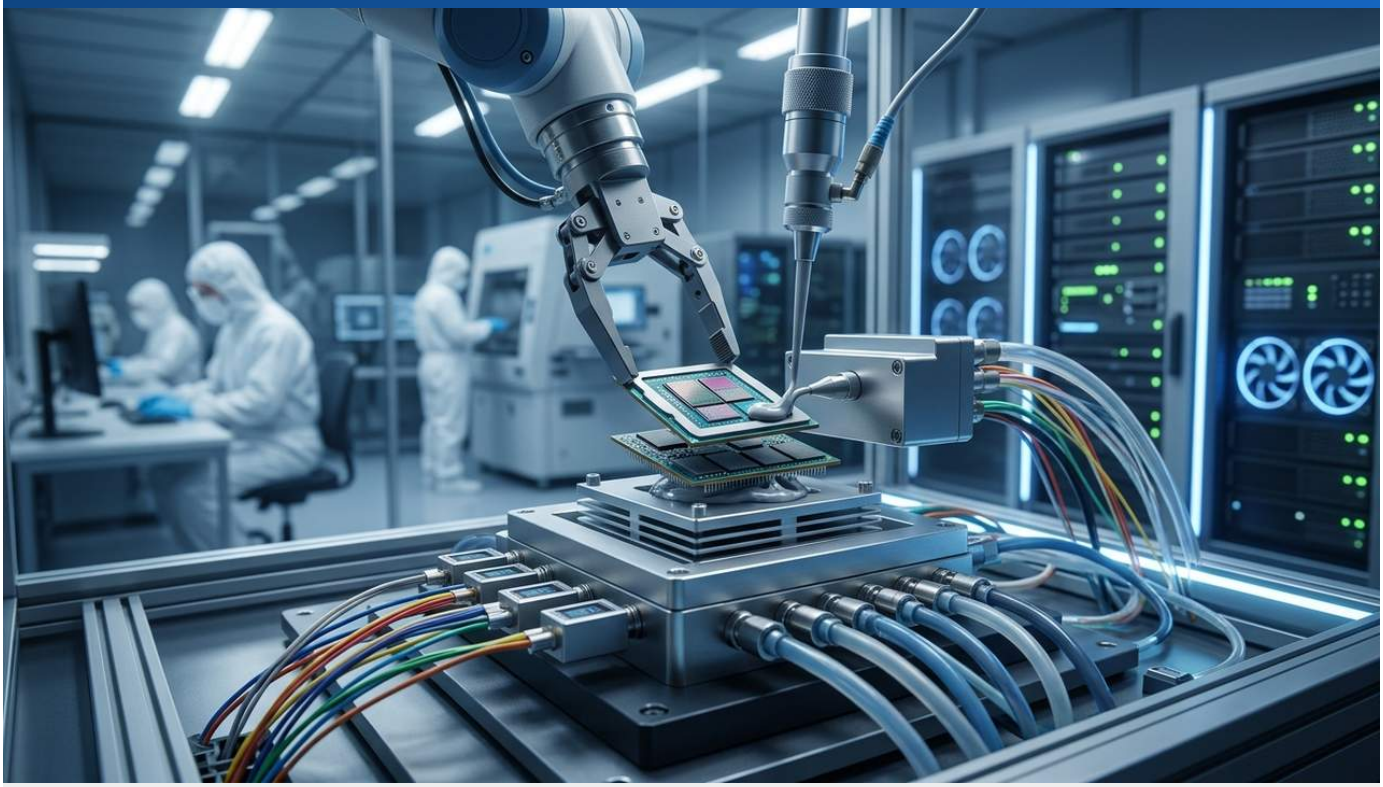
Strategic Significance and Outlook

By strengthening its presence in the European market, Shinko Electric Industries aims to further solidify its global business foundation. The company plans to continue investing actively in R&D for next-generation packaging technologies to support the evolution of AI in automotive and industrial sectors, providing solutions that meet diverse customer demands. In particular, it will enhance technology development to address trends such as modularization and heterogeneous integration, thereby maintaining its competitive advantage in the market.

Source: #

#09 Resonac Develops Innovative Thermal Management Materials Achieving 30% Thermal Conductivity Improvement for AI/HPC Semiconductor Packages

Published August 22, 2026 Chemical Daily Japan



OVERVIEW

Resonac has announced the development of groundbreaking thermal interface materials (TIMs) and encapsulants that boast a 30% improvement in thermal conductivity over conventional products. This innovation directly addresses critical heat issues in high-performance AI/HPC semiconductor packages. The new materials are expected to significantly suppress internal temperature rise, enhancing chip reliability and lifespan, thus proving a vital breakthrough for unlocking the full potential of AI chips.

IN DEPTH

Key Findings

Resonac has successfully developed next-generation thermal management materials that offer a groundbreaking solution to the urgent challenges of increasing power consumption and heat generation in AI (Artificial Intelligence) and HPC (High-Performance Computing) semiconductor packages. The newly developed thermal interface materials (TIMs) and encapsulants demonstrate a remarkable 30% improvement in thermal conductivity compared to existing products, enabling highly efficient heat dissipation from within the package. This technological achievement is crucial for maintaining low operating temperatures of AI chips, which in turn significantly improves chip stability, long-term reliability, and overall lifespan. AI chips perform vast computations for learning and inference, leading to substantial localized heat generation; without proper thermal management, their full potential cannot be realized. Resonac's new materials represent a key technology for facilitating the further performance enhancement and widespread adoption of AI chips.

Technical and Material Details

The thermal management materials developed by Resonac achieve high thermal conductivity and low thermal resistance through the optimized compounding of nanocarbon materials and specialized ceramic fillers. Key features include:

- **High Thermal Conductivity:** Achieving over 30% improvement in thermal conductivity compared to conventional products, significantly enhancing heat transfer efficiency from the chip to the heatsink.
- **Low Thermal Resistance:** Excellent thin-film forming properties and interfacial adhesion minimize thermal resistance along the heat transfer path.
- **High Reliability:** Maintains stable performance under thermal cycling and humid conditions, ensuring long-term durability.
- **Processability:** Optimized processing characteristics such as coatability and curability, facilitating easy application in mass production processes.

These properties enable uniform heat dissipation and temperature management in advanced packaging structures that stack multiple chips, such as CPUs, GPUs, and High Bandwidth Memory (HBM).

Background and Industry Context

As semiconductor miniaturization approaches its physical limits, packaging technology has become a critical frontier for improving chip performance. Particularly with the advent of chiplet and 3D stacking technologies, power density within packages has dramatically increased, leading to a proportional rise in heat generation. This thermal issue is one of the biggest bottlenecks for scaling AI/HPC chip performance, making advancements in cooling solutions indispensable. Resonac's latest development marks a significant step toward resolving this bottleneck and is expected to have a profound impact on the entire industry.

Strategic Significance and Outlook

Resonac plans to actively propose its newly developed thermal management materials to major semiconductor manufacturers and OSATs (Outsourced Semiconductor Assembly and Test providers) to achieve early market adoption. In the future, the company aims to continue developing materials with even higher thermal conductivity and capabilities to support diverse packaging structures, thereby solidifying its position as a leading company in solving semiconductor thermal issues. This technology is expected to find applications not only in AI but also across a wide range of high-density and high-heat fields, including 5G/6G communication, data centers, automotive, and power electronics.

Source: #

#10 Ajinomoto Fine-Techno to Expand ABF Film Production Capacity, Anticipates Easing AI Chip Supply Shortages by Early 2027

Published August 21, 2026 The Wall Street Journal Japan

OVERVIEW

Ajinomoto Fine-Techno disclosed plans to significantly boost its production capacity for Ajinomoto Build-up Film (ABF) film across multiple manufacturing sites, driven by exploding demand for AI chips. The company projects to meet most major customer demands by early 2027. However, tight supply for specific ultra-high-performance grades of ABF film may persist, highlighting ongoing challenges in this critical segment.

IN DEPTH

Key Findings

Ajinomoto Fine-Techno has announced a substantial expansion of its production capacity for ABF (Ajinomoto Build-up Film) film, a flagship product, in response to the rapid surge in demand for AI chips. This expansion plan spans multiple manufacturing sites, and the company anticipates being able to largely meet robust customer demand by early 2027. ABF film is a crucial material for high-performance semiconductor packages such as CPUs and GPUs, and it is indispensable for the increasing multi-layering and finer wiring required by advanced AI processors. Resolving the long-standing ABF substrate shortage, which has been a bottleneck for AI chip supply, heavily relies on stabilizing the supply of ABF film. Ajinomoto Fine-Techno's announcement marks a significant milestone in supporting the healthy growth of the entire AI industry.

Technical and Product Details

ABF film is an insulating film used during the formation of wiring layers in printed circuit boards, requiring the following characteristics:

- **High Heat Resistance:** Maintains stable quality even under high temperatures encountered during semiconductor manufacturing processes.
- **Low Dielectric Loss:** Minimizes signal loss during high-frequency signal transmission, enabling high-speed data communication.
- **Fine Processability:** Exhibits excellent processing characteristics for accurately forming sub-micron level fine wiring patterns.
- **Low Coefficient of Thermal Expansion:** Mitigates CTE mismatch between chips and substrates, preventing package warpage and cracks, thereby enhancing reliability.

In addition to increasing production of existing products, the company is also focusing on developing and expanding capacity for 'ultra-high-performance grade' ABF films, which meet the even higher performance demands of next-generation AI chips. However, for this specific grade, the technical difficulty is high, suggesting that supply may remain tight.

Background and Industry Context

Major semiconductor players like NVIDIA, AMD, and Intel are accelerating their AI chip development race, leading to an unprecedented demand for high-performance ABF substrates and their raw material, ABF film. The increasing complexity of AI chips, especially their integration with HBM (High Bandwidth Memory), requires more layers in ABF substrates and more advanced material properties. Consequently, the shortage of ABF film has directly impacted AI chip production schedules, making the actions of key suppliers like Ajinomoto Fine-Techno a focal point of industry attention.

Strategic Significance and Outlook

Ajinomoto Fine-Techno's capacity expansion is expected to significantly contribute to stabilizing the supply of AI chips towards early 2027. The company plans to continue monitoring market demand and making strategic capital investments to strengthen its position as a core supplier within the AI semiconductor ecosystem. Furthermore, it will focus on R&D to pursue even higher performance, supporting the future evolution of AI technology from a materials perspective.

Source: #

#11 Japan Introduces New Subsidy Program for Advanced Packaging R&D, Focusing on Heterogeneous Integration and 3D Stacking to Enhance Competitiveness

Published August 20, 2026 METI Press Release Japan

OVERVIEW

Japan's Ministry of Economy, Trade and Industry (METI) unveiled a new subsidy program to support R&D and mass production investment in advanced packaging technologies for strengthening the domestic semiconductor industry. The initiative prioritizes heterogeneous integration and 3D stacking to bolster the supply chain and establish Japan as a technology hub. This aims to attract domestic and international investment, revitalizing Japan's overall semiconductor ecosystem.

IN DEPTH

Key Findings

Japan's Ministry of Economy, Trade and Industry (METI) has announced the introduction of a new subsidy program specifically targeting advanced packaging technologies, aiming to restore Japan's international competitiveness and secure future growth in the semiconductor industry. This groundbreaking initiative is designed to strongly promote R&D in heterogeneous integration and 3D stacking technologies, as well as capital investment for their mass production. As semiconductor miniaturization approaches its physical limits, advanced packaging, which integrates chips with different functionalities into a single package, is becoming key to improving chip performance and reducing costs. The Japanese government aims to establish global leadership in this field, thereby strengthening Japan's strategic position in the semiconductor supply chain and enhancing national security.

Overview of the Subsidy Program and Key Technologies

The new subsidy program features the following characteristics:

- **Target Areas:** Heterogeneous integration technologies (e.g., chiplets, SiP, Co-Packaged Optics), 3D stacking technologies (e.g., HBM, TSV, hybrid bonding), and supporting materials, manufacturing equipment, and inspection systems.
- **Eligible Entities:** Domestic and international semiconductor-related companies, research institutions, and universities are eligible, with collaborative research and consortium formation encouraged.
- **Objective:** To support integrated development from basic research to practical application and mass production, accelerating technological innovation and establishing a robust domestic supply chain.
- **Investment Attraction:** The subsidies aim to attract domestic and international investment into advanced packaging, enhancing Japan's appeal as a technology hub.

METI particularly identifies the establishment of high-density, high-performance packaging technologies, essential for AI accelerators in data centers and next-generation HPC (High-Performance Computing) chips, as an urgent priority.

Background and Industry Context

With global competition for semiconductor dominance intensifying, countries like the U.S., South Korea, Europe, and China are increasing national investments in the semiconductor industry, with advanced packaging emerging as a 'new battleground.' While Japan's semiconductor industry once led the world, it has seen a decline in international competitiveness in recent years. However, Japan still holds a high share in semiconductor manufacturing equipment and materials. The current subsidy program reflects a strategy to leverage these strengths to re-emerge in advanced packaging. Strengthening the supply chain is also crucial from an economic security perspective.

Strategic Significance and Outlook

This subsidy program is poised to inject new vitality into Japan's semiconductor industry and foster international technological collaboration. By aligning with initiatives such as Rapidus, a domestic advanced logic foundry, Japan aims to build an integrated, cutting-edge semiconductor ecosystem from front-end to back-end. In the long term, this investment is expected to accelerate technological innovation in Japan and serve as a foundation for the development of next-generation technologies such as AI, IoT, and autonomous driving.

Source: #

#12 Applied Materials Unveils New Hybrid Bonding Platform for High-Volume 3D Stacked Chip Manufacturing, Enabling Ultra-Fine Pitch Integration

Published August 28, 2026 Business Wire USA

OVERVIEW

Applied Materials has launched a new hybrid bonding platform designed for high-volume manufacturing of next-generation 3D stacked chips. This innovative system achieves high-precision alignment and high throughput at ultra-fine pitches, significantly improving yield. Expected to resolve bottlenecks in AI/HPC chip production, it is a key technology accelerating the commercialization of 3D-ICs.

IN DEPTH

Key Findings

Applied Materials has unveiled a new hybrid bonding platform aimed at enabling the mass production of 3D stacked chips, which are essential for realizing next-generation high-performance semiconductors. This state-of-the-art system achieves ultra-fine pitch, high-precision alignment, and high throughput simultaneously in hybrid bonding—a technology that directly joins chips to chips or chips to wafers at a molecular level, surpassing conventional limitations. Hybrid bonding plays a decisive role in enhancing performance and power efficiency for AI (Artificial Intelligence) and HPC (High-Performance Computing) chips by significantly increasing connection density and shortening signal transmission distances compared to traditional micro-bump connections. This new platform from Applied Materials represents a major step towards the commercial mass production of a technology previously in R&D, marking a crucial breakthrough that will accelerate the adoption of 3D-ICs (3D Integrated Circuits).

Technical and Platform Details

The main features and technical advantages of the new platform include:

- **Ultra-Fine Pitch Capability:** Enables hybrid bonding at extremely fine connection pitches, below several microns, leading to higher density stacking.
- **High-Precision Alignment:** Advanced optical systems and control technologies achieve sub-micron level alignment accuracy for multiple chips, minimizing bonding defects.
- **High Throughput:** Integrates high-speed handling and bonding processes, optimizing productivity for mass production lines.
- **Process Integration and Yield Improvement:** Optimizes the entire process chain from pre-bonding treatment to bonding and final inspection, contributing to overall yield enhancement.
- **Flexible Compatibility:** Supports both die-to-wafer (D2W) and wafer-to-wafer (W2W) hybrid bonding methods.

This platform is expected to be applied across various advanced packaging applications, including next-generation HBM (High Bandwidth Memory) stacks, chiplet interconnections, and 3D-SoCs (System-on-Chips).

Background and Industry Context

As semiconductor miniaturization faces the limits of Moore's Law, chiplet technology and 3D stacking have emerged as new frontiers for improving semiconductor performance and cost efficiency. Hybrid bonding is a foundational technology for enabling these advancements, indispensable for resolving power consumption, heat generation, and data transmission speed challenges in AI chips. As a leading semiconductor equipment manufacturer, Applied Materials is playing a critical role in alleviating this bottleneck, thereby accelerating innovation across the entire industry.

Strategic Significance and Outlook

Applied Materials plans to deploy this new platform to major semiconductor manufacturers and OSATs (Outsourced Semiconductor Assembly and Test providers), actively supporting the mass production adoption of 3D stacked chips. Looking ahead, the company aims to apply this technology to more complex heterogeneous integration and next-generation technologies like optoelectronic convergence, continuing to lead the evolution of semiconductor packaging technology. This technology will serve as a fundamental pillar supporting data-centric future societies, including AI, HPC, 5G/6G communication, and autonomous driving.

Source: #

#13 KLA Unveils AI-Powered High-Speed, High-Precision Defect Inspection Solution to Boost Yield in Advanced Packages like CoWoS

Published August 27, 2026 SEMI Global USA

OVERVIEW

KLA has introduced a new AI-powered inspection system for high-speed, high-precision defect detection in high-density RDLs and 3D stacked structures. This solution supports yield management in advanced packaging processes, addressing inspection challenges in technologies like CoWoS. It aims to enhance the manufacturing reliability of next-generation AI/HPC chips, significantly impacting the industry's ability to scale production.

IN DEPTH

Key Findings

KLA Corporation has announced a new AI (Artificial Intelligence)-algorithm-equipped defect inspection solution that revolutionizes quality control in advanced semiconductor packaging processes. This new equipment is capable of detecting minute defects within high-density RDLs (redistribution layers) and complex 3D stacked structures with greater speed and precision than conventional inspection tools. As AI and HPC (High-Performance Computing) chip performance escalates, advanced packaging technologies like CoWoS (Chip-on-Wafer-on-Substrate) are becoming widespread. However, in these complex structures, subtle defects such as foreign particles, short/open circuits, via failures, and cracks directly impact yield. KLA's new inspection solution addresses these challenges by identifying and analyzing defects early in the manufacturing process, contributing to overall yield improvement and reduced production costs.

Technical and Solution Details

Key technical features of KLA's new inspection system include:

- **AI-Powered Pattern Recognition:** Proprietary AI algorithms automatically learn and differentiate normal from abnormal patterns in vast inspection data. This enables high-precision detection of subtle or new types of defects often missed by traditional rule-based inspections.
- **High-Speed Scanning and Data Processing:** Advanced optics and image processing technologies allow for rapid, comprehensive scanning of large substrates and wafers. Concurrently, an integrated AI processor provides real-time analysis of detected defect data, supporting swift decision-making.
- **3D Structural Defect Visualization:** Combined with 3D imaging techniques like computed tomography (CT), the system visualizes hidden defects within multi-layer structures and bonding imperfections between stacked chips.
- **Feedback for Process Control:** Detected defect data is fed back into the manufacturing process to optimize parameters and improve engineering, establishing a continuous yield improvement loop.

This solution proves particularly valuable for quality assurance in cutting-edge packaging technologies such as chiplet integration, HBM (High Bandwidth Memory) stacking, and hybrid bonding.

Background and Industry Context

The evolution of advanced packaging technologies has created a new competitive arena within the semiconductor industry, where stabilizing manufacturing yield is paramount. Technologies like CoWoS integrate multiple logic chips and HBM onto a silicon interposer, meaning that interconnect reliability, in addition to component quality, dictates overall yield. As a global leader in semiconductor inspection and metrology, KLA consistently provides solutions for the most advanced challenges. This announcement represents a move to redefine quality control in the era of AI chips.

Strategic Significance and Outlook

KLA plans to further evolve its AI-integrated inspection and metrology solutions to address increasingly complex advanced packaging challenges. Future goals include real-time inline quality control, predictive analytics, and fully automated inspection flows. This will enable semiconductor manufacturers to reduce AI/HPC chip production costs, shorten time-to-market, and strengthen the foundation for accelerating innovation in the AI era.

Source: #

#14 Onto Innovation Unveils High-Precision, High-Speed Metrology Solution to Accelerate Panel Level Packaging Mass Production

Published August 26, 2026 Photonics.com USA

OVERVIEW

Onto Innovation has announced a high-precision metrology solution designed to overcome mass production challenges in Panel Level Packaging (PLP). This new technology enables high-speed measurement of fine structures on large substrates, contributing to process control and yield optimization. It is expected to enhance PLP cost efficiency and accelerate its adoption for semiconductors in smartphones, wearables, and IoT devices.

IN DEPTH

Key Findings

Onto Innovation has unveiled a groundbreaking high-precision metrology solution poised to significantly advance the mass production of Panel Level Packaging (PLP), a highly anticipated next-generation semiconductor packaging technology. PLP offers the potential for substantial manufacturing cost reductions by simultaneously packaging numerous chips on larger panels compared to traditional wafer-level packaging (WLP). However, the increased panel size has historically presented challenges in process control. Onto Innovation's new technology aims to overcome these PLP manufacturing hurdles, particularly the difficulty in managing dimensional accuracy and detecting defects in fine structures on large substrates. This is expected to improve PLP yield and reliability, further enhancing cost efficiency and accelerating the widespread adoption of PLP for semiconductors in smartphones, wearable devices, and IoT devices across diverse applications.

Technical and Solution Details

The metrology solution announced by Onto Innovation boasts the following key technical features:

- **High-Speed Scanning for Large Panels:** Combines high-resolution imaging with high-speed stage control to rapidly scan the entire surface of large panels, up to 600mm x 600mm, enabling comprehensive data acquisition.
- **High-Precision Measurement of Fine Structures:** Provides highly accurate, non-contact measurement of sub-micron level fine wiring, bumps, vias, and RDLs (Redistribution Layers).
- **AI-Powered Defect Detection and Classification:** Incorporates machine learning algorithms to automatically identify and classify defect patterns from vast amounts of measurement data. This reduces false positives, improving inspection efficiency and accuracy.
- **Real-Time Feedback for Process Control:** Acquired measurement data is analyzed in real-time and immediately fed back into the manufacturing process for parameter adjustments and process improvements. This enables early detection of process drift and supports continuous yield optimization.

This solution is particularly effective in addressing common PLP challenges such as wafer warpage, pattern misalignment, and foreign material contamination.

Background and Industry Context

PLP is attracting significant attention as a promising approach for low-cost, high-volume production of advanced packaging technologies such as flip-chip, fan-out, and SiP (System-in-Package). Especially with the miniaturization and multi-functionality of mobile devices and IoT equipment, packaging cost efficiency directly impacts product competitiveness. However, achieving uniform process control on large substrates has been a significant technical challenge and a barrier to mass production until now. Onto Innovation's announcement reduces this barrier, paving the way for the widespread adoption of PLP.

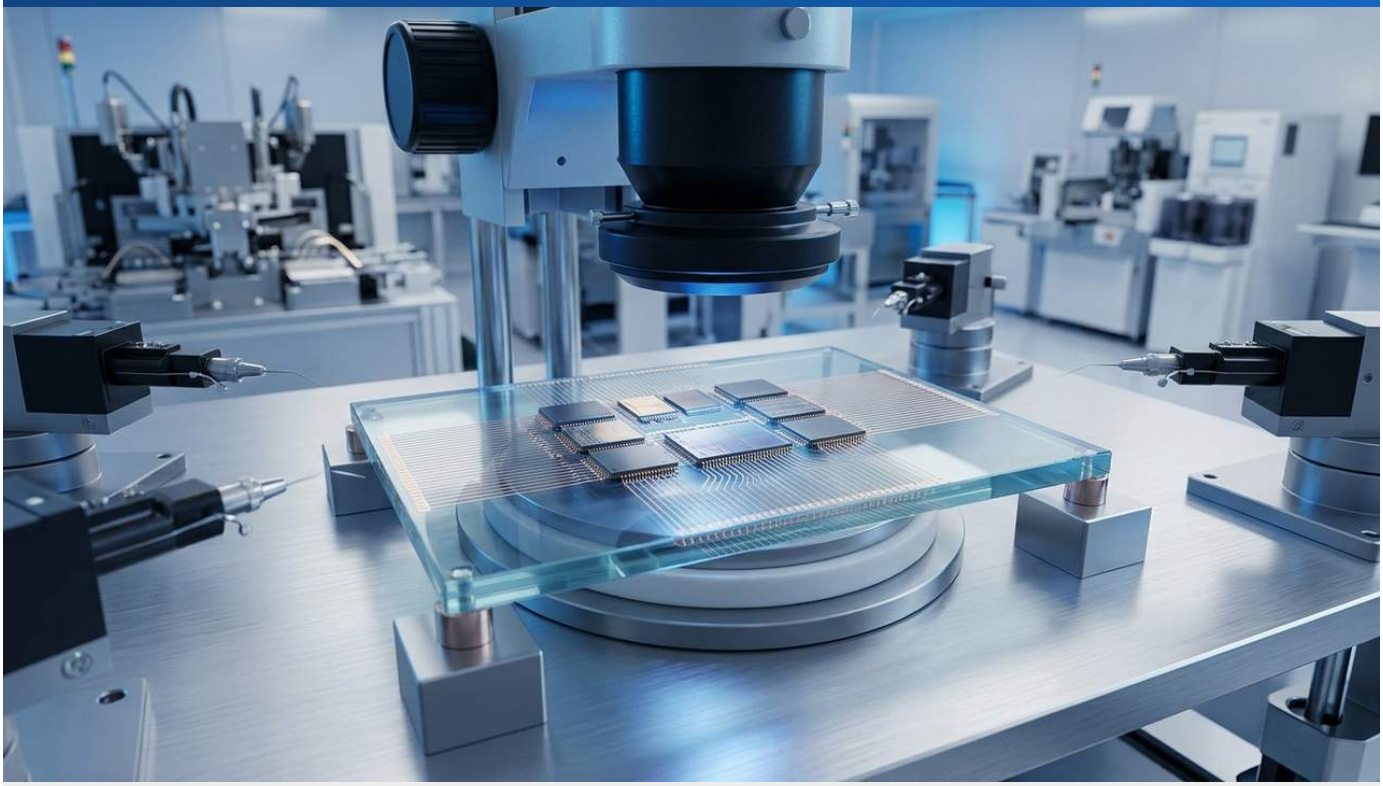
Strategic Significance and Outlook

As a leading company in PLP metrology technology, Onto Innovation plans to continue its technological innovation, adapting to more complex package structures and new materials. This solution will be an indispensable tool for semiconductor manufacturers and OSATs (Outsourced Semiconductor Assembly and Test providers) to enhance PLP competitiveness and create new market opportunities. In the long term, the proliferation of PLP is expected to enable both cost reduction and performance improvement in semiconductor devices, contributing to a society where high-performance semiconductors are utilized in an even broader range of applications.

Source: #

#15 imec Announces Breakthrough in 3D Stacked Packaging with Glass Substrates, Accelerating Commercialization for AI/HPC Applications

Published Published August 25, 2026　EETimes　ベルギー



OVERVIEW

imec, the renowned Belgian microelectronics research institute, has announced a significant breakthrough in 3D stacked packaging, leveraging glass substrates as interposers. This innovation is pivotal for next-generation AI/HPC applications, offering advantages like low dielectric loss, superior thermal stability, and fine processability over conventional materials. imec is actively collaborating with industry partners to accelerate the commercialization of this transformative technology, poised to redefine semiconductor integration.

IN DEPTH

Background: The Imperative for Advanced Packaging

As the semiconductor industry grapples with the slowing pace of Moore's Law, advanced packaging technology has emerged as a critical frontier for driving chip performance enhancements and cost efficiencies. High-performance interposers are indispensable for realizing the full potential of chiplet architectures and 3D-ICs, enabling heterogeneous integration and increased functional density. Among various contenders, glass substrates have rapidly gained prominence as a compelling candidate for these next-generation interposers. Their inherent material properties offer distinct advantages over traditional organic or silicon alternatives.

Global investments in glass substrate technology are escalating, with significant research and development efforts underway in regions such as the U.S. and South Korea. Against this backdrop, imec's latest breakthrough underscores Europe's strategic position and potential to lead in this pivotal technological race, promising to reshape the future of semiconductor integration for demanding applications like AI and High-Performance Computing (HPC).

A Major Step Forward in Glass-Based 3D Packaging

imec, the world-leading microelectronics research institute headquartered in Belgium, has unveiled a pivotal technological breakthrough in 3D stacked packaging utilizing glass substrates. This highly anticipated development is poised to significantly advance the creation of higher-performance and more power-efficient integrated circuits, particularly for Artificial Intelligence (AI) and High-Performance Computing (HPC) applications.

Glass substrates present several compelling advantages over incumbent organic or silicon interposers. Key benefits include superior intrinsic flatness, exceptionally low dielectric loss, high thermal stability, and an inherent suitability for fine-pitch processing. These attributes are critical for enabling ultra-high-density integration of diverse chiplets and High Bandwidth Memory (HBM), facilitating faster signal propagation, reducing parasitic capacitance, and ultimately lowering overall power consumption. imec's achievement represents a substantial stride towards the commercialization of this innovative technology, drawing significant interest across the semiconductor ecosystem.

Technical Innovations Enabling the Breakthrough

imec's significant advancements in 3D stacked packaging with glass substrates are underpinned by several critical technical innovations:

- **Ultra-Fine Through-Glass Via (TGV) Technology:** imec has successfully established precise control over sidewall etching and achieved high aspect ratios in the formation of Through-Glass Vias. This breakthrough overcomes previous manufacturing challenges, ensuring exceptionally high wiring density and superior electrical performance essential for high-speed data transfer.
- **Low-Warpage and High-Reliability Processing:** Novel processing techniques have been developed to effectively mitigate warpage during the handling and fabrication of large-format glass substrates. This control is crucial for enhancing manufacturing yield during subsequent chip stacking operations and significantly improving overall package reliability and longevity.
- **Advanced Heterogeneous Integration Capabilities:** imec has pioneered technologies for the efficient integration of a diverse array of chiplets—including logic, memory, and RF components—fabricated using disparate materials and processes, onto a single glass interposer. This capability is fundamental for constructing complex, high-performance System-in-Packages (SiPs).
- **Synergy with Electro-Optical Integration:** Beyond electrical interconnects, imec is also actively researching the fabrication of optical waveguides and components directly on glass substrates. This foresight anticipates the future integration of optical interconnects, paving the way for even higher bandwidth and lower power communication within advanced packages.

To accelerate the practical application of these technologies, imec is actively engaged in collaborative R&D efforts with a consortium of leading industry partners, including major semiconductor manufacturers and equipment suppliers.

Industry Impact and Future Outlook

imec's pioneering 3D stacked packaging technology, leveraging glass substrates, is projected to find critical applications within the next few years across high-demand sectors such as AI/HPC processors, high-performance network infrastructure, and advanced autonomous driving systems. The accelerated commercialization of this technology promises to dramatically enhance chip design flexibility, facilitating the development of increasingly complex and high-performance System-in-Package (SiP) solutions.

Looking ahead, imec is committed to the continuous development of this foundational technology, driving innovation across the broader semiconductor industry. By providing key enabling technologies, imec aims to support and shape the evolution of next-generation electronics, ensuring sustained advancements in performance, power efficiency, and functionality for the most challenging computing tasks.

Source: #

#16 Fraunhofer IZM Demonstrates High-Density Flexible Hybrid Substrate (FHS) Technology, Opening New Frontiers for Wearable and IoT Devices

Published August 24, 2026 Semiconductor Engineering Germany

OVERVIEW

Fraunhofer IZM has demonstrated Flexible Hybrid Substrate (FHS) technology, enabling high-density wiring. This innovative approach integrates diverse semiconductor chips and passive components onto a flexible substrate, achieving both miniaturization and high performance. Anticipated for advanced packaging in wearables and IoT devices, FHS brings new design freedom to next-generation electronics.

IN DEPTH

Key Findings

Germany's applied research institution, Fraunhofer IZM (Fraunhofer Institute for Reliability and Microintegration), has conducted the latest demonstration of its High-Density Flexible Hybrid Substrate (FHS) technology. This FHS technology opens new possibilities for next-generation compact and high-performance electronic products by achieving both excellent flexibility and high integration, which were difficult to realize with conventional rigid printed circuit boards. FHS enables the direct mounting of multiple semiconductor chips (e.g., ASICs, MCUs) and passive components (resistors, capacitors) onto a flexible, bendable, and twistable substrate, connecting them with high-density wiring. This technology is expected to significantly reduce footprint and enhance functionality in applications requiring miniaturization and flexible form factors, such as wearable devices, medical sensors, implants, and various IoT (Internet of Things) devices.

Technical and Development Details

Key features of the FHS technology demonstrated by Fraunhofer IZM include:

- **High-Density Wiring:** Applies fine line/space (L/S) technology to flexible substrates to create complex circuit patterns and numerous I/O connections.
- **Heterogeneous Integration:** Seamlessly integrates not only silicon-based semiconductor chips but also different types of components such as MEMS (Micro-Electro-Mechanical Systems) sensors, RF modules, and power management ICs on the same substrate.
- **Flexibility and Durability:** Utilizes thin, bendable polymer materials for the substrate, ensuring high durability against repeated bending and twisting. This enables use in dynamic environments, such as body-worn devices.
- **Thermal Management:** Integrates thermally conductive materials and structural designs that allow for efficient heat dissipation from high-heat components, despite the flexible nature of the material.
- **Miniaturization and Lightweighting:** Significantly improves the form factor of end products by making the entire package thinner, smaller, and lighter.

IZM emphasizes that this FHS technology enables applications across a wide range of fields, including medical, automotive, aerospace, and consumer electronics.

Background and Industry Context

The explosive growth of IoT devices and the evolution of wearables are further driving the miniaturization and performance enhancement of electronic products. Conventional rigid printed circuit boards and individual packaged components are increasingly struggling to meet these demands, creating a need for new packaging technologies that combine flexibility with integration. Flexible hybrid substrate technology addresses these market needs, and technological innovations by research institutions have a significant impact on product development across the industry.

Strategic Significance and Outlook

Fraunhofer IZM's FHS technology is expected to bridge the gap from prototype to mass production. Moving forward, the institution aims to deepen collaboration with material suppliers, manufacturing equipment manufacturers, and end-product manufacturers to achieve early practical application and market introduction of this technology. The widespread adoption of FHS will accelerate the emergence of smaller, more multifunctional, and body-conformable wearable devices, as well as smart sensors that can be deployed in various environments, bringing new value to our lives and industrial activities.

Source: #

#17 Austrian AT&S Accelerates IC Substrate Capacity Expansion for High-Performance Computing (HPC), Responding to Data Center Demand

Published Published August 23, 2026 Business Journal オーストリア

OVERVIEW

Austrian-based AT&S, a leading package substrate manufacturer, is significantly accelerating its IC substrate capacity expansion, primarily targeting high-performance computing (HPC) applications. This strategic investment aims to meet surging demand from data centers and AI servers while ensuring a stable supply for key customers. The company is also intensifying R&D into high-layer, high-density wiring substrates, solidifying its leadership in the critical HPC market.

IN DEPTH

Key Findings

AT&S, an Austrian-headquartered global package substrate manufacturer, has decided to significantly accelerate its IC substrate production capacity expansion to meet the rapidly expanding demand across the High-Performance Computing (HPC) market. This aggressive investment aims to secure a stable supply of high-functional IC substrates essential for AI (Artificial Intelligence) and data center server processors, thereby reinforcing AT&S's competitive edge in the HPC sector. For HPC applications, sophisticated semiconductor chips like CPUs, GPUs, and AI accelerators demand packaging substrates exhibiting exceptionally high electrical performance and reliability to process vast datasets at unparalleled speeds. AT&S's accelerated capacity expansion is meticulously designed to meet these cutting-edge requirements and is critical for fulfilling its supply commitments to major semiconductor manufacturers.

Technical and Product Details

The IC substrates at the core of AT&S's expanded production and technological advancements incorporate the following key features:

- **High Layer Count and High-Density Wiring:** Enabling fine-line/space wiring patterns within multi-layer substrates to accommodate the extensive I/O counts of high-performance chips.
- **Low Dielectric Loss Materials:** Utilizing specialized low-dielectric materials to minimize signal attenuation during high-speed, high-frequency signal transmission.
- **High Heat Dissipation Design:** Integrating highly thermally conductive materials and optimized structural designs for efficient heat dissipation, crucial for cooling high-power-density chips.
- **Warpage Suppression Technology:** Mitigating warpage in increasingly larger and multi-layered substrates, thereby enhancing yield during the critical packaging process.

These advanced technologies are indispensable for packaging AI accelerators leveraging High Bandwidth Memory (HBM) and next-generation CPUs built with chiplet architectures.

Background and Industry Context

The rapid evolution of Artificial Intelligence (AI) and the expansive growth of cloud computing are fueling significant investments in data center infrastructure, resulting in an explosive surge in demand for HPC IC substrates. Industry projections indicate that the HPC IC substrate market is poised for annual growth exceeding 10%, raising concerns about potential supply chain bottlenecks. Against this backdrop, aggressive capacity expansion by key suppliers like AT&S is paramount for sustaining the healthy growth of the entire semiconductor industry. Furthermore, AT&S's production increase from its European base strategically contributes to diversifying the global supply chain, which often exhibits a concentration in Asia.

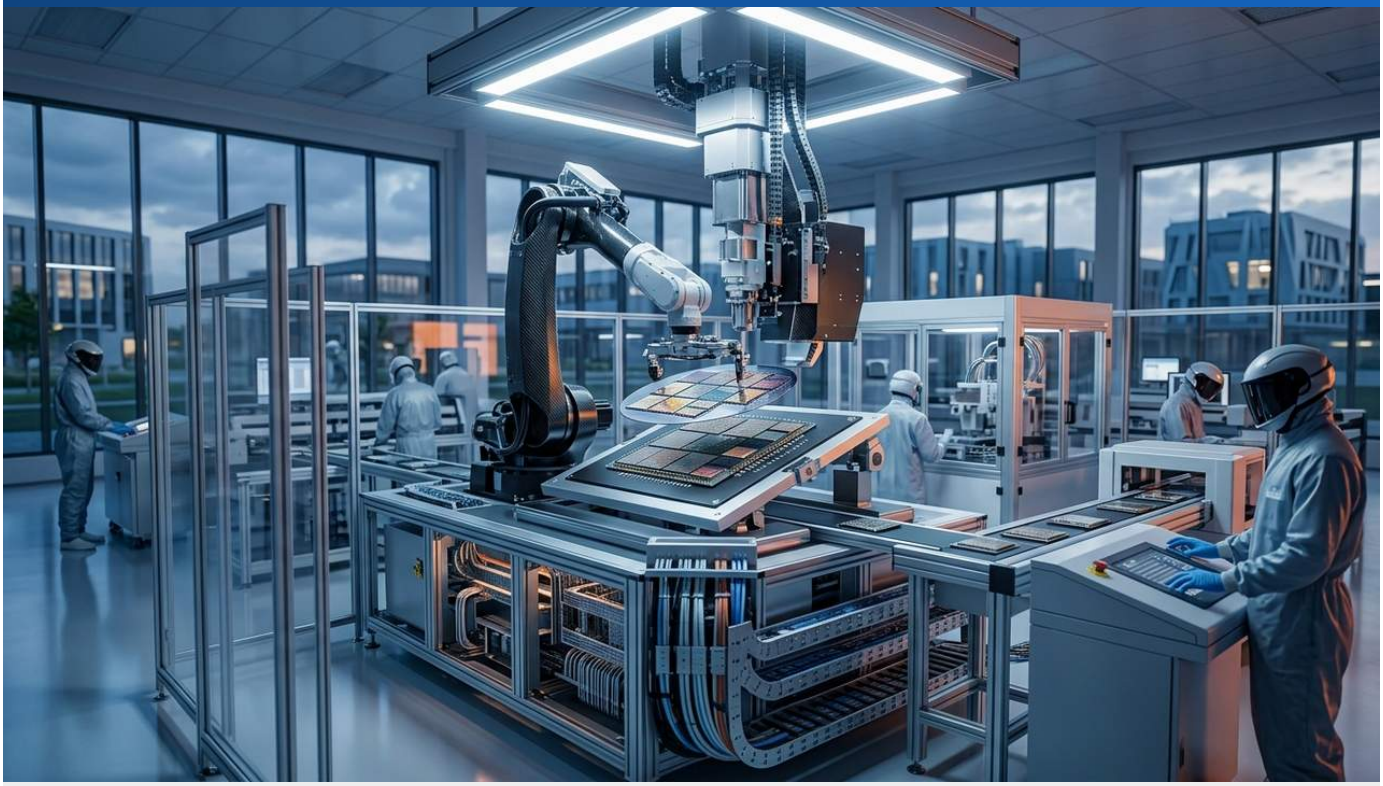
Strategic Significance and Outlook

AT&S intends to further solidify its leadership in the HPC market through sustained R&D and strategic capital investments. Looking ahead, the company aims to drive advancements in finer pitch interconnections, develop materials optimized for even higher frequencies, and introduce environmentally sustainable manufacturing processes, thereby delivering next-generation packaging solutions to the market. AT&S's accelerated strategy will be pivotal in supporting the ongoing technological evolution of semiconductors in the burgeoning AI era.

Source: #

#18 Infineon Strengthens Advanced Packaging Collaboration in Europe under EU Chips Act, Building Chiplet and Heterogeneous Integration Supply Chain

Published August 22, 2026 Reuters Germany



OVERVIEW

Infineon announced strengthened partnerships for advanced packaging technology development within Europe, leveraging the EU Chips Act. This strategy aims to build an indigenous supply chain for chiplet technology and heterogeneous integration, boosting semiconductor strategic autonomy. The initiative targets stable supply of high-performance chips for the automotive and industrial control sectors, enhancing European industrial competitiveness.

IN DEPTH

Key Findings

German semiconductor manufacturer Infineon Technologies has announced a significant strengthening of its partnerships for advanced packaging technology development within the European Union, under the framework of the EU Chips Act. This move represents a crucial step for Europe's semiconductor industry to establish strategic autonomy and enhance international competitiveness amidst the global restructuring of semiconductor supply chains. Infineon will specifically focus on chiplet technology and heterogeneous integration, deepening collaboration with research institutions, universities, and other companies within the EU. This enhanced cooperation aims to secure a stable supply of high-performance semiconductors required in key sectors such as automotive, industrial control, and power management, thereby reducing external dependencies.

Technical and Collaboration Details

Infineon's focus areas in advanced packaging technology include:

- **Chiplet Technology:** Combining small chips (chiplets) with different functionalities and integrating them into a single package. This contributes to design flexibility, cost efficiency, and performance improvement.
- **Heterogeneous Integration:** Integrating different types of semiconductors, such as logic, memory, sensors, and RF, into one package to achieve system miniaturization and enhanced functionality.
- **SiP (System-in-Package) Solutions:** Integrating multiple functional blocks into a single package to achieve system miniaturization, higher performance, and lower power consumption.
- **Advanced Interconnection Technologies:** Miniaturization technologies such as hybrid bonding, micro-bump connections, and RDL (Redististribution Layer).

These technological developments are closely linked to strengthening mass production capabilities at manufacturing sites within Europe, aiming to complete the entire value chain from R&D to production within the EU. Infineon will leverage its expertise in power semiconductors and automotive semiconductors into the advanced packaging sector.

Background and Industry Context

Rising geopolitical tensions and supply chain disruptions caused by the COVID-19 pandemic have prompted countries worldwide to encourage the repatriation or regionalization of semiconductor manufacturing capabilities. The EU Chips Act aims to double the EU's share of global semiconductor production to 20% by 2030, mobilizing over 43 billion euros (approximately 6.8 trillion JPY) in public and private investment. Infineon's announcement aligns with this large-scale strategy, aiming for semiconductor self-sufficiency, particularly in the automotive and industrial sectors where Europe has strong capabilities.

Strategic Significance and Outlook

Infineon's initiative will accelerate the development of an advanced packaging technology ecosystem in Europe, playing a critical role in enhancing the overall competitiveness of the region's semiconductor industry. In the future, this collaboration is expected to generate new innovations, further strengthening Europe's technological leadership in areas such as autonomous driving, renewable energy, and smart factories. Through these technologies, Infineon aims to contribute to the realization of a more sustainable and intelligent society.

Source: #

#19 STMicroelectronics Unveils Modular SiP Solution for Automotive AI Market, Driving Miniaturization and Performance in Autonomous Driving and ADAS

Published August 21, 2026 Electronics Weekly Switzerland/France

OVERVIEW

STMicroelectronics has launched a new modular System-in-Package (SiP) solution specifically designed for automotive AI applications. This solution integrates multiple chips to reduce footprint and boost performance. It addresses the demand for high-performance, space-efficient packaging driven by the proliferation of autonomous driving and advanced driver-assistance systems (ADAS), accelerating electronic system innovation in next-generation vehicles.

IN DEPTH

Key Findings

STMicroelectronics has announced a groundbreaking modular System-in-Package (SiP) solution for automotive AI applications, addressing the rapid evolution of autonomous driving and Advanced Driver-Assistance Systems (ADAS). This new solution significantly reduces system footprint and simultaneously enhances performance and power efficiency by highly integrating multiple diverse semiconductor chips—such as AI processors, microcontrollers, memory, and power management ICs—into a single, compact package. While high-performance chips are essential for automotive AI, which demands real-time processing of vast amounts of data, efficiently integrating them within the limited space of a vehicle has been a challenge. STMicroelectronics' modular SiP resolves this issue, contributing to the miniaturization and lightweighting of electronic control units (ECUs) and sensor modules in next-generation automobiles. This enables automotive manufacturers to incorporate more complex and high-performance AI functionalities into vehicles more flexibly and cost-effectively.

Technical and Solution Details

Key features of the modular SiP solution offered by STMicroelectronics include:

- **Heterogeneous Integration:** Integrates chips with different process technologies and functionalities (e.g., CMOS logic, BiCMOS RF, MEMS) within a single package.
- **Space-Saving Design:** Minimizes board area by densely arranging multiple chips vertically or horizontally. This facilitates easier integration into compact automotive sensor modules like ADAS cameras, radars, and LiDAR units.
- **Enhanced Performance and Lower Power Consumption:** Reduces signal transmission delays and power loss by shortening inter-chip wiring distances, improving overall system performance and power efficiency.
- **High Reliability:** Ensures high reliability, compliant with stringent automotive quality standards (e.g., AEC-Q100), to withstand harsh temperature changes, vibrations, and shocks.
- **Improved Development Efficiency:** Customers can save effort by avoiding individual component integration and focus on system-level validation, thereby reducing development time and costs.

This solution particularly accelerates the realization of decentralized AI architectures, where edge AI processing is completed within the vehicle.

Background and Industry Context

The automotive industry is undergoing a significant transformation driven by 'CASE' (Connected, Autonomous, Shared, Electric), with automotive semiconductors at its core. The advancement of autonomous driving levels and sophisticated infotainment systems are explosively driving demand for automotive AI chips, with the automotive semiconductor market projected to reach $100 billion by 2030. As a key supplier of automotive semiconductors, STMicroelectronics is focusing on packaging technology innovation to capitalize on this market growth.

Strategic Significance and Outlook

STMicroelectronics' modular SiP solution will strengthen the company's competitiveness in the automotive AI market and deepen partnerships with major automotive manufacturers. The company plans to continue advancing heterogeneous integration technologies, thermal management solutions, and security feature integration to keep pace with the evolution of automotive AI. This technology is expected to be an indispensable element in accelerating the adoption of autonomous vehicles and realizing a safer, more comfortable mobility society.

Source: #

#20 Glass Substrates in Advanced Packaging Accelerate from Prototype to Mass Production, Emerging as Key Technology for HBM and Chiplet Integration

Published August 28, 2026 Solid State Technology USA

OVERVIEW

Advanced packaging technology utilizing glass substrates is rapidly transitioning from R&D to mass production within the semiconductor industry. Glass substrates, superior to conventional organic substrates in flatness, thermal stability, and electrical properties, are highly promising for HBM and chiplet integration. Multiple IDMs and OSATs have reportedly initiated pilot production, contributing to enhanced performance for next-generation AI/HPC chips.

IN DEPTH

Key Findings

Within the semiconductor industry, the adoption of glass substrates for advanced packaging technology is rapidly accelerating its transition from the prototype stage to full-scale mass production. This swift shift is driven by the unique advantages of glass substrates, which are highly valued for enhancing the performance of semiconductors, particularly for AI (Artificial Intelligence) and High-Performance Computing (HPC) applications. Compared to traditional organic interposers, glass substrates boast superior flatness, high thermal stability, and low dielectric loss. These properties are critical for maintaining signal integrity and achieving efficient thermal management when integrating HBM (High Bandwidth Memory) stacks and multiple chiplets at extremely high densities. Industry sources indicate that several leading IDMs (Integrated Device Manufacturers) and OSATs (Outsourced Semiconductor Assembly and Test providers) have already commenced pilot production using glass substrates, with full market introduction envisioned from 2027 onwards.

Technical Advantages and Overcoming Mass Production Challenges

The primary technical advantages of glass substrates include:

- **Exceptional Flatness:** Significantly flatter surface compared to organic substrates, enabling high yield for hybrid bonding at ultra-fine pitches and stacking thin chips.
- **Superior Thermal Stability:** Coefficient of Thermal Expansion (CTE) is close to silicon, reducing thermal mismatch between chips and substrates. This prevents package warpage and connection reliability degradation due to thermal stress.
- **Low Dielectric Loss:** Excellent high-frequency signal transmission characteristics contribute to faster data transfer speeds and improved signal quality.
- **High-Density Through-Glass Vias (TGVs):** Allows for the formation of minute TGVs, enabling high-density wiring layers and 3D interconnections.

Previous mass production challenges included handling large glass substrates, achieving low-cost and high-yield TGV formation, and managing thermal stress between glass and chips. However, advancements in material technology, equipment technology, and process technology are overcoming these hurdles, making glass substrates a viable solution for practical use.

Background and Industry Context

As semiconductor performance improvements, traditionally achieved through miniaturization, approach physical limits and costs escalate, advanced packaging technologies like chiplets and 3D stacking have become primary drivers for performance enhancement and cost efficiency. Within this trend, glass substrates are positioned as an ideal platform, particularly for enabling ultra-high-density heterogeneous integration. Governments in the U.S., South Korea, and Japan are also increasing investments in this technology, making it a new focal point in the next-generation semiconductor competition.

Strategic Significance and Outlook

Advanced packaging using glass substrates is expected to be adopted in a wide range of applications, including AI, HPC, next-generation memory (HBM4 and beyond), and high-performance mobile processors. The acceleration of mass production will significantly increase chip design flexibility, enabling the realization of more complex and high-performance System-in-Package (SiP) solutions. Glass substrate technology is poised to drive the next wave of innovation in the semiconductor industry, increasing its presence significantly in the coming years as a foundational technology supporting the development of data-driven societies.

Source: #