Semiconductor_BackEnd

Weekly Intelligence Report

2026-09-06 | 21 articles | 7 countries

troy-technical.jp

This Week's Keyword

AI Packaging Bottleneck

HBM & Substrates now critical constraints

21	7	90%	$95B
articles	countries	surge	backlog
Analyzed this week	Source diversity	TSMC equipment orders	Dell AI server orders

All 21 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	TSMC CoWoS Capacity	Market Analysis	●●○○○	●●●●●	●●●●●	●●●●○	●●●●●	TSMC's CoWoS capacity surged 9X, yet 10% AI chip shortage persists, with NVIDIA securing 60% of output.
#02	Taiwan OSATs Boost AI	Corporate Strategy	●●○○○	●●●●●	●●●●○	●●●●○	●●●●●	Taiwanese OSATs plan $14.4B Capex, ASE deepens TSMC CoWoS collaboration to meet AI chip demand.
#03	Taiwan-Lithuania Pact	Collaboration	●●●○○	●●●○○	●●●○○	●●○○○	●●●●●	Taiwan and Lithuania ink €5.6M pact to develop advanced packaging machinery using laser and AI tech.
#04	TSMC Kaohsiung Cluster	Corporate Strategy	●●○○○	●●●●○	●●●●○	●●●○○	●●●●●	TSMC establishes an advanced packaging cluster in Kaohsiung, aiming for 25-50% efficiency gains with suppliers.
#05	Scientech Forecasts Growth	Corporate Forecast	●●○○○	●●●●○	●●●○○	●●●○○	●●●●○	Scientech forecasts 50% shipment growth driven by AI demand, targeting next-gen CoPoS market entry.
#06	Powertech Panel-Level Pkg	New Product	●●●●○	●●●○○	●●●●○	●●●○○	●●●●○	Powertech targets early 2027 for world's first mass production of AI server panel-level packaging (PLP).
#07	China's Top 3 OSATs	Corporate Strategy	●●○○○	●●●●○	●●●●○	●●●●○	●●●●●	China's top 3 OSATs invest over 15B Yuan into advanced packaging amid H1 profit surge driven by AI.
#08	Equip/Materials Market	Market Overview	●○○○○	●●●●●	●●●●●	●●●○○	●●●●●	Semiconductor equipment and materials market booming due to inference AI demand and expanded Chinese investment.
#09	Applied Materials HBM	New Product	●●●●○	●●●●○	●●●●○	●●●●○	●●●●●	Applied Materials launches new HBM & 3D packaging systems, acquires ASMPT NEXX to scale AI compute.
#10	HBM Primary Bottleneck	Market Analysis	●○○○○	●●●●●	●●●●●	●●●○○	●●●●●	AI supply chain maxed out; 40-week lead times become new norm as HBM emerges as primary bottleneck over TSMC CoWoS.
#11	Intel's EMIB-T Pkg	Corporate Strategy	●●●○○	●●●○○	●●●●○	●●●○○	●●●●●	Intel's EMIB-T advanced packaging projected for significant contribution by 2029, attracting Google's interest.
#12	KLA Adv Pkg Business	Corporate Forecast	●●○○○	●●●●○	●●●●○	●●●○○	●●●●●	KLA's advanced packaging business set for $1.1B revenue, 70%+ growth driven by AI demand and yield resolution.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#13	Glass Substrates Emerge	Research	●●●●○	●●○○○	●●●●○	●●●○○	●●●●○	Glass substrates emerge as key breakthrough for next-gen AI chip packaging; Intel, TSMC, Samsung accelerate development.
#14	Samsung/LG Substrates	Corporate Strategy	●●○○○	●●●●○	●●●●○	●●●●○	●●●●○	Samsung Electro-Mechanics & LG Innotek boost AI substrate capacity; H1 utilization nears 90% amid tight supply.
#15	High-End ABF Shortage	Market Analysis	●○○○○	●●●●○	●●●●○	●●●○○	●●●●○	High-end ABF substrate shortage intensifies due to massive AI chips, with Taiwanese makers facing fierce competition.
#16	TRUMPF Glass TGV	Academic Breakthrough	●●●●○	●●●○○	●●●●○	●●●●○	●●●●○	TRUMPF resolves glass substrate TGV coating bottleneck with HiPIMS, accelerating next-gen AI chip packaging.
#17	Simmtech AI Substrate	Corporate Strategy	●●○○○	●●●○○	●●●○○	●●●○○	●●●●○	Simmtech to invest 400B Won in next-gen AI server substrate production, with capacity expansion starting 2028.
#18	TSMC SVP 90% Surge	Corporate Statement	●○○○○	●●●●○	●●●●○	●●●●○	●●●●○	TSMC SVP reports 90% surge in equipment orders in six months driven by AI demand, equivalent to building 20 fabs.
#19	Dell Record Q2 Revenue	Corporate Statement	●○○○○	●●●●○	●●●●○	●●●●○	●●●●○	Dell reports record Q2 revenue of $47B with $95B AI server backlog; entire supply chain at 'redline'.
#20	Amkor/NVIDIA P'ship	Partnership	●●●○○	●●●●○	●●●●○	●●●●○	●●●●○	Amkor Technology and NVIDIA announce $1.5B advanced packaging partnership to accelerate AI multi-die integration.
#21	Unimicron 90% Surge	Corporate Statement	●○○○○	●●●●○	●●●●○	●●●●○	●●●●○	Unimicron reports 90% surge in equipment demand from AI; Japanese SME dependence creates ABF substrate bottleneck.

●●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low | Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI supply chain diversified enough to mitigate HBM and ABF substrate bottlenecks?

The AI supply chain is at 'redline' (Dell, #19), with HBM (NVIDIA, #10) and high-end ABF substrates (Unimicron, #21) now the primary bottlenecks. TSMC CoWoS capacity is still tight despite 9X expansion (#01). Evaluate your exposure to single-source dependencies and regional concentration.

❷ Are you investing in next-gen packaging materials like glass substrates, or risking obsolescence?

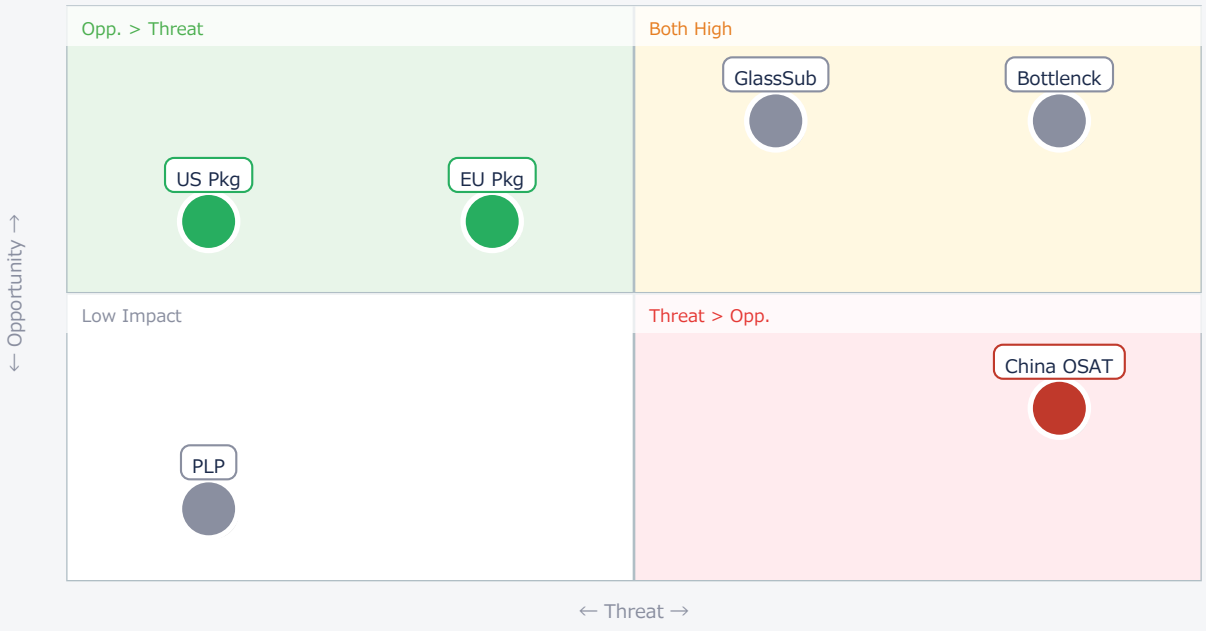
Glass substrates are emerging as a critical breakthrough for future AI packaging, with Intel, TSMC, and Samsung accelerating development (#13). TRUMPF's HiPIMS technology resolves a key manufacturing bottleneck for Through-Glass Vias (#16). Assess your R&D; and strategic partnerships in this area.

❸ How will China's aggressive OSAT expansion impact your market share and IP strategy?

China's top 3 OSATs are investing over 15 billion Yuan into advanced packaging, driven by H1 profit surges from AI demand (#07). This signals a strategic drive for self-sufficiency and enhanced competitiveness. Review your competitive landscape and intellectual property protection strategies.

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
Bottlenck	Critical	Alt. pkg/materials	Supply disruption
GlassSub	Critical	New material tech	Tech shift risk
US Pkg	Opp.	Domestic capacity	IP competition
EU Pkg	Opp.	EU tech access	Limited scale
China OSAT	Threat	New market	IP/market share
PLP	Ref.	Cost efficiency	Niche market

Deep Dive ① — TRUMPF Solves Glass Substrate TGV Bottleneck

#16 | 2026/09/03 | TRUMPF | Tech Novelty●●●●● Proximity●●●○○ Market Impact●●●●○ Data Reliability●●●●○ US/EU Relevance●●●●●

TRUMPF has introduced a High-Power Impulse Magnetron Sputtering (HiPIMS) approach that resolves a critical manufacturing challenge for next-gen AI chip packaging: reliably coating millions of minute Through-Glass Vias (TGVs) in glass substrates. This innovation enables uniform conductive coatings inside deep, narrow holes, accelerating the practical application of glass substrates.

Glass substrates offer superior mechanical strength, thermal stability, low dielectric loss, and a CTE close to silicon, enabling finer wiring and high-density TGVs for high-speed data transmission. TRUMPF's HiPIMS technology ensures high-quality conductive layer deposition, improving yields and performance stability for complex AI packages.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The published numbers are realistic, as TRUMPF is a leading equipment supplier with proven expertise. The technical barrier of uniform TGV coating was significant, and this solution is a genuine breakthrough. [Opportunity] for US/EU materials & component suppliers to partner with TRUMPF and integrate glass substrate solutions into their offerings, gaining a first-mover advantage in next-gen packaging. [Threat] for OEMs & device manufacturers who do not adapt to glass substrates, risking being left behind in AI chip performance. Next actions: [R&D;] Evaluate HiPIMS-enabled glass substrate samples immediately. [Procurement] Identify potential suppliers for HiPIMS-coated glass substrates by next quarter. [Strategy] Develop a roadmap for integrating glass substrates into future AI/HPC product designs within six months.

Deep Dive ② — Applied Materials Boosts HBM & 3D Packaging

#09 | 2026/09/04 | Exoswan Insights | Tech Novelty●●●●○ Proximity●●●●○ Market Impact●●●●○ Data Reliability●●●●○ US/EU Relevance●●●●●

Applied Materials has launched new CMP, ECD, deposition, and e-beam systems specifically for HBM and 3D packaging, and acquired ASMPT's NEXX business. This move capitalizes on escalating AI computing demand, with advanced packaging business growth forecast over 50% this year.

The new systems address intricate demands of HBM stacking, chiplet integration, and advanced interconnects, crucial for high-performance 3D packaging. The acquisition expands Applied Materials' portfolio in heterogeneous integration, leveraging its material science expertise to tackle thermal management, power delivery, and signal integrity challenges.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: Applied Materials' forecast of 50%+ growth is realistic given the AI boom and their strategic acquisitions. The technical barriers for HBM and 3D packaging are primarily yield and throughput, which these new systems aim to address. [Opportunity] for US/EU OEMs & device manufacturers to leverage these advanced tools for higher-performance, denser AI chips, potentially reducing time-to-market. [Threat] for smaller equipment suppliers who cannot match AMAT's comprehensive portfolio and R&D; investment. Next actions: [Procurement] Engage with Applied Materials to understand the capabilities and lead times of these new systems for your advanced packaging lines this month. [R&D;] Evaluate how these new systems can enhance your HBM and 3D packaging roadmaps, focusing on yield and performance improvements, within the next quarter. [Business Dev] Explore potential partnerships with AMAT for co-development on specific advanced packaging challenges.

Deep Dive ③ — HBM Emerges as Primary AI Bottleneck

#10 | 2026/09/03 | Markets Insider | Tech Novelty●○○○○ Proximity●●●●● Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●●

The AI supply chain faces severe constraints, with 40-week lead times becoming the new norm. High Bandwidth Memory (HBM) has replaced TSMC's CoWoS advanced packaging as the primary bottleneck, with NVIDIA's CFO forecasting demand to be roughly double supply.

HBM manufacturing demands sophisticated 3D packaging and stringent yield control, with limited qualified suppliers. While Samsung, SK hynix, and Micron are increasing investments, their pace lags demand. Other critical components like ABF substrates and T-glass also face shortages, indicating widespread scarcity across the AI supply chain.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The 40-week lead times and NVIDIA's demand forecast are highly realistic, reflecting the current 'redline' state of the AI supply chain. The technical barriers for HBM expansion are complex 3D stacking, TSV manufacturing, and yield management. [Opportunity] for US/EU materials & component suppliers to rapidly scale production of HBM-related materials (e.g., advanced bonding materials, inspection tools) and for technology licensors to offer alternative memory integration IP. [Threat] for OEMs & device manufacturers who rely on single HBM suppliers, facing significant production delays and competitive disadvantage. Next actions: [Procurement] Conduct an immediate audit of HBM and ABF substrate supply contracts and explore alternative suppliers/technologies this week. [Strategy] Develop a multi-year HBM supply diversification plan, including potential domestic production incentives, within one month. [R&D;] Accelerate research into alternative high-bandwidth memory solutions or packaging architectures that reduce reliance on HBM.

Other Notable Articles

#07 China's Top 3 OSATs (JCET, Tongfu, Huatian) Pour Over 15 Billion Yuan into Advanced Packaging Amid H1 Profit Surge Driven by AI (Digital Today (SCMP引用))
Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●●

China's aggressive investment in advanced packaging signals a push for self-sufficiency and increased global competition.

#03 Taiwan and Lithuania Ink €5.6M Tech Pact to Develop Advanced Packaging Machinery for Next-Gen Chips (Taiwan News)
Tech Novelty●●●○○ Proximity●●●○○ Market Impact●●●○○

This EU-Taiwan collaboration could yield novel advanced packaging machinery, diversifying the equipment supply chain.

#06 Powertech Targets Early 2027 for World's First Mass Production of AI Server Panel-Level Packaging (トナリズム)
Tech Novelty●●●●○ Proximity●●●○○ Market Impact●●●●○

Panel-level packaging offers significant cost and throughput advantages for large AI processors; monitor its commercialization.

#11 Intel's EMIB-T Advanced Packaging Projected for Significant Contribution by 2029 as CoWoS Constraints Drive Google's Interest (TrendForce)
Tech Novelty●●●○○ Proximity●●●○○ Market Impact●●●●○

Intel's EMIB-T offers a viable alternative to CoWoS, providing supply diversification for AI/HPC chip designers.

#15 High-End ABF Substrate Shortage Intensifies Due to Massive AI Chips: Taiwanese Makers & Equipment Suppliers Face Fierce Competition (Medium (by Julien Nauy))

Tech Novelty●○○○○ Proximity●●●●● Market Impact●●●●●

The severe ABF substrate shortage, driven by complex AI chip requirements, demands immediate supply chain risk mitigation.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Conduct an emergency audit of HBM, ABF substrate, and CoWoS capacity allocations and lead times for all critical AI projects.
- [Strategy] Initiate a task force to assess geopolitical risks associated with semiconductor supply chain concentration in Taiwan and China.

Short-term (1 month)

- [R&D;] Begin preliminary evaluation of glass substrate technology and TRUMPF's HiPIMS solution for future packaging roadmaps.
- [Business Dev] Explore partnerships with US/EU advanced packaging equipment suppliers (e.g., Applied Materials, KLA) to secure capacity and co-develop solutions.

Medium-long term (quarter+)

- [Executive] Develop a comprehensive supply chain diversification strategy, including potential investments in domestic or allied-nation advanced packaging capabilities.
- [Legal/IP] Review intellectual property strategies to protect advanced packaging innovations and monitor competitive IP developments, especially from Chinese OSATs.

Semiconductor_BackEnd — Selected Articles

Date: 2026-09-06

Articles: 21

Table of Contents

#19 Simmtech to Invest 400 Billion Won in Next-Gen AI Server Substrate Production: Capacity Expansion Starts 2028

#20 TSMC SVP Reports 90% Surge in Equipment Orders in Six Months Driven by AI Demand: Equivalent to Building 20 Fabs Globally Simultaneously

#21 Dell Reports Record Q2 Revenue of $47 Billion with $95 Billion AI Server Backlog; Entire Supply Chain, Including DRAM, HBM, ABF Substrates, at 'Redline'

#22 Amkor Technology and NVIDIA Announce $1.5 Billion Advanced Packaging Partnership to Accelerate AI Multi-Die Integration

#23 Unimicron Reports 90% Surge in Equipment Demand from AI, Japanese SME Dependence on ABF Substrates Creates Bottleneck

#01 TSMC CoWoS Capacity Expands 9X in 3 Years, Yet 10% AI Chip Shortage Persists with NVIDIA Securing 60%

Published August 31, 2026 XenoSpectrum Taiwan

OVERVIEW

TSMC's CoWoS advanced packaging capacity has surged nine-fold over three years, but a 10% supply shortage for AI chips remains due to soaring demand. NVIDIA currently secures approximately 60% of TSMC's CoWoS output for 2026, leaving limited capacity for other major AI chip developers. TSMC plans a further 60%+ capacity expansion by 2027 and aims for 2028-2029 mass production of next-gen CoPoS packaging in Taiwan and Arizona to alleviate future bottlenecks.

IN DEPTH

Key Findings: TSMC's CoWoS Capacity Growth and Persistent AI Chip Shortage

Despite a remarkable nine-fold increase in TSMC's monthly CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity over the past three years, a significant 10% supply shortage for AI chips continues. This persistent deficit highlights that the exponential growth in AI demand is outstripping even aggressive manufacturing capacity expansions, posing a critical challenge for high-performance AI accelerator development and deployment globally.

Technical & Market Details: NVIDIA's Dominance and Next-Gen CoPoS Investments

By the end of 2026, TSMC targets a monthly CoWoS production capacity of 120,000 to 140,000 wafers. However, a substantial portion of this capacity is already committed to key customers, with NVIDIA securing an estimated 60% of TSMC's CoWoS output for 2026. This allocation solidifies NVIDIA's dominant position in the AI hardware market but leaves a competitive landscape for the remaining 40% among other leading AI chip designers such as AMD, Broadcom, and Google. The scarcity of CoWoS capacity, particularly in complex processes like Chip-on-Wafer (CoW) attachment and the manufacturing of silicon interposers with Through-Silicon Vias (TSVs), multi-layer Redistribution Layers (RDLs), and SoIC (System-on-Integrated-Chips) hybrid bonding, remains a critical bottleneck impacting production yields and throughput. These highly precise integration steps are key determinants of the overall supply chain's efficiency and ability to scale.

Background & Industry Context: Geographical Concentration and Future Strategy

This situation underscores the inherent risks associated with the geographical concentration of AI hardware production in Taiwan. Experts project this concentration risk to persist until at least 2028-2029, raising concerns about geopolitical vulnerabilities and supply chain resilience. To mitigate these bottlenecks and address future demand, TSMC is aggressively investing in further expansion. The company plans to boost CoWoS capacity by over 60% by 2027. Furthermore, TSMC initiated an R&D line for the next-generation CoPoS (Chip-on-Panel-on-Substrate) advanced packaging technology in 2025, with mass production slated to commence between 2028 and 2029 at its facilities in Chiayi, Taiwan, and Phoenix, Arizona. These strategic investments aim to stabilize the future supply of AI chips and maintain TSMC's technological leadership in advanced packaging.

Strategic Significance & Outlook: Impact on AI Industry and TSMC's Pivotal Role

TSMC's CoWoS capacity expansion is a pivotal factor influencing the global growth trajectory of the AI industry. Resolving these supply shortages would enable the release of a greater volume of AI chips into the market, accelerating the adoption and advancement of AI technologies across various sectors. The current constrained environment, however, highlights the fragility of the broader AI semiconductor supply chain. This vulnerability is prompting governments and corporations worldwide to explore diversification strategies and bolster domestic production capabilities. Through its proactive investments in cutting-edge packaging technologies, TSMC is poised to address these challenges head-on, continuing to play a central role in driving AI-driven technological innovation and shaping the future of high-performance computing.

Source: https://xenospectrum.com/en/cowos-packaging-bottleneck-nvidia/

Collected: September 04, 2026 | Automated Research System (Gemini API)

#02 Taiwan's OSATs Boost AI Capacity with $14.4B Capex; ASE Deepens TSMC CoWoS Collaboration to Meet Soaring Demand

Published September 03, 2026 Domino Theory Taiwan

OVERVIEW

Five leading Taiwanese chip packaging and test companies plan a record $14.4 billion (NT$460 billion) in capital expenditures this year to meet surging AI chip demand, matching TSMC's own advanced packaging investments. ASE Technology, the world's largest OSAT, is intensifying collaboration with TSMC to outsource portions of its advanced packaging processes, specifically to alleviate CoWoS supply bottlenecks. With NVIDIA securing over half of TSMC's CoWoS capacity, other major chip designers like Broadcom and AMD are increasingly relying on OSATs for high-end packaging, fueling a widespread equipment supply boom across Taiwan's ecosystem.

IN DEPTH

Key Findings: Taiwanese OSATs Plan $14.4 Billion Capex to Address AI Boom

Taiwan's five leading chip packaging and testing companies are set to invest a monumental NT$460 billion (approximately $14.4 billion USD) in capital expenditures this year. This record investment, which mirrors TSMC's own spending in advanced packaging, underscores the critical role of Taiwan's back-end semiconductor industry in addressing the surging global demand for AI chips.

Technical & Market Details: ASE's Strategy and Shifting Supply Dynamics

ASE Technology, the world's largest Outsourced Semiconductor Assembly and Test (OSAT) provider, is at the forefront of this expansion. Facing extreme tightness in TSMC's CoWoS packaging capacity—a crucial technology for AI accelerators—ASE is strengthening its collaboration with TSMC. This involves ASE taking on parts of the advanced packaging process, effectively offloading some of TSMC's workload and helping alleviate critical bottlenecks. ASE itself announced a record $8.5 billion in capital expenditures for 2026, driven by the escalating AI demand.

This dynamic reflects a significant shift in the market structure for AI chip design. With NVIDIA reportedly securing over half of TSMC's CoWoS capacity, other major AI chip developers such as Broadcom, AMD, and Google are increasingly turning to OSAT firms for advanced 2.5D/3D packaging solutions. Consequently, Taiwanese advanced packaging equipment suppliers, including companies like C Sun, are reporting a substantial increase in orders from OSATs, signaling a robust investment cycle across the entire supply chain.

Background & Industry Context: Strengthening Taiwan's Ecosystem Competitiveness

Taiwan has long been a global leader in semiconductor manufacturing and back-end services. The massive capital injection further cements its strategic importance in the era of AI semiconductors. Advanced packaging technologies are indispensable for realizing high-performance AI chips, serving as the key to efficiently integrating logic dies, High Bandwidth Memory (HBM), and other critical components. Taiwanese OSAT companies are at the forefront of this technological evolution, playing a vital role in enhancing AI chip performance and power efficiency.

Strategic Significance & Outlook: Taiwan's Role in Sustaining AI Industry Growth

These aggressive investments by the Taiwanese OSAT ecosystem are poised to significantly bolster the sustained growth of the global AI industry. As AI chip supply bottlenecks ease, the accelerated development and deployment of AI applications across a broader range of sectors are expected. Taiwan's robust division of labor, with TSMC handling cutting-edge wafer fabrication and OSATs managing advanced packaging and testing, ensures its continued central role in the semiconductor supply chain through the AI era. This collaborative model is becoming increasingly crucial for meeting the complex technological and market demands of advanced computing.

Source: https://dominotheory.com/taiwanese-packaging-ecosystem-adjusts-to-ai-boom/

Collected: September 04, 2026 | Automated Research System (Gemini API)

#03 Taiwan and Lithuania Ink €5.6M Tech Pact to Develop Advanced Packaging Machinery for Next-Gen Chips

Published September 04, 2026 Taiwan News Taiwan

OVERVIEW

Taiwan and Lithuania have signed an MOU to jointly develop advanced packaging machinery for next-generation chips, committing €5.6 million (approx. $6.5 million USD) over two years in a public-private partnership. The collaboration will integrate Lithuania's advanced laser technology with Taiwan's expertise in digital imaging, AI control, and high-precision scanning modules to foster private sector cooperation. This initiative aims to assist Taiwanese equipment manufacturers in expanding into advanced packaging applications, with projections of generating over NT$300 million in industrial benefits.

IN DEPTH

Key Findings: Taiwan and Lithuania Forge Strategic Alliance for Advanced Chip Packaging Machinery

Taiwan and Lithuania have officially entered into a significant Memorandum of Understanding (MOU) to jointly develop advanced packaging machinery for next-generation semiconductors. This two-year, public-private partnership will see both governments co-investing a total of €5.6 million (approximately $6.5 million USD) to spur technological collaboration between their private sectors. This strategic alliance aims to diversify the global semiconductor supply chain and accelerate innovation in cutting-edge semiconductor manufacturing.

Technical Details: Integrating Laser Technology with AI for Precision Manufacturing

The core of this partnership lies in combining Lithuania's globally recognized high-power laser technology with Taiwan's strengths in digital laser imaging, AI-controlled systems, and high-precision scanning modules. This technological fusion is expected to drive the development of highly precise machinery essential for advanced packaging processes. Specifically, it targets new manufacturing solutions for wafer-level packaging, 3D stacking, and chiplet integration, enabling denser and higher-performance semiconductor devices. This innovation holds the potential to significantly enhance manufacturing accuracy and efficiency, particularly for AI accelerators and High-Performance Computing (HPC) semiconductors.

Background & Industry Context: Supply Chain Resilience and Economic Impact

The signing of this MOU carries substantial significance amidst global semiconductor supply chain disruptions and heightened geopolitical risks. Taiwan stands as a global hub for semiconductor manufacturing, while Lithuania is a European leader in laser technology. By synergizing their respective strengths, the collaboration is anticipated to create new options within the semiconductor equipment market, contributing to a more resilient and diversified supply chain. Economically, this cooperation is projected to help Taiwanese equipment manufacturers expand into advanced packaging application markets, generating over NT$300 million (approximately $9.3 million USD) in industrial benefits. This will strengthen economic ties and elevate the technological prowess of both nations.

Strategic Significance & Outlook: International Cooperation Driving Innovation

The Taiwan-Lithuania technical cooperation will be concretely advanced through international technical seminars, academic and industrial exchanges, and technology matching programs. Such close collaboration can contribute to the standardization of future advanced packaging technologies and create ripple effects across the broader semiconductor industry. The development of next-generation technologies like AI, IoT, and autonomous driving critically depends on high-performance and efficient semiconductor packaging. This partnership marks a crucial step in strengthening those foundational technologies. Both nations are set to jointly drive innovation within the global semiconductor ecosystem through this promising collaboration.

Source: https://www.taiwannews.com.tw/news/6433926

Collected: September 04, 2026 | Automated Research System (Gemini API)

#04 TSMC Establishes Kaohsiung Advanced Packaging Cluster, Aims for Up to 50% Efficiency Gains

Published September 02, 2026 digitimes Taiwan

OVERVIEW

TSMC announced the establishment of an advanced packaging materials and equipment supply chain cluster in Kaohsiung's Baipu Industrial Park, Taiwan. This strategic move aims to enhance efficiency in advanced packaging processes by 25% to 50% through a collaborative verification platform with suppliers. The new cluster will bolster production capacity and optimize the entire supply chain to meet the escalating demand for AI chips.

IN DEPTH

Key Findings: TSMC to Boost Advanced Packaging Efficiency by Up to 50% with New Kaohsiung Cluster

TSMC has announced its expansion into Kaohsiung's Baipu Industrial Park in southern Taiwan, where it will establish the island's first advanced packaging materials and equipment supply chain cluster. This strategic initiative is designed to dramatically improve efficiency in advanced packaging processes by 25% to 50% through the creation of a collaborative verification platform with its key suppliers. This move is expected to significantly contribute to bolstering semiconductor production capacity for the AI era.

Technical & Market Details: Enhancing Supplier Collaboration and Production Optimization

The cluster's primary objective is to intensify collaboration between TSMC and its critical suppliers by co-locating them within the same industrial park. This proximity will accelerate the development cycle of new technologies and expedite problem-solving during manufacturing, from R&D to mass production. For complex advanced packaging technologies like CoWoS and SoIC, a vertically integrated approach, where material suppliers, equipment manufacturers, and TSMC collaborate seamlessly, is essential for maintaining high yields and throughput. Centralized management of material supply, equipment calibration, and process optimization is expected to reduce overall supply chain risks and significantly shorten time-to-market for advanced chip solutions.

Background & Industry Context: Responding to AI Demand and Geopolitical Risks

Amidst a global surge in demand for AI, High-Performance Computing (HPC), and high-speed communication technologies, advanced packaging has become a crucial enabler for enhancing semiconductor performance and power efficiency. However, the intricate manufacturing processes involved in advanced packaging, such as CoWoS, also carry risks associated with concentration in specific suppliers. TSMC's establishment of this cluster aims to mitigate these risks, bolster supply chain resilience, and alleviate the existing bottlenecks in AI chip supply. Kaohsiung has long been one of TSMC's significant manufacturing hubs, and this new investment further solidifies the region's position as a critical center for advanced semiconductor fabrication.

Strategic Significance & Outlook: Strengthening Taiwan's Semiconductor Ecosystem and Global Competitiveness

The formation of the cluster in Baipu Industrial Park is poised to strengthen Taiwan's entire semiconductor ecosystem, enhancing its global competitiveness. The target of up to 50% efficiency improvement promises not only cost reductions but also a dramatic acceleration in product delivery to market. This is a strategic move for TSMC to maintain its technological leadership and respond rapidly to the demands of its key customers in the fast-evolving AI market. The innovations emerging from this cluster are expected to have a profound impact on the global semiconductor industry, driving the development of next-generation technologies.

Source: https://www.digitimes.com/news/a20260902PD233/tsmc-packaging-equipment-kaohsiung-materials.html

#05 Scientech Forecasts 50% Shipment Growth Driven by AI Demand, Targets Next-Gen CoPoS Market Entry

Published September 03, 2026 Taipei Times Taiwan

OVERVIEW

Scientech, a Taiwanese supplier of advanced packaging equipment and reclaimed wafers, anticipates a 50% year-over-year increase in shipments this year, fueled by robust AI application demand and rapid technological shifts. The company's production lines are projected to operate at full capacity through year-end, with sustained growth expected into next year. This optimistic outlook is underpinned by TSMC's forecast of an 80% surge in CoWoS packaging capacity from 2022 to 2027, and Scientech is actively pursuing entry into the next-generation CoPoS packaging supply chain.

IN DEPTH

Key Findings: Scientech Projects 50% Shipment Growth from AI Boom, Eyes CoPoS Market

Scientech, a leading Taiwanese supplier of advanced packaging equipment and reclaimed wafers, has announced a projected 50% year-over-year increase in shipments for the current year. This significant growth is primarily driven by the insatiable demand from AI applications and rapid technological advancements in the semiconductor sector. The company anticipates its production lines will run at full capacity through the end of the year, with this growth momentum expected to continue into the next fiscal year.

Technical & Market Details: Contributing to CoWoS Expansion and Strategic Move to CoPoS

Scientech's optimistic forecast is rooted in TSMC's projection that its CoWoS (Chip-on-Wafer-on-Substrate) advanced packaging capacity will surge by 80% between 2022 and 2027. CoWoS is a pivotal technology for AI accelerators, and its production expansion presents substantial business opportunities for related equipment and material suppliers. Scientech plays a crucial role in this supply chain by providing essential precision equipment for CoWoS manufacturing and supplying reclaimed wafers. These reclaimed wafers, which are reprocessed test wafers, contribute significantly to cost reduction and environmental sustainability, supporting efficient production ecosystems.

Furthermore, Scientech is actively pursuing entry into the supply chain for the next-generation CoPoS (Chip-on-Panel-on-Substrate) packaging technology. CoPoS holds the potential to accommodate larger substrate sizes and integrate an even greater number of chiplets, making it a critical technology for future ultra-high-performance AI chips and HPC semiconductors. The technological evolution from CoWoS to CoPoS introduces new demands for packaging equipment and materials, prompting companies like Scientech to accelerate their R&D and capital investments.

Background & Industry Context: Equipment Manufacturers' Vital Role in the AI Semiconductor Ecosystem

The current AI boom is fueling unprecedented growth across the semiconductor industry, with advanced packaging identified as a key bottleneck. High-performance AI chips heavily rely on complex 2.5D/3D integrated packaging, necessitating a consistent supply of precise equipment and high-quality materials. Specialized companies like Scientech are playing a decisive role in expanding advanced packaging capacity, and their growth serves as a barometer for the overall health of the AI semiconductor ecosystem.

Strategic Significance & Outlook: Continuous Innovation and Market Expansion

Scientech's strong shipment projections and proactive push into CoPoS underscore the sustained expansion of the AI semiconductor market and the high appetite for investment in advanced packaging technologies. Through continuous innovation and capacity enhancements, the company is poised to solidify its position as a critical enabler for next-generation AI chips. As AI technology evolves, the market for advanced packaging equipment and related materials is expected to maintain robust growth, with adaptability to new technologies like CoWoS and CoPoS becoming a key determinant of competitive advantage.

Source: https://www.taipeitimes.com/News/biz/archives/2026/09/04/2003863637

#06 Powertech Targets Early 2027 for World's First Mass Production of AI Server Panel-Level Packaging

Published Published September 01, 2026　トナリズム　Taiwan

OVERVIEW

Powertech Technology, a leading Taiwanese OSAT, has unveiled plans to commence mass production of panel-level packaging (PLP) for AI semiconductors and server CPUs by early 2027. This initiative establishes the world's first high-volume PLP facility dedicated to AI chips, strategically addressing the escalating demand for advanced AI processors by offering greater substrate area, enhanced cost efficiencies, and superior performance compared to traditional wafer-level packaging.

IN DEPTH

Background & Context

The relentless expansion of AI applications has fueled an unprecedented demand for high-performance, efficiently manufactured AI semiconductors. Advanced packaging technologies like Panel-Level Packaging (PLP) are now indispensable for overcoming the physical and electrical limitations of traditional methods, enabling greater integration density, reduced latency, and improved power efficiency. With AI accelerators requiring massive data processing capabilities, sophisticated high-density packaging capable of accommodating chiplets and High Bandwidth Memory (HBM) stacks is paramount. Powertech's investment represents a strategic response to this critical market imperative, reinforcing Taiwan's leading position in the global semiconductor ecosystem and mitigating potential supply chain bottlenecks for critical AI components, a challenge recently observed in CoWoS packaging capacity.

Key Announcements

Powertech Technology (PTI), a prominent Taiwanese Outsourced Semiconductor Assembly and Test (OSAT) provider, has announced its strategic plan to commence mass production of panel-level packaging (PLP) services for artificial intelligence (AI) semiconductors and server CPUs by early 2027. This initiative marks a significant milestone, as the facility is anticipated to be the world's first large-scale PLP operation specifically dedicated to AI chip manufacturing, directly addressing the critical demand for advanced packaging solutions in the booming AI sector.

Technical Deep Dive into Panel-Level Packaging (PLP)

Panel-level packaging (PLP) represents a next-generation approach to semiconductor packaging, distinguishing itself from traditional wafer-level packaging (WLP) by utilizing large, rectangular panels instead of smaller, circular silicon wafers. This methodology allows for a substantially increased number of chips to be processed simultaneously, leading to significant enhancements in production throughput and cost efficiency, particularly beneficial for large-die AI processors and High-Performance Computing (HPC) semiconductors. PTI's adoption of PLP technology is poised to deliver high-density, high-performance packaging solutions, which are crucial for advanced AI chips that frequently integrate High Bandwidth Memory (HBM) and complex 2.5D/3D architectures. The larger panel size, potentially up to 600mm x 600mm, facilitates a higher package-per-panel ratio, drastically improving overall processing economics compared to conventional 300mm wafer-based methods.

Strategic Significance & Outlook

The commencement of PLP mass production by Powertech is expected to significantly expand the global supply capacity for AI semiconductors, thereby accelerating the development and deployment of AI technologies across diverse industries. Furthermore, PTI's pioneering initiative could catalyze broader industry adoption of PLP, encouraging other OSAT providers and foundries to invest in similar advanced packaging capabilities. This trend is likely to lead to a reduction in per-chip costs for AI processors and facilitate their integration into a wider array of applications, spanning from edge devices to hyperscale data centers. Powertech is strategically positioned to remain a pivotal player in driving the growth of the AI semiconductor market, with its advancements closely monitored by industry stakeholders, potentially establishing a new benchmark for advanced packaging efficiency and scalability.

Source: https://tonarism.co.jp/media/media_detail.php?b_id=261

Collected: September 04, 2026 | Automated Research System (Gemini API)

#07 China's Top 3 OSATs (JCET, Tongfu, Huatian) Pour Over 15 Billion Yuan into Advanced Packaging Amid H1 Profit Surge Driven by AI

Published Published August 27, 2026 Digital Today (SCMP引用) China

OVERVIEW

China's three leading OSAT firms—JCET, Tongfu Microelectronics, and Huatian Technology—have reported significant profit surges in H1 2026, largely due to escalating AI semiconductor demand. In response, these giants are collectively investing over 15 billion RMB (approximately $2.2 billion USD) into expanding their advanced packaging capabilities. This aggressive move highlights China's strategic push for greater self-sufficiency and competitiveness in critical semiconductor technologies globally.

IN DEPTH

Background

The rapid evolution and widespread adoption of AI technology have created an explosive demand for high-performance AI chips. Satisfying this demand necessitates advanced packaging solutions capable of overcoming the limitations of conventional techniques, positioning advanced packaging as a critical bottleneck in the modern semiconductor supply chain. Nationally, China has strategically prioritized reducing its external dependence in the semiconductor industry and achieving technological self-sufficiency. The aggressive investments by the three OSAT leaders represent concrete steps toward realizing this national objective. Furthermore, in an increasingly competitive global AI semiconductor market, bolstering advanced packaging capabilities is a crucial determinant of international competitiveness, especially amid intensifying US-China technological rivalry.

Key Findings

China's three preeminent Outsourced Semiconductor Assembly and Test (OSAT) providers—JCET, Tongfu Microelectronics, and Huatian Technology—recorded substantial increases in net profit during the first half of 2026. This growth was predominantly driven by the robust demand for AI semiconductors. Individually, JCET reported a 79.4% year-over-year surge in net profit, Tongfu Microelectronics experienced an impressive increase of up to 337%, and Huatian Technology saw a 259% expansion. Capitalizing on these strong financial results, the trio has collectively earmarked capital expenditures exceeding 15 billion RMB (approximately $2.2 billion USD) specifically for the development and expansion of advanced packaging technologies.

Technical Details

Advanced packaging technologies are fundamental for achieving significant performance enhancements and miniaturization in AI semiconductors and High-Performance Computing (HPC) applications. Key areas include chiplet integration, 2.5D/3D stacking, and High Bandwidth Memory (HBM) implementation. The investments from these Chinese OSAT leaders are heavily concentrated in these critical domains: JCET is constructing a new advanced packaging facility in Shanghai's Lingang area, backed by a 7.8 billion RMB investment. Tongfu Microelectronics, partly driven by next-generation AMD processor projects, successfully raised 4.2 billion RMB, with 888 million RMB specifically allocated for memory production expansion. Huatian Technology, meanwhile, plans a 3 billion RMB investment for a memory-related factory in Nanjing, projected to have an annual capacity of 430 million units. These strategic capital outlays clearly underscore China's ambition to secure comprehensive capabilities across the entire AI chip supply chain, spanning from design and manufacturing to final packaging.

Strategic Significance & Outlook

The substantial investments by China's top three OSATs into advanced packaging hold the potential to significantly reshape the global semiconductor packaging landscape. Should these investments prove successful, China could solidify a more robust position in advanced AI semiconductor packaging, thereby expanding its influence throughout the global semiconductor supply chain. This expansion is anticipated to substantially boost the supply capacity of AI chips, potentially enabling a broader spectrum of AI applications in the future. However, amidst escalating geopolitical tensions and intensifying technological rivalry, the advancements made by Chinese companies may also introduce new dynamics and challenges within the international semiconductor ecosystem, making their future trajectory a closely watched phenomenon.

Source: https://www.digitaltoday.co.kr/jp/view/96999/china-top-three-semiconductor-packaging-firms-profit-surge-h1-15-billion-yuan-expansion-race

#10 Semiconductor Manufacturing Equipment and Materials Market Booming with Inference AI Demand and Expanded Chinese Investment; Silicon Wafer Sector Shows Recovery Signs

Published Published August 27, 2026　電子デバイス産業新聞（産業タイムズ社）　Japan

OVERVIEW

The semiconductor manufacturing equipment and materials market is experiencing an unexpected boom, fueled by surging demand for inference AI and significant renewed investment from China. Even the previously challenged silicon wafer market is showing clear signs of recovery. This revitalization, driven by AI proliferation and global supply chain strategies, is positively impacting the entire semiconductor industry.

IN DEPTH

Key Findings

The global semiconductor manufacturing equipment and materials market is experiencing an unexpected surge, surpassing initial forecasts. This boom is propelled by two primary factors: the escalating demand for Artificial Intelligence (AI) inference capabilities and substantial, renewed investments in semiconductor manufacturing within China. Notably, even the silicon wafer market, long challenged by difficult conditions, is now showing signs of recovery and price stabilization. This strongly indicates a broader revitalization of the entire semiconductor ecosystem, heralding entry into a new growth cycle.

Technical Details

The escalating demand for inference AI is driving the need for high-performance chips across a spectrum of applications, from edge devices to data centers. This has expanded demand for AI-specific processors, high-bandwidth memory (HBM), and the advanced packaging technologies crucial for their integration. Manufacturing these complex chips necessitates not only highly advanced front-end equipment, such as EUV lithography tools, but also sophisticated back-end equipment for dicing, bonding, and inspection, alongside specialized materials like high-purity gases, photoresists, and polishing slurries. Concurrently, as part of a national strategy to enhance self-sufficiency, China's semiconductor industry is injecting substantial capital into expanding manufacturing capacity and fostering technological innovation, creating significant tailwinds for the equipment and materials market. The recovery of the silicon wafer market directly reflects this invigorated semiconductor production activity, with particularly robust demand observed for both 8-inch and 12-inch wafers.

Background & Context

Leading up to the mid-2020s, the semiconductor industry grappled with challenges including data processing limits, rising power consumption, and escalating manufacturing costs. However, the advent of generative AI has fundamentally re-evaluated the role of semiconductors, making specialized hardware indispensable for efficient inference AI execution. In parallel, geopolitical factors have spurred nations to strengthen their semiconductor supply chains and enhance domestic production capabilities, with China notably accelerating its investments in the sector as part of this global trend. This confluence of factors has stimulated demand for a wide range of equipment and materials, spanning from front-end to back-end semiconductor manufacturing processes, with heightened expectations particularly for high-precision Japanese equipment and high-quality materials.

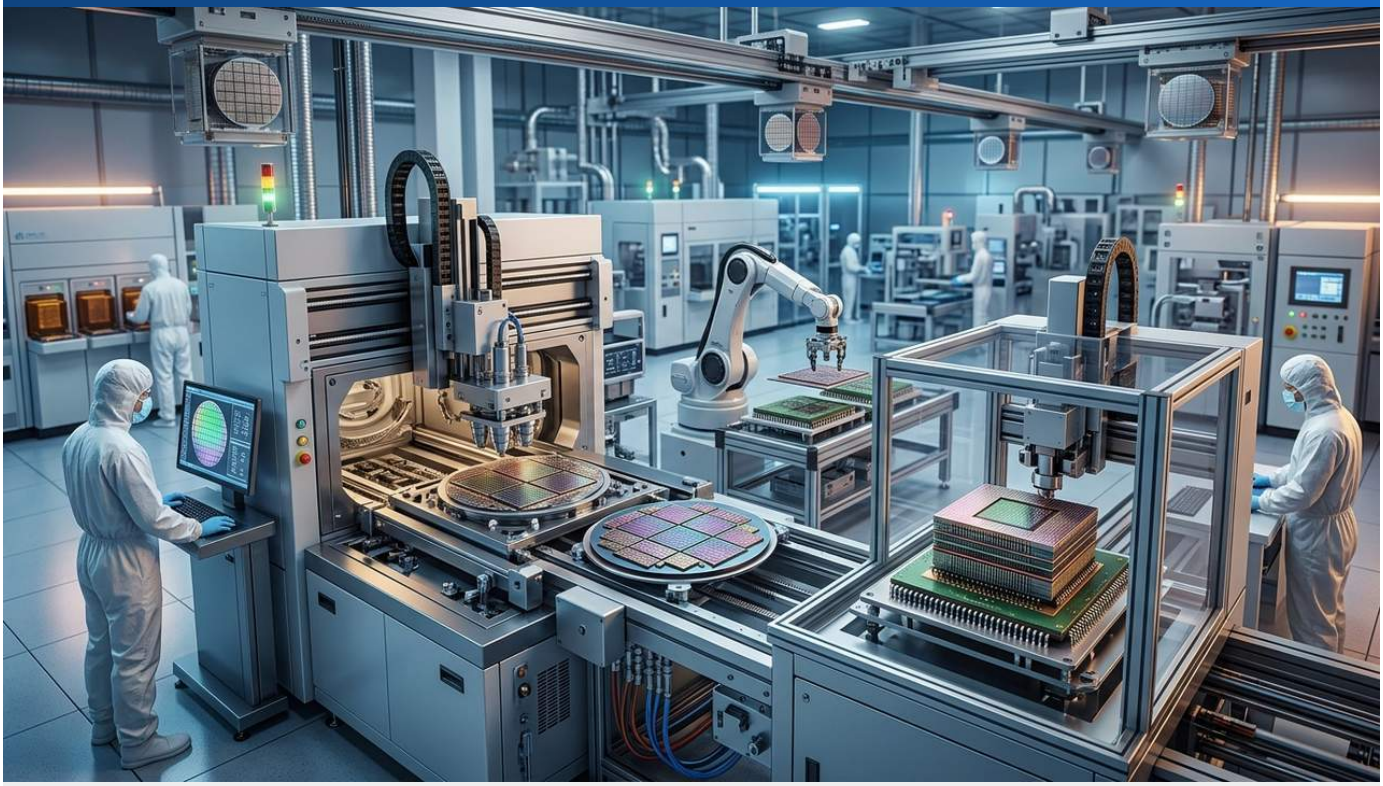
Strategic Significance & Outlook

The current vitality of the semiconductor manufacturing equipment and materials market is not a fleeting phenomenon; rather, it is underpinned by structural changes: the long-term expansion of AI demand and geopolitical restructuring of supply chains. As inference AI continues to evolve, new manufacturing technologies and materials will be perpetually required. The importance of advanced packaging technology, in particular, is set to further increase, projecting sustained growth for the market of related equipment and materials. The stabilization of the silicon wafer market is crucial for establishing a healthy growth foundation for the entire semiconductor industry, and its future trajectory will be closely monitored. Japanese suppliers are strategically positioned to capitalize on this market growth and further strengthen their technological leadership.

Source: https://www.sangyo-times.jp/scn/headindex.aspx

#11 Applied Materials Launches New HBM & 3D Packaging Systems, Acquires ASMPT NEXX to Scale AI Compute

Published September 04, 2026 Exoswan Insights USA



OVERVIEW

Applied Materials has introduced new CMP, ECD, deposition, and e-beam systems for HBM and 3D packaging, alongside acquiring ASMPT's NEXX business, to capitalize on the escalating demand for AI computing. The company forecasts its advanced packaging business to grow over 50% this year, emphasizing material science's critical role in realizing next-generation packages with potentially over 300 chips and 500 billion transistors.

IN DEPTH

Key Findings

Applied Materials has unveiled new Chemical Mechanical Planarization (CMP), Electrochemical Deposition (ECD), deposition, and e-beam systems specifically designed for High Bandwidth Memory (HBM) and 3D packaging, in response to the massive scaling requirements of AI computing. Concurrently, the company has strategically acquired ASMPT's NEXX business to further bolster its advanced packaging capabilities. Applied Materials anticipates its advanced packaging business to grow by over 50% in 2026, driven by the vision of next-generation packages potentially integrating over 300 chips, 500 billion transistors, and more than 2,000 miles of wiring.

Technical & Clinical Details

The newly launched systems by Applied Materials address the intricate demands of HBM stacking, chiplet integration, and advanced interconnects crucial for high-performance 3D packaging. The CMP technology ensures critical planarization and uniformity across multiple layers, while the ECD and deposition systems precisely form the material layers essential for creating dense wiring and connections. The e-beam systems are deployed for advanced inspection and defect detection, vital for improving yields in increasingly complex packaging processes.

The acquisition of ASMPT's NEXX business signifies a strategic move by Applied Materials to expand its solution portfolio in the advanced packaging market, particularly to meet the surging demand for heterogeneous integration and HBM. This integration further leverages Applied Materials' expertise in materials science and process engineering to tackle challenges inherent in next-generation AI chip packaging, such as thermal management, power delivery, and signal integrity.

Background & Context

The explosive growth of AI is having a profound impact across the entire semiconductor industry, dramatically increasing demand for chips in data centers, edge AI, and High-Performance Computing (HPC). This necessitates moving beyond traditional 2D packaging to advanced techniques that integrate multiple dies vertically and horizontally. Gary Dickerson, CEO of Applied Materials, has underscored AI as the "biggest growth inflection point" for the semiconductor industry, emphasizing that material science will play a pivotal role in enabling these new architectures. The company's strategy is squarely focused on proactively addressing this technological shift and establishing leadership in advanced packaging.

Strategic Significance & Outlook

Enhancing AI chip performance critically depends on packaging technologies that can integrate a higher number of chips, transistors, and interconnects. Applied Materials' initiatives directly address this need, laying the groundwork for the high levels of integration and complexity required by future AI chips. The company's ongoing innovation and strategic acquisitions are expected to further solidify its competitive edge in the advanced packaging market and reinforce its position as a leading player in the semiconductor manufacturing equipment sector. The evolution of materials science, in particular, is anticipated to be key to unlocking breakthroughs in future AI computing.

Source: https://exoswan.com/advanced-packaging-stocks

Collected: September 04, 2026 | Automated Research System (Gemini API)

#12 AI Supply Chain Maxed Out: 40-Week Lead Times Become New Normal as HBM Emerges as Primary Bottleneck Over TSMC CoWoS

Published September 03, 2026 Markets Insider USA

OVERVIEW

The AI supply chain faces severe constraints, with 40-week lead times becoming the new norm. High Bandwidth Memory (HBM) has replaced TSMC's CoWoS advanced packaging as the primary bottleneck, driven by NVIDIA's CFO forecasting demand to be roughly double supply. This critical state, dubbed 'redline' operation, signifies that minor disruptions in any part of the supply chain have widespread ripple effects, severely impacting AI infrastructure deployment.

IN DEPTH

Key Findings

The AI supply chain is experiencing unprecedented strain, with lead times for critical components now routinely extending to 40 weeks. This significant elongation in lead times introduces substantial delays and uncertainty in the procurement of AI-related products. While TSMC's CoWoS advanced packaging was previously identified as the primary bottleneck, High Bandwidth Memory (HBM) has now emerged as a new, and potentially more severe, constraint in the supply chain. This situation is further corroborated by NVIDIA's CFO, who anticipates demand to be approximately double the available supply, indicating that the entire supply chain is operating at a 'redline' capacity.

Technical & Clinical Details

HBM is an essential high-speed, high-density memory solution vital for AI accelerators and High-Performance Computing (HPC) chips. It achieves significantly higher bandwidth compared to conventional DRAM by vertically stacking multiple DRAM dies and interconnecting them via Through-Silicon Vias (TSVs). The manufacturing of HBM demands sophisticated 3D packaging technologies and stringent yield control. Production capacity expansion is particularly challenging due to the limited number of qualified suppliers. While key manufacturers like Samsung, SK hynix, and Micron are increasing investments to ramp up production of next-generation HBM, such as HBM3 and HBM4, their pace currently lags behind the surging demand.

Furthermore, reports from Dell indicate that other critical components, including DRAM, NAND, specific CPUs, mature node chips, and key materials like ABF substrates and T-glass, are also facing shortages. This widespread scarcity poses significant challenges for the construction of AI infrastructure, demonstrating that AI demand impacts every stage of the semiconductor supply chain. The complexity of the situation means that resolving a single bottleneck will not alleviate the overall challenges.

Background & Context

The rapid evolution of AI technology has triggered an explosive increase in demand for AI chips, such as GPUs and Application-Specific Integrated Circuits (ASICs). These chips heavily rely on HBM and advanced packaging technologies to process vast amounts of data at high speeds. TSMC's CoWoS technology has been a cornerstone for manufacturing AI chips, and its supply shortage has been a long-standing industry concern. However, the subsequent surge in HBM demand, coupled with its manufacturing complexity and limited supplier base, has propelled it into the forefront as the new primary bottleneck. This scenario compels semiconductor manufacturers, AI chip design companies, and system integrators to reassess and prioritize supply chain risk management, diversification strategies, and long-term supply assurance.

Strategic Significance & Outlook

The HBM supply shortage is expected to directly impact AI server shipment schedules, potentially slowing the deployment pace of AI infrastructure in the short term. While leading HBM manufacturers are accelerating capacity expansion, meeting advanced manufacturing processes and stringent quality requirements takes time, suggesting that prolonged lead times will persist for the foreseeable future. This situation is likely to stimulate increased investment in HBM manufacturers and accelerate the development of alternative or complementary memory technologies and packaging methods. Enhancing supply chain transparency and establishing robust collaborative frameworks across the entire ecosystem will be crucial for the sustained growth of the semiconductor industry in the age of AI.

Source: https://markets.businessinsider.com/news/stocks/ai-supply-chain-is-maxed-out-40-week-lead-times-become-the-new-normal-stockalpha-ai-analysis-finds-1036517727

Collected: September 04, 2026 | Automated Research System (Gemini API)

#13 Intel's EMIB-T Advanced Packaging Projected for Significant Contribution by 2029 as CoWoS Constraints Drive Google's Interest

Published August 31, 2026 TrendForce Taiwan

OVERVIEW

Intel's EMIB (Embedded Multi-die Interconnect Bridge) technology, particularly EMIB-T, is attracting strong interest from major tech firms like Google amid persistent TSMC CoWoS supply constraints. Intel projects its advanced packaging business to accelerate revenue contribution in late 2027 and become a major revenue driver by 2029. This segment targets approximately 40% gross margins and 30% operating margins with relatively modest capital expenditure, positioning it as a key pillar of Intel's future growth.

IN DEPTH

Key Findings

Intel's EMIB (Embedded Multi-die Interconnect Bridge) advanced packaging technology, particularly its EMIB-T (EMIB on Tile) variant, is drawing significant interest from leading technology companies, including Google, amidst ongoing supply constraints for TSMC's CoWoS (Chip-on-Wafer-on-Substrate) packaging. Intel projects that its advanced packaging business, spearheaded by EMIB-T, will begin making substantial revenue contributions in late 2027 and become a major contributor to the company's overall revenue by 2029. This business segment is reported to target approximately 40% gross margins and 30% operating margins with relatively low capital expenditure, positioning it as a critical pillar of Intel's long-term growth strategy.

Technical & Clinical Details

EMIB is a cutting-edge technology that connects multiple chiplets (small semiconductor dies) manufactured on different process nodes through a high-performance, low-power bridge. This approach offers enhanced design flexibility, improved cost efficiency, and better manufacturing yields compared to producing a single, monolithic chip. EMIB-T further evolves this technology to meet the demands of highly integrated AI and High-Performance Computing (HPC) chips. A key advantage of EMIB is its ability to embed a silicon bridge directly within the substrate, eliminating the need for an interposer like CoWoS, which can reduce package height and cost.

Currently, TSMC's CoWoS capacity is severely strained due to the explosive demand for AI chips, prompting major technology companies to seek supply diversification. Intel's EMIB-T presents an attractive alternative solution, with MediaTek officially announcing its parallel adoption of both CoWoS and EMIB-T for the development of its ultra-large AI ASICs. Furthermore, SK hynix is reportedly receiving EMIB-enabled substrates from Intel to explore co-packaging solutions for HBM and system semiconductors, signaling a growing trend towards diversifying the advanced packaging supply chain.

Background & Context

The rapid advancement of AI is driving a new paradigm shift in the semiconductor industry, where not just chip performance but also overall system integration and packaging technology are becoming decisive competitive factors. Intel, traditionally an Integrated Device Manufacturer (IDM), has been strengthening its foundry services (Intel Foundry Services, IFS) in recent years, aiming to boost its market presence by offering advanced process and packaging technologies to third parties. EMIB technology is a crucial component of Intel's proposed chiplet ecosystem, and by aligning with open interface standards like Universal Chiplet Interconnect Express (UCIe), it is expected to significantly enhance the flexibility of future semiconductor designs.

Strategic Significance & Outlook

Intel's EMIB-T has the potential to establish itself as a critical alternative advanced packaging solution in the AI and HPC markets as long as CoWoS supply constraints persist. The projection of significant contributions from Intel's advanced packaging business by 2029 underscores the company's view of packaging as a key differentiator within its foundry strategy. This move is expected to promote diversification across the broader semiconductor supply chain, reducing reliance on single packaging technologies. With its robust profit margin targets and relatively low capital expenditure requirements, Intel is positioning this advanced packaging business as a high-growth, high-profit driver to enhance its long-term competitiveness.

Source: https://www.trendforce.com/news/2026/08/31/news-intels-advanced-packaging-led-by-emib-t-reportedly-set-to-hit-its-stride-in-2029-dram-manufacturing-return-ruled-out/

Collected: September 04, 2026 | Automated Research System (Gemini API)

#14 KLA's Advanced Packaging Business Set for $1.1 Billion Revenue, 70%+ Growth Driven by AI Demand and Yield Bottleneck Resolution

Published September 03, 2026 Quartz USA

OVERVIEW

KLA is significantly benefiting from accelerating demand for advanced packaging inspection, metrology, and process control tools due to the increasing complexity of AI/HPC chips and hybrid bonding advancements. Its advanced packaging business is projected to grow over 70% in 2026, reaching approximately $1.1 billion in revenue. KLA's systems are essential for identifying defects early and preventing costly production losses, especially as defect-related costs in chiplet and stacked memory packages escalate.

IN DEPTH

Key Findings

KLA is experiencing substantial benefits from the escalating demand for inspection, metrology, and process control solutions in advanced packaging, driven by the increasing complexity of AI and High-Performance Computing (HPC) chips and the progression of hybrid bonding technologies. The company's advanced packaging business is projected to achieve over 70% revenue growth in 2026, reaching approximately $1.1 billion. This growth is directly attributable to the critical need for KLA's technology to identify defects in early manufacturing stages and prevent expensive production losses, especially as the economic impact of defects in multi-die integrated packages like chiplets and High Bandwidth Memory (HBM) dramatically increases.

Technical & Clinical Details

AI and HPC chips often employ heterogeneous integration, involving the complex arrangement of multiple chiplets and memory dies both vertically and horizontally. In such intricate setups, even minute defects during the packaging process can lead to final product failure or significant yield degradation. To address these advanced packaging challenges, KLA offers a comprehensive portfolio of process control platforms, including sophisticated optical inspection systems, high-precision dimensional metrology tools, and chemical analysis solutions for material characterization.

Emerging interconnect technologies like hybrid bonding (direct copper-to-copper bonding) enable higher connection densities and shorter signal paths. However, they also impose extremely tight manufacturing tolerances, making microscopic particles or alignment errors catastrophic. KLA's systems provide high-resolution defect detection capabilities and real-time process feedback to manage these challenges effectively. Similar to Onto Innovation's Dragonfly G5 platform being adopted for HBM4 and 2.5D AI packaging, and Camtek's surging orders for advanced packaging inspection, KLA maintains a strong market position with its broad portfolio.

Background & Context

As AI drives transformations across both ends of the semiconductor manufacturing process, KLA is meeting market needs through its extensive range of process control platforms. The increasing size and layer count of AI chip designs significantly escalate manufacturing costs and timelines, making the economic loss from a single defect substantial. Consequently, the value of rigorous inspection and metrology at every stage of the manufacturing process has dramatically increased. With governments, including those implementing the U.S. CHIPS Act, focusing on semiconductor supply chain resilience and domestic manufacturing capacity, process control equipment suppliers like KLA play a strategically vital role due to their indispensable contribution to manufacturing efficiency and yield improvement.

Strategic Significance & Outlook

The evolution of AI chips is relentless, and packaging complexity will only continue to grow. The introduction of technologies such as glass substrates and novel interconnects will demand even more sophisticated inspection and metrology capabilities. KLA, leveraging its broad portfolio and extensive expertise, is expected to maintain its leadership in process control within the advanced packaging market, even as competition intensifies with rivals like Onto Innovation and Applied Materials. Future technological developments for KLA will likely focus on enhancing defect detection precision, incorporating AI-driven data analysis, and enabling automated process optimization. These advancements are crucial for reducing AI chip manufacturing costs and accelerating time-to-market, thereby serving as a critical foundation for the overall growth of the AI industry.

Source: https://qz.com/kla-gains-from-advanced-packaging-can-it-outpace-onto-amat

Collected: September 04, 2026 | Automated Research System (Gemini API)

#15 Glass Substrates Emerge as Key Breakthrough for Next-Gen AI Chip Packaging: Intel, TSMC, Samsung Accelerate Development

Published September 01, 2026 Industry Analyst International

OVERVIEW

Glass substrates are increasingly recognized as a critical breakthrough for next-generation AI chip packaging, with industry leaders like Intel, TSMC, and Samsung Electro-Mechanics accelerating their development. Glass offers potential for larger package sizes, finer interconnects, and higher connection densities than traditional organic substrates. Its superior dimensional stability and thermal expansion coefficient, close to silicon, are key advantages, while TRUMPF addresses through-glass via coating challenges with HiPIMS technology.

IN DEPTH

Key Findings

Glass substrates are emerging as a pivotal breakthrough technology for next-generation AI chip packaging, with industry leaders such as Intel, TSMC, and Samsung Electro-Mechanics significantly accelerating their development efforts. Glass substrates offer the potential to support larger package sizes, finer interconnects, and higher connection densities compared to conventional organic substrates. Particularly, their coefficient of thermal expansion (CTE) closely matches that of silicon, which is highly valued for dimensional stability in large-scale chiplet integration, promising enhanced performance and cost reduction for AI and High-Performance Computing (HPC) chips.

Technical & Clinical Details

The primary advantages of glass substrates lie in their superior mechanical strength, thermal stability, and low dielectric loss characteristics. These properties enable the formation of finer line/space (L/S) wiring and high-density Through-Glass Vias (TGVs). TGVs are minute electrical interconnections passing through the glass substrate, facilitating high-speed, low-latency data transmission between chiplets and High Bandwidth Memory (HBM).

Intel announced its glass core substrate as an alternative to organic chip packaging in September 2023, which is currently in the final qualification stages. Absolics, a subsidiary of SKC, is conducting package-level reliability evaluations for glass substrates produced at its Georgia factory in Taiwan, with results expected by year-end. Samsung Electro-Mechanics and LG Innotek are also advancing their glass substrate programs, and Dai Nippon Printing aims for full-scale mass production by 2028. A significant manufacturing challenge involves reliably coating millions of TGVs; TRUMPF has introduced a High Power Impulse Magnetron Sputtering (HiPIMS) approach to form more uniform conductive coatings inside deep, narrow holes, aiming to resolve this bottleneck.

Background & Context

The explosive demand for AI chips is pushing the boundaries of traditional packaging technologies. The strain on TSMC's CoWoS capacity and the HBM supply shortage have underscored the critical need for alternative, advanced packaging materials. Glass substrates are rapidly gaining industry attention as a promising candidate to address these challenges. Especially with the proliferation of chiplet architectures and heterogeneous integration, the CTE mismatch between different materials profoundly affects package reliability and yield. The silicon-like CTE of glass substrates mitigates this issue, enabling the realization of larger, higher-performance AI chips. Government policies, such as the CHIPS Act in various countries, are also supporting the development of advanced packaging technologies and strengthening domestic manufacturing capabilities, thereby accelerating investment in glass substrate development.

Strategic Significance & Outlook

Glass substrates are establishing their technological superiority en route to full-scale commercialization, projected for 2028 and beyond. Should companies like Absolics complete their reliability evaluations, adoption by major chip manufacturers, including Intel, could accelerate. Innovations in manufacturing processes, such as TRUMPF's HiPIMS technology, are indispensable for overcoming key bottlenecks in glass substrate mass production and enhancing cost efficiency. The widespread adoption of glass substrates is expected to further boost AI chip performance, enabling new breakthroughs across a wide range of applications, from data centers to edge AI devices. This will likely propel the semiconductor industry into its next phase of growth.

Source: https://www.nepconasia.com/en-gb/media/press-release/2026/9/1.html

Collected: September 04, 2026 | Automated Research System (Gemini API)

#16 Samsung Electro-Mechanics & LG Innotek Boost AI Substrate Capacity: H1 Utilization Nears 90%

Published Published August 27, 2026 TrendForce Taiwan

OVERVIEW

The proliferation of AI data centers has created a critical shortage and driven up prices for advanced substrates essential for GPUs and HBM. In response, Samsung Electro-Mechanics (SEM) and LG Innotek are aggressively expanding production, with SEM's Packaging Solution Division reporting a 41% sales and 237% operating profit surge in H1 2026, as overall H1 utilization rates for AI-focused advanced substrates approach 90%.

IN DEPTH

Background

The relentless pursuit of performance enhancement in AI chips mandates ever-broader data transmission bandwidth between processors and memory, dramatically fueling demand for advanced packaging technologies and high-functional substrates. Advanced packaging solutions, such as TSMC's CoWoS (Chip-on-Wafer-on-Substrate), are currently facing severe supply shortages, thereby transforming GPUs, HBM, and the ABF substrates that interconnect them into critical bottlenecks across the entire AI supply chain. This environment is compelling semiconductor manufacturers to bolster their in-house packaging capabilities and diversify their supply chains. Concurrently, governments, exemplified by initiatives like the U.S. CHIPS Act and the European Chips Act, are actively supporting the domestic resilience of semiconductor supply chains and strengthening investments in advanced packaging and substrates.

Key Findings

The rapid proliferation of AI data centers has led to an extremely tight demand for advanced substrates integrating GPUs and High Bandwidth Memory (HBM), causing substantial price increases. Capitalizing on this booming market, Samsung Electro-Mechanics (SEM)'s Packaging Solution Division achieved remarkable growth in the first half of 2026, reporting a 41% year-on-year increase in sales and a staggering 237% rise in operating profit. LG Innotek is also expanding its semiconductor substrate factory in Vietnam, while Ibiden and Unimicron are bolstering their investments in ABF (Ajinomoto Build-up Film) substrates. This collectively demonstrates a concerted effort by major manufacturers to significantly boost advanced substrate production for AI applications, pushing H1 utilization rates close to 90%.

Technical Deep Dive

Advanced substrates for AI chips require larger areas, higher layer counts, and finer wiring patterns compared to conventional counterparts. ABF substrates, specifically, are pivotal for enabling high-density interconnections between high-performance AI processors and HBM. With AI chips demanding 2.6 to 3 times the substrate area and 12 to 18 or more layers than traditional chips, manufacturing complexity has significantly escalated, posing challenges to maintaining high yields.

SEM boasts strong competitiveness in system LSI packaging technology and FC-BGA (Flip-Chip Ball Grid Array) substrates, strategically focusing on high-value-added products for AI, servers, and automotive applications. The company's impressive financial performance underscores the success of this strategy. LG Innotek's expansion of its Vietnamese factory is geared towards increasing production capacity for advanced packaging substrates like COF (Chip-on-Film) and FC-CSP (Flip-Chip Chip Scale Package), catering to the diverse requirements of AI devices. Leading ABF substrate manufacturers, including Taiwan's Unimicron and Nan Ya PCB, and Japan's Ibiden, are also accelerating capital investments and expanding production capacities to meet the burgeoning AI demand.

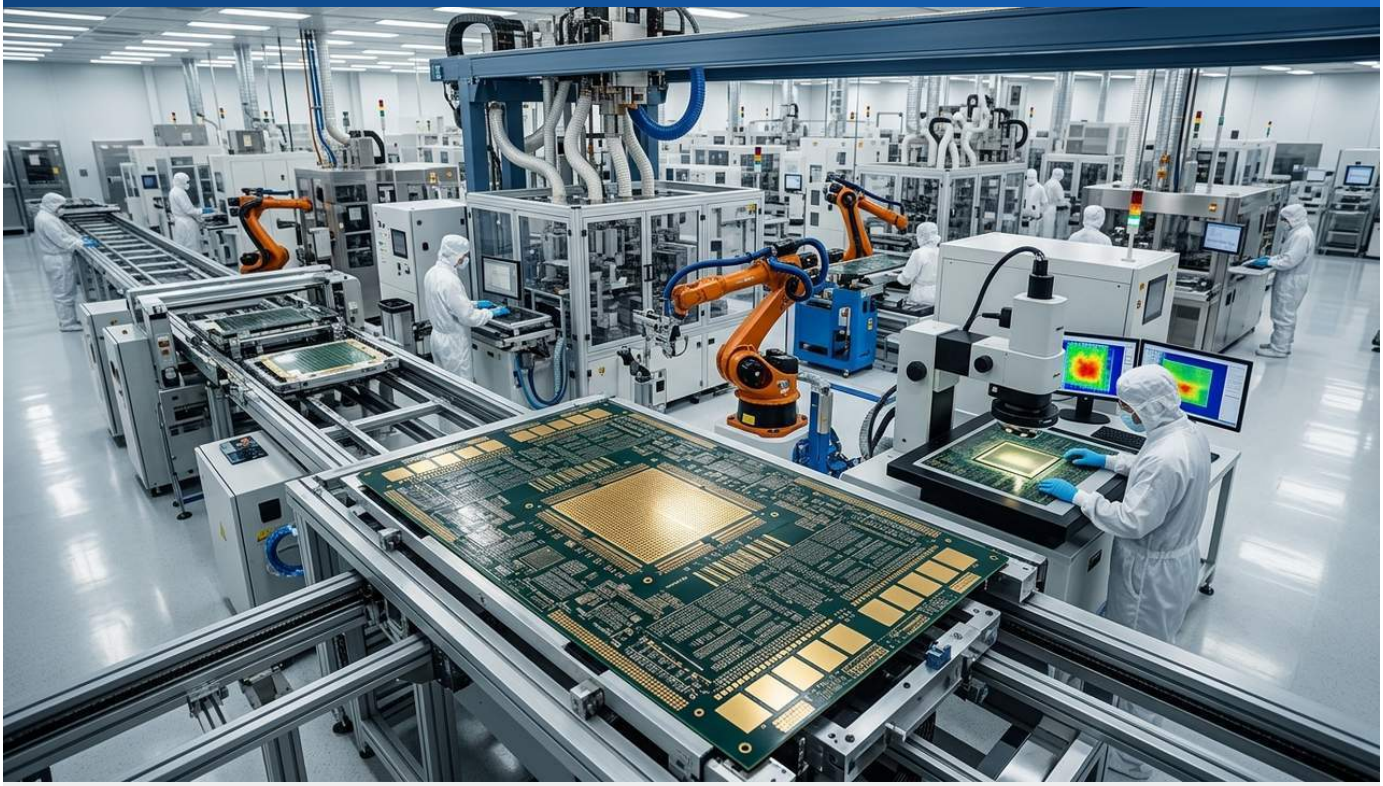
Strategic Outlook

Demand for AI chips is projected to maintain its upward trajectory, indicating that the shortage of advanced substrates will likely persist for an extended period. While major manufacturers are committed to continued capital investment and capacity expansion, achieving a balance between supply and demand will require considerable time, given the sophisticated technologies and lengthy qualification processes involved. A particular supply chain risk arises from the current reliance on small to medium-sized Japanese enterprises for key upstream materials like T-Glass. The proactive initiatives by Samsung Electro-Mechanics and LG Innotek are therefore crucial for maintaining and strengthening competitiveness in the AI-era semiconductor market, necessitating a sustained focus on technological innovation and the establishment of highly efficient production systems. Furthermore, the introduction of novel technologies, such as glass substrates, will be paramount for long-term supply stabilization and enhanced performance.

Source: https://www.trendforce.com/news/2026/08/27/news-samsung-electro-mechanics-lg-innotek-ramp-up-ai-substrate-capacity-as-1h-utilization-reportedly-nears-90/

#17 High-End ABF Substrate Shortage Intensifies Due to Massive AI Chips: Taiwanese Makers & Equipment Suppliers Face Fierce Competition

Published September 02, 2026 Medium (by Julien Nauy) International



OVERVIEW

The high-end ABF (Ajinomoto Build-up Film) substrate market for AI chips faces a severe supply shortage, reflecting a 're-evaluation of manufacturing difficulty' distinct from traditional ABF markets. AI chips demand 2.6 to 3 times larger substrate areas and 12 to 18+ layers, making yield maintenance a critical challenge. Taiwanese manufacturers like Unimicron, Nan Ya PCB, Kinsus, and Zhen Ding, along with related equipment suppliers, are intensely competing in this high-growth sector.

IN DEPTH

Key Findings

The high-end ABF (Ajinomoto Build-up Film) substrate market for AI chips is experiencing a severe supply shortage, which is not merely due to increased demand but rather a structural issue stemming from a 're-evaluation of manufacturing difficulty.' AI chips require 2.6 to 3 times larger substrate areas and 12 to 18 or more layers compared to conventional CPUs or GPUs. This dramatically increases manufacturing complexity, making the maintenance of high yields exceptionally challenging. Consequently, leading Taiwanese manufacturers such as Unimicron, Nan Ya PCB, Kinsus, and Zhen Ding, along with their associated manufacturing equipment suppliers, are engaged in fierce competition within this high-barrier, high-end ABF market.

Technical & Clinical Details

ABF substrates are indispensable laminated substrates for high-performance semiconductor packaging, widely utilized in Flip-Chip Ball Grid Array (FC-BGA) packages. For AI chips, which require tight integration of GPUs and HBM (High Bandwidth Memory), substrates must be larger, have more layers, and feature finer wiring (line width/space: L/S). For instance, while traditional ABF substrates typically have fewer than 8 layers, AI chip variants commonly require 12 to over 18 layers.

The increase in layer count and area exacerbates challenges such as alignment precision in multilayer wiring formation, accuracy in via hole processing, and the reliability of electrical connections between layers. Furthermore, large substrates are prone to greater warping and dimensional changes during manufacturing, which is a major contributor to yield loss. Process control equipment manufacturers like KLA and Onto Innovation provide high-precision inspection, metrology, and defect detection solutions to address these issues and improve yields. Unimicron, for example, has approved additional capital expenditure, focusing 80-85% on ABF substrates, and has significantly increased pre-orders for critical equipment for 2027-2028, signaling a strong commitment to AI chip ABF substrate manufacturing.

Background & Context

The explosion of AI demand has had a widespread impact across the entire semiconductor manufacturing supply chain, with bottlenecks sequentially shifting from front-end processes to packaging, substrates, and materials. Amidst persistent shortages in TSMC's CoWoS (Chip-on-Wafer-on-Substrate) packaging and soaring HBM demand, the supply of high-functional ABF substrates has also become a critical issue. AI server vendors like Dell have identified ABF substrate shortages as a major source of supply chain tension, impeding the deployment of AI infrastructure. This situation exemplifies how Taiwan's semiconductor packaging ecosystem is adapting to the AI boom, highlighting the increasing strategic importance of not only OSATs (Outsourced Semiconductor Assembly and Test) but also substrate manufacturers.

Strategic Significance & Outlook

The shortage of high-end ABF substrates is likely to persist as AI chip evolution continues. The introduction of new upstream materials like T-Glass (glass substrates) will further enhance ABF substrate performance and alter manufacturing difficulties. In this market, stable supply chain establishment and risk management, alongside technological innovation, will be key to success. While Taiwanese manufacturers aim to maintain their competitive edge in this high-end market, leveraging years of experience and technical prowess, strong competitors like Japan's Ibiden and Shinko Electric, South Korea's Samsung Electro-Mechanics, and Austria's AT&S also exist. The expansion of AI computing will fundamentally reshape the cooperative dynamics of the entire semiconductor supply chain.

Source: https://medium.com/@JulienNauy/ai-substrates-are-not-all-in-short-supply-taiwans-real-high-end-abf-race-04cdff72e30a

Collected: September 04, 2026 | Automated Research System (Gemini API)

#18 TRUMPF Resolves Glass Substrate TGV Coating Bottleneck with High-Power HiPIMS, Accelerating Next-Gen AI Chip Packaging

Published September 03, 2026 TRUMPF Germany

OVERVIEW

TRUMPF has introduced a High-Power Impulse Magnetron Sputtering (HiPIMS) approach to address a key manufacturing challenge in next-generation AI chip packaging: reliably coating millions of minute Through-Glass Vias (TGVs) in glass substrates. This HiPIMS technology facilitates the formation of more uniform conductive coatings inside the deep, narrow holes of glass substrates. Glass is gaining attention as an advanced packaging material for its ability to support high-density interconnects and fast, efficient data transmission, with TRUMPF's innovation accelerating its practical application.

IN DEPTH

Key Findings

TRUMPF has presented a groundbreaking solution to a major manufacturing challenge in next-generation AI chip packaging, specifically the reliable and uniform coating of millions of minute Through-Glass Vias (TGVs) in glass substrates. The company's introduction of a High-Power Impulse Magnetron Sputtering (HiPIMS) approach enables the formation of more uniform and high-quality conductive coatings inside the deep, narrow holes of glass substrates. This innovation effectively removes a critical bottleneck for the commercialization of glass substrates, thereby accelerating the realization of advanced packaging for AI and High-Performance Computing (HPC) chips.

Technical & Clinical Details

Glass substrates are considered an ideal material for next-generation AI chip packaging due to their advantageous properties compared to traditional organic substrates, including a coefficient of thermal expansion (CTE) close to silicon, high dimensional stability, excellent electrical characteristics (low dielectric loss), and fine processability. These features enable the creation of finer line width/space (L/S) wiring and high-density Through-Glass Vias (TGVs). TGVs are minute electrical interconnections that pass through the glass substrate, facilitating high-speed, low-latency data transmission between chiplets and HBM (High Bandwidth Memory).

However, a significant technical hurdle in their manufacturing process has been the challenge of forming millions of TGVs and uniformly depositing conductive layers on their inner walls. Non-uniform TGV coatings can lead to variations in electrical resistance and reduced reliability, negatively impacting the final package performance.

TRUMPF's HiPIMS technology generates a high-density, high-energy plasma, allowing sputtered particles from the target material to reach deep and uniformly into the TGV interiors on the substrate. This ensures the deposition of high-quality conductive layers, such as copper, on the sidewalls and bottoms of the TGVs, securing reliable electrical connections. This precise deposition capability directly translates into improved yields and performance stability for complex AI packages that integrate more chiplets and HBM.

Background & Context

The explosive growth of AI is driving structural changes in the semiconductor industry, making packaging technology a critical factor in determining overall system performance, beyond just processor advancements. The strain on TSMC's CoWoS (Chip-on-Wafer-on-Substrate) capacity and the HBM supply shortage have accelerated demand for new advanced packaging materials like glass substrates. Leading companies such as Intel, TSMC, and Samsung Electro-Mechanics are heavily investing in glass substrate R&D, eagerly anticipating its commercialization. TRUMPF's HiPIMS technology breaks through a key technological barrier in glass substrate manufacturing, playing a crucial role in promoting innovation across the entire supply chain and accelerating the market entry of AI chips.

Strategic Significance & Outlook

The introduction of HiPIMS technology by TRUMPF significantly paves the way for glass substrates to become a mainstream solution in next-generation AI chip packaging. This technological advancement is expected to improve mass production costs and yields for glass substrates, accelerating their full-scale commercialization, which is projected to occur from 2028 onwards. Increased adoption of glass substrates will lead to even higher performance and integration levels for AI chips, enabling more complex AI models and new applications. Innovations from equipment manufacturers like TRUMPF are crucial for strengthening the entire semiconductor manufacturing supply chain's technological ecosystem and supporting the exponential increase in computing power during the AI era.

Source: https://technode.global/2026/09/03/trumpf-glass-substrates-ai-chip-packaging-hipims/

Collected: September 04, 2026 | Automated Research System (Gemini API)

#19 Simmtech to Invest 400 Billion Won in Next-Gen AI Server Substrate Production: Capacity Expansion Starts 2028

Published September 02, 2026 The Elec Inc. South Korea

OVERVIEW

Simmtech announced a phased 400 billion won (approx. $300 million) investment to expand production capacity for next-generation substrates used in AI servers. New facilities in Cheongju will boost output for SOCAMM module PCBs, multi-layer mSAP substrates, and system IC semiconductor substrates. The new lines are scheduled to sequentially begin operation from 2028, projected to increase annual SOCAMM module production capacity from 300 billion to 500 billion won.

IN DEPTH

Key Findings

Simmtech announced a significant phased investment totaling 400 billion won (approximately $300 million) to expand its production capacity for next-generation substrates, addressing the growing demand from AI servers. This investment, formalized through a Memorandum of Understanding (MOU) with North Chungcheong Province and Cheongju City, will see new production facilities built in Oksan-myeon, Cheongju City, and within unused spaces at existing plants. These expansions will substantially increase manufacturing capabilities for SOCAMM (System-on-Chip Advanced Memory Module) module PCBs, multi-layer mSAP (modified Semi-Additive Process) substrates, and semiconductor substrates for system ICs. The new lines are slated to commence operations sequentially from 2028, with the annual production capacity for SOCAMM modules expected to increase from the current 300 billion won to 500 billion won.

Technical & Clinical Details

Next-generation substrates for AI servers are critical for enabling high-density interconnections between high-performance AI processors and HBM (High Bandwidth Memory). SOCAMM module PCBs are essential components in these complex AI systems, facilitating efficient integration of memory and processors. The mSAP technology, which Simmtech excels in, allows for finer circuit patterns than traditional subtractive processes, achieving high-density wiring and low-loss characteristics. This maximizes the high-speed data processing capabilities of AI chips. Simmtech, a leading South Korean semiconductor substrate manufacturer with a strong foundation in mSAP technology, is further strengthening its technological advantage and addressing the advanced packaging needs of the AI era with this investment.

As AI chips become larger and more multi-layered, substrates demand stricter dimensional stability, warpage control, and thermal management properties. Simmtech's new production facilities will be equipped with state-of-the-art manufacturing technologies and cleanroom environments to meet these requirements, ensuring high-yield mass production. The scheduled commencement of operations from 2028 is particularly well-timed with the ongoing growth cycle of AI infrastructure, and is expected to contribute to alleviating supply chain challenges such as the ABF substrate and T-glass shortages reported by AI server vendors like Dell.

Background & Context

The rise of AI data centers has had a widespread impact across the entire semiconductor industry, especially dramatically increasing demand for high-performance GPUs, HBM, and advanced materials like ABF and IC substrates that connect them. The tight supply of TSMC's CoWoS (Chip-on-Wafer-on-Substrate) packaging has created bottlenecks throughout the supply chain, presenting new business opportunities for substrate manufacturers like Simmtech. The South Korean government has designated the semiconductor industry as a national strategic sector, actively promoting the strengthening of advanced manufacturing capabilities domestically. Simmtech's investment aligns with this national strategy, ensuring South Korea plays a crucial role in the AI-era semiconductor supply chain.

Strategic Significance & Outlook

Simmtech's substantial investment is expected to significantly enhance its competitiveness in the next-generation AI server substrate market. The new lines, operational from 2028, will provide essential supply capacity for the continuous expansion of AI infrastructure, contributing to the stabilization of the global AI semiconductor supply chain. With SOCAMM module PCB production capacity increasing to 500 billion won, Simmtech is expected to deepen partnerships with AI chip design companies and memory manufacturers, leading technological innovation. As AI chips continue to evolve, demanding higher density, faster speeds, and lower power consumption from substrate technologies, Simmtech's ongoing research and development and capital investments will remain a key focus.

Source: https://www.thelec.net/news/articleView.html?idxno=13591

Collected: September 04, 2026 | Automated Research System (Gemini API)

#20 TSMC SVP Reports 90% Surge in Equipment Orders in Six Months Driven by AI Demand: Equivalent to Building 20 Fabs Globally Simultaneously

Published September 03, 2026 TechSoda Taiwan

OVERVIEW

TSMC Senior VP Cliff Hou reported an astonishing 90% surge in equipment orders over six months, driven by AI demand far exceeding forecasts, equivalent to constructing nearly 20 fabs worldwide simultaneously. Unimicron Technology's chairman stated that AI chips are driving larger, multi-layered, and more complex substrates, leading to 'extremely tight' ABF substrate capacity. Critically, key upstream materials like T-Glass are heavily dependent on small and medium-sized Japanese suppliers, exacerbating the severe shortage.

IN DEPTH

Key Findings

TSMC Senior Vice President Cliff Hou reported an astonishing 90% surge in TSMC's equipment orders over the past six months, driven by AI demand that has far outstripped previous forecasts. He noted that the scale of this demand is equivalent to simultaneously building approximately 20 semiconductor manufacturing fabs worldwide. This severe strain is echoed by Chien Shan-Chieh, Chairman of Unimicron Technology, who emphasized that AI chips are pushing for larger, multi-layered, and more complex substrates, leading to an 'extremely tight' capacity for ABF (Ajinomoto Build-up Film) substrates. A significant contributing factor to this acute shortage is the heavy reliance on small and medium-sized Japanese enterprises for key upstream materials like T-Glass (glass substrates).

Technical & Clinical Details

AI chips, particularly GPUs and ASICs (Application-Specific Integrated Circuits), require massive packages with multiple cores, HBM (High Bandwidth Memory), and complex interconnections to process vast amounts of data at high speeds. Manufacturing such chips necessitates not only cutting-edge wafer process technology but also advanced packaging techniques like CoWoS (Chip-on-Wafer-on-Substrate). CoWoS integrates multiple chiplets via an interposer and achieves high-bandwidth connections with HBM, but its manufacturing process is exceptionally complex, and expanding production capacity demands significant time and investment.

ABF substrates play a crucial role in electrically connecting the processor and HBM within CoWoS packages, vital for maximizing AI chip performance. ABF substrates for AI chips demand 2.6 to 3 times larger areas and 12 to over 18 layers compared to traditional substrates, significantly increasing manufacturing difficulty. This leads to challenges in maintaining yields and concentrates demand among a limited number of suppliers. Furthermore, glass substrates (T-Glass) are gaining attention as a next-generation packaging material, requiring innovative technologies like TRUMPF's HiPIMS (High Power Impulse Magnetron Sputtering) for their fabrication.

Background & Context

The explosive growth of AI has had a widespread impact across the entire semiconductor supply chain, creating shortages and bottlenecks at every stage, from front-end wafer fabrication to packaging, substrates, and materials. Reports that Nvidia is securing the majority of global CoWoS capacity indicate that major AI chip players are striving to dominate the supply chain. Governments, including those enacting the U.S. CHIPS Act and the European Chips Act, are also providing policy support for strengthening domestic semiconductor manufacturing capabilities and diversifying supply chains, which in turn encourages investment from key suppliers like TSMC and Unimicron.

Strategic Significance & Outlook

The surge in TSMC's equipment orders and the severe ABF substrate shortage suggest that the AI chip demand-supply gap will not be resolved in the short term. Particularly, the bottleneck in upstream materials like T-Glass, which are heavily dependent on small and medium-sized Japanese companies, threatens the overall resilience of the supply chain. This situation is prompting the entire semiconductor industry to re-evaluate the importance of broader supplier collaboration, investment in new manufacturing technologies, and strategic material procurement. The commercialization of glass substrate technology and the emergence of alternative packaging solutions like Intel's EMIB-T will be key to stabilizing future AI chip supply chains. The expansion of AI computing will fundamentally reshape the cooperative dynamics of the semiconductor industry and accelerate further innovation.

Source: https://techsoda.substack.com/p/global-market-watch-tsmcs-cliff-hou

Collected: September 04, 2026 | Automated Research System (Gemini API)

#21 Dell Reports Record Q2 Revenue of $47 Billion with $95 Billion AI Server Backlog; Entire Supply Chain, Including DRAM, HBM, ABF Substrates, at 'Redline'

Published September 02, 2026 KuCoin International

OVERVIEW

Dell reported record Q2 revenue of $47 billion and an impressive $95 billion backlog for AI servers. However, Dell executives stated that the entire supply chain, including DRAM, NAND, specific CPUs, mature node chips, and critically, ABF substrates and T-glass, is under severe strain. While AI infrastructure is booming, component procurement remains the biggest challenge, highlighting a 'redline' operational status across the entire AI supply chain.

IN DEPTH

Key Findings

Dell has reported a record-breaking $47 billion in revenue for the second quarter of 2026, accompanied by an extraordinary $95 billion backlog in AI server orders. While this signifies robust demand for AI infrastructure, Dell executives simultaneously warned that the entire supply chain is under extreme tension. Specifically, critical components such as DRAM, NAND flash memory, certain CPUs, and mature node chips, in addition to ABF (Ajinomoto Build-up Film) substrates and T-glass (glass substrates), are facing severe shortages. This situation underscores that the entire AI supply chain is operating at a 'redline' capacity.

Technical & Clinical Details

AI servers heavily rely on high-performance GPUs, HBM (High Bandwidth Memory), and sophisticated packaging technologies and substrates to integrate these components. Dell's $95 billion AI server backlog reflects the immense demand from data centers and enterprise customers for advanced AI workload processing capabilities. However, key components essential for building these AI systems, particularly HBM, are now among the most critical bottlenecks, similar to the challenges previously seen with TSMC's CoWoS packaging.

ABF substrates serve as vital interconnects between AI chip processors and HBM. With the increasing size and layer count of AI chips, these substrates require significantly larger areas and more complex structures than traditional designs. T-glass (glass substrates) is an emerging next-generation packaging material, anticipated to contribute to further performance enhancements in AI chips due to its high dimensional stability and superior electrical properties. The scarcity of these advanced materials and components directly constrains the production and shipment of AI servers, posing a major impediment to revenue realization for system vendors like Dell. The supply chain remains in a fragile state, where a delay in any single component can cause ripple effects throughout the entire system.

Background & Context

The rapid advancement of AI is creating unprecedented demand and structural challenges throughout the semiconductor industry. As AI chip designs become more complex and larger, the importance of advanced packaging technologies and high-functional substrates increases. The focus of the bottleneck has shifted from TSMC's CoWoS to HBM. Global semiconductor shortages, particularly limits in manufacturing capacity for advanced nodes, combined with the restricted supply sources for specific materials like ABF substrates and T-glass, exacerbate the vulnerability of the entire supply chain. While investments in semiconductor manufacturing capacity, such as those under the U.S. CHIPS Act, are progressing, it is expected to take time to catch up with the pace of AI demand.

Strategic Significance & Outlook

The situation where major system vendors like Dell face severe supply chain constraints despite holding record AI server backlogs highlights both the long-term growth potential of the AI infrastructure market and the critical challenges in component procurement. In the short term, shortages of HBM, ABF substrates, T-glass, and other components will continue to restrict AI server shipments. In the mid to long term, closer collaboration among semiconductor manufacturers, material suppliers, and system vendors, along with strategic investments in supply chain diversification and resilience, will be essential. The commercialization of glass substrates and the development of new packaging technologies will be key to achieving sustainable growth in the AI era.

Source: https://www.kucoin.com/news/flash/dell-reports-record-q2-revenue-of-47b-ai-server-backlog-hits-95b

Collected: September 04, 2026 | Automated Research System (Gemini API)

#22 Amkor Technology and NVIDIA Announce $1.5 Billion Advanced Packaging Partnership to Accelerate AI Multi-Die Integration

Published September 02, 2026 IMAPS 3D InCites Content Platform USA

OVERVIEW

Amkor Technology and NVIDIA announced a multi-year partnership in July 2026, including a $1.5 billion advanced packaging and development agreement, to drive next-generation technology for AI and accelerated computing platforms and expand U.S. advanced packaging capabilities. This collaboration addresses new demands on substrate routing density, dimensional stability, and warpage control arising from larger packages. Amid surging demand for multi-die integration, hybrid bonding, and HBM, the partnership accelerates industry innovation by emphasizing performance, thermal management, and mechanical stability.

IN DEPTH

Key Findings

Amkor Technology and NVIDIA announced a multi-year partnership in July 2026, which includes a substantial $1.5 billion advanced packaging and development agreement. This collaboration aims to drive next-generation technology for AI and accelerated computing platforms and to expand advanced packaging capabilities within the United States. This strategic alliance is specifically designed to address new technical demands on substrate routing density, dimensional stability, and warpage control, which arise from the increasingly larger package sizes necessitated by evolving AI chips. With the surging demand for multi-die integration, hybrid bonding, and High Bandwidth Memory (HBM), the partnership is set to accelerate industry innovation by prioritizing performance, thermal management, and mechanical stability at the package level.

Technical & Clinical Details

Maximizing the performance of AI chips requires the efficient and high-density integration of multiple processor dies, HBM, and other components within a single package. This multi-die integration relies on advanced packaging technologies such as 2.5D packaging, exemplified by TSMC's CoWoS (Chip-on-Wafer-on-Substrate), and 3D packaging techniques like hybrid bonding. Hybrid bonding directly joins chips, achieving significantly higher density and finer pitch interconnects than traditional wire bonding or flip-chip technologies. This reduces signal transmission distances, thereby enhancing performance and power efficiency.

However, the trend towards larger packages introduces new challenges in substrate design and manufacturing. Key issues include efficiently routing high-density interconnections within limited space, maintaining dimensional stability despite coefficient of thermal expansion (CTE) mismatches between different materials, and controlling substrate warpage during manufacturing. These factors directly impact yield and reliability. The Amkor-NVIDIA partnership focuses on joint development to address these challenges, aiming to create innovative solutions by combining Amkor's advanced packaging technologies and manufacturing expertise with NVIDIA's AI chip design capabilities.

Background & Context

The explosive growth of AI has profoundly impacted the entire semiconductor industry, transforming advanced packaging from a chip performance bottleneck into a primary differentiator. The tight supply of TSMC's CoWoS capacity has prompted leading AI chip designers like NVIDIA to diversify their supply chains and secure alternative packaging solutions. The U.S. CHIPS Act has allocated substantial funding to bolster domestic advanced packaging capabilities, and the Amkor-NVIDIA partnership aligns perfectly with this policy framework. This collaboration contributes to strengthening the AI-related semiconductor manufacturing ecosystem within the U.S. and carries strategic significance in enhancing global supply chain resilience.

Strategic Significance & Outlook

The multi-year partnership between Amkor and NVIDIA represents a critical step towards elevating the performance of AI and accelerated computing chips to the next level. Through joint development, it is expected to yield higher-performing, more power-efficient, and more reliable packaging solutions. Critically, the expansion of advanced packaging capabilities in the U.S. will play a vital role in diversifying supply chain risks and increasing resilience against geopolitical fluctuations. This partnership may also encourage the formation of similar strategic alliances between other chip design companies and OSATs (Outsourced Semiconductor Assembly and Test providers), potentially accelerating the restructuring of the entire semiconductor manufacturing ecosystem in the AI era.

Source: https://www.3dincites.com/2026/09/advanced-packaging-the-foundation-of-next-generation-semiconductor-innovation/

Collected: September 04, 2026 | Automated Research System (Gemini API)

#23 Unimicron Reports 90% Surge in Equipment Demand from AI, Japanese SME Dependence on ABF Substrates Creates Bottleneck

Published September 03, 2026 BigGo Finance Taiwan

OVERVIEW

Unimicron Technology Chairman Chien Shan-Chieh stated that escalating AI demand has severely impacted the substrate sector, worsening supply-demand imbalance due to heavy reliance on small and medium-sized Japanese suppliers for key tools like ABF materials and TGV technology. TSMC Senior VP Cliff Hou also reported a 90% surge in equipment orders over six months, equivalent to building 20 fabs globally. Unimicron approved additional capital expenditure, focusing 80-85% on ABF substrates, and significantly increased equipment pre-orders for 2027-2028.

IN DEPTH

Key Findings

Chien Shan-Chieh, Chairman of Unimicron Technology, highlighted that the rapid surge in AI (Artificial Intelligence) demand is profoundly impacting the semiconductor substrate sector, leading to a worsening supply-demand imbalance. This is primarily attributed to a significant reliance on small and medium-sized Japanese suppliers for crucial manufacturing tools, including ABF (Ajinomoto Build-up Film) materials and Through-Glass Via (TGV) technology. Concurrently, TSMC Senior Vice President Cliff Hou reported that AI-driven demand has far exceeded forecasts, resulting in an astounding 90% increase in TSMC's equipment orders over the past six months, a scale comparable to simultaneously constructing approximately 20 fabs worldwide. In response to this situation, Unimicron has approved additional capital expenditure, concentrating approximately 80-85% on ABF substrates, and has significantly increased its pre-orders for critical equipment for the 2027-2028 period, aiming to address this critical bottleneck.

Technical & Clinical Details

The pursuit of higher performance in AI chips is driving revolutionary changes in substrate design. Compared to conventional chips, AI chips necessitate larger substrate areas, higher layer counts (typically 12 to over 18 layers), and finer wiring structures. This dramatically elevates the manufacturing difficulty of ABF substrates, making it extremely challenging to maintain high yields. ABF substrates are an indispensable component in AI packages that densely integrate GPUs and HBM (High Bandwidth Memory), enabling high-speed data transmission between the processor and memory.

Specifically, TGV (Through-Glass Via) technology is a key technique for forming minute electrical connections in glass substrates, which are gaining attention as a next-generation packaging material. However, the formation of TGVs and the uniform conductive coating of their inner walls (e.g., using TRUMPF's HiPIMS technology) require highly advanced technology and specialized equipment, with a limited number of suppliers. Small and medium-sized Japanese enterprises hold global leadership in these niche but critical technological fields, making their supply capacity a bottleneck for the entire AI-era semiconductor supply chain. Unimicron's capital investment is specifically aimed at addressing the increasing demand for AI chip ABF substrates, focusing on introducing new manufacturing technologies and expanding production capacity.

Background & Context

The explosive demand for AI is exerting unprecedented pressure on the entire semiconductor manufacturing supply chain, causing bottlenecks to sequentially shift from front-end processes to packaging, substrates, and materials. While the tight supply of TSMC's CoWoS (Chip-on-Wafer-on-Substrate) packaging has long been a concern, ABF substrates and HBM (High Bandwidth Memory) have now emerged as new primary bottlenecks. This situation is fundamentally reshaping the cooperative dynamics of the entire semiconductor industry, necessitating close collaboration among material suppliers, equipment manufacturers, foundries, and packaging companies. Governments worldwide, particularly through initiatives like the U.S. CHIPS Act, are supporting the strengthening of supply chain resilience and expanding domestic manufacturing capabilities.

Strategic Significance & Outlook

The supply-demand imbalance, as pointed out by Unimicron Chairman Chien Shan-Chieh, is highly likely to persist as AI chip evolution continues. The shortage of TGV technology and materials, especially those dependent on small and medium-sized Japanese enterprises, will directly impact the time-to-market for AI chips. Unimicron's aggressive capital investment and long-term equipment pre-orders represent a strategic move to alleviate this challenge and meet the substrate demands of the AI era. The expansion of AI computing is extending from advanced processes to packaging, substrates, and materials, fundamentally restructuring the cooperative dynamics of the entire semiconductor supply chain. Going forward, the commercialization of glass substrates and the introduction of new packaging materials will be key to stabilizing the supply chain and enhancing performance.

Source: https://finance.biggo.com/news/4ddf34c2-ffa8-4c6c-b885-494b082dc711

Collected: September 04, 2026 | Automated Research System (Gemini API)