Semiconductor_BackEnd

Weekly Intelligence Report

2026-09-13 ¦ 23 articles ¦ 9 countries

troy-technical.jp

This Week's Keyword

AI Packaging Surge

HBM, Substrates & Equipment Drive Growth

23	9	120,000	$1.1B
articles	countries	wafers/month	USD
Total Articles Analyzed	Source Countries	NVIDIA CoWoS Capacity	KLA AP Revenue (2026)

All 23 Articles This Week — 5-Axis Evaluation Matrix

How to read columns — Tech Novelty: degree of breakthrough Market Proximity: closeness to commercialization Market Impact: industry-wide effect Data Reliability: quantitative data & peer review US/EU Relevance: direct impact on US/European companies & supply chains

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#01	Samsung HBM Arch	New Product	●●●●	●●●○	●●●●	●●●●	●●●●	Samsung Foundry introduces 2.xD Cube packaging for next-gen HBM, boosting AI/HPC performance and efficiency.
#02	NVIDIA CoWoS Boost	Corporate Strategy	●●●○	●●●●	●●●●	●●●○	●●●●	NVIDIA plans 3.5x CoWoS capacity increase by end-2026 to secure HBM4 supply and advance CoWoP packaging.
#03	Scientech AP Equip	Market Report	●●●○	●●●○	●●●●	●●●○	●●●○	Scientech's advanced packaging equipment shipments surge 50% amid AI demand; TSMC's CoPoS mass production expected 2027.
#04	Samsung Japan R&D;	Corporate Strategy	●●○○	●●○○	●●●○	●●○○	●●●●	Samsung opens advanced packaging R&D; center in Yokohama to collaborate with Japanese suppliers on HBM development.
#05	Taiwan-Lithuania AP	Collaboration	●●●○	●●○○	●●●○	●●●○	●●●●	Taiwan and Lithuania ink € 5.6M MOU to jointly develop next-gen advanced packaging equipment, leveraging laser tech.
#06	Taiwan MOEA RDL	Research	●●●●	●●○○	●●●○	●●○○	●●●○	Taiwan's MOEA unveils Double-Sided RDL process for CoPoS packaging, improving interconnect density and yield.
#07	Samsung 3D Memory	Corporate Strategy	●●●●	●○○○	●●●●	●●○○	●●●●	Samsung reveals 3D-stacked memory roadmap (HBM5, zHBM, zNAND-O) to address AI-era memory bottlenecks.
#08	API Bonding Platf.	New Product	●●●○	●●●●	●●●○	●●○○	●●●○	API launches GEMINI PRO, NUERA PRO, and AP-M3500 bonding platforms to tackle next-gen semiconductor packaging challenges.
#09	Substrate Bottleneck	Market Overview	●●○○	●●●●	●●●●	●●●○	●●●●	Broadcom CEO highlights substrate bottleneck; Toppan's AST building FC-BGA plant in Singapore for 2026 production.
#10	SEM Next-Gen Substr	New Product	●●●○	●●●○	●●●●	●●○○	●●●○	Samsung Electro-Mechanics unveils five next-gen package substrates, including glass and automotive FCBGA, for AI, auto, mobile.
#11	Micron HBM Capacity	Corporate Strategy	●●●○	●●●●	●●●●	●●●○	●●●●	Micron aims to double HBM capacity to 100k wafers/month by end-2026, focusing on 12-high HBM4 for NVIDIA's Vera Rubin.
#12	Hybrid Bond Market	Market Report	●○○○	●●●●	●●●○	●●●●	●●●○	Hybrid bonding equipment market to hit $1.73B in 2026, growing to $2.58B by 2032, driven by AI and HBM.

#	Article Title	Type	Tech Novelty	Market Proximity	Market Impact	Data Reliability	US/EU Relevance	Summary
#13	Samsung 4nm HBM4	Corporate Strategy	●●●○	●●●●	●●●●	●●●○	●●●●	Samsung allocates over 50% of its 4nm foundry capacity (15k wafers/month) to HBM4 base die production.
#14	NXP Malaysia Cap.	Corporate Strategy	●●○○	●●●●	●●●○	●●○○	●●●●	NXP to more than double semiconductor back-end capacity in Malaysia, targeting automotive and industrial sectors.
#15	TRUMPF Glass TGV	Research	●●●●	●●○○	●●●●	●●○○	●●●●	TRUMPF's HiPIMS technology resolves glass substrate TGV coating bottleneck, accelerating next-gen AI chip packaging.
#16	ABF Substrate Short	Market Overview	●○○○	●●●●	●●●●	●●●○	●●●●	Critical shortage of high-end ABF substrates due to AI chip growth drives intense competition among Taiwanese suppliers.
#17	KLA AP Revenue	Corporate Report	●●○○	●●●●	●●●●	●●●●	●●●●	KLA's advanced packaging process control revenue to hit $1.1B in 2026, driven by AI/HPC and hybrid bonding.
#18	Onto AP Growth	Corporate Report	●●○○	●●●●	●●●●	●●●●	●●●●	Onto Innovation's advanced packaging business grew 80% in 2026, fueled by Dragonfly G5 for HBM4 and 2.5D AI.
#19	AMAT AP Growth	Corporate Report	●●○○	●●●●	●●●●	●●●●	●●●●	Applied Materials forecasts >70% advanced packaging revenue growth in 2026, driven by AI and HBM demand.
#20	SKorea AP Invest	Corporate Strategy	●●○○	●●●●	●●●●	●●●○	●●●●	South Korea accelerates advanced packaging investments, including SK Hynix's $3.87B US plant, solidifying AI supply chain.
#21	Taiyo-imec RDL	Research	●●●●	●●○○	●●●○	●●●●	●●●●	Taiyo Holdings and imec achieve 700nm 3-layer RDL on 12-inch wafers with new materials for advanced packaging.
#22	Laser Debonding	Technology Trend	●●●○	●●●○	●●●○	●●○○	●●●○	Laser debonding technology is becoming critical for improving thin wafer yield in HBM and hybrid bonding processes.
#23	Equip Invest Shift	Market Report	●○○○	●●●●	●●●●	●●●○	●●●●	Semiconductor equipment investment shifts to Korea and Taiwan, driving H1 2026 growth due to AI and HBM demand.

●●●○ High ●●●○○ Med-High ●●○○○ Med ●○○○○ Low ¦ Yellow highlight = featured article

Three Questions That Demand Your Decision This Week

❶ Is your AI/HPC product roadmap exposed to packaging bottlenecks?

NVIDIA, Micron, and Samsung are aggressively expanding CoWoS/HBM capacity and innovating packaging. Evaluate if your current or future AI/HPC platforms face supply risks or performance limitations due to packaging constraints. What is your strategy to secure advanced packaging capacity and HBM supply for 2027 and beyond?

❷ How will next-gen substrates and 3D memory architectures impact your designs?

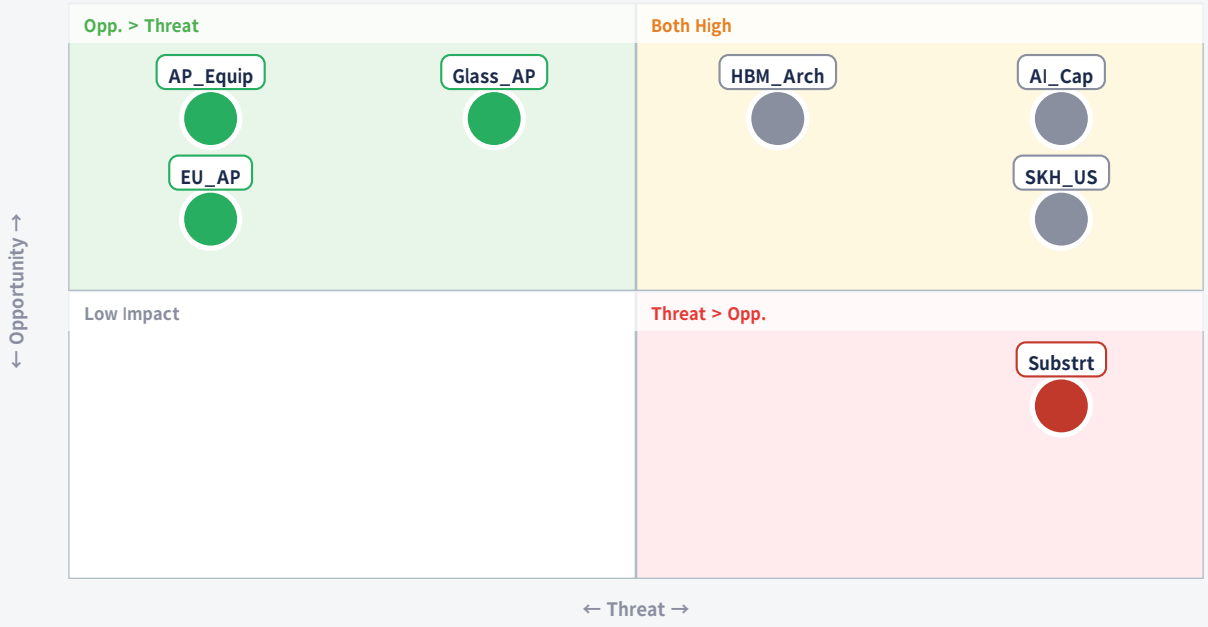
Glass substrates (TRUMPF) and advanced RDL (Taiyo/imec) are resolving critical bottlenecks, while Samsung is pushing HBM5, zHBM, and zNAND-O. Assess if your current material and design choices will be obsolete. Are you actively engaging with suppliers on these emerging technologies to integrate them into your future products?

❸ Are you leveraging geopolitical shifts to strengthen your supply chain?

South Korea is making massive advanced packaging investments, including SK Hynix's US plant, and Taiwan/Lithuania are collaborating on equipment. Analyze how these regional investments and collaborations impact your supply chain resilience and competitive positioning. Are you exploring new partnerships or domestic investments to de-risk and localize critical backend processes?

Opportunities vs. Threats for US/European Companies

Opportunity vs. Threat Matrix for US/European Companies



Item	Quadrant	↑ Opportunity	↓ Threat
AI_Cap	Critical	Secure HBM supply	Capacity race
HBM_Arch	Critical	New arch adoption	Tech obsolescence
SKH_US	Critical	US mfg base	Asian dominance
AP_Equip	Opp.	Equipment sales	Competition
Glass_AP	Opp.	New material enabler	Limited suppliers
EU_AP	Opp.	EU tech growth	Catch-up needed

Substrt	Threat	New suppliers	Supply chain risk

Deep Dive ① — TRUMPF's Glass Substrate TGV Breakthrough

#15 ¦ 2026/09/06 ¦ Asianews.network ¦ Tech Novelty●●●●○ Proximity●●○○○ Market Impact●●●●○ Data Reliability●●○○○ US/EU Relevance●●●●●

Germany's TRUMPF has resolved a critical bottleneck in Through Glass Via (TGV) coating for glass substrates using high-power HiPIMS technology. This breakthrough enables uniform, highly adhesive metallic film deposition deep within TGVs, significantly reducing electrical resistance and enhancing signal reliability.

This innovation is crucial for mass production of next-gen AI chip packaging, where glass substrates offer superior flatness, thermal stability, and electrical properties over silicon. It accelerates the adoption of multi-layer AI chip packaging with higher performance and energy efficiency.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The published numbers are qualitative but the technical challenge addressed is real and significant. [Opportunity] for US/EU materials & equipment suppliers to partner with TRUMPF or develop complementary solutions for glass substrates. For OEMs, this enables next-gen AI chip designs. [Threat] for companies relying on traditional substrate materials or without advanced TGV coating capabilities, as glass substrates become viable. Technical barriers include scaling HiPIMS for high-volume manufacturing and integrating glass substrates into existing fab lines. Next actions: [R&D;] Evaluate HiPIMS for other advanced packaging processes by end-Q4 2026. [Business Dev] Explore partnerships with TRUMPF and glass substrate manufacturers by end-Q4 2026.

Deep Dive ② — SK Hynix's US Advanced Packaging Investment

#20 ¦ 2026/09/04 ¦ Investment Monitor ¦ Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●● Data Reliability●●●○○ US/EU Relevance●●●●●

SK Hynix is investing $3.87 billion in a new HBM advanced packaging facility in Indiana, USA, alongside a ₩19 trillion ($12.9 billion) plant in South Korea. This massive investment aims to meet surging AI semiconductor export demand and solidify South Korea's role as a global hub for HBM manufacturing and advanced packaging.

This move, coupled with U.S. firms pledging $2 billion in South Korea's chip sector, reinforces the U.S.-South Korea alliance and diversifies the global semiconductor supply chain. It addresses critical packaging bottlenecks for AI chips, which have historically constrained production.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: The investment figures are concrete and realistic, reflecting the strategic importance of advanced packaging. [Opportunity] for US materials & equipment suppliers to support SK Hynix's Indiana facility, and for US OEMs to benefit from localized HBM packaging. [Threat] for EU companies if they do not establish similar strategic partnerships or domestic advanced packaging capabilities, potentially increasing reliance on Asian supply chains. Technical barriers include workforce development and rapid technology transfer to the new US facility. Next actions: [Procurement] Identify opportunities to supply SK Hynix's Indiana plant by end-Q4 2026. [Strategy] Assess implications of US-Korea supply chain strengthening on EU competitiveness by end-Q1 2027.

Deep Dive ③ — Samsung's 3D-Stacked Memory Roadmap

#07 ¦ 2026/09/03 ¦ Design And Reuse ¦ Tech Novelty●●●●● Proximity●○○○○ Market Impact●●●●● Data Reliability●●○○○ US/EU Relevance●●●●○

Samsung Electronics unveiled an ambitious 3D-stacked memory strategy at SEMICON Taiwan, including HBM5, zHBM (new interface), and zNAND-O (NAND with computing functions). This roadmap aims to overcome AI-era memory limits by vertically stacking memory and computing devices to boost bandwidth, capacity, and power efficiency.

This approach fundamentally addresses the 'memory wall' problem, crucial for large language models and generative AI. zNAND-O, in particular, integrates processing closer to memory, eliminating data movement bottlenecks for edge and data center AI.

▶ Strategic Analyst's Perspective

Strategic Analyst's Perspective: This is a highly ambitious roadmap, pushing the boundaries of memory architecture. The concepts (zHBM, zNAND-O) represent academic breakthroughs, but commercialization is 5+ years away. [Opportunity] for US/EU IP holders and technology licensors to develop complementary IP for new memory interfaces or processing-in-memory architectures. For OEMs, this signals future design paradigms. [Threat] for existing memory providers and system architects if they fail to innovate beyond current HBM standards. Technical barriers include yield, thermal management, and standardization of new interfaces. Next actions: [R&D;] Initiate exploratory research into zHBM/zNAND-O concepts and potential integration challenges by Q1 2027. [Strategy] Begin long-term scenario planning for memory architecture shifts by mid-2027.

Other Notable Articles

NVIDIA to Boost CoWoS Production Capacity by 3.5x to Over 120,000 Wafers/Month by End-2026, Securing HBM4 Supply (SemiconductorX)
Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●●

NVIDIA's massive CoWoS expansion and CoWoP development are critical for AI GPU supply and future packaging tech.

Broadcom CEO Warns of Substrate Bottleneck for High-End Chips; Toppan Subsidiary AST to Build FC-BGA Plant in Singapore (業界メディア)
Tech Novelty●●○○○ Proximity●●●●○ Market Impact●●●●●

Substrate shortage is a new critical bottleneck for high-end chips; Toppan's Singapore plant aims to alleviate this by end-2026.

Micron Reportedly Targets Doubling HBM Capacity to 100,000 Wafers/Month by End-2026, Boosting 12-High HBM4 for NVIDIA Vera Rubin (digitimes)
Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●●

Micron's aggressive HBM capacity expansion for NVIDIA's next-gen AI platform intensifies market competition.

Samsung Allots Over 50% of 4nm Foundry Capacity to HBM4 Base Die Production, Totaling 15,000 Wafers Per Month (ZDNet Korea (Wccftechによる引用))
Tech Novelty●●●○○ Proximity●●●●○ Market Impact●●●●●

Samsung dedicating half its 4nm capacity to HBM4 base dies highlights the strategic importance and demand for HBM.

Recommended Actions This Week

Action recommendations based on article evaluation matrix and opportunity/threat analysis.

Immediate (this week)

- [Procurement] Conduct an urgent audit of HBM and advanced substrate supply contracts for 2027, identifying potential exposure to capacity bottlenecks and single-source risks.
- [Strategy] Initiate a competitive intelligence brief on Samsung's 2.xD Cube and 3D-stacked memory roadmap to understand potential impacts on future product competitiveness.
- [Executive] Review current advanced packaging investment strategies in light of major capacity expansions by NVIDIA, Micron, and SK Hynix, especially regarding US-based facilities.

Short-term (1 month)

- [R&D;] Task a cross-functional team to evaluate the technical feasibility and integration challenges of glass substrates and advanced RDL technologies for next-generation designs.
- [Business Dev] Explore partnership opportunities with European advanced packaging equipment and materials suppliers (e.g., TRUMPF, imec) to leverage regional innovation and diversify supply.
- [Legal/IP] Assess the intellectual property landscape around next-gen HBM architectures (zHBM, zNAND-O) to identify potential licensing opportunities or infringement risks.

Medium-long term (quarter+)

- [Strategy] Develop a multi-year roadmap for advanced packaging technology adoption, including investments in internal capabilities or strategic acquisitions to secure critical expertise.
- [Procurement] Establish long-term agreements with diversified suppliers for advanced packaging equipment and materials, including those in emerging regional hubs like Southeast Asia.
- [R&D;] Fund exploratory research into novel memory-computing architectures and advanced interconnect technologies to stay ahead of the 'memory wall' and maintain technological leadership.

troy-technical.jp/en ¦ Original curation. Article copyrights belong to respective authors. ¦ Gemini API + Claude ¦ 2026-09-13

Semiconductor_BackEnd — Selected Articles

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#16 High-End ABF Substrate Supply Faces Critical Shortage Amid Gigantic AI Chip Growth, Fueling Intense Competition Among Taiwanese Manufacturers

#17 KLA Achieves $1.1 Billion in Advanced Packaging Process Control Revenue, Driven by Surging AI Chip Demand

#18 Onto Innovation's Advanced Packaging Business Achieves 80% Growth, Driven by Dragonfly G5 for HBM4 and 2.5D AI

#19 Applied Materials Forecasts Over 70% Growth in Advanced Packaging Revenue, Total Revenue Up 40%, Driven by AI and HBM Demand

#20 South Korea Accelerates Advanced Packaging Investments, Establishing Itself as Core of Global AI Semiconductor Supply Chain

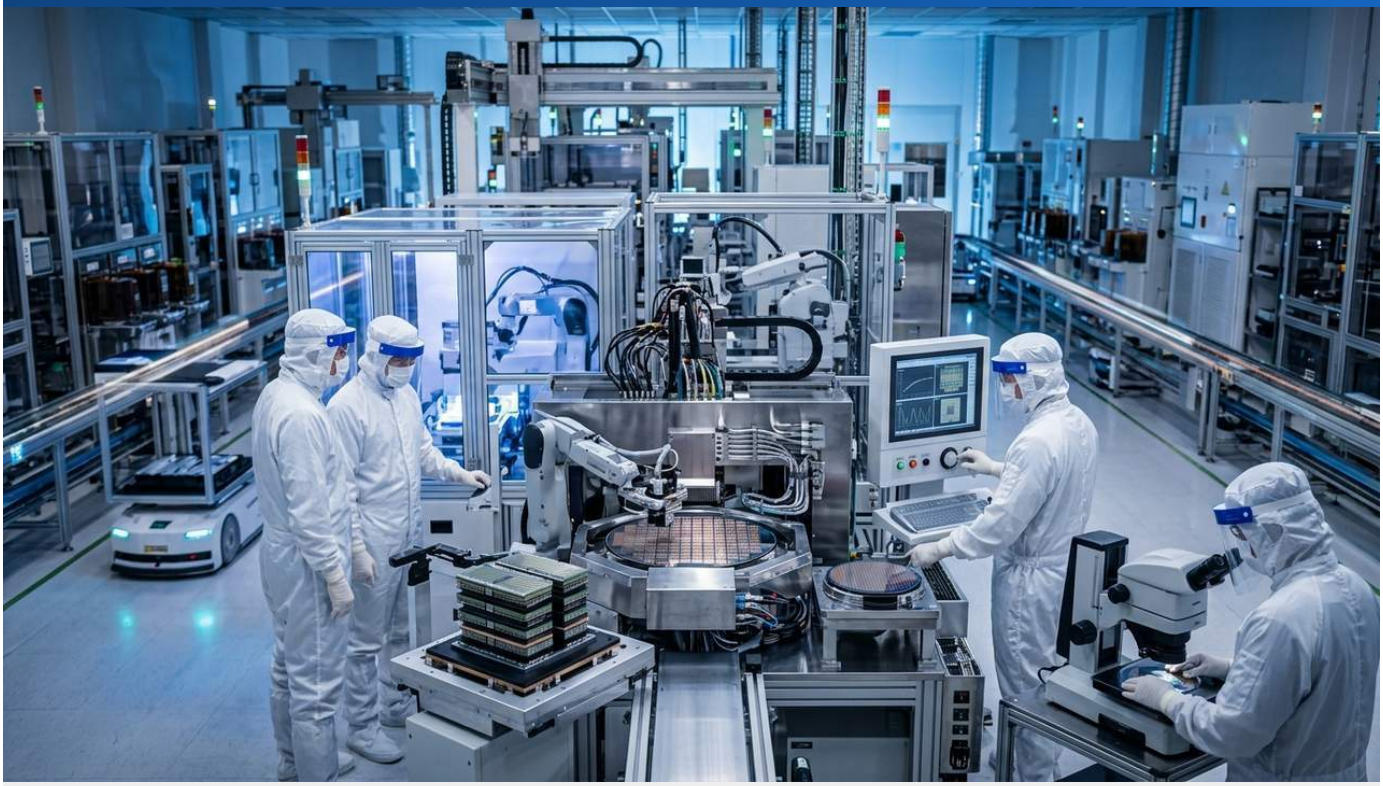
#21 Taiyo Holdings, in Collaboration with imec, Successfully Forms 700nm Precision 3-Layer RDL on 12-inch Wafers

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#23 Semiconductor Equipment Investment Shifts to Korea and Taiwan, Driving Growth in H1 2026

#01 Samsung Foundry Unveils Next-Gen HBM Architecture Leveraging Advanced Packaging for AI/HPC Performance

Published September 04, 2026 Samsung Foundry South Korea



OVERVIEW

Samsung Foundry announced a new HBM architecture that combines advanced logic nodes with advanced packaging, promising significantly higher bandwidth and energy efficiency for AI and HPC systems. Its 2.xD Cube packaging platform integrates multiple chips into a single package, improving bandwidth, latency, and power efficiency. This strategic shift aims to accelerate system-level semiconductor innovation, addressing the growing demands of data-intensive applications.

IN DEPTH

Key Findings: Samsung Revolutionizes AI/HPC Performance with Advanced Packaging

Samsung Foundry has revealed a new strategy for AI and High-Performance Computing (HPC) systems, combining next-generation High Bandwidth Memory (HBM) architectures with advanced packaging technologies to dramatically boost data throughput and energy efficiency. This initiative aims to transcend traditional chip design limitations and accelerate system-level semiconductor innovation.

Technical Details: Fusion of 2.xD Cube and Advanced Logic Nodes

- **2.xD Cube Packaging:** Samsung's 2.xD Cube packaging is an innovative technology that integrates multiple disparate chips (e.g., logic, memory) into a single package. This approach significantly shortens data transfer distances between chips, leading to substantial improvements in bandwidth, reduced latency, and enhanced overall power efficiency.
- **Leveraging Advanced Logic Nodes:** The next-generation HBM architecture incorporates state-of-the-art logic node technology into the HBM base die. This enhances the HBM module's inherent processing capabilities and intelligence, mitigating bottlenecks between HBM and the main processor.
- **AI/HPC Optimization:** These technologies are specifically designed to maximize system performance for AI training, inference, and other large-scale data processing required by HPC applications, providing a robust foundation for future computational demands.

Background & Context: The Imperative for System-Level Innovation

The rapid evolution of AI and HPC has exposed critical challenges in traditional semiconductor design, particularly concerning data volume and power consumption. With the slowing pace of Moore's Law, advanced packaging techniques that efficiently integrate multiple chips are becoming crucial for future semiconductor performance gains. Samsung's strategy underscores a growing industry trend towards optimizing entire systems rather than just individual components.

Strategic Significance & Outlook: Impact on the Semiconductor Ecosystem

This technological breakthrough is poised to significantly influence the design of next-generation AI accelerators and data center infrastructure. Samsung Foundry aims to empower its customers to build more powerful and energy-efficient AI/HPC systems through this packaging technology, thereby strengthening its competitive position in the foundry market. This move is likely to spur other industry players to accelerate their own system-level packaging approaches, fostering widespread innovation across the entire semiconductor ecosystem.

Source: https://semiconductor.samsung.com/news-events/tech-blog/advanced-packaging-and-the-shift-to-system-level-semiconductor-innovation/

Collected: September 11, 2026 | Automated Research System (Gemini API)

#02 NVIDIA to Boost CoWoS Production Capacity by 3.5x to Over 120,000 Wafers/Month by End-2026, Securing HBM4 Supply

Published September 04, 2026 SemiconductorX USA



OVERVIEW

NVIDIA plans to scale its CoWoS (Chip-on-Wafer-on-Substrate) production capacity by 3.5x to 120,000–130,000 wafers per month by the end of 2026, up from 35,000, driven largely by its own demand. The company is set to consume approximately 60% of TSMC's total CoWoS allocation in 2026, with HBM4 supplied by SK Hynix (70%) and Samsung (30%). Furthermore, NVIDIA is co-developing CoWoP (Chip on Wafer on PCB) with SPIL to eliminate substrate layers, aiming for improved efficiency and cost reduction in AI semiconductor supply chains.

IN DEPTH

Key Findings: NVIDIA Massively Expands CoWoS Capacity and Solidifies HBM4 Supply Chain

NVIDIA is aggressively pursuing a plan to expand its CoWoS (Chip-on-Wafer-on-Substrate) packaging production capacity by approximately 3.5 times, from its current 35,000 wafers per month to 120,000–130,000 wafers per month by the end of 2026. This monumental expansion is predominantly driven by NVIDIA's own escalating demand for AI GPUs, underscoring a critical strategy to stabilize the supply of HBM4 memory and GPUs essential for its next-generation AI platforms.

Technical & Supply Chain Details: CoWoS Allocation and HBM4 Supplier Strategy

- **Dramatic CoWoS Capacity Increase:** NVIDIA is projected to consume roughly 60% of TSMC's total CoWoS production capacity in 2026, a testament to its dominant position in the AI chip market. This significant scale-up is expected to alleviate the packaging bottleneck that has historically constrained AI accelerator production.
- **Diversified HBM4 Supply:** To ensure a robust and stable supply of high-bandwidth memory (HBM4), NVIDIA will source approximately 70% from SK Hynix and 30% from Samsung. This diversified approach mitigates the risk of over-reliance on a single supplier.
- **CoWoP Technology Development:** In collaboration with SPIL (part of the ASE Group), NVIDIA is advancing a novel packaging technology known as CoWoP (Chip on Wafer on PCB). This innovation aims to eliminate the intermediate substrate layer used in traditional CoWoS, potentially reducing packaging complexity, lowering costs, decreasing latency, and enabling further miniaturization.

Background & Industry Context: AI Demand and Supply Chain Pressure

The proliferation and sophistication of AI models have driven an unprecedented demand for high-performance GPUs, along with their associated HBM and advanced packaging technologies. Specifically, 2.5D packaging solutions like CoWoS are indispensable for integrating GPUs and HBM, and their limited production capacity has long been a bottleneck for AI chip supply. NVIDIA's announcement signifies a proactive strategic investment to address this bottleneck and accommodate future market growth.

Strategic Significance & Outlook: Intensifying AI Semiconductor Competition and NVIDIA's Lead

NVIDIA's substantial increase in CoWoS capacity and investment in innovative packaging technologies like CoWoP will further solidify its competitive advantage in the AI semiconductor market. The ability to rapidly bring more AI GPUs to market could widen its lead over rivals. Should CoWoP technology achieve practical implementation, it promises reductions in packaging costs and performance enhancements, profoundly impacting the overall economics of AI hardware.

Source: https://semiconductorx.com/spotlight-nvidia.html

#03 Scientech Sees 50% Surge in Advanced Packaging Equipment Shipments Driven by AI Demand; TSMC's CoPoS Production Set for 2027 Launch

Published September 03, 2026 Taipei Times Taiwan



OVERVIEW

Scientech Corp, a supplier of advanced packaging equipment and reclaimed wafers, anticipates a 50% year-on-year increase in shipments for 2026, fueled by robust AI application demand and rapid technological shifts. Its production lines are fully booked through year-end, with growth expected to continue into 2027. Scientech also noted TSMC is building a pilot line for CoPoS packaging, projecting mass production to commence in another year.

IN DEPTH

Key Findings: Scientech Achieves 50% Surge in Advanced Packaging Equipment Shipments; TSMC CoPoS Mass Production Expected Post-2027

Scientech Corp, a Taiwanese supplier of advanced packaging equipment and reclaimed wafers, announced an expected 50% year-on-year increase in equipment shipments for 2026. This growth is driven by robust demand from AI applications and rapid technological transitions in the semiconductor industry. The company's production lines are operating at full capacity through the end of the year, with sustained growth projected into 2027. This highlights the current high demand and future prospects in the advanced packaging market.

Technical & Market Details: CoPoS Packaging Status and Scientech's Contribution

- **Surging Shipments:** Scientech's advanced packaging equipment is critical for enabling heterogeneous integration and 3D stacking technologies, which are essential for enhancing AI chip performance. The 50% increase in shipments indicates a healthy expansion across the entire semiconductor back-end market.
- **TSMC CoPoS Development:** Scientech referenced that TSMC, a leader in the semiconductor industry, is currently constructing a pilot line for CoPoS (Chip-on-Package-on-Substrate) packaging. This technology aims to enable more advanced chip integration, with mass production anticipated to take another year. This suggests that cutting-edge packaging technologies are still in the development and optimization phases.
- **Reclaimed Wafer Business:** The company also provides reclaimed wafers, a crucial business that contributes to cost reduction and environmental footprint minimization in semiconductor manufacturing processes.

Background & Industry Context: AI Revolution Driving Back-End Investment

The rapid advancements in AI, HPC, and autonomous driving necessitate increasingly powerful and energy-efficient chips. Meeting these requirements demands not only conventional miniaturization but also advanced back-end technologies such as chiplet integration and 2.5D/3D packaging. Semiconductor manufacturers worldwide are making significant investments in packaging capabilities to meet this demand, and equipment suppliers like Scientech are major beneficiaries.

Strategic Significance & Outlook: Sustained Growth and Technical Challenges

Scientech's strong performance reflects the robust growth trend in the advanced packaging market, which is expected to continue its momentum in the coming years. TSMC's CoPoS like next-generation technologies, once mass-produced, will further generate new demand. However, the complexity of new packaging technologies presents technical challenges such as stabilizing mass production yields and optimizing costs. Scientech aims to maintain its market leadership by providing equipment and solutions that address these evolving challenges.

Source: https://www.taipeitimes.com/News/biz/archives/2026/09/04/2003863637

Collected: September 11, 2026 | Automated Research System (Gemini API)

#04 Samsung Electronics Establishes Advanced Packaging R&D Center in Yokohama to Deepen Collaboration with Japanese Suppliers for HBM Technologies

Published September 09, 2026 digitimes South Korea



OVERVIEW

Samsung Electronics has opened an advanced packaging research center in Yokohama, Japan, to strengthen development cooperation with Japanese suppliers of critical materials and equipment for HBM. This strategic move aims to narrow the market share gap with competitor SK Hynix in the HBM market and establish technological superiority. Samsung plans to leverage Japan's high-tech capabilities and robust supply chain to accelerate next-generation HBM development.

IN DEPTH

Key Findings: Samsung Electronics Boosts HBM Competitiveness with Advanced Packaging R&D Center in Yokohama

Samsung Electronics has established a state-of-the-art advanced packaging research center in Yokohama, Japan, in a strategic move to bolster its competitiveness in High Bandwidth Memory (HBM) technology. The new center is designed to foster closer collaboration and accelerate joint development with leading Japanese suppliers of high-performance materials and precision equipment essential for HBM manufacturing. This strategic facility is crucial for Samsung's efforts to narrow the technological and market share gap with SK Hynix, a key competitor in the HBM market.

Technical & Strategic Details: Synergy with Japanese Materials and Equipment Technology

- **Strategic Location:** Yokohama's proximity to major Japanese R&D hubs, where world-class semiconductor material and equipment manufacturers are concentrated, allows Samsung to rapidly develop and implement the latest packaging technologies through direct collaboration with these companies.
- **Accelerating HBM Development:** HBM is a next-generation memory technology that offers significantly higher data bandwidth than conventional DRAM, essential for demanding applications in AI, HPC, and data centers. Packaging technology is a critical factor determining HBM performance and yield, making innovation in this area indispensable.
- **Competition with SK Hynix:** SK Hynix is considered a leader in the HBM market. Through this research center, Samsung aims to catch up, particularly in the development of HBM3e and next-generation HBM4, by integrating Japanese expertise and technology.

Background & Industry Context: Semiconductor Supply Chain Realignment and Japan's Role

Recent geopolitical risks and intensifying technological competition have prompted a realignment of the semiconductor supply chain. Advanced packaging, in particular, has seen its importance skyrocket with the evolution of chiplet technology and 3D stacking. Japan possesses world-leading technologies in semiconductor materials and equipment, such as photoresists, high-purity gases, and precision manufacturing tools, playing an indispensable role in advanced packaging innovation.

Strategic Significance & Outlook: Global Technological Collaboration and Market Impact

Samsung Electronics' establishment of an R&D center in Japan exemplifies the growing importance of global technological collaboration and is expected to contribute to further advancements in HBM technology. This move also creates new business opportunities for Japanese suppliers and could deepen collaboration within the semiconductor ecosystems of both Japan and South Korea. Accelerated improvements in next-generation HBM performance are anticipated to further drive innovation in the AI and HPC sectors, impacting the entire industry significantly.

Source: https://www.digitimes.com/news/a20260909VL200.html

Collected: September 11, 2026 | Automated Research System (Gemini API)

#05 Taiwan and Lithuania Ink €5.6 Million MOU for Joint Development of Next-Gen Advanced Packaging Technologies

Published September 04, 2026 CNA / Taiwan News Taiwan



OVERVIEW

Taiwan and Lithuania have signed an MOU for joint development of advanced packaging equipment for next-generation chips, backed by €5.6 million (NT$205 million) in government funding over two years. This partnership aims to integrate Lithuania's laser technology with Taiwan's strengths in digital imaging, precision scanning, and AI. The collaboration seeks to combine each nation's semiconductor expertise to accelerate innovation in back-end processes and foster private sector cooperation.

IN DEPTH

Key Findings: Taiwan and Lithuania Collaborate on Next-Gen Advanced Packaging with €5.6 Million Joint Development MOU

Taiwan and Lithuania have officially signed a Memorandum of Understanding (MOU) aimed at jointly developing advanced packaging equipment for next-generation chips. This strategic alliance seeks to integrate the strengths of both nations to accelerate technological innovation in the critical back-end sector of the semiconductor industry. Over a two-year period, a total of €5.6 million (approximately NT$205 million) in government funding will be allocated to support the joint projects.

Technical & Strategic Details: Integrating Laser Technology and Digital Imaging

- **Focus of Technology Integration:** The MOU specifically targets combining Lithuania's globally recognized high-power and energy-efficient laser source technologies with Taiwan's expertise in digital laser imaging, AI control, and high-precision scanning modules. The goal is to develop equipment necessary for next-generation precision packaging processes.
- **Government-Led Funding:** The €5.6 million government funding will facilitate cooperation between private companies and research institutions in both countries through international seminars, academic and industrial exchanges, and technology matching programs. This demonstrates a strong national commitment to advancing semiconductor technology.
- **Requirements for Next-Gen Chips:** Advanced packaging is crucial for integrating chiplets, 2.5D/3D stacking, and utilizing new materials like glass substrates. These technologies enable performance enhancements for cutting-edge applications such as AI, HPC, and autonomous driving.

Background & Industry Context: Diversifying Semiconductor Supply Chains and Europe's Strategy

Amid rising geopolitical tensions and concerns over global supply chain vulnerabilities, many countries are striving to strengthen and diversify their semiconductor production capabilities. Taiwan is a global hub for semiconductor manufacturing, while Lithuania is a significant player in photonics and laser technology within Europe. This partnership aligns with the spirit of the European Union's (EU) Chips Act, potentially contributing to the strengthening of Europe's semiconductor ecosystem.

Strategic Significance & Outlook: Accelerating Innovation and Strengthening International Competitiveness

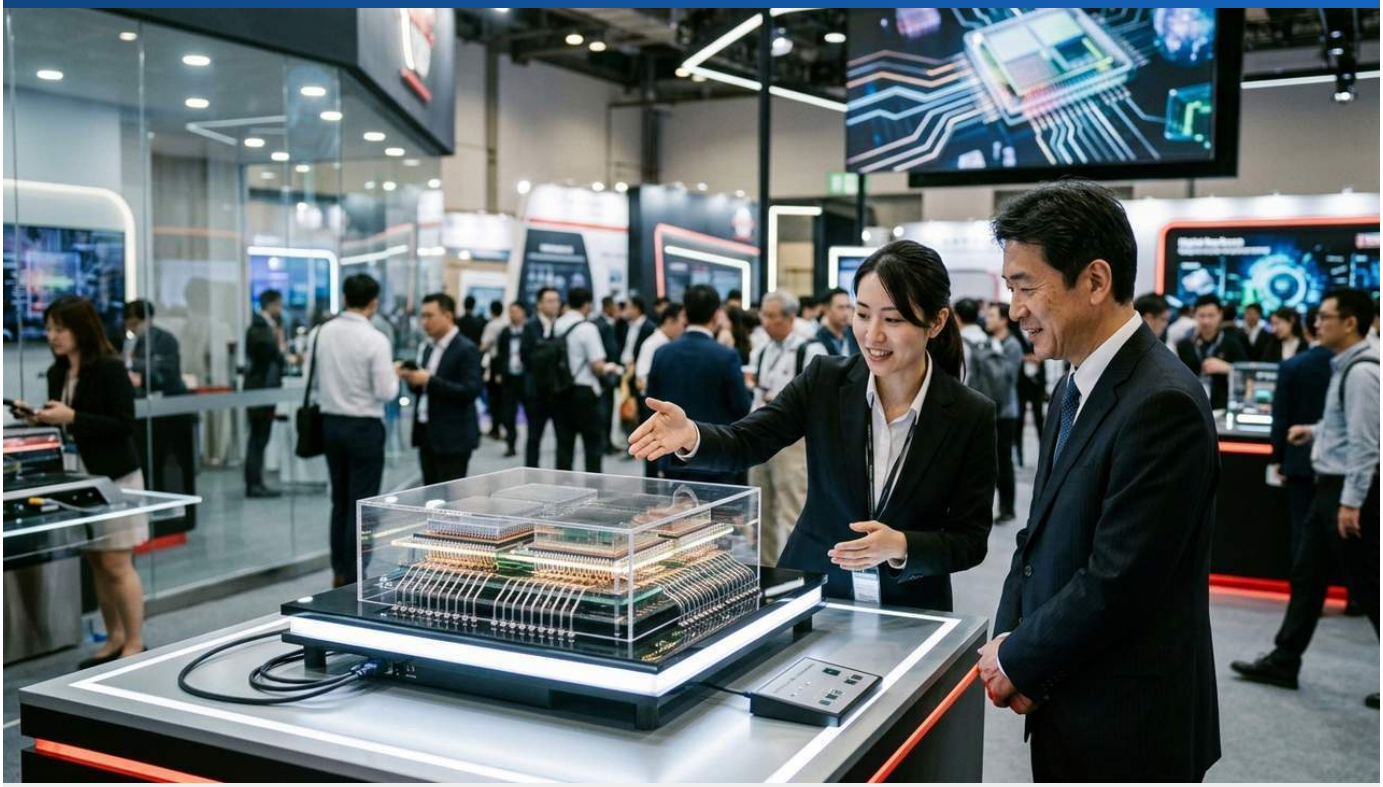
The collaboration between Taiwan and Lithuania represents a potent opportunity to accelerate technological innovation in advanced packaging and enhance the international competitiveness of both nations. Precision processing technologies, particularly those based on lasers, are key to next-generation packaging. If this joint development succeeds, it could introduce new solutions to the global semiconductor back-end market. This is expected to lead to more powerful and efficient AI chips and HPC systems, creating ripple effects across a wide range of industries.

Source: https://focustaiwan.tw/business/202609040012

Collected: September 11, 2026 | Automated Research System (Gemini API)

#06 Taiwan's MOEA Unveils 29 Cutting-Edge Semiconductor Innovations, Including Double-Sided RDL Process for CoPoS Packaging at SEMICON Taiwan 2026

Published September 03, 2026 Ministry of Economic Affairs (MOEA) Taiwan



OVERVIEW

Taiwan's Ministry of Economic Affairs (MOEA) showcased 29 cutting-edge technology innovations at SEMICON Taiwan 2026, encompassing advanced packaging, AI data center power management, and semiconductor testing/manufacturing equipment. Notably, the "Double-Sided RDL Key Process Integration Technology" for CoPoS applications garnered significant attention. This technology enables more precise alignment and stacking of wiring layers, enhancing package design flexibility and manufacturing yield, and is key for next-generation chip fabrication in global supply chains.

IN DEPTH

Key Findings: Taiwan's MOEA Reveals 29 Advanced Semiconductor Technologies, Including Double-Sided RDL for CoPoS

Taiwan's Ministry of Economic Affairs (MOEA) unveiled 29 groundbreaking technological innovations at the SEMICON Taiwan 2026 Technology Pavilion, covering advanced packaging, AI data center power management, and semiconductor testing and manufacturing equipment. These technologies are designed to address challenges in next-generation semiconductor manufacturing and reinforce global supply chains. Particular attention was drawn to the "Double-Sided RDL Key Process Integration Technology" tailored for CoPoS (Chip-on-Package-on-Substrate) applications.

Technical Details: Advancements in Double-Sided RDL and CoPoS Packaging

- **Benefits of Double-Sided RDL Technology:** This novel double-sided Re-Distribution Layer (RDL) process integration technology forms fine wiring layers on both sides of the package substrate, significantly enhancing the interconnect density between chips and the substrate. This enables more complex circuit designs, increases package design flexibility, and meets the demands of high-performance chips.
- **Precision Alignment and Stacking:** The technology allows for highly precise alignment and stacking of wiring layers, especially critical for multi-layer advanced package structures. This contributes to improved manufacturing yield and the mass production of reliable, high-performance chips.
- **Application to CoPoS Packaging:** CoPoS, when combined with chiplet and 3D stacking technologies, offers a packaging solution with extremely high integration and performance for AI and HPC applications. The technology presented by MOEA aims to further boost the performance and productivity of CoPoS packaging.

Background & Industry Context: Rising Strategic Importance of Semiconductor Back-End

With the advancements in AI, HPC, and 5G, semiconductor performance improvements can no longer solely rely on miniaturization. Advanced packaging technologies such as chiplet integration and 3D stacking – collectively known as "semiconductor back-end processes" – have become critical in determining overall chip performance, power efficiency, and cost. Taiwan's MOEA recognizes this industry trend and is promoting investment and innovation in advanced packaging technologies as a national strategy.

Strategic Significance & Outlook: Contribution to Global Supply Chains and Market Competitiveness

These technological innovations announced by the MOEA are essential for Taiwan's semiconductor industry to maintain its leading role in the global supply chain. Specifically, the double-sided RDL technology for CoPoS could be a significant breakthrough in the development and manufacturing of next-generation AI chips and data center semiconductors. This is expected to further strengthen Taiwan's technological advantage in advanced packaging and enhance its competitiveness in the global semiconductor market.

Source: #

#07 Samsung Electronics Unveils 3D-Stacked Memory Strategy Including HBM5, zHBM, and zNAND-O at SEMICON Taiwan, Tackling AI-Era Memory Limits

Published Published September 03, 2026　Design And Reuse (thelec.netからの情報)　South Korea



OVERVIEW

At SEMICON Taiwan 2026, Samsung Electronics presented a bold 3D-stacked memory strategy designed to overcome the limitations of current memory architectures in the AI era. This roadmap introduces HBM5, zHBM with an innovative interface, and zNAND-O for processing-in-memory, all leveraging vertical integration to dramatically increase bandwidth, capacity, and power efficiency crucial for next-generation AI and high-performance computing workloads.

IN DEPTH

Background

The relentless evolution of artificial intelligence, particularly the proliferation of Large Language Models (LLMs) and generative AI, has precipitated an unprecedented demand for memory systems capable of processing colossal datasets at blistering speeds. Traditional memory designs, however, frequently encounter the 'memory wall' – a critical bottleneck where the data transfer rate between the processor and memory severely limits overall system performance. This fundamental architectural challenge hinders the scalability and efficiency required for advanced AI applications, necessitating a radical rethinking of memory technology.

Key Findings

In response to these pressing challenges, Samsung Electronics unveiled a comprehensive 3D-stacked memory strategy at the Memory Executive Summit during SEMICON Taiwan 2026. This ambitious roadmap is engineered to revolutionize memory bandwidth, capacity, and power efficiency through advanced vertical integration techniques.

At its core, Samsung's strategy revolves around a **vertical stacking architecture** that integrates memory chips directly with computing devices. This innovative approach achieves a substantial increase in memory capacity without expanding the horizontal footprint, a crucial advantage in compact, high-density systems. Furthermore, vertical stacking dramatically **reduces data transfer distances** between chips, thereby accelerating data transfer speeds, minimizing latency, maximizing effective data bandwidth, and significantly cutting power consumption – all paramount considerations for high-performance computing environments.

The strategy introduces three cornerstone technologies:

- **HBM5:** Positioned as the successor to current High Bandwidth Memory (HBM) standards, HBM5 promises even higher stack configurations and significantly greater bandwidth, pushing the boundaries of data throughput.
- **zHBM:** This variant of HBM technology differentiates itself with a novel, more efficient, and faster interface, diverging from conventional HBM interfaces to further optimize data flow and system integration.

- **zNAND-O:** A groundbreaking technology that integrates NAND flash memory with specific computing functionalities. By enabling data processing closer to the memory layer, zNAND-O aims to eliminate notorious data movement bottlenecks and improve overall power efficiency, making it particularly vital for both edge AI and data center applications.

This strategic move is expected to intensify competition within the fiercely contested HBM market. The successful commercialization of these 3D stacking technologies holds the potential to deliver transformative performance gains and power efficiency improvements across a broad spectrum of demanding applications, including AI accelerators, high-performance computing (HPC), advanced data centers, and sophisticated edge AI devices. Samsung's roadmap represents a pivotal paradigm shift for the entire semiconductor industry, laying down a critical foundation for the next generation of computing architectures.

Source: Unknown

Collected: September 11, 2026 | Automated Research System (Gemini API)

#08 API Unveils GEMINI PRO, NUERA PRO, and AP-M3500 Bonding Platforms for Next-Gen Semiconductors at SEMICON Taiwan 2026, Addressing Key Packaging Bottlenecks

Published September 05, 2026 API (Advanced Packaging Intelligence) Unknown



OVERVIEW

API (Advanced Packaging Intelligence) reported a successful exhibition of next-generation advanced packaging technologies at SEMICON Taiwan 2026. Their GEMINI PRO, NUERA PRO, and AP-M3500 in-line bonding platforms, addressing heterogeneous bonding, warpage control, and AMHS fab integration, garnered strong international customer interest. These solutions are critical for overcoming packaging bottlenecks and enabling high-performance, efficient manufacturing of semiconductors for AI and HPC.

IN DEPTH

Key Findings: API Showcases High-Performance Bonding Platforms at SEMICON Taiwan 2026, Receiving Strong International Acclaim

Following the conclusion of SEMICON Taiwan 2026, API (Advanced Packaging Intelligence) announced a significant success in showcasing its advanced packaging solutions designed to support next-generation semiconductor manufacturing. The company's featured in-line bonding platforms—GEMINI PRO, NUERA PRO, and AP-M3500—address critical challenges in advanced packaging, including heterogeneous bonding, package warpage control, and AMHS (Automated Material Handling System) fab integration. These innovations attracted substantial interest from international customers.

Technical Details: Addressing Major Packaging Bottlenecks

- **GEMINI PRO Platform:** This platform delivers high-precision die bonding and high-efficiency throughput, meeting the demands of complex heterogeneous integration. It enables the high-density integration of chips with different functionalities into a single package.
- **NUERA PRO Platform:** Features technology designed to effectively control warpage, a significant issue particularly with large substrates and thinned packages. Warpage control is crucial as it directly impacts bonding accuracy and final product yield.
- **AP-M3500 In-line Bonding Platform:** Offers high-speed and high-precision bonding processes seamlessly integrated with automated material handling systems (AMHS) in semiconductor fabrication lines. This significantly enhances overall fab production efficiency and data management.
- **Key Challenges Addressed:** The exhibition highlighted how these products provide effective solutions for technical bottlenecks in next-generation packaging, such as fine-pitch interconnects, thermal management, and power delivery.

Background & Industry Context: Indispensability of Advanced Packaging in the AI Era

The increasing demand for high-performance computing in areas like AI, HPC, and 5G communications presents new challenges for semiconductor chip design and manufacturing. Traditional single-chip performance scaling is reaching its limits, making advanced technologies such as heterogeneous integration (combining multiple chiplets) and 2.5D/3D packaging indispensable. The realization of these technologies critically depends on high-precision bonding equipment and robust quality/productivity management throughout the manufacturing process, elevating the role of equipment suppliers like API.

Strategic Significance & Outlook: Contributing to Semiconductor Industry Efficiency and Performance

API's advanced bonding solutions directly contribute to the efficiency of semiconductor manufacturing processes and the next-generation chips performance improvement. The strong international customer interest demonstrates that these technologies are addressing urgent market needs, suggesting potential for API to expand its market share and contribute to industry standardization. As the AI era progresses, the demand for more complex and sophisticated packaging solutions is expected to grow, positioning API as a key player in this evolving landscape.

Source: https://www.sgapi.com/news/33

#09 Broadcom CEO Warns of Substrate Bottleneck for High-End Chips; Toppan Subsidiary AST to Build FC-BGA Plant in Singapore

Published Published September 04, 2026　業界メディア　Global



OVERVIEW

Broadcom CEO Hock Tan has identified advanced packaging substrates as a critical new bottleneck for high-end chip production, particularly for demanding AI accelerators and network processors, alongside advanced wafers and high-bandwidth memory. To address this looming supply challenge, Advanced Substrate Technologies (AST), a subsidiary of Japan's Toppan, is constructing a new Flip-Chip Ball Grid Array (FC-BGA) substrate plant in Singapore, aiming to begin production by late 2026 and stabilize the global supply chain for AI and HPC applications.

IN DEPTH

Background: The Evolving Semiconductor Supply Chain

For decades, the semiconductor industry predominantly focused on front-end miniaturization to drive performance gains. However, with the advent of the AI era, the significance of back-end processes—particularly advanced packaging and its foundational component, the substrate—has been profoundly re-evaluated. Optimal performance and reliable supply of advanced chips now depend critically on the optimization of every segment of the supply chain. Substrates serve as the essential 'bridge' connecting complex chips to printed circuit boards (PCBs), making their performance and stable supply a vital lifeline for the accelerating growth of AI and High-Performance Computing (HPC).

Key Findings: Broadcom Flags Substrate Bottleneck, Toppan Subsidiary Responds

Hock Tan, CEO of Broadcom, has issued a stark warning: advanced packaging substrates are now emerging as a critical bottleneck in the production of high-end chips, standing alongside well-known constraints like advanced wafers and High-Bandwidth Memory (HBM). This bottleneck is particularly acute for cutting-edge processors such as high-performance network processors and AI accelerators, which demand sophisticated Flip-Chip Ball Grid Array (FC-BGA) substrates featuring substantially larger surface areas and an exceedingly high number of interconnect layers. These substrates are indispensable for efficiently transmitting massive data volumes and power to and from the chip.

While innovations like chiplet technology and 2.5D/3D packaging have dramatically advanced chip integration, the complexity of designing and manufacturing these corresponding substrates has also surged, resulting in a significant production capacity bottleneck. This substrate shortage is directly impacting the supply of finished high-end chips, constraining the growth of critical technologies.

To directly address this escalating challenge, Advanced Substrate Technologies (AST), a subsidiary of Japan’s Toppan Printing, is making a strategic investment. The company is constructing a new state-of-the-art facility for high-end FC-BGA substrates in Singapore, with production slated to commence by the end of 2026. This investment is deemed crucial for stabilizing the global supply of semiconductors vital for AI and HPC applications.

Strategic Significance and Future Outlook

The establishment of AST's new Singapore plant is projected to significantly alleviate the existing supply deficit, thereby fortifying the advanced packaging ecosystem, especially within Southeast Asia. The facility is designed to incorporate cutting-edge manufacturing technologies to meet the escalating demand for these critical components.

This strategic move by AST also reflects a broader industry trend toward regionalization and diversification of semiconductor supply chains, aiming to build resilience against future disruptions. Stabilizing the supply of advanced substrates is paramount for sustaining the rapid development and deployment of AI accelerators and HPC systems. It is anticipated that other leading substrate manufacturers will follow suit with similar expansion investments, further enhancing the overall robustness of the global semiconductor supply chain.

However, as substrate technology continues its rapid evolution, continuous innovation and close collaboration across materials science, equipment development, design, and manufacturing stages will be imperative to proactively prevent the emergence of new bottlenecks and ensure the uninterrupted progress of high-performance computing.

Source: Unknown

#10 Samsung Electro-Mechanics Unveils Five Next-Gen Semiconductor Package Substrate Products for AI, Automotive, and Mobile Markets at KPCA Show

Published September 09, 2026 Global Sources South Korea



OVERVIEW

Samsung Electro-Mechanics showcased next-generation semiconductor package substrate technologies at KPCA Show, targeting high-end chip applications like AI servers, automotive systems, and mobile devices. Emphasizing advanced packaging as a key growth driver, the company exhibited five innovative products, including 2.5D and 2.1D package substrates, glass substrates, automotive FCBGA substrates, and ultra-thin CSP substrates. This portfolio highlights their strategic commitment to meeting the diverse demands of high-performance applications.

IN DEPTH

Key Findings: Samsung Electro-Mechanics Unveils Five Next-Gen Package Substrate Products for AI, Automotive, and Mobile

Samsung Electro-Mechanics (SEM) showcased its next-generation semiconductor package substrate technologies at the KPCA Show, targeting a broad spectrum of high-end chip applications including AI servers, automotive systems, mobile devices, laptops, and tablets. The company underscored advanced packaging as the critical enabler for unlocking performance and efficiency in these burgeoning sectors, exhibiting a total of five innovative products. This move clearly delineates SEM's technological leadership and strategic focus in addressing the diversifying and increasingly sophisticated demands of modern electronics.

Technical & Product Details: Diversified Advanced Packaging Substrate Portfolio

- **2.5D and 2.1D Package Substrates:** These substrates are essential for integrating multiple chips, such as GPUs and HBM, delivering the high bandwidth and power efficiency required by AI accelerators and HPC applications. 2.5D enables integration via an interposer, while 2.1D enhances inter-chip connectivity through more cost-effective methods.
- **Glass Substrates:** Positioned as a novel material for future ultra-high-density packaging, glass substrates offer superior flatness, thermal stability, and electrical properties. They enable finer wiring and higher layer counts, holding promise for next-generation chiplet integration platforms.
- **Automotive FCBGA Substrates:** With the advancements in autonomous driving and Advanced Driver-Assistance Systems (ADAS), automotive semiconductors demand exceptionally high reliability and durability. SEM's automotive FCBGA substrates are engineered to meet these stringent requirements, ensuring stable operation in high-temperature environments.
- **Ultra-thin CSP (Chip Scale Package) Substrates:** Designed for mobile devices like smartphones and wearables that prioritize miniaturization and lightweight design, these substrates enable extremely compact packages very close to the chip size, thereby increasing device design flexibility.

Background & Industry Context: Substrate Importance in Semiconductor Back-End

The proliferation of AI, coupled with the electrification and smart evolution of automobiles, and the advancement of 5G/6G communications, places unprecedented demands on semiconductor chips for performance and reliability. Meeting these demands requires not just performance enhancements from individual chips, but also a crucial role from package substrates that connect and protect them. Especially with the rise of heterogeneous integration, the substrate acts as a platform for efficiently integrating disparate chips, with its design and material technology now dictating the overall semiconductor performance.

Strategic Significance & Outlook: New Market Opportunities and Accelerated Innovation

Samsung Electro-Mechanics' this next-generation package substrate technologies are poised to significantly boost its competitiveness in high-growth markets such as AI, automotive, and mobile. Investments in innovative materials like glass substrates, in particular, signal the future direction of packaging technology. Through continuous R&D and expansion of its product portfolio, SEM is set to further solidify its position as a key solution provider in the global semiconductor supply chain.

Source: https://www.globalsources.com/sourcing-digest/samsung-electro-mechanics-advances-next-generation-semiconductor-packaging-for-ai-automotive-and-mobile-markets/

Collected: September 11, 2026 | Automated Research System (Gemini API)

#11 Micron Reportedly Targets Doubling HBM Capacity to 100,000 Wafers/Month by End-2026, Boosting 12-High HBM4 for NVIDIA Vera Rubin

Published September 04, 2026 digitimes USA



OVERVIEW

Micron is reportedly targeting a near-doubling of its High Bandwidth Memory (HBM) production capacity to approximately 100,000 wafers per month by the end of 2026. This significant expansion focuses on ramping up production of 12-high HBM4 specifically for NVIDIA's next-generation "Vera Rubin" AI platform. This strategic move aims to intensify HBM market competition and solidify Micron's position as a key HBM supplier.

IN DEPTH

Key Findings: Micron to Double HBM Capacity by End-2026, Supplying 12-High HBM4 for NVIDIA

Micron Technology is reportedly planning to significantly expand its High Bandwidth Memory (HBM) production capacity, aiming to double it to approximately 100,000 wafers per month by the end of 2026. This strategic move is primarily focused on substantially increasing the production of higher-performance 12-high HBM4 memory, specifically for NVIDIA's next-generation AI platform, "Vera Rubin." By doing so, Micron intends to solidify its position as a major HBM supplier and close the gap with competitors Samsung and SK Hynix.

Technical & Market Details: 12-High HBM4 for NVIDIA's Vera Rubin Platform

- **Rapid HBM Capacity Expansion:** A monthly production target of 100,000 wafers represents a massive expansion plan within the HBM industry. This investment is expected to alleviate the supply shortage of HBM, a core component of AI accelerators, and further promote the widespread adoption of AI technology.
- **12-High HBM4 to the Forefront:** While 8-layer stacks have been prevalent for previous HBM generations, 12-high HBM4 offers significantly greater capacity and bandwidth, meeting the next-generation performance requirements of AI chip developers like NVIDIA. This technology necessitates fine-pitch Through Silicon Via (TSV) connections and advanced stacking techniques.
- **NVIDIA Vera Rubin Platform:** NVIDIA's new AI platform is anticipated to deliver computational power and data processing speeds that surpass previous AI accelerators, achieved through the integration of cutting-edge GPUs and HBM4. Micron's HBM supply will be a crucial component for the success of this platform.

Background & Industry Context: AI Demand Drives Memory Market Transformation

Training and operating large-scale AI models require memory capable of processing vast datasets at high speeds. HBM has become the de facto standard for AI accelerators due to its superior bandwidth and power efficiency. This surge in demand is prompting memory manufacturers to make new investments and innovations distinct from the traditional DRAM market, positioning HBM as one of the primary drivers of growth in the semiconductor industry.

Strategic Significance & Outlook: Intensifying HBM Market Competition and Supply Chain Realignment

Micron's HBM capacity expansion plan will undoubtedly intensify competition in the HBM market. With Samsung and SK Hynix holding leading positions, Micron's aggressive investment has the potential to shift the balance of power among suppliers. This competition is expected to accelerate technological innovation, leading to performance improvements and cost reductions for HBM, ultimately contributing to the further advancement of AI technology. Simultaneously, HBM manufacturing demands sophisticated back-end processes and a robust supply chain, creating significant business opportunities for related equipment and material manufacturers.

Source: https://www.digitimes.com/news/a20260904VL206.html

#12 Hybrid Bonding Equipment Market Projected to Reach $1.73 Billion in 2026, Growing to $2.58 Billion by 2032

Published September 06, 2026 360iResearch Global



OVERVIEW

This article provides an overview of a market research report published by 360iResearch. The hybrid bonding equipment market is projected to reach $1.73 billion in 2026, with a compound annual growth rate (CAGR) of 6.85% to reach $2.58 billion by 2032. This growth is primarily driven by increasing demand for advanced packaging in AI, HBM, chiplets, and high-performance logic.

IN DEPTH

This article provides an overview of a market research report published by 360iResearch.

Report Overview

This report focuses on the current status and future projections of the global hybrid bonding equipment market. The market under review encompasses diverse semiconductor back-end applications where hybrid bonding technology is applied. The study covers key regions including North America, Europe, Asia Pacific, Latin America, and the Middle East & Africa, with a forecast period spanning from 2026 to 2032.

Key Research Findings

The hybrid bonding equipment market is projected to achieve a market size of $1.73 billion USD in 2026. Subsequently, it is expected to grow at a compound annual growth rate (CAGR) of 6.85% during the forecast period until 2032, reaching an estimated market size of $2.58 billion USD. This growth is strongly propelled by the escalating demand for advanced packaging solutions in critical areas such as Artificial Intelligence (AI), High Bandwidth Memory (HBM), chiplets, and high-performance logic. The analysis also highlights that advancements in sub-micron connection pitches and improved electrical performance are indispensable for the technological evolution and market expansion of this segment.

About the Publisher

360iResearch is a global research firm that provides market intelligence reports across various industry sectors. The company offers in-depth market analysis, competitive landscape assessments, growth forecasts, and profound insights into key trends, serving as a vital information source for strategic business decision-making.

Source: https://www.360iresearch.com/library/intelligence/hybrid-bonding-equipment

Collected: September 11, 2026 | Automated Research System (Gemini API)

#13 Samsung Allots Over 50% of 4nm Foundry Capacity to HBM4 Base Die Production, Totaling 15,000 Wafers Per Month

Published Published September 07, 2026 ZDNet Korea (Wccftechによる引用) South Korea



OVERVIEW

Samsung Electronics is reportedly allocating over 50% of its advanced 4nm foundry capacity—specifically 15,000 wafers per month out of an estimated 30,000 total—to the production of HBM4 base dies. This strategic move, leveraging its Pyeongtaek S5 and S6 lines, aims to address the severe HBM supply shortage, which has become a critical bottleneck for high-performance AI accelerator production. The decision underscores Samsung's intent to strengthen its position in the rapidly expanding AI semiconductor market and alleviate supply chain pressures for key customers.

IN DEPTH

Background: AI Demand Reshapes Foundry Priorities

The artificial intelligence (AI) revolution has triggered an unprecedented shift in demand within the semiconductor industry, particularly in the foundry market. Beyond traditional general-purpose logic chips and mobile SoCs, there's been a surge in demand for specialized components like High Bandwidth Memory (HBM) base dies and advanced packaging solutions such as CoWoS, which form the core of modern AI accelerators. As a result, foundry companies are increasingly compelled to allocate their limited advanced process capacity to strategically important and more profitable AI-related components.

Key Findings: Samsung Dedicates Half of 4nm Capacity to HBM4 Base Dies

Samsung Electronics is reportedly dedicating over 50% of its state-of-the-art 4nm manufacturing capacity to the production of HBM4 chip base dies. This strategic decision directly responds to a severe market condition where HBM demand significantly outstrips supply, acting as a critical bottleneck for next-generation AI accelerators. This aggressive production shift is a core strategy to mitigate the HBM4 supply shortage and to maintain and strengthen Samsung's competitiveness in the rapidly evolving AI semiconductor market. Specifically, the advanced foundry lines S5 and S6 at its Pyeongtaek campus are being utilized for this high-priority HBM4 base die manufacturing.

Technical & Production Details

- **Massive Capacity Shift:** Samsung Electronics' total 4nm process foundry capacity is reportedly around 30,000 wafers per month. Out of this, approximately 15,000 wafers are specifically allocated for HBM4 base die manufacturing. This significant allocation means half of Samsung's advanced process production resources are concentrated on a single, strategically vital product, underscoring the high priority placed on HBM.

- **Role of the HBM4 Base Die:** HBM architecture involves multiple DRAM chips stacked vertically atop a base die, which is essentially a logic chip. This base die is crucial, housing the memory controller, testing functions, and the interface that connects to the GPU via Through Silicon Vias (TSVs). Manufacturing this component on a cutting-edge 4nm process is vital for maximizing HBM4's power efficiency, optimizing data processing capabilities, and overall dictating the performance of the HBM stack.
- **Alleviating AI Chip Supply Bottleneck:** The availability of HBM has emerged as one of the primary bottlenecks in the production of high-performance AI accelerators. Samsung's substantial investment in HBM4 base die production aims to ease this critical supply constraint and stabilize the provision of HBM4 to key customers, including industry leaders like NVIDIA and AMD.

Strategic Implications & Outlook

This significant production shift by Samsung Electronics is expected to intensify the competitive landscape for dominance in the burgeoning HBM market, particularly against rival SK Hynix. By committing a substantial portion of its 4nm capacity to HBM4, Samsung aims to significantly increase its HBM product supply and establish a crucial technological advantage. This heightened competition is anticipated to drive further innovation and efficiency improvements in HBM technology, ultimately contributing to the overall advancement of AI infrastructure. Furthermore, this move underscores the increasing strategic value of foundries and the paramount importance of advanced packaging solutions within the entire semiconductor supply chain as AI continues to reshape the industry.

Source: https://wccftech.com/report-samsungs-4nm-lines-run-at-full-tilt-as-hbm4-chips-eat-up-to-60-of-foundry-output/

Collected: September 11, 2026 | Automated Research System (Gemini API)

#14 NXP to More Than Double Semiconductor Back-End Capacity at Malaysian Facility

Published Published September 03, 2026　日系半導体製造装置　Malaysia



OVERVIEW

NXP has announced a substantial expansion of its Malaysian facility, targeting a more than twofold increase in semiconductor back-end production capacity. This strategic investment is a direct response to the escalating global demand for semiconductors, especially from the automotive and industrial sectors, and reflects a broader trend of bolstering supply chain resilience through significant OSAT (Outsourced Semiconductor Assembly and Test) sector investment.

IN DEPTH

Background

In recent years, the accelerating pace of digital transformation, the widespread adoption of electric vehicles (EVs), and the global proliferation of 5G communication networks have collectively fueled a sustained and significant increase in semiconductor demand. The automotive semiconductor sector, in particular, has experienced profound supply constraints, underscoring the critical need for robust manufacturing capabilities. This backdrop has propelled major integrated device manufacturers (IDMs) like NXP to invest heavily in production capacity. Malaysia has long been established as a pivotal hub for semiconductor back-end operations, and NXP's strategic expansion further solidifies its enduring presence in Southeast Asia. As an IDM, NXP's commitment to augmenting its internal back-end capacity is a clear strategic move towards building a more resilient, self-sufficient, and dependable supply chain, crucial for navigating future market volatilities and ensuring stable supply to its diverse customer base across various industries.

Key Findings

NXP has unveiled ambitious plans for a substantial expansion of its semiconductor manufacturing facility in Malaysia, aiming to more than double its current back-end production capacity. This significant capital expenditure is strategically directed at addressing the escalating global demand for semiconductors, particularly within NXP's core segments of automotive and industrial control systems, which require increasingly sophisticated and reliable components.

The expansion will involve the integration of cutting-edge packaging technologies and advanced testing equipment. This upgrade is designed to enable the production of increasingly complex and high-performance semiconductor devices. A key focus will be on supporting advanced packaging techniques such as Multi-Chip Modules (MCM) and System-in-Package (SiP). These technologies are essential for developing the high-density, high-functionality semiconductors required by next-generation applications in artificial intelligence (AI) and the Internet of Things (IoT), thereby ensuring a stable supply for these critical and rapidly growing markets.

This investment is anticipated to significantly ramp up during fiscal year 2026 and reach full operational capacity within a few years. The more than doubling of NXP's production capacity in Malaysia is expected to not only enhance the company's market share but also ensure a stable supply for its customers, contributing significantly to the overall stability and resilience of the global semiconductor supply chain. Malaysia, with its skilled workforce and favorable business environment, is strategically positioned to remain a critical investment destination for advanced semiconductor back-end manufacturing.

Source: https://www.sangyo-times.jp/

Collected: September 11, 2026 | Automated Research System (Gemini API)

#15 TRUMPF Resolves Glass Substrate TGV Coating Bottleneck with High-Power HiPIMS, Accelerating Next-Gen AI Chip Packaging Mass Production

Published September 06, 2026 Asianews.network Germany



OVERVIEW

Germany's TRUMPF announced a breakthrough in Through Glass Via (TGV) coating for glass substrates, a critical bottleneck, by leveraging its high-power HiPIMS (High Power Impulse Magnetron Sputtering) technology. This innovation is expected to significantly accelerate the mass production of next-generation AI chip packaging, contributing to the realization of higher performance and more energy-efficient AI semiconductors. Glass substrates, with their superior electrical and thermal properties, play a crucial role in advanced packaging for AI chips.

IN DEPTH

Key Findings

TRUMPF has announced a significant breakthrough in the Through Glass Via (TGV) coating process for glass substrates, a foundational element in next-generation AI chip packaging. Utilizing its proprietary high-power HiPIMS (High Power Impulse Magnetron Sputtering) technology, TRUMPF has successfully eliminated a long-standing bottleneck, which is anticipated to dramatically boost the mass production capabilities for high-density, high-performance AI chips and have a profound impact across the industry.

Technical / Clinical Details

TGVs are microscopic electrical pathways that penetrate glass substrates, indispensable for achieving both high-frequency performance and high-density interconnections. However, uniformly applying a high-quality conductive coating to the inner walls of these TGVs has been extremely challenging, presenting a significant bottleneck in the manufacturing process. TRUMPF's high-power HiPIMS technology achieves a higher ionization rate and deposition speed compared to conventional sputtering methods, enabling the formation of uniform and highly adhesive metallic films deep within the TGVs. This advancement leads to reduced electrical resistance, enhanced signal transmission reliability, and a substantial improvement in manufacturing throughput. Glass substrates offer compelling advantages over silicon, including lower dielectric loss, superior coefficient of thermal expansion matching, and potentially lower cost, positioning them as an ideal platform for multi-layer AI chip packaging.

Background & Context

The relentless pursuit of higher AI chip performance increasingly relies not just on traditional miniaturization techniques but also on advanced packaging technologies like 3D stacking and multi-chiplet integration. Especially in AI accelerators incorporating High Bandwidth Memory (HBM), the data transfer speed between chips becomes a bottleneck, making low-dielectric-loss materials like glass substrates and high-density TGVs indispensable. Previously, the difficulty of TGV coating had hindered the broader adoption of glass substrates. TRUMPF's latest technological innovation removes this barrier, paving the way for more widespread implementation of high-performance AI packaging based on glass substrates.

Strategic Significance & Outlook

TRUMPF's resolution of the TGV coating bottleneck introduces new degrees of freedom in the design and manufacturing of next-generation AI chips. This will accelerate the trend towards higher performance, greater integration density, and lower power consumption for AI chips, driving AI innovation in diverse applications such as data centers, edge AI, and autonomous driving. Leveraging this technology, TRUMPF is expected to strengthen its leadership in the semiconductor manufacturing equipment market and create new market opportunities through collaborations with glass substrate suppliers and AI chip manufacturers. This technology will be critical in improving the cost-efficiency and production scale of AI chips, providing an essential foundation for the overall advancement of the AI industry.

Source: https://asianews.network/trumpf-makes-glass-substrates-ready-for-the-next-generation-of-ai-chips/

Collected: September 11, 2026 | Automated Research System (Gemini API)

#16 High-End ABF Substrate Supply Faces Critical Shortage Amid Gigantic AI Chip Growth, Fueling Intense Competition Among Taiwanese Manufacturers

Published September 06, 2026 Tom's Hardware Taiwan



OVERVIEW

The escalating computational power and physical size of AI chips have led to a severe global shortage in the supply of high-end Ajinomoto Build-up Film (ABF) substrates, a core component. In response, intense competition has ignited among leading Taiwanese manufacturers and semiconductor equipment suppliers to rapidly expand production capacity, causing significant distortions in the global supply-demand balance. The stable supply of ABF substrates has become a critical determinant of the AI industry's growth.

IN DEPTH

Key Findings

The relentless pursuit of higher computational power and the consequent physical enlargement of AI chips have resulted in a critical global shortage of high-end Ajinomoto Build-up Film (ABF) substrates. This supply crunch has sparked fierce competition among Taiwan's leading substrate manufacturers and related semiconductor equipment suppliers, all scrambling to rapidly expand production capacity, which is severely impacting the overall supply-demand equilibrium of the AI chip market.

Technical / Clinical Details

ABF substrates serve as crucial interposers in high-performance AI chips and High-Performance Computing (HPC) processors, connecting the chip to the printed circuit board (PCB). Their inherent thinness, low dielectric loss, and fine circuit patterning capabilities enable multi-layer interconnections and high-frequency signal transmission, making them indispensable for efficiently integrating High Bandwidth Memory (HBM) and large processor dies. As AI chips grow in size and complexity, they demand larger and more intricate ABF substrates, significantly increasing manufacturing complexity and time. Specifically, the technology required to precisely form thousands or even tens of thousands of microscopic wiring vias is exceptionally advanced, limiting the number of suppliers capable of delivering high-quality products.

Background & Context

The explosive adoption of generative AI has led to an unprecedented deployment of high-performance AI accelerators in data center AI servers. This has caused demand for ABF substrates from AI chip manufacturers to surge at a pace far exceeding initial predictions. While substantial investments have been made in the ABF substrate market over the past few years, the rate of AI chip evolution and the increasing sophistication of their specifications have outstripped these efforts, leading to the current supply deficit. Taiwan is a global hub for leading ABF substrate manufacturers, including Unimicron, Kinsus Interconnect Technology, and ASE Group, playing a pivotal role in the global supply chain. Consequently, the production expansion race in Taiwan is a matter of critical importance for the global AI industry.

Strategic Significance & Outlook

The shortage of high-end ABF substrates directly impacts AI chip production plans and could temporarily slow the overall growth rate of the AI industry. However, this challenge simultaneously presents a significant opportunity for substrate manufacturers and equipment suppliers for new investments and technological innovation. Taiwanese companies are expected to continue substantial capital investments to boost production capacity. Furthermore, material manufacturers are anticipated to accelerate the development of next-generation ABF materials that are easier to manufacture and offer improved performance. While it is expected to take several years to alleviate this supply-demand imbalance, in the long term, a stable ABF substrate supply system will be established, reinforcing the foundation for the sustained development of the AI industry.

Source: https://www.tomshardware.com/tech-industry/semiconductors/the-state-of-abf-substrates-in-data-center-silicon-in-2026-solving-the-supply-crunch-and-material-wall-beneath-every-ai-accelerator

#17 KLA Achieves $1.1 Billion in Advanced Packaging Process Control Revenue, Driven by Surging AI Chip Demand

Published September 03, 2026 Quartz USA



OVERVIEW

KLA projects approximately $1.1 billion in revenue from its advanced packaging process control systems in 2026, marking over 70% year-over-year growth, driven by the increasing complexity of AI and HPC chips. The shift to technologies like hybrid bonding is increasing demand for inspection and measurement steps, expanding KLA's market share from 7% to 8%. KLA has leveraged its AI investments since 2015 across its product portfolio for image processing and recipe development, ensuring sustained high profitability. The company reported $3.66 billion in Q4 revenue, with Q1 guidance indicating further growth.

IN DEPTH

Key Findings: KLA Achieves $1.1 Billion in Advanced Packaging Process Control Revenue, Marking Over 70% Growth

KLA is experiencing significant growth in its advanced packaging process control systems business, driven by the intricate integration demands of AI and High-Performance Computing (HPC) chips. The company anticipates achieving approximately $1.1 billion in revenue from this sector in 2026, representing over 70% year-over-year growth. This surge is strongly supported by the transition to innovative packaging technologies such as hybrid bonding, which inherently generates an increased number of inspection and measurement steps. KLA's fiscal Q4 revenue reached $3.66 billion, with Q1 guidance suggesting continued expansion, indicating the company is a major beneficiary of the AI-driven demand boom.

Technical and Market Details: Hybrid Bonding and AI Contributions

The adoption of hybrid bonding technology introduces sensitivity requirements below 1 micron in semiconductor packaging, drastically increasing the need for more frequent sampling and inspection. This fundamentally expands the demand for KLA's process control tools. KLA projects its market share in the advanced packaging segment to grow from 7% to 8% in 2026. Furthermore, the company initiated investments in AI technology in 2015 and now leverages AI across its entire product portfolio for image processing, recipe development, and application engineering, thereby optimizing manufacturing processes and enhancing defect detection capabilities. AI systems, including HBM and DRAM, necessitate more sophisticated manufacturing processes and capacity expansions, further boosting demand for KLA's inspection and measurement tools.

Background and Industry Context: AI Chip Complexity Drives Process Control Demand

AI chips are aggressively adopting advanced packaging techniques like die stacking and heterogeneous integration to achieve performance gains, which has dramatically increased manufacturing process complexity. This complexity makes highly precise and reliable process control, inspection, and metrology solutions indispensable for maintaining manufacturing yields and minimizing defects. KLA, as a leader in semiconductor defect detection and characterization, is at the forefront of this AI-driven trend, with its expertise and technology contributing to chip manufacturers' ability to uphold production quality.

Future Outlook: Sustained AI-Driven Growth and Market Expansion

KLA anticipates enjoying structurally higher demand and continued growth due to robust investments in AI-driven advanced logic, memory, and advanced packaging, which will fuel demand for its process control products. The company's strong revenue generation and solid operating margins enable reinvestment in the business while also supporting shareholder returns through share buybacks and dividends. Advanced packaging creates more process steps and opportunities for defects, further expanding KLA's market opportunities. The expectation that AI-driven complexity, advanced packaging, and an expanding service base will sustain KLA's high return on invested capital underpins the company's bright growth outlook.

Source: https://qz.com/kla-gains-from-advanced-packaging-can-it-outpace-onto-amat

#18 Onto Innovation's Advanced Packaging Business Achieves 80% Growth, Driven by Dragonfly G5 for HBM4 and 2.5D AI

Published September 09, 2026 Investing.com USA



OVERVIEW

Onto Innovation announced its advanced packaging business grew by 80% year-over-year in 2026, fueled by robust demand from HBM and 2.5D logic applications. The company's Dragonfly G5 platform has been adopted for HBM4 and 2.5D AI packaging, and along with Atlas G6, is expected to drive growth beyond 2027. The panel-level packaging market is projected to reach $1 billion within a few years, with Onto Innovation targeting $200-300 million in revenue from this segment. The company's equipment benefits from increased demand due to semiconductor manufacturing complexity, AI workloads, HPC, and data center expansion.

IN DEPTH

Key Findings: Onto Innovation's Advanced Packaging Business Soars by 80%, Driven by Next-Gen Products

Onto Innovation has announced an impressive 80% year-over-year growth in its advanced packaging business for 2026. This significant expansion is almost equally fueled by strong demand from High Bandwidth Memory (HBM) and 2.5D logic applications. Notably, the company's new Dragonfly G5 platform has been adopted for HBM4 launches and 2.5D AI packaging, and alongside the Atlas G6, is anticipated to drive further growth beyond 2027. The company is significantly benefiting from structural demand increases stemming from the escalating complexity of semiconductor manufacturing, AI workloads, High-Performance Computing (HPC), and data center expansions.

Technical and Market Details: Precision Process Control and Panel-Level Packaging Expansion

Onto Innovation's equipment plays a crucial role in process control, inspection, and metrology, enabling chip manufacturers to detect defects and characterize features in advanced semiconductor and packaging lines. As chip architectures become more sophisticated, incorporating stacking and heterogeneous integration, advanced tools for identifying defects, improving yields, and maintaining production quality become indispensable. The company's Dragonfly G5, a process control tool excelling in optical inspection, 3D metrology, and packaging lithography, is rapidly gaining market adoption. Furthermore, while panel-level packaging is still in its early stages, Onto Innovation projects it to grow into a $1 billion market within a few years, targeting $200-300 million in revenue from this segment. The company's record order backlog is directly linked to AI-related capital expenditures, sustained by high demand for HBM.

Background and Industry Context: AI Revolution Demands Enhanced Precision

The AI revolution places unprecedented demands on the semiconductor industry, particularly in advanced packaging, where high-density integration and complexity are rapidly increasing to maximize chip performance. Consequently, even minute defects in the manufacturing process can severely impact overall product yield, making traditional inspection and metrology techniques increasingly inadequate. High-precision process control solutions, such as those offered by Onto Innovation, are vital for overcoming these challenges and enabling the mass production of cutting-edge chips. The company's tools and software serve as essential infrastructure for leading fabs to maintain high yields.

Future Outlook: Sustained Innovation and Expanding Market Opportunities

Onto Innovation is actively engaged in price negotiations for both new and existing products as it prepares for the 2027 budgeting season, aiming for continued revenue expansion. The rapid adoption of the Dragonfly G5 and Atlas G6 underscores the company's technological leadership and market relevance. The ongoing growth in the AI, HPC, and advanced packaging markets will serve as long-term growth drivers for Onto Innovation. Proactive entry into emerging markets like panel-level packaging is expected to further broaden the company's future growth opportunities, solidifying its central role in the evolution of the semiconductor industry.

Source: https://www.investing.com/news/transcripts/onto-innovation-at-citis-2026-global-tmt-conference-growth-broadens-93CH-4894668

Collected: September 11, 2026 | Automated Research System (Gemini API)

#19 Applied Materials Forecasts Over 70% Growth in Advanced Packaging Revenue, Total Revenue Up 40%, Driven by AI and HBM Demand

Published September 11, 2026 TradingKey USA



OVERVIEW

Applied Materials projects approximately 40% growth in its total revenue for 2026, benefiting significantly from the increasing complexity in AI chip and HBM manufacturing. The company anticipates over 70% growth in its advanced packaging business and over 50% in its process control business. In Q3 2026, Applied Materials reported record revenue of $9.115 billion, a 25% year-over-year increase, with non-GAAP gross margins expanding to 50.4%. The company has strengthened its advanced packaging capabilities through acquisitions in panel-level plating and X-ray technology, and investments in hybrid bonding, positioning AI as the "biggest technology inflection point" it has ever seen.

IN DEPTH

Key Findings: Applied Materials Sees Over 70% Growth in Advanced Packaging Revenue, 40% Total Revenue Growth Driven by AI and HBM

Applied Materials is significantly benefiting from the increasing complexity in AI chip and High Bandwidth Memory (HBM) manufacturing, projecting approximately 40% year-over-year growth in its total revenue for 2026. Specifically, the advanced packaging business is expected to grow by over 70%, and the process control business by more than 50%. The company reported a record Q3 2026 revenue of $9.115 billion, representing a 25% increase from the previous year, with non-GAAP gross margins expanding to 50.4%, indicating improved profitability.

Technical and Portfolio Details: Comprehensive Processes and Strategic Acquisitions

As chip structures become more intricate, new materials and process steps are required, leading to increased demand for deposition, etch, planarization, inspection, and packaging equipment. Applied Materials is one of the equipment companies with the broadest exposure to these processes, offering a wide portfolio for advanced packaging including deposition, copper plating, CMP, bonding, and E-beam process control. The company has reinforced its advanced packaging capabilities through acquisitions of panel-level plating and X-ray technology firms and actively invests in hybrid bonding technology. New CMP, ECD, deposition, and E-beam systems for HBM and 3D packaging were also announced in June 2026, enhancing its responsiveness to cutting-edge technologies.

Background and Industry Context: AI as the "Biggest Technology Inflection Point"

The CEO of Applied Materials identifies AI as the "biggest technology inflection point" seen in his lifetime, emphasizing its role as a multi-year growth driver. Cutting-edge foundry logic, DRAM including HBM, and advanced packaging account for 80% of wafer fab equipment (WFE) growth this year, driven by AI system demand and robust ecosystem-wide investments. Customer capital expenditure forecasts and cloud provider investments are on the rise, with HBM and 3DIC identified as the fastest-growing segments this year.

Future Outlook: Panel-Level Packaging and Continuous Innovation

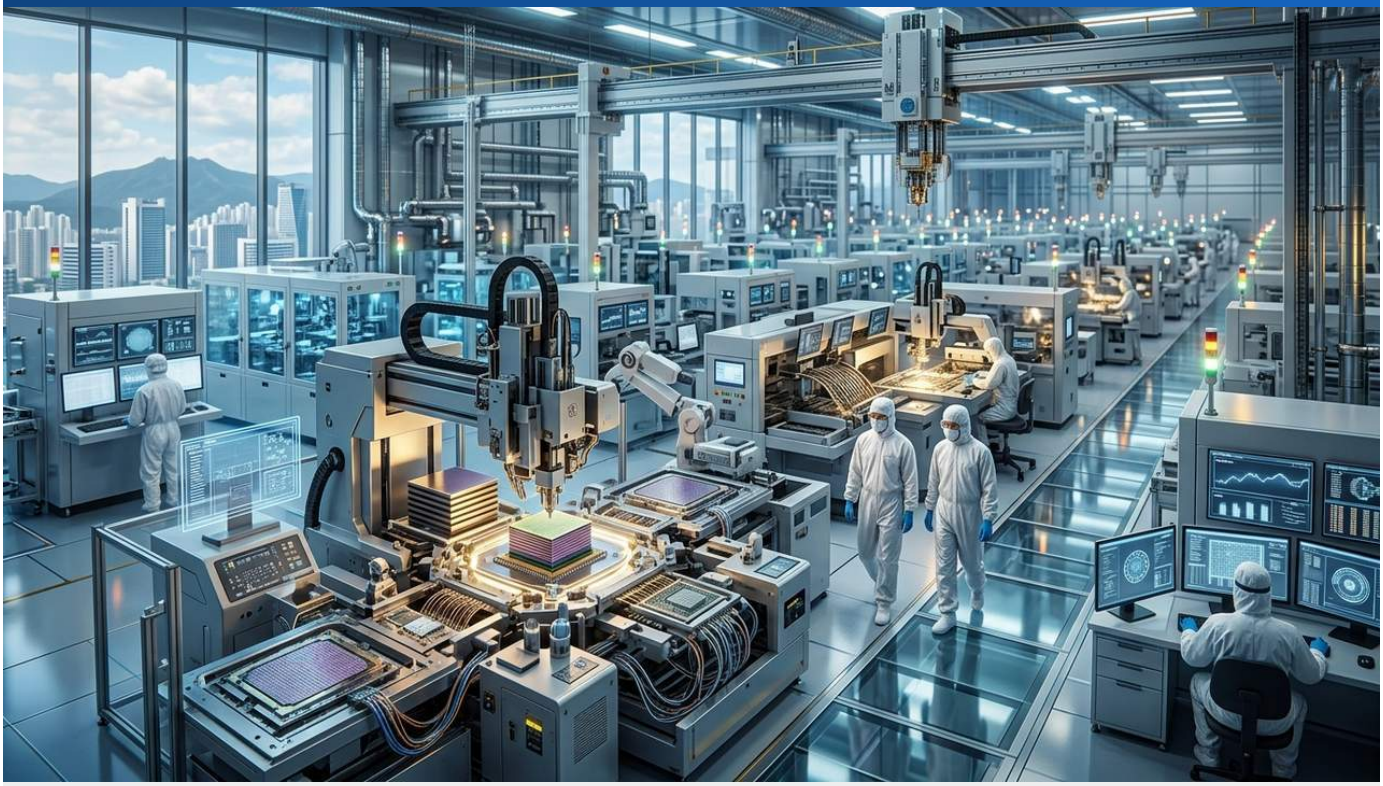
While recognizing panel-level packaging as being in its development phase, Applied Materials is strengthening its capabilities through investments in larger substrates and recent acquisitions. Process diagnostics and control, particularly E-beam inspection, are expected to grow by over 50% due to increasing device complexity, further boosting Applied Materials' future revenues. As advanced packaging becomes a primary industrial battleground, driven by AI and data center expenditures, Applied Materials is poised to play a central role in this new growth cycle through its extensive technology portfolio and strategic investments.

Source: https://www.tradingkey.com/analysis/stocks/us-stocks/262163164-applied-materials-amat-ai-chips-hbm-growth-analysis-tradingkey

Collected: September 11, 2026 | Automated Research System (Gemini API)

#20 South Korea Accelerates Advanced Packaging Investments, Establishing Itself as Core of Global AI Semiconductor Supply Chain

Published September 04, 2026 Investment Monitor South Korea、USA



OVERVIEW

South Korea is significantly boosting its advanced packaging investments to meet surging AI semiconductor export demand. SK Hynix plans to complete a ₩19 trillion ($12.9 billion) advanced packaging plant in Korea by late 2027 and is investing $3.87 billion in a new HBM advanced packaging facility in Indiana, USA. Additionally, U.S. firms Air Products and Axcelis Technologies have pledged a total of $2 billion in South Korea's chip and clean energy sectors, and Samsung Electronics is expanding strategic collaboration with Broadcom for next-gen AI infrastructure. These moves reinforce South Korea's position as a global hub for HBM manufacturing and advanced packaging.

IN DEPTH

Key Findings: South Korea Pours Massive Investments into Advanced Packaging to Meet AI Semiconductor Demand

Amidst a surge in AI semiconductor export demand, South Korea is accelerating massive investments in advanced packaging, solidifying its pivotal role in the global supply chain. SK Hynix has unveiled plans to construct an advanced semiconductor packaging plant in South Korea by the end of 2027, with an investment of approximately ₩19 trillion ($12.9 billion USD). Furthermore, in August 2026, the company announced plans for a $4 billion (also reported as $3.87 billion) HBM advanced packaging facility in Indiana, USA. These investments underscore South Korea's strong commitment to establishing and maintaining its position as a global leader in High Bandwidth Memory (HBM) and advanced packaging technologies.

Technical and Market Details: Strategic Partnerships and Diverse Backend Players

Samsung Electronics and Broadcom signed a Memorandum of Understanding in July 2026 to expand strategic collaboration on next-generation AI infrastructure, encompassing memory, foundry, and advanced packaging technologies. This move aims to accelerate integration and technological innovation across the entire AI ecosystem. Major U.S. companies are also strengthening their investments in South Korea: Air Products is establishing ultra-high purity gas, specialty rare gas, and hydrogen supply facilities at a new semiconductor production site in Pyeongtaek. Axcelis Technologies plans to expand its ion implantation equipment business in Pyeongtaek, adding engineering, prototype development, and training capabilities. Key South Korean backend companies include HANA Micron, which manages critical processes such as flip-chip, wafer-level packaging, and test platforms for SOC, RF, and power management chips. Nepes is also gaining attention in the advanced packaging and materials sectors, catering to AI demand. SK Hynix, in particular, is driving specific technological innovations, such as applying an advanced MR-MUF process to HBM4E, reducing thermal resistance by 17% compared to existing products.

Background and Industry Context: Geopolitical Investment Shift Driven by AI

The advent of AI has profoundly altered the semiconductor manufacturing paradigm, with advanced packaging emerging as a new bottleneck. This constraint is so severe that even major AI chip manufacturers like Nvidia face shortages in CoWoS and other advanced packaging capacities. Increased U.S. investments and collaborations are designed to enhance global supply chain resilience and strengthen the economic aspects of the U.S.-South Korea alliance. Semiconductor equipment sales in the first half of 2026 saw a significant increase of 32.4% in South Korea and 24.0% in Taiwan, indicating a decisive geographical shift in the growth drivers of the global semiconductor equipment market away from China.

Future Outlook: South Korea's Strategic Positioning in the AI Era

The South Korean government and its corporations are pursuing strategic investments and international collaborations to solidify the nation's status as a semiconductor powerhouse in the AI era. The construction of large-scale domestic factories and investments in HBM packaging facilities in the U.S. aim to secure supply capabilities through both vertical integration and global expansion. Furthermore, the increasing complexity of advanced packaging will drive innovation and investment across the entire ecosystem, from inspection and metrology equipment to materials. Through these initiatives, South Korea is expected to further strengthen its indispensable role as a hub in the global AI semiconductor supply chain.

Source: https://www.investmentmonitor.ai/news/us-pledge-2bn-for-south-korea/

#21 Taiyo Holdings, in Collaboration with imec, Successfully Forms 700nm Precision 3-Layer RDL on 12-inch Wafers

Published Published September 10, 2026 Quantum Zeitgeist Japan、ベルギー



OVERVIEW

Taiyo Holdings, in collaboration with imec, announced at IEEE ESTC 2026 the successful formation of a 3-layer Redistribution Layer (RDL) with a critical dimension of 700 nanometers on 12-inch wafers. This achievement, enabled by their new FPIM series materials, marks a significant advance in fine-pitch wiring, crucial for high-density interconnections in advanced semiconductor packaging for AI and high-performance computing (HPC) chips. The materials demonstrate high compatibility with essential dual damascene processes for sub-1.6 micrometer pitches.

IN DEPTH

The Packaging Imperative for AI

As the demand for artificial intelligence (AI) and high-performance computing (HPC) continues its exponential growth, the semiconductor industry is increasingly looking beyond traditional transistor scaling (Moore's Law) for performance gains. Advanced packaging, particularly chiplet integration and high-density interconnections, has emerged as a critical enabler. Redistribution Layers (RDLs) serve as the vital 'bridges' that efficiently and rapidly connect multiple chiplets within a package. However, as packages grow larger and the number of wiring layers increases, the limitations of existing substrate materials and fine processing technologies have become significant bottlenecks, constraining the evolution of next-generation AI accelerators and High Bandwidth Memory (HBM).

A Precision Leap in Advanced Packaging

At the IEEE ESTC 2026 conference, Taiyo Holdings announced a groundbreaking collaboration with imec, successfully demonstrating the formation of a 3-layer Redistribution Layer (RDL) with an unprecedented critical dimension (CD) of 700 nanometers on 12-inch wafers. This achievement represents a crucial step forward in fine-pitch wiring for advanced semiconductor packaging. Enabled by Taiyo Holdings' newly developed FPIM series materials, this technology is poised to dramatically increase connection density between chips, establishing a foundational technology for the continued evolution of high-performance AI chips and HPC packaging.

Enabling Ultra-Fine-Pitch Wiring: The Role of FPIM and Dual Damascene

RDLs are multi-layered wiring structures designed to provide electrical connections between chiplets or between chips and external packages. Their miniaturization is paramount for enhancing overall packaging density and performance. Taiyo Holdings' new FPIM series materials played a pivotal role in this breakthrough, exhibiting superior processability, electrical properties, and reliability essential for achieving 700nm precision in 3-layer RDL formation. A key insight from imec's analysis confirms that a dual damascene process is indispensable for realizing wiring pitches below 1.6 micrometers. Crucially, Taiyo Holdings' new FPIM materials demonstrate high compatibility with this dual damascene process, positioning them as a key enabler for next-generation ultra-fine-pitch wiring technologies. This innovation is also expected to contribute to improved yield and reduced manufacturing costs in wafer-level thin-film processing.

Shaping the Future of AI and HPC

The successful development of 700nm high-precision RDL formation technology pushes the boundaries of current advanced packaging capabilities. This innovation is likely to play a significant role in future standardized packaging platforms by enabling the integration of more functions and higher performance into limited space, particularly in high-density interposers and advanced chiplet integration schemes. The collaborative research between Taiyo Holdings and imec underscores the critical importance of material and process innovations in the semiconductor backend for advancing computational power in the AI era. It is anticipated that the application of the FPIM series materials and this advanced RDL technology in mass production will substantially enhance the design flexibility and manufacturing efficiency of high-performance chips, paving the way for even more powerful and compact computing solutions.

Source: https://quantumzeitgeist.com/three-layer-rdl-taiyo-holdings-700/

Collected: September 11, 2026 | Automated Research System (Gemini API)

#22 Laser Debonding Technology Becomes Critical for Improving Thin Wafer Yield in HBM and Hybrid Bonding

Published September 04, 2026 Microtreat Global



OVERVIEW

Laser debonding is gaining importance as the cleanest and least damaging wafer separation technology for high-value 3D integration and advanced packaging. For ultra-thin wafers (20-50 micrometers) in HBM, chiplets, and compound semiconductor power devices, temporary bonding followed by laser debonding is an essential module for achieving high yields. Fused quartz carrier wafers provide mechanical support during thin wafer processing, while laser debonding separates the device wafer from the carrier by using a laser beam transmitted through the transparent carrier to absorb the temporary bonding adhesive or release layer without damage.

IN DEPTH

Key Findings: Laser Debonding Becomes Essential for Yield Improvement in Thin Wafer Processing for HBM and Hybrid Bonding

Laser debonding technology is rapidly increasing in importance as the cleanest and least damaging wafer separation method for high-value 3D integration and advanced packaging processes. Particularly in areas such as High Bandwidth Memory (HBM), chiplets, and compound semiconductor power devices, where device wafers are processed to extremely thin dimensions (below 20-50 micrometers), temporary bonding followed by efficient and low-stress debonding is an indispensable module for ensuring high yields. This technology involves directing a laser beam through a transparent carrier (typically glass or quartz) to absorb the temporary bonding adhesive or release layer, thereby separating the device wafer from the carrier without damage.

Technical and Process Details: Role of Fused Quartz Carrier Wafers and Laser Processing

In HBM and hybrid bonding processes, device wafers undergo multiple delicate steps, including temporary bonding, back grinding, Through-Silicon Via (TSV) exposure, dielectric deposition, redistribution layer processing, polishing, and cleaning, before final stacking. Throughout these stages, a rigid, thermally stable, and optically transparent platform is required to mechanically support the thin wafers. Fused quartz carrier wafers are ideal for meeting these demands, preventing warping and breakage of wafers during processing. In the semiconductor laser processing equipment market, laser dicing and laser debonding tools play crucial roles. Laser dicing uses non-contact, high-energy laser beams for precise processing of advanced semiconductor materials, reducing mechanical stress. Laser debonding is employed to remove temporary bonding layers without damaging delicate structures, widely supporting advanced packaging technologies including wafer-level processing.

Background and Industry Context: Advancements in 3D Integration and Ultra-Thinning

Driven by increasing demand for AI and high-performance computing, the semiconductor industry is accelerating its shift towards advanced packaging technologies such such as 3D stacking and heterogeneous integration to enhance performance. This trend makes wafer thinning unavoidable, and traditional mechanical debonding methods posed a high risk of damage to these delicate, thin wafers. Laser debonding significantly mitigates this risk by enabling non-contact wafer separation, thereby contributing to yield improvement. This technology is becoming a critical element in overcoming bottlenecks in ultra-thin semiconductor manufacturing processes and enabling the realization of next-generation devices.

Future Outlook: Evolution as a Key Enabler for Advanced Packaging

Laser debonding technology will continue to evolve alongside the proliferation of advanced packaging techniques like HBM and chiplets. There is a growing demand for even thinner device wafers and compatibility with a wider range of temporary bonding materials, driving ongoing optimization of laser parameters such as wavelength, power, scan speed, and pulse width. Improvements in the quality and cost reduction of fused quartz carrier wafers will also accelerate the adoption of this technology. Through these advancements, laser debonding is projected to solidify its position as a key enabler for enhancing yield and reliability in advanced packaging.

Source: https://www.szmicrotreat.com/news/wafer-level-and-advanced-packaging-buyer-guide.html

Collected: September 11, 2026 | Automated Research System (Gemini API)

#23 Semiconductor Equipment Investment Shifts to Korea and Taiwan, Driving Growth in H1 2026

Published Published September 09, 2026 The Information Network USA, South Korea, Taiwan



OVERVIEW

In the first half of 2026, global semiconductor equipment sales witnessed a significant geographical pivot, with South Korea (up 32.4%) and Taiwan (up 24.0%) emerging as primary growth drivers, displacing China. This shift, accounting for 68.6% of the total $11.96 billion increase, is propelled by substantial investments in Taiwan's leading-edge logic and advanced packaging, alongside South Korea's expansion in High Bandwidth Memory (HBM) and advanced DRAM.

IN DEPTH

Background

The recent geographical shift in semiconductor equipment investment is rooted in a confluence of evolving technological demands and significant geopolitical factors. Intensifying trade tensions and technological competition between the United States and China have initiated a profound restructuring of the global semiconductor supply chain. This environment has prompted an acceleration of investments in reliable partners, particularly for strategically crucial AI-related technologies. South Korea and Taiwan, leveraging their established positions as central hubs for global semiconductor manufacturing and their advanced technological prowess, are key beneficiaries of this realignment. Fundamentally, this investment pivot is deeply intertwined with these nations' broader economic security strategies in the burgeoning AI era.

Key Findings

In the first half of 2026, global semiconductor equipment sales experienced a decisive geographical pivot, with South Korea and Taiwan emerging as the primary growth catalysts, shifting focus from China. South Korea's sales surged by 32.4%, while Taiwan recorded a robust 24.0% increase. Of the total global sales increase of $11.96 billion, South Korea contributed $4.41 billion and Taiwan $3.80 billion, together accounting for 68.6% of the growth. This significant trend is strongly driven by substantial investments in leading-edge logic and advanced packaging capabilities in Taiwan, alongside aggressive expansions in High Bandwidth Memory (HBM) and advanced DRAM in South Korea.

Technical and Market Analysis

The burgeoning demand for artificial intelligence (AI) is profoundly reshaping capital expenditure strategies across the semiconductor industry. To meet the demanding performance specifications of AI chips, advancements are required not only in miniaturized logic manufacturing but also in sophisticated memory solutions like High Bandwidth Memory (HBM) and advanced packaging technologies, including 2.5D/3D stacking. Consequently, fabs in South Korea and Taiwan, which have established leadership in these critical technologies, are seeing their capital expenditure priorities significantly elevated. Illustratively, SK Hynix, a dominant HBM supplier, has unveiled substantial advanced packaging investments both within South Korea and in Indiana, USA. Concurrently, Taiwanese foundries, exemplified by TSMC, underpin AI chip production with their state-of-the-art logic and pioneering advanced packaging solutions such as CoWoS. This concentrated investment in South Korea and Taiwan signifies not just a geographical reallocation but also the definitive future direction of semiconductor technology evolution in the AI era.

Future Outlook

Provided the AI and high-performance computing (HPC) markets sustain their growth trajectory, semiconductor equipment investments in South Korea and Taiwan are projected to remain robust. This sustained investment will further solidify both regions' pivotal roles in global semiconductor production capacity. However, this also anticipates intensified global competition, particularly as other regions, notably the United States and Europe, actively pursue strategies to bolster their domestic semiconductor manufacturing capabilities. The contest for leadership in HBM and advanced packaging technologies is thus expected to persist as a central and defining theme within the semiconductor industry for the foreseeable future.

Source: https://drrobertcastellano.substack.com/p/the-semiconductor-equipment-boom

Collected: September 11, 2026 | Automated Research System (Gemini API)