TROY TECHNICAL

ADHESIVES & SEALANTS
WEEKLY REPORT

September 12 - September 18, 2026 | Issue 2026-W37

Bond-line performance, cure process, durability and cross-industry qualification

30	10
ANALYZED ARTICLES	PRIORITY THEMES

Issued 2026-09-18 | English edition | fixed approved cover artwork

Adhesives & Sealants: the boundary moved from isolated claims to qualification evidence

30 English articles were reviewed independently from the Japanese edition. Ten themes are retained for management decisions.

SIGNAL 01 | CHEMISTRY

KAIST Develops Glucose-Derived Bio-Hot-Melt Adhesive from E. coli, Outperforming Petroleum Counterparts on Stainless

Researchers at KAIST have engineered E. coli to produce novel bio-based hot-melt adhesive polymers (poly(4HB-co-PhLA) and poly(3HB-co-4HB-co-PhLA)) from glucose, presenting a sustainable alternative to petroleum-derived adhesives.

SIGNAL 02 | FORMULATION

Non-Woven Adhesives Market Grows; Bostik Expands APAO Production, Henkel Co-Develops Bio-Based Hot Melt

This article is an overview of a market research report published by SNS Insider. The non-woven adhesives market is experiencing growth, primarily driven by increasing demand from hygiene product manufacturers.

SIGNAL 03 | APPLICATION & CURE

NovoLINC Unveils MaxLINC, Achieving Industry-Leading 0.7 mm2•K/W Thermal Resistance for Multi-Kilowatt AI Chips

NovoLINC has launched MaxLINC, an advanced thermal interface material (TIM) designed for high-performance AI computing, achieving an industry-leading thermal resistance as low as 0.7 mm2•K/W.

SIGNAL 04 | QUALIFIED PRODUCT

Tyndall National Institute Unveils Three Papers at ESTC 2026 Advancing Photonic Packaging and

Researchers from Tyndall National Institute presented three pivotal papers at ESTC 2026, showcasing significant innovations in photonic packaging, co-packaged optics, and chiplet integration technologies. Dr.

DECISION

Focus this week's management attention on bond-line performance, cure process, durability and cross-industry qualification. Move only when the linked evidence can be reproduced under your own operating conditions.

THREE MANAGEMENT MOVES

1. Buyers: evaluate the complete joint or sealed system under process and lifetime conditions.
2. Suppliers: provide substrate preparation, cure window, rework, aging and failure-analysis evidence.
3. Executives: track adhesion aging, cure variability, outgassing, regulation, repair and scale.

EVIDENCE DISCIPLINE

FACT states what the collected English source reports. BUSINESS READ and ACTION are editorial interpretations. UNKNOWN lists information that the source file does not establish. A linked article is not treated as independent confirmation of every claim.

Five numbers or evidence anchors that require conditions

0.7 mm
A24

SOURCE-BOUND CONDITION
NovoLINC has launched MaxLINC, an advanced thermal interface material (TIM) designed for high-performance AI computing, achieving an industry-leading thermal resistance as low as 0.7 mm2•K/W.

$3 billion
A26

SOURCE-BOUND CONDITION
Tata Electronics announced a $3 billion investment in India's first indigenous semiconductor packaging facility in Jagiroad, Assam, and a strategic partnership with advanced packaging equipment provider Besi.

6%
A10

SOURCE-BOUND CONDITION
The reactive silicone compound market is projected to expand at a Compound Annual Growth Rate (CAGR) of 4-6% from 2026 to 2035.

P04
A31

SOURCE-BOUND CONDITION
Researchers from Tyndall National Institute presented three pivotal papers at ESTC 2026, showcasing significant innovations in photonic packaging, co-packaged optics, and chiplet integration technologies. Dr.

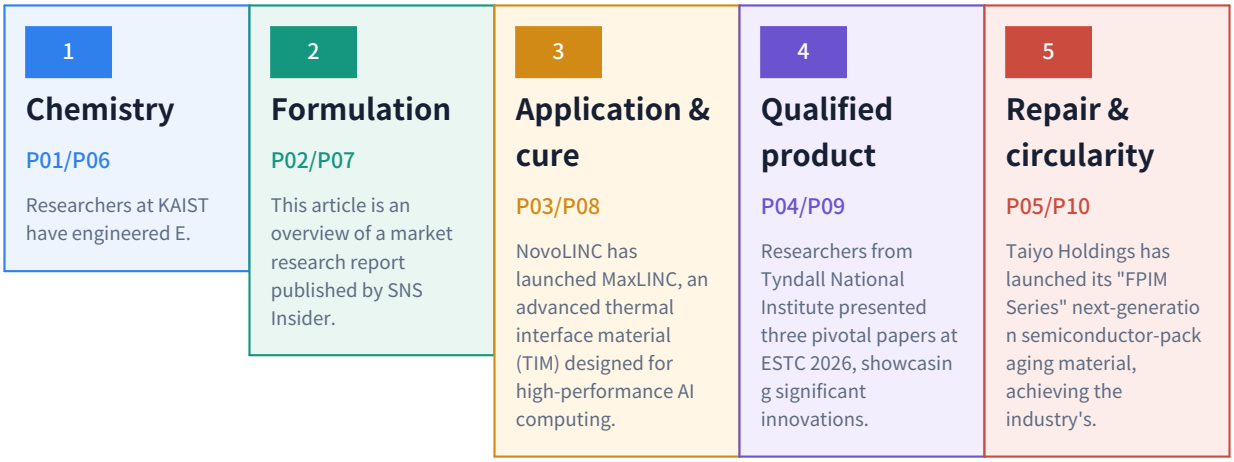
P05
A27

SOURCE-BOUND CONDITION
Taiyo Holdings has launched its "FPIM Series" next-generation semiconductor-packaging material, achieving the industry's first three-layer Redistribution Layer (RDL) formation with a 700-nm critical dimension (CD) on.

HOW TO USE THESE NUMBERS
Each value is shown with the condition stated in the collected English article. Do not compare values across different test methods, device sizes, operating temperatures or commercial stages without normalizing those conditions.

Where the value chain moved

Each stage combines one leading theme and one supporting theme. The report treats handoffs as evidence transfers, not decorative arrows.



EVIDENCE REQUIRED AT EACH HANDOFF

Chemistry to Formulation	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck adhesion aging, cure variability, outgassing, regulation, repair and scale.
Formulation to Application & cure	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck adhesion aging, cure variability, outgassing, regulation, repair and scale.
Application & cure to Qualified product	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck adhesion aging, cure variability, outgassing, regulation, repair and scale.
Qualified product to Repair & circularity	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck adhesion aging, cure variability, outgassing, regulation, repair and scale.

COMMON CONTROL POINT

No theme moves to a commercial commitment until a named owner has reproduced the relevant evidence and documented adhesion aging, cure variability, outgassing, regulation, repair and scale.

Priority map: maturity and business impact

P01	KAIST Develops Glucose-Derived Bio-Hot-Melt Adhesive from E. coli, Outperforming Petroleum Counterparts on Stainless
P02	Non-Woven Adhesives Market Grows; Bostik Expands APAO Production, Henkel Co-Develops Bio-Based Hot Melt
P03	NovoLINC Unveils MaxLINC, Achieving Industry-Leading 0.7 mm2•K/W Thermal Resistance for Multi-Kilowatt AI Chips
P04	Tyndall National Institute Unveils Three Papers at ESTC 2026 Advancing Photonic Packaging and
P05	Taiyo Holdings Achieves First 700nm CD Three-Layer RDL Formation on 12-Inch Wafers with
P06	Taiyo Holdings Launches Next-Gen Semiconductor Packaging Material ' FPIM Series,' First to Achieve 700nm
P07	Tata Electronics Invests $3 Billion in India's First Semiconductor Packaging Facility, Partners with
P08	UV-Curable Adhesive Market Projected for Sustained Growth Through 2035, Driven by Electronics Miniaturization
P09	Researchers Develop Wafer-Scale Bonded Active Photonics Interposer: Pioneering Low-Loss, High-Bandwidth Optoelectronic Integration
P10	IndexBox Report: Electronics Demand to Drive Reactive Silicone Compound Market at 4-6% CAGR

REPRODUCIBLE POSITIONING RULE

Horizontal position uses five discrete stages: Research, Prototype, Joint evaluation, Product adoption and Scale. Vertical position uses three impact levels: single use, multiple customers and multiple supply tiers. Bubble diameter reflects the editorial score inherited from the weekly selection rubric.

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P01 KAIST Develops Glucose-Derived Bio-Hot-Melt Adhesive from E. coli, Outperforming Petroleum Counterparts on Stainless

A11 | Chemistry | Joint evaluation

Date not stated

FACT

Researchers at KAIST have engineered E. coli to produce novel bio-based hot-melt adhesive polymers (poly(4HB-co-PhLA) and poly(3HB-co-4HB-co-PhLA)) from glucose, presenting a sustainable alternative to petroleum-derived adhesives. This biodegradable material demonstrated superior adhesion to stainless steel, achieving 4.58 megapascals (MPa) compared to 4.20 MPa for commercial petroleum-based glues.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P01.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 22/25 | MATURITY 3/5 | IMPACT 1/3

P02 Non-Woven Adhesives Market Grows; Bostik Expands APAO Production, Henkel Co-Develops Bio-Based Hot Melt

A20 | Formulation | Product adoption

Date not stated

FACT

This article is an overview of a market research report published by SNS Insider. The non-woven adhesives market is experiencing growth, primarily driven by increasing demand from hygiene product manufacturers. Bostik expanded its APAO adhesive production capacity with a new manufacturing line in 2026, targeting elastic attachment applications.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P02.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 21/25 | MATURITY 4/5 | IMPACT 2/3

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P03 NovoLINC Unveils MaxLINC, Achieving Industry-Leading 0.7 mm2•K/W Thermal Resistance for Multi-Kilowatt AI Chips

A24 | Application & cure | Product adoption

Date not stated

FACT

NovoLINC has launched MaxLINC, an advanced thermal interface material (TIM) designed for high-performance AI computing, achieving an industry-leading thermal resistance as low as 0.7 mm2•K/W. This new TIM offers over 20% cooling energy savings for AI servers compared to current products, effectively addressing the critical thermal bottleneck in multi-kilowatt AI accelerators. NovoLINC is expanding operations to support the growing demand and commercialization of MaxLINC.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P03.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 21/25 | MATURITY 4/5 | IMPACT 2/3

P04 Tyndall National Institute Unveils Three Papers at ESTC 2026 Advancing Photonic Packaging and

A31 | Qualified product | Pilot

Date not stated

FACT

Researchers from Tyndall National Institute presented three pivotal papers at ESTC 2026, showcasing significant innovations in photonic packaging, co-packaged optics, and chiplet integration technologies. Dr. Sharon Butler demonstrated scalable manufacturing for healthcare and sensing with a co-packaged bio-imaging system integrating hybrid lasers on a glass interposer. Concurrently, Dr.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P04.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 20/25 | MATURITY 2/5 | IMPACT 2/3

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P05 Taiyo Holdings Achieves First 700nm CD Three-Layer RDL Formation on 12-Inch Wafers with

A27 | Repair & circularity | Pilot

Date not stated

FACT

Taiyo Holdings has launched its "FPIM Series" next-generation semiconductor-packaging material, achieving the industry's first three-layer Redistribution Layer (RDL) formation with a 700-nm critical dimension (CD) on 12-inch wafers. Developed in collaboration with imec since October 2022, this material is optimized for dual damascene processes essential for fine-pitch wiring in advanced semiconductor packaging.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P05.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 20/25 | MATURITY 2/5 | IMPACT 2/3

P06 Taiyo Holdings Launches Next-Gen Semiconductor Packaging Material 'FPIM Series,' First to Achieve 700nm

A14 | Chemistry | Research

Date not stated

FACT

Taiyo Holdings, in collaboration with imec, has launched its " FPIM Series," a next-generation semiconductor packaging material that enables the first successful formation of a three-layer Redistribution Layer (RDL) with 700-nm Critical Dimension (CD) on 12-inch wafers.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P06.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | IMPACT 1/3

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P07 Tata Electronics Invests $3 Billion in India's First Semiconductor Packaging Facility, Partners with

A26 | Formulation | Research

Date not stated

FACT

Tata Electronics announced a $3 billion investment in India's first indigenous semiconductor packaging facility in Jagiroad, Assam, and a strategic partnership with advanced packaging equipment provider Besi. This collaboration aims to significantly enhance India's advanced packaging capabilities by leveraging Besi's cutting-edge technologies.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P07.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | IMPACT 3/3

P08 UV-Curable Adhesive Market Projected for Sustained Growth Through 2035, Driven by Electronics Miniaturization

A22 | Application & cure | Joint evaluation

Date not stated

FACT

The UV-Curable Adhesive market is forecasted for sustained growth through 2035, primarily propelled by the ongoing miniaturization of electronics and a shift away from thermal and solvent-based bonding methods. Leading players like Henkel and Dymax Corporation are innovating to supply these adhesives for critical electronics, medical, and industrial applications. This technology offers rapid curing and precise bonding, significantly enhancing manufacturing process efficiency.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P08.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 20/25 | MATURITY 3/5 | IMPACT 3/3

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P09 Researchers Develop Wafer-Scale Bonded Active Photonics Interposer: Pioneering Low-Loss, High-Bandwidth Optoelectronic Integration

A32 | Qualified product | Scale-up

Date not stated

FACT

Researchers have developed a wafer-scale bonded active photonics interposer that integrates photonic devices with electronic circuits at the wafer level, enabling low-loss, high-bandwidth communication with mass production scalability. This technology leverages through-silicon vias and advanced wafer-bonding techniques to overcome traditional integration challenges related to scalability, yield, alignment, and thermal management.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P09.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 20/25 | MATURITY 5/5 | IMPACT 2/3

P10 IndexBox Report: Electronics Demand to Drive Reactive Silicone Compound Market at 4-6% CAGR

A10 | Repair & circularity | Research

Date not stated

FACT

This article provides an overview of a market research report published by IndexBox. The reactive silicone compound market is projected to expand at a Compound Annual Growth Rate (CAGR) of 4-6% from 2026 to 2035. This growth is predominantly driven by robust demand from the electronics and electrical equipment manufacturing sectors, where these compounds are essential for conformal coatings, potting materials, and dielectric encapsulants.

WHY IT MATTERS

The decision relevance is bond-line performance, cure process, durability and cross-industry qualification. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, provide substrate preparation, cure window, rework, aging and failure-analysis evidence.

ACTION

Within 30 days, evaluate the complete joint or sealed system under process and lifetime conditions; record the evidence and owner against P10.

UNKNOWN

Still unproven or incompletely stated: adhesion aging, cure variability, outgassing, regulation, repair and scale.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | IMPACT 2/3

Playbook and 0-5 year roadmap

STAKEHOLDER	NOW | 0-30 DAYS	NEXT | 1-12 MONTHS	LATER | 1-5 YEARS
Operating companies	evaluate the complete joint or sealed system under process and lifetime conditions	Run production-like qualification with explicit acceptance and stop criteria.	Build a portfolio and architecture that can absorb technology and supplier changes.
Materials, equipment and technology suppliers	provide substrate preparation, cure window, rework, aging and failure-analysis evidence	Create shared reliability, process-window and failure-analysis data with customers.	Standardize interfaces, traceability, lifecycle support and recovery services.
Trading, investment and legal teams	Map adhesion aging, cure variability, outgassing, regulation, repair and scale.	Contract for capacity, quality, change notice, liability, alternatives and exit.	Diversify regional, technical and customer concentration risk.

ROADMAP

NOW | 0-30 DAYS
Evidence ledger
Owner: Strategy + quality
Deliverable: claim, source, condition, owner

NOW | 0-30 DAYS
Risk screen
Owner: Procurement + legal
Deliverable: unknowns, alternatives, stop

NEXT | 1-12 MONTHS
Joint qualification
Owner: R&D + supplier
Deliverable: process window and failure data

NEXT | 1-12 MONTHS
Commercial gate
Owner: Business + finance
Deliverable: unit economics and capacity

LATER | 1-5 YEARS
Platform strategy
Owner: Executive team
Deliverable: portfolio and interface roadmap

LATER | 1-5 YEARS
Service layer
Owner: Operations + channel
Deliverable: monitoring, maintenance and recovery

GO / NO-GO GATES

GATE	OWNER	REQUIRED EVIDENCE	NO-GO CONDITION
G1 Evidence	**Quality**	Source, test conditions and reproducibility	No traceable evidence
G2 Integration	**R&D**	Interface, process window and failure analysis	Cannot meet system conditions
G3 Commercial	**Business**	Capacity, total cost, contract and alternatives	Economics or supply cannot be supported
G4 Lifecycle	**Operations**	Monitoring, maintenance, change notice and exit	No accountable operating plan

ANALYZED ARTICLES | ITEMS 01-16

Every title and URL is displayed in full. URLs wrap without shortening and remain clickable. A verified-reference label means the translated HTML did not retain its original source URL.

ID	FULL ARTICLE TITLE	FULL SOURCE / VERIFIED REFERENCE URL - CLICKABLE
A01	SK Hynix Breakthrough: Mass Reflow Underfill Molding Overcomes HBM Stacking Thermal Challenges, While Micron's Hybrid Bonding Slashes Power Consumption by 30%	https://www.csis.org/analysis/beyond-memory-cycle-ai-hbm-and-new-semiconductor-shortage
A02	NIST and UCSD Develop Predictive Modeling for Cure Behavior and Thermal Endurance of Advanced Packaging Epoxy Underfills	https://semiengineering.com/modeling-predicts-cure-and-thermal-endurance-of-advanced-packaging-underfill-nist-ucsd-et-al/
A03	Advanced Packaging Warpage Mitigation: Research Advances in Incorporating Negative Coefficient of Thermal Expansion Materials into Epoxy Molding Compounds and Underfills	https://semiengineering.com/negative-expansion-materials-resist-warpage/
A05	Advanced AI Chips Face Intensified Thermal Management Challenges: TSMC Plans 20-Layer HBM Integration in 14x Reticle CoWoS by 2028, Microchannel Cooling Emerges as Key Technology	https://eu.36kr.com/en/p/3978316580617224
A06	Sub-2nm Nodes Blur Process Boundaries as Chiplet Integration Drives Increased Thermal Density and Structural Stress, Hybrid Bonding Emerges as Key Solution	https://semiengineering.com/redefining-processes-at-sub-2nm/
A07	Panel Warpage Control Emerges as Key Bottleneck Hindering FOPLP Cost Advantage in Advanced Packaging	https://eaapartners.substack.com/p/the-bottleneck-is-real-foplp-is-solving
A08	Semiconductor Progress Bottleneck Shifts from Circuit Design to New Material Integration and Interfacial Control	https://astratrainer.com/blog/future-industries/materials/semiconductor-materials-jobs
A09	Semiconductor Equipment & Materials Market for HBM, Chiplets, and Low-CTE Materials Forecasted to Outpace Overall Wafer Equipment Growth	https://mobilityforesights.com/blog/making-advanced-chips-euv-etch-deposition
A10	IndexBox Report: Electronics Demand to Drive Reactive Silicone Compound Market at 4-6% CAGR Through 2035	https://www.indexbox.io/blog/reactive-silicone-compound-market-to-accelerate-on-electronics-demand-driving-growth-through-2035/
A11	KAIST Develops Glucose-Derived Bio-Hot-Melt Adhesive from E. coli, Outperforming Petroleum Counterparts on Stainless Steel	https://www.eurekalert.org/news-releases/1144212
A12	POSTECH Develops Heat-Releasable Medical Patch with Shape-Memory Pyramid Structure, Minimizing Skin Damage for Fragile Skin	https://biz.chosun.com/en/en-science/2026/09/16/CWTSV2LEQVGCDAOZCXU66HU3DY/
A13	Global Battery Manufacturing Reaches 4 TWh as Adhesives for EV Battery Pack Integration Gain Critical Industrial Relevance	https://www.24chemicalresearch.com/blog/31707/battery-manufacturing-hits-twh-ev-battery-pack-integration-adhesives
A14	Taiyo Holdings Launches Next-Gen Semiconductor Packaging Material 'FPIM Series,' First to Achieve 700nm CD Three-Layer RDL on 12-inch Wafers	https://www.prnewswire.com/news-releases/taiyo-holdings-launches-next-generation-semiconductor-packaging-material-fpim-series-achieving-its-first-three-layer-rdl-formation-with-700-nm-cd-on-12-inch-wafers-302874600.html
A15	Henkel Unveils Low-Diisocyanate PUR Hot-Melt Adhesives and More at SICAM 2026 to Boost Furniture Production Efficiency	https://www.henkel.com/press-and-media/press-releases-and-kits/2026-09-16-less-rework-faster-cycle-times-2240430
A16	TESA Revolutionizes Car Design and Assembly with Advanced Automotive Adhesives for EV Electrification and HMI Evolution	https://www.tesa.com/en/industry/markets/automotive

ANALYZED ARTICLES | ITEMS 17-32

Every title and URL is displayed in full. URLs wrap without shortening and remain clickable. A verified-reference label means the translated HTML did not retain its original source URL.

ID	FULL ARTICLE TITLE	FULL SOURCE / VERIFIED REFERENCE URL - CLICKABLE
A17	KAIST Develops Smartphone-Controlled Adhesive Microneedle Electronic Medicine for Remote Pain Management	https://ground.news/article/pain-can-be-remotely-managed-via-smartphone-development-of-adhesive-microneedle-electronic-medicine_e49016
A18	Samsung Electro-Mechanics and Qualcomm Jointly Develop Organic Bridge Technology for 2.1D AI Semiconductor Packaging	https://www.thelec.net/news/articleView.html?idxno=13907
A20	Non-Woven Adhesives Market Grows; Bostik Expands APAO Production, Henkel Co-Develops Bio-Based Hot Melt	https://www.snsinsider.com/reports/non-woven-adhesives-market-11124
A21	Gel-Based Cooling Pad Market Poised for Growth Through 2035, Driven by Biopharma Cold Chain and EV Demand	https://www.indexbox.io/blog/gel-based-cooling-pads-market-forecast-to-2035-driven-by-biopharma-cold-chain-expansion/
A22	UV-Curable Adhesive Market Projected for Sustained Growth Through 2035, Driven by Electronics Miniaturization	https://www.indexbox.io/blog/uv-curable-adhesive-market-to-accelerate-on-electronics-miniaturization-forecast-points-higher-toward-2035/
A23	Penn State and Kurt J. Lesker Company Form Atomic-Scale Processing Hub for Semiconductors and Quantum Tech	https://www.psu.edu/news/materials-research-institute/story/penn-state-kurt-j-lesker-company-partner-advance-atomic-scale
A24	NovoLINC Unveils MaxLINC, Achieving Industry-Leading 0.7 mm2•K/W Thermal Resistance for Multi-Kilowatt AI Chips	https://www.prnewswire.com/news-releases/novolinc-launches-maxlinc-achieving-industry-leading-0-7-mmkw-thermal-resistance-for-multi-kilowatt-ai-chips-302882340.html
A25	KAIST Engineers E. coli to Produce Glucose-Based Biodegradable Hot-Melt Adhesives, Outperforming Petroleum Counterparts	https://www.miragenews.com/kaist-creates-glucose-based-adhesive-alternative-1745846/
A26	Tata Electronics Invests $3 Billion in India's First Semiconductor Packaging Facility, Partners with Besi to Boost Advanced Packaging	https://www.tataelectronics.com/w/tata-electronics-and-besi-enter-strategic-partnership-to-strengthen-advanced-packaging-capabilities
A27	Taiyo Holdings Achieves First 700nm CD Three-Layer RDL Formation on 12-Inch Wafers with New FPIM Series for Advanced Semiconductor Packaging	https://www.morningstar.com/news/pr-newswire/20260910hk44704/taiyo-holdings-launches-next-generation-semiconductor-packaging-material-fpim-series-achieving-its-first-three-layer-rdl-formation-with-700-nm-cd-on-12-inch-wafers
A28	TESA Unveils Innovative Adhesive Solutions to Meet Demands of Miniaturized and Complex Electronic Devices	https://www.tesa.com/en/industry/markets/electronics
A29	Fact.MR Forecasts Bio-Based Structural Adhesives Market to Reach $3.0 Billion by 2036, Driven by Renewable Feedstock Demand	https://www.factmr.com/report/bio-based-structural-bonding-adhesives-market
A30	3M Launches Cooling Film Reflecting Over 85% Solar Radiation, Cutting Vehicle Interior Temperatures by up to 10°F Without Energy Input	https://simplywall.st/stocks/us/capital-goods/nyse-mmm/3m/news/cooling-film-launch-could-matter-for-3m-stock-mmm
A31	Tyndall National Institute Unveils Three Papers at ESTC 2026 Advancing Photonic Packaging and Chiplet Integration	https://www.tyndall.ie/news/tyndall-researchers-showcase-advanced-packaging-innovation-through-three-published-papers-at-estc-2026/
A32	Researchers Develop Wafer-Scale Bonded Active Photonics Interposer: Pioneering Low-Loss, High-Bandwidth Optoelectronic Integration	https://www.eurekalert.org/news-releases/1144463

Adhesives_Sealants — Selected Articles

Date: 2026-09-20

Articles: 27

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#17 Samsung Electro-Mechanics and Qualcomm Jointly Develop Organic Bridge Technology for 2.1D AI Semiconductor Packaging

#18 Non-Woven Adhesives Market Grows; Bostik Expands APAO Production, Henkel Co-Develops Bio-Based Hot Melt

#19 Gel-Based Cooling Pad Market Poised for Growth Through 2035, Driven by Biopharma Cold Chain and EV Demand

#20 Penn State and Kurt J. Lesker Company Form Atomic-Scale Processing Hub for Semiconductors and Quantum Tech

#21 NovoLINC Unveils MaxLINC, Achieving Industry-Leading 0.7 mm²·K/W Thermal Resistance for Multi-Kilowatt AI Chips

#22 KAIST Engineers E. coli to Produce Glucose-Based Biodegradable Hot-Melt Adhesives, Outperforming Petroleum Counterparts

#23 Tata Electronics Invests $3 Billion in India's First Semiconductor Packaging Facility, Partners with Besi to Boost Advanced Packaging

#24 Taiyo Holdings Achieves First 700nm CD Three-Layer RDL Formation on 12-Inch Wafers with New FPIM Series for Advanced Semiconductor Packaging

#25 TESA Unveils Innovative Adhesive Solutions to Meet Demands of Miniaturized and Complex Electronic Devices

#26 3M Launches Cooling Film Reflecting Over 85% Solar Radiation, Cutting Vehicle Interior Temperatures by up to 10°F Without Energy Input

#27 Tyndall National Institute Unveils Three Papers at ESTC 2026 Advancing Photonic Packaging and Chiplet Integration

#28 Researchers Develop Wafer-Scale Bonded Active Photonics Interposer: Pioneering Low-Loss, High-Bandwidth Optoelectronic Integration

#01 SK Hynix Breakthrough: Mass Reflow Underfill Molding Overcomes HBM Stacking Thermal Challenges, While Micron's Hybrid Bonding Slashes Power Consumption by 30%

Published September 17, 2026 CSIS USA

OVERVIEW

SK Hynix has established a lead in HBM chip stacking by investing heavily in 'Mass Reflow Underfill Molding' (MR-MUF), a novel packaging technique that resolves the thermal and physical constraints of multi-die HBM stacks. Concurrently, Micron has developed a hybrid bonding technology for stacked chips, achieving a 30% reduction in power consumption compared to competing designs by significantly lowering thermal resistance at interconnect points. These innovations are critical for scaling HBM performance and reliability in the demanding AI and high-performance computing sectors.

IN DEPTH

Key Findings

SK Hynix has secured a significant advantage in HBM chip stacking by pioneering 'Mass Reflow Underfill Molding' (MR-MUF), a new packaging technology designed to overcome the thermal and physical challenges inherent in HBM die stacking. In parallel, Micron has developed an advanced hybrid bonding technique for stacked chips, which not only reduces thermal resistance at interconnection points but also achieves a remarkable 30% reduction in power consumption compared to rival designs. These breakthroughs are set to redefine the capabilities and efficiency of next-generation semiconductor packaging.

Technical / Clinical Details

SK Hynix's MR-MUF technology fundamentally addresses the thermal stress and physical deformation issues commonly associated with traditional thermo-compression bonding (TCB) and non-conductive film (NCF) methods. By simultaneously filling and curing underfill resin across multiple HBM dies, MR-MUF ensures uniform thermal distribution and stress mitigation, thereby enhancing HBM module reliability and manufacturing yield for high-density stacks. Micron's hybrid bonding, on the other hand, utilizes direct copper-to-copper bonding, dramatically increasing interconnect density and improving electrical and thermal conductivity over conventional micro-bump connections. This approach substantially lowers thermal resistance across the interconnect layers, leading to more efficient thermal management for the entire chip and a 30% reduction in power consumption. This power efficiency is particularly crucial for power-intensive AI workloads and contributes significantly to system-level energy savings.

Background & Context

The exponential growth of artificial intelligence and high-performance computing applications has fueled an unprecedented demand for High Bandwidth Memory (HBM). However, advancing HBM performance requires ultra-thin dies, increased stacking layers, and robust solutions for thermal management and mechanical integrity—challenges that conventional packaging technologies struggle to meet. The limitations of older methods have created a bottleneck, making innovative material and process technologies like those from SK Hynix and Micron essential. These advancements are key to resolving the emerging semiconductor shortage specific to HBM supply, which is less about fabrication capacity and more about advanced packaging capabilities.

Strategic Significance & Outlook

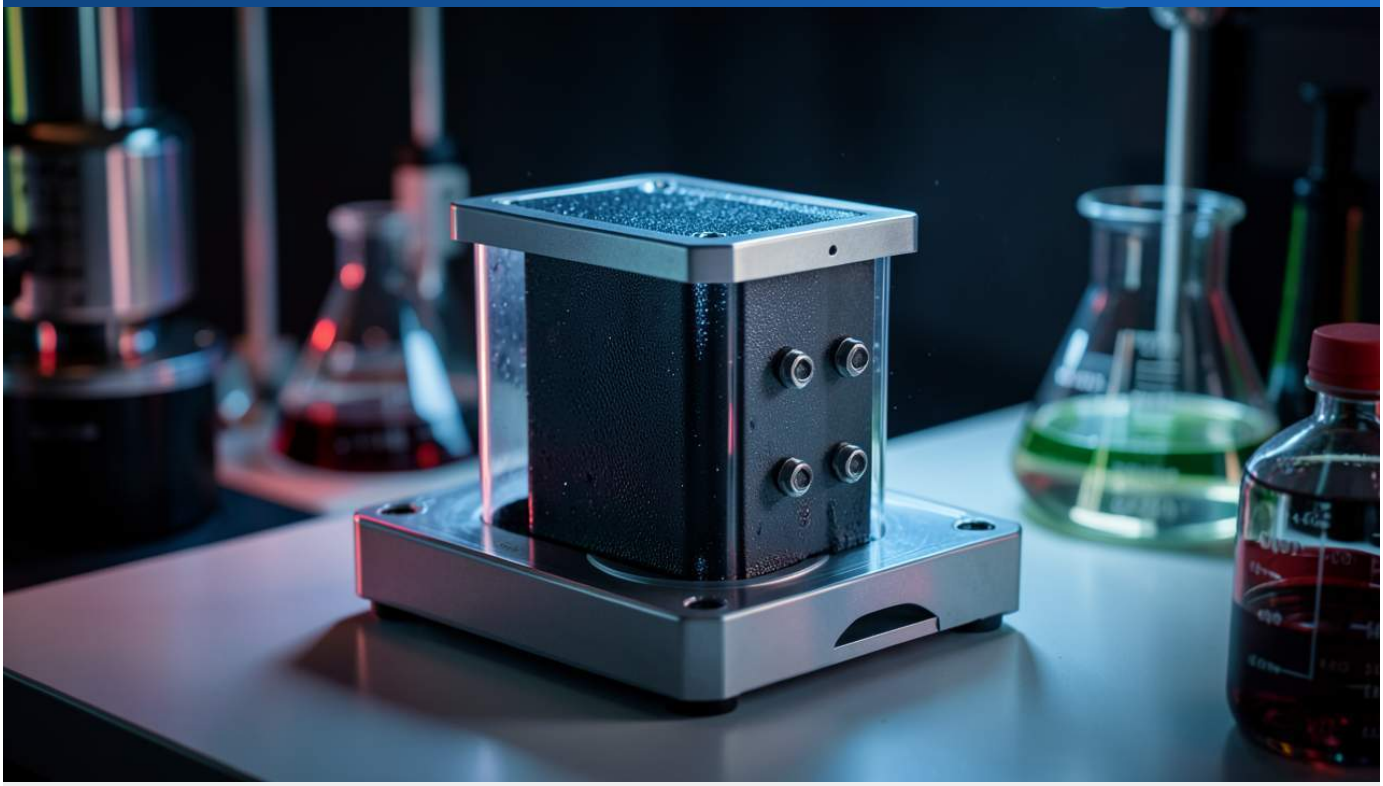
The adoption of these advanced packaging technologies by industry leaders like SK Hynix and Micron will profoundly influence the future design and deployment of HBM and next-generation semiconductor products. These innovations are expected to accelerate the proliferation of HBM into thermal-constrained applications, including mobile devices and edge AI hardware. Furthermore, these techniques will drive the evolution of chiplet-based heterogeneous integration and 3D IC architectures, potentially reshaping the broader semiconductor industry roadmap. The enhanced manufacturing efficiency and improved reliability offered by MR-MUF and hybrid bonding will also contribute to cost reductions in final products, further accelerating the widespread adoption of AI chips across various sectors.

Source: https://www.csis.org/analysis/beyond-memory-cycle-ai-hbm-and-new-semiconductor-shortage

Collected: September 18, 2026 | Automated Research System (Gemini API)

#02 NIST and UCSD Develop Predictive Modeling for Cure Behavior and Thermal Endurance of Advanced Packaging Epoxy Underfills

Published September 11, 2026 Semiconductor Engineering USA



OVERVIEW

Researchers from the National Institute of Standards and Technology (NIST) and the University of California San Diego (UCSD) have published a technical paper detailing a new modeling technique to accurately predict the cure behavior and thermal endurance of highly-filled epoxy underfills for advanced semiconductor packaging. This kinetic modeling, integrating data from differential scanning calorimetry (DSC) and thermogravimetric analysis (TGA) with diffusion principles, promises to accelerate the development of critical materials. The approach significantly enhances mechanical integrity, redistributes thermomechanical stresses, and improves solder joint reliability in fine-pitch interconnect architectures like flip-chip.

IN DEPTH

Key Findings

A collaborative research effort by the National Institute of Standards and Technology (NIST) and the University of California San Diego (UCSD) has yielded a novel modeling technique capable of precisely predicting the cure behavior and thermal endurance of highly-filled epoxy underfills used in advanced semiconductor packaging. This breakthrough is poised to significantly enhance the mechanical integrity and reliability of flip-chip and other fine-pitch interconnect architectures by optimizing stress redistribution within these critical components.

Technical / Clinical Details

The innovative modeling approach integrates data obtained from sophisticated thermal analysis techniques, specifically Differential Scanning Calorimetry (DSC) and Thermogravimetric Analysis (TGA), into a comprehensive kinetic model that incorporates diffusion effects. DSC provides detailed insights into the curing kinetics, reaction heat, and glass transition temperatures, while TGA evaluates the material's thermal decomposition behavior and overall thermal stability. By leveraging these experimental inputs, the researchers developed a robust model that accurately forecasts both the rate of cure during processing and the long-term thermal degradation of the underfill material under operational conditions. This predictive capability allows for quantitative assessment of how effectively the underfill mitigates thermomechanical stresses on solder joints and maintains package reliability over its expected lifespan. Consequently, this tool offers a powerful means to tailor underfill materials precisely to specific application requirements, ensuring optimal performance.

Background & Context

In advanced semiconductor packaging, particularly for flip-chip and 2.5D/3D integration, underfill materials are indispensable. They fill the gap between the chip and the substrate, primarily to mitigate stresses arising from the coefficient of thermal expansion (CTE) mismatch between dissimilar materials. As chip miniaturization and integration density continue to increase, these thermomechanical stresses become a primary driver of device failure. Highly-filled epoxy underfills, with their high filler content, are designed to tune CTE and bolster mechanical strength. However, optimizing their curing process and ensuring long-term thermal endurance have remained persistent challenges. The research from NIST and UCSD provides a scientific framework to predict and address these critical issues.

Strategic Significance & Outlook

This predictive modeling technology is anticipated to dramatically shorten the research and development cycles for advanced packaging materials, thereby accelerating the market introduction of higher-performance and more reliable semiconductor devices. Material manufacturers can reduce the need for extensive trial-and-error experimentation, enabling more efficient design of underfills with targeted thermomechanical properties. Furthermore, this technique will become an indispensable tool for optimizing thermal management and reliability design in next-generation packaging for AI chips and High-Performance Computing (HPC). Ultimately, this research is expected to contribute to the realization of more robust, durable, and long-lasting electronic devices across the semiconductor industry.

Source: https://semiengineering.com/modeling-predicts-cure-and-thermal-endurance-of-advanced-packaging-underfill-nist-ucsd-et-al/

Collected: September 18, 2026 | Automated Research System (Gemini API)

#03 Advanced Packaging Warpage Mitigation: Research Advances in Incorporating Negative Coefficient of Thermal Expansion Materials into Epoxy Molding Compounds and Underfills

Published September 17, 2026 Semiconductor Engineering USA

OVERVIEW

Active research is progressing on utilizing negative coefficient of thermal expansion (CTE) materials in epoxy molding compounds (EMC) and underfills to effectively mitigate warpage in large semiconductor packages. Researchers at Brewer Science highlight the potential of this approach, anticipating significant contributions to thermal stress management and warpage suppression through precise CTE matching between disparate materials. This technology is deemed essential for improving mechanical reliability and manufacturing yields in next-generation high-performance devices.

IN DEPTH

Key Findings

Advanced research is actively exploring the incorporation of negative Coefficient of Thermal Expansion (CTE) materials into epoxy molding compounds (EMC) and underfills to effectively mitigate warpage in large semiconductor packages. This innovative approach promises to significantly improve thermal stress management and warpage control by better matching the CTEs of different materials within the package, which is critical for the reliability of next-generation high-performance devices.

Technical / Clinical Details

Semiconductor packages are complex assemblies composed of various materials—such as silicon dies, substrates, and encapsulants—each possessing distinct CTEs. During temperature fluctuations in manufacturing processes and operational thermal cycling, these CTE mismatches generate significant thermal stresses, leading to package warpage. Negative CTE materials exhibit the unique property of shrinking when heated, making them ideal additives to EMCs and underfills. By incorporating these materials, the expansion of other positive CTE components can be counteracted, effectively bringing the overall package's effective CTE closer to zero. Researchers at Brewer Science indicate that negative CTE materials can leverage various mechanisms to cancel out thermal expansion efficiently. This precise CTE matching technology is crucial for ensuring the reliability of fine-pitch interconnections in advanced packaging types like flip-chip and HBM, thereby extending device longevity and performance stability.

Background & Context

The relentless pursuit of higher performance and miniaturization in semiconductor devices has led to larger package sizes and increasingly complex stacking architectures. For high-performance computing (HPC) and AI chips, thermal management and mechanical reliability are paramount concerns. Package warpage directly impacts manufacturing yield through defects in wire bonds and solder joints, and it compromises the long-term reliability of the final product. Addressing warpage is thus critical for both manufacturing efficiency and product quality. The introduction of negative CTE materials offers a fundamental solution to these challenges, enabling CTE matching that was previously difficult to achieve with conventional materials.

Strategic Significance & Outlook

The application of negative CTE materials in EMCs and underfills represents a pivotal shift in advanced packaging technology. Once established, this technology will empower designers to create larger and more complex stacked package structures with reduced warpage risks. This is expected to accelerate the realization of next-generation high-performance AI accelerators and data center processors. Beyond semiconductors, this approach also holds potential for other thermal-stress-sensitive electronic components and structural materials, contributing to broader advancements in materials science across diverse industrial sectors.

Source: https://semiengineering.com/negative-expansion-materials-resist-warpage/

Collected: September 18, 2026 | Automated Research System (Gemini API)

#05 Advanced AI Chips Face Intensified Thermal Management Challenges: TSMC Plans 20-Layer HBM Integration in 14x Reticle CoWoS by 2028, Microchannel Cooling Emerges as Key Technology

Published September 11, 2026 36氪 China

OVERVIEW

Thermal management has become a critical challenge in advanced-packaged AI chips, particularly due to thermal coupling issues across chiplets in 2.5D, 3D IC, CoWoS, and HBM architectures. TSMC's roadmap for 2028 includes integrating approximately 10 large computing chips with 20 layers of HBM within a 14x reticle-sized CoWoS platform, which is projected to significantly increase thermal density. To address this, microchannel cooling has been identified as the leading thermal management technology for future high-performance AI packages.

IN DEPTH

Key Findings

Thermal management issues have become acutely prominent in advanced-packaged AI chips, with thermal coupling between chiplets in 2.5D, 3D IC, CoWoS, and HBM architectures posing a significant hurdle. TSMC has unveiled plans to integrate around 10 large computing chips and 20 layers of HBM within a 14x reticle-sized CoWoS platform by 2028. This ambitious integration is expected to dramatically increase thermal density, leading microchannel cooling to be identified as the primary thermal management technology for future high-performance AI packages.

Technical / Clinical Details

As AI chip performance escalates, the power consumption and heat generation per unit area have risen sharply. In chiplet architectures, the tight integration of multiple logic dies and HBM stacks exacerbates thermal coupling, leading to hot spot formation and overall temperature increases. TSMC's evolution of CoWoS (Chip-on-Wafer-on-Substrate) technology further intensifies this challenge. The planned 14x reticle-sized CoWoS for 2028 represents a substantial increase in area compared to current standard CoWoS, aiming to integrate up to 10 large computing chips and 20 layers of HBM into a single package. At such high integration densities, conventional air cooling or heat sinks are insufficient. This is where microchannel cooling technology steps in. This technique involves creating minuscule channels (microchannels) directly within or immediately beneath the chip to circulate a cooling fluid, achieving extremely high heat transfer efficiency. This enables efficient heat removal from the chip, maintaining stable operating temperatures crucial for sustained performance.

Background & Context

The increasing complexity and scale of AI models place immense pressure on the computational capabilities of semiconductor chips. With the deceleration of Moore's Law, the semiconductor industry has shifted towards advanced packaging technologies like 2.5D/3D packaging, chiplets, and HBM to achieve performance gains. However, these technologies, by vertically and horizontally integrating chips at high densities, inherently lead to elevated thermal densities, making thermal management the system-level bottleneck. Without effective thermal management solutions, the full potential of AI chips cannot be realized. Roadmaps from leading foundries like TSMC, emphasizing cooling technologies, signal a clear direction for the entire industry.

Strategic Significance & Outlook

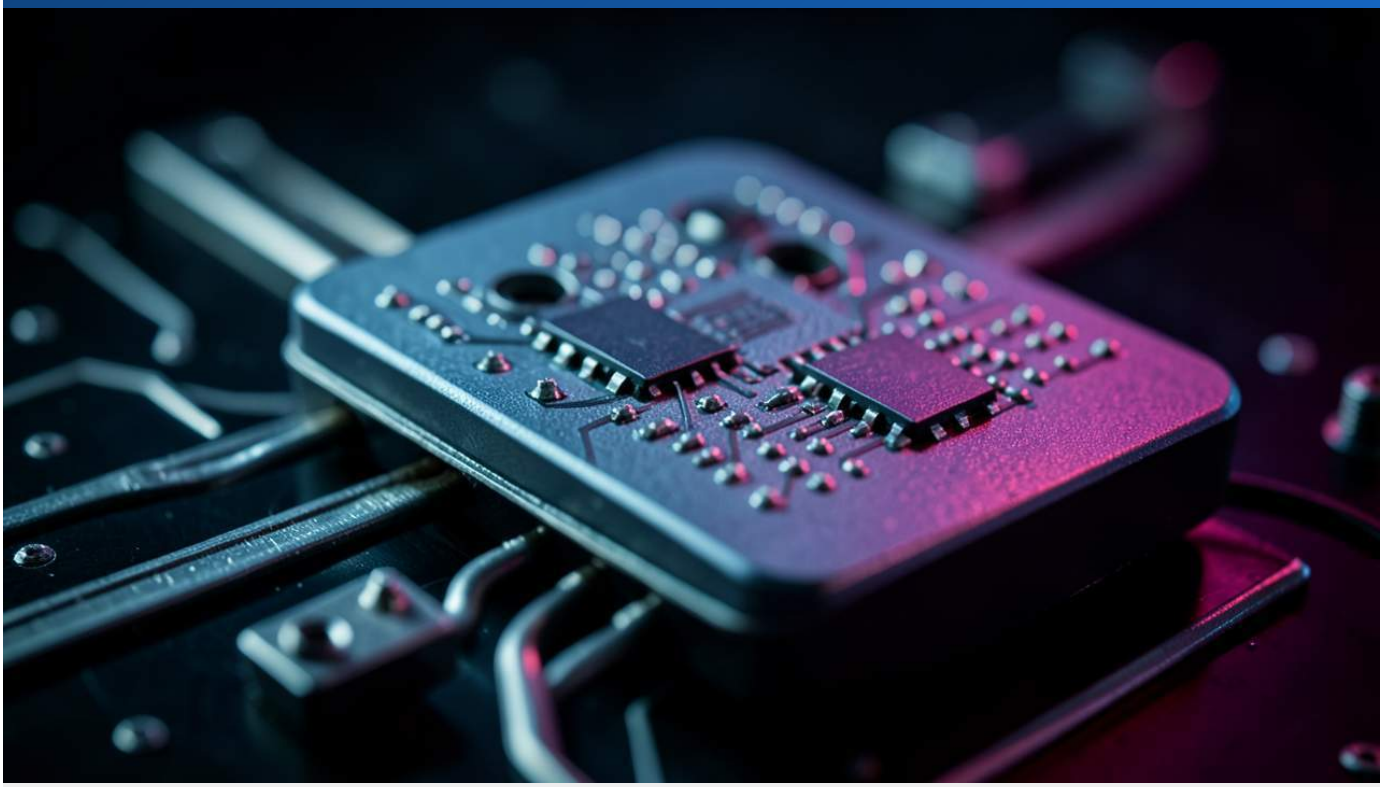
Microchannel cooling technology is set to become an indispensable component for future high-performance AI chips and HPC systems. Its commercial realization will necessitate further innovations in materials science, fluid dynamics, and precision manufacturing techniques. Key areas of focus will include selecting optimal cooling fluids, optimizing channel designs, and developing reliable pumping and piping systems. Integrating cooling systems within the package and their synergy with power delivery are also crucial considerations. Successful deployment of microchannel cooling is expected to break current thermal design limits for AI chips, open new frontiers in AI processing capabilities, and contribute significantly to energy efficiency improvements in data centers worldwide.

Source: https://eu.36kr.com/en/p/3978316580617224

Collected: September 18, 2026 | Automated Research System (Gemini API)

#06 Sub-2nm Nodes Blur Process Boundaries as Chiplet Integration Drives Increased Thermal Density and Structural Stress, Hybrid Bonding Emerges as Key Solution

Published September 10, 2026 Semiconductor Engineering USA



OVERVIEW

At sub-2nm process nodes, shrinking transistors and heightened process sensitivities are blurring traditional manufacturing boundaries, leading to increased thermal density and structural stress in chiplet-based designs. This intensified stress causes warpage and structural instability in thin dies and wafers. To address these critical challenges, advanced bonding techniques such as hybrid bonding are gaining significant attention as a pivotal solution for next-generation semiconductor manufacturing.

IN DEPTH

Key Findings

In semiconductor manufacturing at sub-2nm process nodes, the miniaturization of transistors and increased sensitivity to various processes are blurring the traditional boundaries between manufacturing stages. Critically, the growing trend of integrating numerous dies as chiplets is leading to escalating thermal density and structural stress. This phenomenon results in warpage and structural instability, particularly in the delicate thin dies and wafers. To counteract these profound challenges, hybrid bonding technology is emerging as an indispensable solution.

Technical / Clinical Details

At nodes below 2nm, the behavior of materials at the atomic level profoundly impacts device performance, leading to an intimate interplay between individual processes like etching, deposition, and lithography. Tiny transistors react sensitively to even minor process variations, directly leading to performance degradation and yield reduction. Furthermore, modern high-performance processors increasingly integrate multiple functional blocks as chiplets to boost computational power. While this chiplet aggregation enhances packaging density, it concentrates heat sources, drastically increasing thermal density. Compounding this, the coefficient of thermal expansion (CTE) mismatch between chiplets made of different materials escalates structural stress, raising the risk of warpage and mechanical failure, especially in thin, fragile dies and wafers. Hybrid bonding addresses these issues by enabling direct metal-to-metal and dielectric-to-dielectric bonding. Compared to conventional micro-bump connections, hybrid bonding achieves higher density, lower resistance, and superior thermal conductivity. This optimizes electrical and thermal performance between chiplets and significantly enhances structural stability.

Background & Context

As the physical limits of Moore's Law draw near, the semiconductor industry is extending the concept of 'scaling' beyond mere transistor miniaturization to include 3D stacking and chiplet-based advanced packaging for performance enhancement. However, this approach introduces new challenges related to thermal management, mechanical stress, and manufacturing complexity. Chips fabricated at sub-2nm nodes, in particular, demand unprecedented levels of precision and control. The blurring of process boundaries necessitates holistic optimization from design to manufacturing, requiring tight collaboration across materials science, process chemistry, and equipment technology.

Strategic Significance & Outlook

Hybrid bonding is poised to accelerate its research and development as an indispensable technology for chiplet integration and advanced packaging at sub-2nm nodes. The widespread adoption of this technology will enable the manufacturing of higher-density, more efficient, and more reliable high-performance semiconductor devices, including AI accelerators, CPUs, and GPUs. Furthermore, in response to the blurring of process boundaries, AI and machine learning-driven process optimization, along with co-optimization of materials and processes, are likely to become new standards in semiconductor manufacturing. These technological innovations will be crucial determinants of performance for the next generation of electronics, underpinning future advancements in computing.

Source: https://semiengineering.com/redefining-processes-at-sub-2nm/

Collected: September 18, 2026 | Automated Research System (Gemini API)

#07 Panel Warpage Control Emerges as Key Bottleneck Hindering FOPLP Cost Advantage in Advanced Packaging

Published September 17, 2026 EAA Partners - Substack USA

OVERVIEW

Panel warpage control is identified as a critical bottleneck preventing Fan-Out Panel Level Packaging (FOPLP) from realizing its theoretical cost advantages in advanced semiconductor manufacturing. This issue, particularly relevant for HBM stacking technologies like CoWoS, poses a significant engineering challenge impacting yield and cost across the industry. Solutions hinge on advancements in molding compounds, underfill materials, and ABF films from material suppliers.

IN DEPTH

Key Findings

A major bottleneck in advanced semiconductor packaging, specifically impeding the theoretical cost advantages of Fan-Out Panel Level Packaging (FOPLP), is the control of panel warpage. As technologies like CoWoS for HBM stacking become more prevalent, mitigating warpage in panel-format manufacturing processes is a pressing engineering challenge that directly affects yield and cost, requiring immediate industry attention.

Technical / Clinical Details

FOPLP aims to reduce costs by manufacturing on larger panel formats compared to traditional wafer-level packaging, but this introduces several engineering hurdles. Foremost among these is thermal warpage, caused by the coefficient of thermal expansion (CTE) mismatch among various material layers—substrates, dies, and encapsulants. Such warpage significantly compromises the reliability of fine-pitch interconnects and connections. Addressing this necessitates the meticulous selection of materials with low CTEs, including advanced molding compounds, appropriate underfill materials, and high-quality Ajinomoto Build-up Films (ABF), alongside precise process control.

Background & Context

High-performance computing (HPC) and artificial intelligence (AI) semiconductors demand increasingly faster and more efficient data processing, driving greater reliance on advanced packaging techniques like 3D stacking and chiplet integration. These technologies facilitate high-speed inter-die interfaces through fine-pitch redistribution layers (RDLs), making thermal management and mechanical stability in packaging paramount. The panel warpage problem is not merely a manufacturing inconvenience but a strategic bottleneck dictating the performance and cost-efficiency of next-generation semiconductors.

Strategic Significance & Outlook

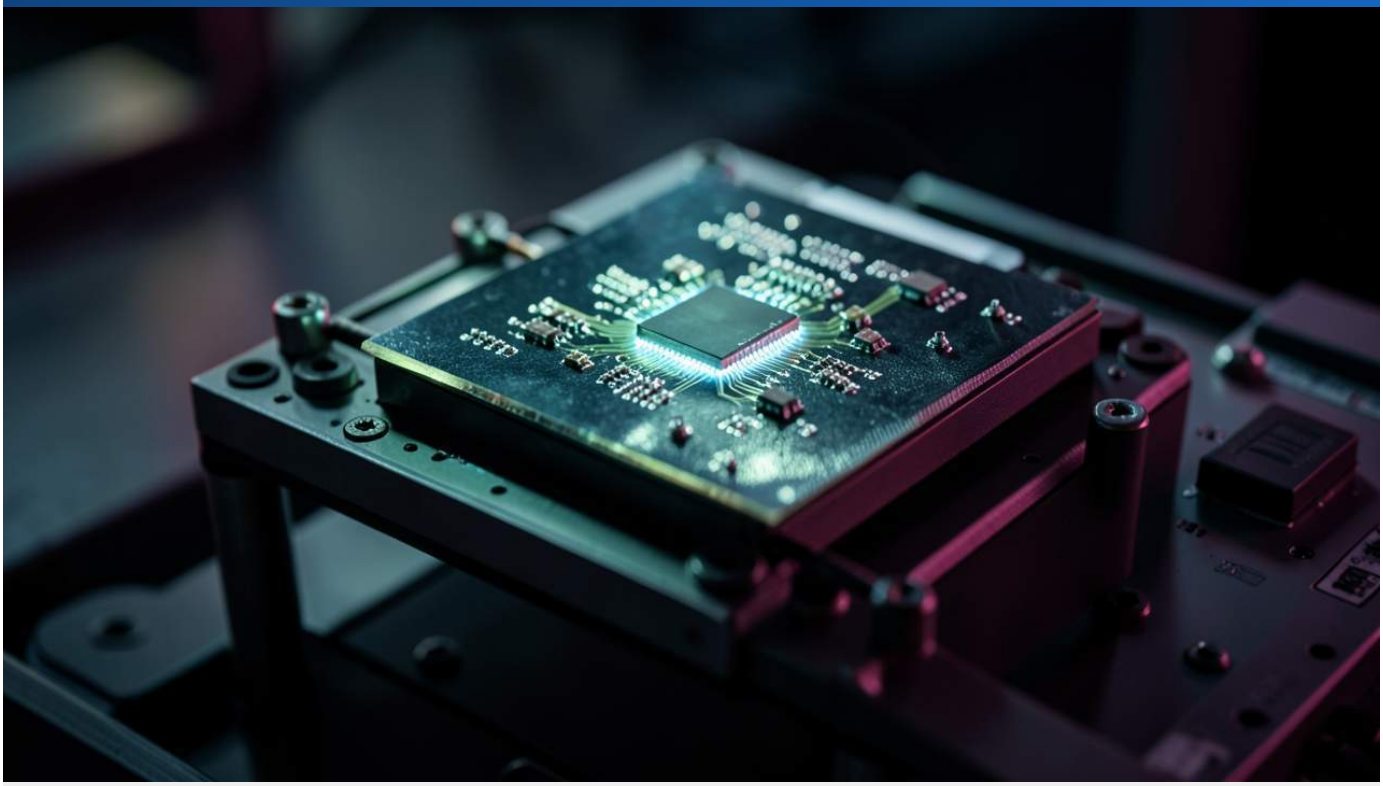
To fully unlock FOPLP's cost advantages, continued innovation in panel warpage control technologies is imperative. This will likely involve a synergistic approach combining advancements in material science, sophisticated simulation techniques, and manufacturing process optimization. Material suppliers are currently investing heavily in developing novel materials with superior low-warpage characteristics. These innovations are expected to significantly contribute to the growth of the advanced packaging market and the overall performance enhancement of semiconductors.

Source: https://eaapartners.substack.com/p/the-bottleneck-is-real-foplp-is-solving

Collected: September 18, 2026 | Automated Research System (Gemini API)

#08 Semiconductor Progress Bottleneck Shifts from Circuit Design to New Material Integration and Interfacial Control

Published September 16, 2026 Astra Trainer USA



OVERVIEW

Astra Trainer reports that the primary constraint on semiconductor advancement has shifted from circuit design to the integration of novel materials. Device failures often occur at interfaces, not within bulk materials, necessitating validation of new material integration without compromising existing stack components. This trend is particularly evident in wide bandgap semiconductors for power electronics, where material science and defect control are now key to technological evolution.

IN DEPTH

Key Findings

Astra Trainer has highlighted a significant shift in the primary bottleneck for semiconductor progress: it is no longer solely circuit design but increasingly the introduction of new materials and their successful integration within existing semiconductor stacks. Crucially, device failures are predominantly observed at the interfaces between different materials rather than within the bulk material itself, positioning material and interfacial behavior as central determinants of next-generation semiconductor performance and reliability.

Technical / Clinical Details

The development of new semiconductor nodes now critically depends on the ability to incorporate novel materials into the device stack and rigorously prove their functionality without detrimental interactions with other components. This is a complex undertaking, requiring not just the discovery of new materials, but a profound understanding and control of how these materials interact with existing manufacturing processes and other layers. In power electronics, particularly with wide bandgap semiconductors like SiC and GaN, the advancement is less about device design and more about the intrinsic quality of materials, the control of crystal defects, and the optimization of interfaces. Operating under high-temperature and high-power conditions, the thermal and mechanical stability of these materials, along with their adhesion and thermal conductivity between different layers, are paramount.

Background & Context

Amidst the deceleration of Moore's Law, the semiconductor industry is confronting the limits of miniaturization, prompting a pivot towards advanced packaging techniques such as 3D stacking, chiplet integration, and the strategic introduction of novel materials to drive performance improvements. In this context, the role of materials science has become more critical than ever. The selection and integration of materials dictate every aspect of semiconductor device performance, including transistor density, power efficiency, signal integrity, and overall reliability. This has led to a surging demand for engineers and researchers with specialized expertise in materials.

Strategic Significance & Outlook

This evolving landscape indicates that materials scientists and engineers will assume an increasingly central role in shaping the semiconductor roadmap. Future semiconductor development will shift its focus from a mere race for miniaturization to the discovery, characterization, and complex integration of innovative materials into intricate multi-layered structures. A deep understanding of material interface physics and chemistry, coupled with advanced defect suppression techniques, is anticipated to be a pivotal driver for the growth of the semiconductor industry moving forward.

Source: https://astratrainer.com/blog/future-industries/materials/semiconductor-materials-jobs

Collected: September 18, 2026 | Automated Research System (Gemini API)

#09 Semiconductor Equipment & Materials Market for HBM, Chiplets, and Low-CTE Materials Forecasted to Outpace Overall Wafer Equipment Growth

Published September 12, 2026 Mobility Foresights India

OVERVIEW

A Mobility Foresights report projects that the semiconductor equipment and materials market supporting sub-3nm logic, HBM, and chiplet integration will grow faster than the overall wafer equipment market. Key drivers include advanced packaging and bonding, interposers, and HBM packaging materials. The report also covers market research on low-CTE materials to limit large package warpage, encapsulants for power modules, and photonic packaging materials, highlighting the increasing importance of materials and equipment in next-generation semiconductor manufacturing.

IN DEPTH

Key Findings

A recent report from Mobility Foresights forecasts that the market for semiconductor equipment and materials supporting next-generation chip manufacturing will expand at a faster rate than the overall wafer manufacturing equipment market. This growth is primarily driven by advancements in sub-3nm logic, high-bandwidth memory (HBM), and chiplet integration technologies, with advanced packaging and bonding techniques, interposers, and specialized HBM packaging materials serving as key growth drivers.

Technical / Clinical Details

The report details the challenges currently facing semiconductor manufacturing and underscores the critical role of materials and equipment in addressing them. To meet the demands for higher performance and density in chips, advanced packaging and bonding technologies are essential. This includes precise die bonding equipment and interposer technologies for connecting multiple chips. HBM packaging materials are crucial for ensuring thermal management and signal integrity in multi-layer memory stacks. Another significant focus is the development of "Low Coefficient of Thermal Expansion (Low CTE)" materials to mitigate warpage issues in increasingly larger packages. Furthermore, encapsulants for power modules are vital for ensuring reliability in high-power environments, and photonic packaging materials are experiencing rising demand in the emerging field of integrating optical communication with electronic circuits. These advancements in materials and equipment significantly enhance semiconductor device performance and reliability, accelerating the development of applications like AI and HPC.

Background & Context

As the semiconductor industry approaches the limits of Moore's Law, chip performance improvements are now heavily dependent not just on miniaturization but also on advanced packaging technologies and innovative materials. HBM and chiplet integration exemplify this new paradigm, maximizing overall system performance and efficiency by tightly integrating chips with diverse functionalities. In such complex structures, physical and chemical compatibility among all components is paramount, necessitating material solutions that can overcome challenges related to heat, mechanical stress, and electromagnetic interference.

Strategic Significance & Outlook

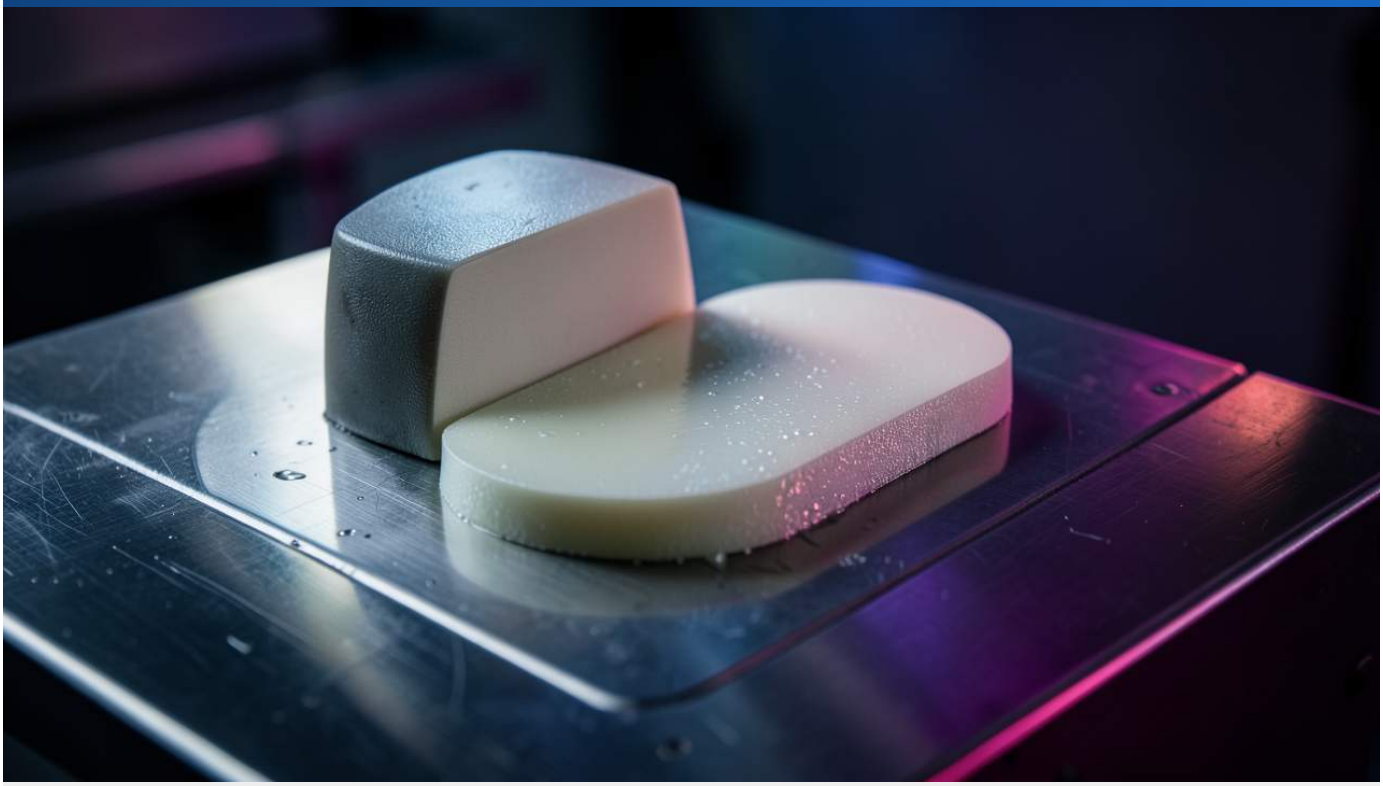
This accelerating growth in the semiconductor equipment and materials market is expected to continue. Investment in materials and equipment related to high-performance packaging, in particular, will remain strong. Companies will enhance their competitiveness by focusing on developing low-CTE materials, high-reliability encapsulants, advanced bonding technologies, and photonic packaging solutions. This trend will foster innovation across the entire semiconductor ecosystem, accelerating the realization of next-generation technologies in fields such as AI, autonomous driving, and cloud infrastructure.

Source: https://mobilityforesights.com/blog/making-advanced-chips-euv-etch-deposition

Collected: September 18, 2026 | Automated Research System (Gemini API)

#10 KAIST Develops Glucose-Derived Bio-Hot-Melt Adhesive from E. coli, Outperforming Petroleum Counterparts on Stainless Steel

Published September 16, 2026 EurekAlert! Science News South Korea



OVERVIEW

Researchers at KAIST have engineered E. coli to produce novel bio-based hot-melt adhesive polymers (poly(4HB-co-PhLA) and poly(3HB-co-4HB-co-PhLA)) from glucose, presenting a sustainable alternative to petroleum-derived adhesives. This biodegradable material demonstrated superior adhesion to stainless steel, achieving 4.58 megapascals (MPa) compared to 4.20 MPa for commercial petroleum-based glues. The breakthrough paves the way for industrial applications in packaging, furniture, electronics, and automobiles, while offering tunability for properties like flexibility and heat resistance.

IN DEPTH

Key Findings

A research team at the Korea Advanced Institute of Science and Technology (KAIST) has successfully developed new bio-based hot-melt adhesive polymers, specifically poly(4HB-co-PhLA) and poly(3HB-co-4HB-co-PhLA), using metabolically engineered E. coli bacteria fed with glucose. This innovative biodegradable adhesive not only offers a sustainable alternative to petroleum-derived glues but also exhibits superior adhesive performance on stainless steel.

Technical Details

- The KAIST team precisely manipulated the metabolic pathways of E. coli to enable the direct biosynthesis of these complex polymers from glucose, establishing a fossil-fuel-independent production process.
- In adhesion strength tests on stainless steel, the bio-adhesive achieved a remarkable 4.58 megapascals (MPa). This figure surpasses the 4.20 MPa recorded by a comparable commercial petroleum-based hot-melt adhesive, indicating a significant advancement in adhesive strength coupled with favorable thermal properties.
- The developed polymers are fully biodegradable and show promising applications across diverse industrial sectors, including packaging, furniture, electronics, and automotive manufacturing. Further research is exploring methods to tune properties such as flexibility and heat resistance, allowing for tailored performance in various end-use scenarios.

Background & Context

Adhesives are ubiquitous in modern manufacturing, but the prevalent reliance on petroleum-based products raises environmental concerns regarding sustainability and waste management. Even in products designed to be biodegradable, the non-biodegradable nature of the adhesives themselves can hinder overall recyclability. The KAIST research directly addresses this challenge by making the adhesive material bio-based and biodegradable, thereby enhancing the sustainability of the entire product lifecycle.

This study underscores the expanding potential of systems metabolic engineering, demonstrating its capability not just for basic polymer synthesis but for producing sophisticated functional materials with high added value. It represents a critical breakthrough in the field of bioplastics.

Strategic Significance & Outlook

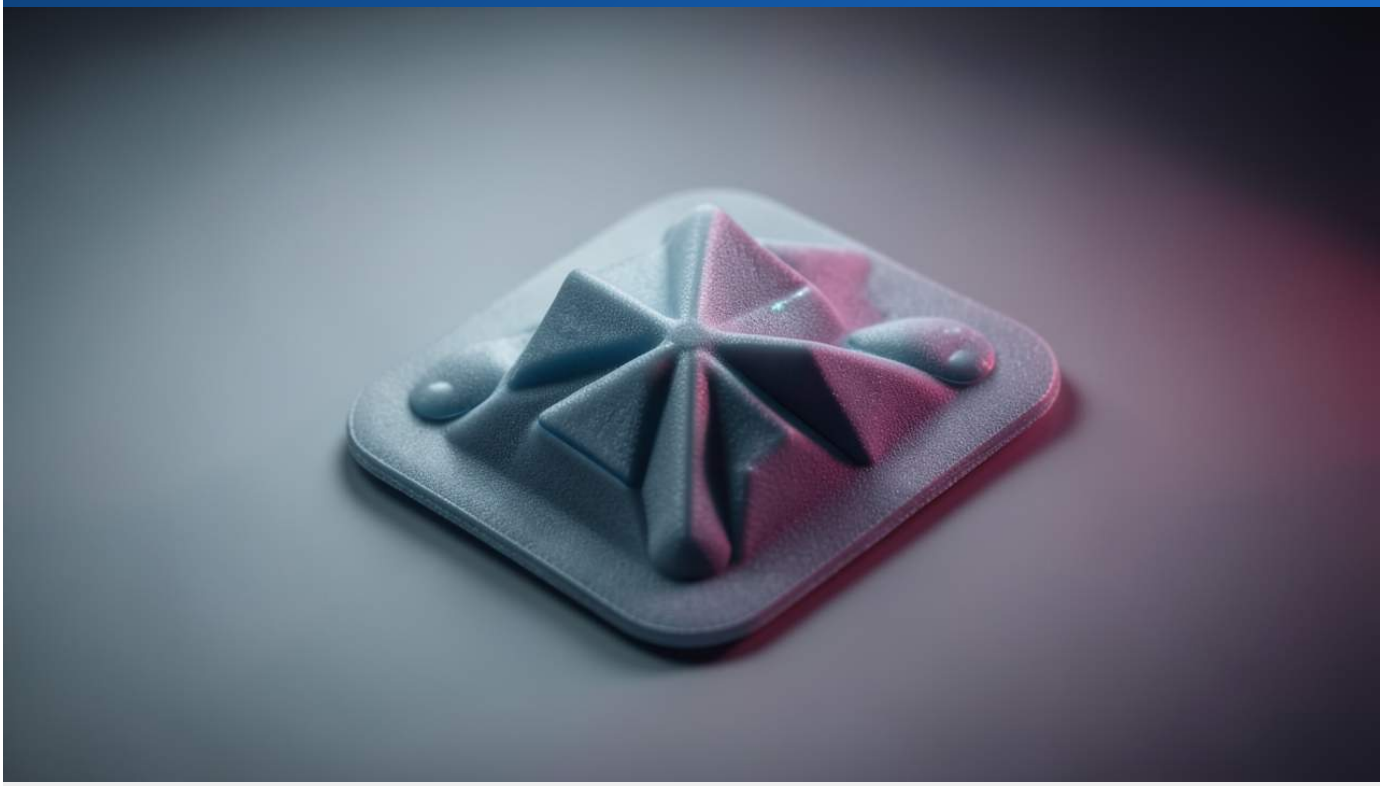
The development of this bio-hot-melt adhesive marks a significant step towards achieving a more sustainable society and advancing green chemistry principles. The ability to produce high-performance adhesives from renewable resources reduces dependence on fossil fuels and mitigates environmental impact. Future efforts will focus on scaling up production, optimizing cost-effectiveness, and conducting extensive validation tests in various industrial applications. Given the growing demand for high-performance and eco-friendly materials, particularly in the automotive and electronics sectors, this technology is poised for widespread commercial adoption.

Source: https://www.eurekalert.org/news-releases/1144212

Collected: September 18, 2026 | Automated Research System (Gemini API)

#11 POSTECH Develops Heat-Releasable Medical Patch with Shape-Memory Pyramid Structure, Minimizing Skin Damage for Fragile Skin

Published September 16, 2026 CHOSUNBIZ South Korea



OVERVIEW

A research team from Pohang University of Science and Technology (POSTECH), in collaboration with Texas Tech and Northwestern Universities, has developed a medical adhesive patch with adjustable adhesion, specifically designed for fragile skin. Utilizing a shape-memory polymer (SMP) with a fine pyramid structure, the patch maintains strong adhesion under normal conditions and allows for easy, low-force removal when heat is applied. This innovation is engineered to significantly reduce skin damage in patients requiring repeated sensor attachment and removal.

IN DEPTH

Key Findings

Researchers at Pohang University of Science and Technology (POSTECH), in partnership with Texas Tech University and Northwestern University, have successfully developed a novel medical adhesive patch that offers adjustable adhesion and easy removal upon heat application. This breakthrough is particularly significant for patients with fragile skin, as it aims to substantially reduce the risk of skin damage associated with medical adhesive use.

Technical / Clinical Details

- The innovative medical patch is based on a shape-memory polymer (SMP) engineered with a fine pyramid-like microstructure on its surface. This unique architecture ensures strong adhesion to the skin under normal conditions, securely holding sensors or dressings in place.
- When subjected to a mild heat stimulus, such as warm water or gentle airflow, the SMP undergoes a shape change. This structural alteration causes the pyramid microstructures to flatten or change configuration, effectively reducing the contact area between the patch and the skin.
- The reduction in contact area dramatically lowers the force required to remove the patch, thereby minimizing irritation and damage to delicate skin. This addresses a common issue with traditional medical adhesives, which often cause stratum corneum stripping or allergic reactions upon removal, especially in vulnerable populations like the elderly, infants, or patients with compromised skin conditions.

Background & Context

Medical adhesive patches are indispensable in healthcare for various applications, including diagnostic sensor attachment, drug delivery, and wound care. However, Medical Adhesive-Related Skin Injury (MARSI) remains a significant challenge, particularly with long-term wear or frequent changes. MARSI can lead to pain, increased infection risk, higher treatment costs, and a substantial decrease in patient quality of life.

This development represents a critical advancement in addressing MARSI by integrating advanced adhesive technology with smart materials science. The utilization of shape-memory polymers provides an elegant solution that simultaneously enhances device usability and patient safety, setting a new standard for medical adhesive design.

Strategic Significance & Outlook

This heat-releasable medical patch is poised to be a transformative tool in home healthcare and the management of chronic conditions requiring frequent monitoring, by significantly reducing patient discomfort. Following clinical trials and regulatory approvals, its practical application will not only improve the quality of life for patients with fragile skin but also alleviate the burden on healthcare providers. Beyond medical uses, this technology holds potential for other industrial applications where controlled, on-demand debonding is desired, offering a versatile platform for future adhesive innovations.

Source: https://biz.chosun.com/en/en-science/2026/09/16/CWTSV2LEQVGCDAOZCXU66HU3DY/

Collected: September 18, 2026 | Automated Research System (Gemini API)

#12 Global Battery Manufacturing Reaches 4 TWh as Adhesives for EV Battery Pack Integration Gain Critical Industrial Relevance

Published September 10, 2026 24ChemicalResearch Unknown

OVERVIEW

As global battery manufacturing reaches 4 terawatt-hours (TWh), adhesives for EV battery pack integration are gaining critical industrial relevance, driven by the shift towards cell-to-pack (CTP) architectures. These multifunctional adhesives provide structural bonding, thermal management, vibration resistance, and electrical insulation. Noteworthy examples include Henkel's Loctite TLB 9270APS, a two-component polyurethane with 2 W/m·K thermal conductivity, and Bergquist TGF 2030APS thermal gap filler at 1.7 W/m·K, addressing the stringent demands of advanced EV battery designs.

IN DEPTH

Key Findings

With global battery manufacturing surging to 4 terawatt-hours (TWh), adhesives are playing an increasingly critical industrial role in electric vehicle (EV) battery pack integration. The accelerating adoption of cell-to-pack (CTP) architectures necessitates the development of multifunctional adhesives capable of structural bonding, efficient thermal management, vibration resistance, and robust electrical insulation.

Technical Details

- The CTP architecture, a key trend in EV battery design, involves integrating battery cells directly into the pack, reducing component count, increasing energy density, and simplifying manufacturing. In this design, adhesives are not merely fasteners but integral components that ensure battery safety and performance.
- Responding to the demand for multifunctional adhesives, Henkel's Loctite TLB 9270APS stands out as a two-component polyurethane thermally conductive adhesive. This material boasts an excellent thermal conductivity of 2 W/m·K, crucial for managing heat dissipation in CTP applications.
- Similarly, Bergquist's TGF 2030APS thermal gap filler is cited for its 1.7 W/m·K thermal conductivity, addressing similar thermal challenges. These materials are essential for efficiently dissipating heat generated by battery cells, preventing overheating that could degrade performance and shorten battery life.
- Beyond thermal properties, these advanced adhesives also provide mechanical protection against shock and vibration for battery cells, and critical electrical insulation to prevent short circuits and current leakage, thereby enhancing the overall reliability and durability of the battery pack.

Background & Context

The burgeoning EV market is driving demand for high-performance and safe battery systems. As more integrated designs like CTP and cell-to-chassis (CTC) replace traditional modular battery packs, the role of adhesion and sealing materials is fundamentally transforming. In these new architectures, adhesives become the 'backbone' of the battery structure and central to thermal management and safety functions, propelling the need for continuous innovation in material science.

Strategic Significance & Outlook

The evolution of EV battery technology will continue to demand even higher performance from adhesives. Future development will focus on achieving superior thermal conductivity, enhanced mechanical strength, faster curing times, and improved sustainability features like reworkability and recyclability. Adhesive manufacturers must deepen their collaboration with automotive and battery producers to deliver innovative solutions that meet the stringent requirements of next-generation EV batteries, which will be key to maintaining market competitiveness.

Source: https://www.24chemicalresearch.com/blog/31707/battery-manufacturing-hits-twh-ev-battery-pack-integration-adhesives

Collected: September 18, 2026 | Automated Research System (Gemini API)

#13 Taiyo Holdings Launches Next-Gen Semiconductor Packaging Material 'FPIM Series,' First to Achieve 700nm CD Three-Layer RDL on 12-inch Wafers

Published September 10, 2026 PR Newswire Japan

OVERVIEW

Taiyo Holdings, in collaboration with imec, has launched its "FPIM Series," a next-generation semiconductor packaging material that enables the first successful formation of a three-layer Redistribution Layer (RDL) with 700-nm Critical Dimension (CD) on 12-inch wafers. This negative-tone photosensitive insulating material for damascene processes is crucial for fine-pitch wiring in advanced semiconductor packaging, particularly for submicron-class RDL design rules, marking a significant breakthrough in enabling high-density integration.

IN DEPTH

Key Findings

Taiyo Holdings has unveiled its "FPIM Series," a groundbreaking next-generation semiconductor packaging material developed in collaboration with imec. This innovative material has achieved a world-first by enabling the successful formation of a three-layer Redistribution Layer (RDL) with a 700-nanometer (nm) Critical Dimension (CD) on 12-inch wafers, marking a substantial leap forward for fine-pitch wiring in advanced semiconductor packaging.

Technical / Clinical Details

- The FPIM Series is a negative-tone photosensitive insulating material specifically designed for damascene processes, which are critical for forming high-density and reliable interconnects in advanced semiconductor fabrication.
- The successful demonstration of three-layer RDL formation with a 700nm CD represents a significant technical achievement. It overcomes previous challenges in stacking multiple ultra-fine wiring layers, which is essential for meeting submicron-class RDL design rules.
- This technology is poised to accelerate the evolution of advanced packaging solutions, including flip-chip and fan-out packaging, which are indispensable for high-performance processors, AI chips, and chiplet integration in High-Performance Computing (HPC) where dense interconnections are paramount.
- The introduction of the FPIM Series is expected to drive further miniaturization, increased operating speeds, and improved power efficiency of semiconductor devices, thereby fostering innovation across diverse applications such as data centers, mobile devices, and IoT hardware.

Background & Context

As the semiconductor industry grapples with the physical limits of Moore's Law, the focus of miniaturization and performance enhancement has increasingly shifted towards advanced packaging technologies. Within this paradigm, particularly with the rise of chiplet architectures and 3D stacking, the RDL—responsible for electrical connections between chips—has become a decisive factor for device performance. Achieving multi-layer RDLs with critical dimensions in the 700nm class has historically presented significant technical hurdles in terms of manufacturability and reliability.

The collaboration between Taiyo Holdings and imec leverages their combined expertise in cutting-edge material development and process technology, and this breakthrough is anticipated to significantly impact the semiconductor industry's technology roadmap.

Strategic Significance & Outlook

The FPIM Series is set to contribute substantially to improving performance and reducing costs in next-generation semiconductor packaging, solidifying Taiyo Holdings' position in the highly competitive semiconductor market. Looking forward, this technology is expected to be applied to even finer RDL pitches and more complex multi-layered structures, forming a foundational technology that supports the continued advancement of data-intensive applications like AI and HPC. It also holds significant implications for enhancing the global presence of Japanese material manufacturers within the semiconductor supply chain.

Source: https://www.prnewswire.com/news-releases/taiyo-holdings-launches-next-generation-semiconductor-packaging-material-fpim-series-achieving-its-first-three-layer-rdl-formation-with-700-nm-cd-on-12-inch-wafers-302874600.html

Collected: September 18, 2026 | Automated Research System (Gemini API)

#14 Henkel Unveils Low-Diisocyanate PUR Hot-Melt Adhesives and More at SICAM 2026 to Boost Furniture Production Efficiency

Published September 17, 2026 Henkel Germany

OVERVIEW

Henkel showcased new adhesive solutions at SICAM 2026 aimed at significantly improving efficiency in furniture production. Key innovations include the Technomelt PUR 260/x ME family of PUR hot-melt adhesives with low free diisocyanates for enhanced worker safety and high-performance edge banding. Additionally, Technomelt KS 928 for high feed speeds (10-50+ m/min) and Technomelt PUR 6258 reactive hot-melt for profile wrapping were introduced, all designed to reduce rework, accelerate cycle times, and provide durability in demanding environments like kitchens and bathrooms.

IN DEPTH

Key Findings

Henkel has introduced a suite of new adhesive solutions at SICAM 2026, specifically engineered to enhance the efficiency of furniture production. These innovations are primarily focused on reducing rework and accelerating cycle times, aiming to elevate both the quality and productivity across critical furniture manufacturing stages, from edge banding to profile wrapping.

Technical / Clinical Details

- **Technomelt PUR 260/x ME Family**: This polyurethane reactive (PUR) hot-melt adhesive family is designed for edge banding applications, with a key feature being its 'low free diisocyanate' content. This significantly improves workplace safety, aligning with stringent new European safety regulations. It offers high bonding strength and water resistance, ensuring excellent durability even in high-humidity environments such as kitchens and bathrooms.
- **Technomelt KS 928**: This hot-melt adhesive is optimized for high feed speeds of 10 to 50+ meters per minute, thereby increasing the throughput of production lines. This contributes to enhanced productivity in high-volume furniture factories.
- **Technomelt PUR 6258**: A reactive hot-melt adhesive tailored for profile wrapping, it provides strong and uniform adhesion even on complex-shaped components. Its superior bonding power and durability extend product lifespan and ensure high-quality finishes.
- Collectively, these adhesives streamline manufacturing processes, shorten curing times, and reduce bonding defects, minimizing rework and shortening overall cycle times. This enables more cost-efficient production operations.

Background & Context

The furniture industry faces increasing demands for diverse aesthetics, enhanced functionality, improved durability, and greater sustainability from consumers. Particularly for products exposed to moisture, such as kitchen and bathroom furniture, the water resistance and durability of adhesives are directly linked to product longevity. Simultaneously, improving production efficiency and ensuring worker safety are ongoing challenges in manufacturing. The shift towards low-free diisocyanate adhesives directly addresses the tightening of EU occupational health and safety regulations, contributing to a general uplift in industry safety standards.

Strategic Significance & Outlook

Henkel's new adhesive solutions provide furniture manufacturers with powerful tools to rapidly adapt to market changes and efficiently produce high-quality, safe products. These technological advancements not only enhance the durability and functionality of furniture but also contribute to improving working conditions in manufacturing plants. It is anticipated that these adhesives will be widely adopted as a crucial factor in boosting the competitiveness of the furniture manufacturing industry, especially as smart factory initiatives continue to advance.

Source: https://www.henkel.com/press-and-media/press-releases-and-kits/2026-09-16-less-rework-faster-cycle-times-2240430

Collected: September 18, 2026 | Automated Research System (Gemini API)

#15 TESA Revolutionizes Car Design and Assembly with Advanced Automotive Adhesives for EV Electrification and HMI Evolution

Published September 16, 2026 TESA Germany

OVERVIEW

TESA's advanced automotive adhesive solutions are crucial for the evolving car design and assembly, especially with the shift towards electric vehicles (EVs) and sophisticated human-machine interfaces (HMI). Their comprehensive portfolio spans bonding, mounting, masking, protection, sealing, thermal management, grounding, shielding, and hole covering. These adhesives ensure durability, weight reduction, and reliability in critical applications like EV battery assembly, thereby enhancing overall vehicle performance and safety.

IN DEPTH

Key Findings

TESA's advanced automotive adhesive solutions are delivering essential innovations in car design and assembly, driven by the rapid transition to electric vehicles (EVs) and the evolution of sophisticated human-machine interfaces (HMIs). These adhesives provide the foundational elements for ensuring durability, weight reduction, and reliability across a wide range of automotive applications, including critical EV battery assembly.

Technical Details

- TESA's extensive adhesive portfolio covers a broad spectrum of functionalities:
  - **Bonding and Mounting**: Securely fastens components, providing structural integrity.
  - **Masking and Protection**: Offers precise masking in processes like painting and acts as a protective layer against external damage.
  - **Sealing**: Prevents ingress of water, dust, and noise, enhancing cabin comfort and component longevity.
  - **Thermal Management**: Efficiently dissipates heat from EV batteries, crucial for maintaining battery performance and safety.
  - **Grounding and Shielding**: Provides electrical grounding to prevent electronic malfunctions and offers electromagnetic shielding.
  - **Hole Covering**: Effectively seals openings in vehicle bodies and components, balancing aesthetics with functionality.
- Compared to traditional mechanical fastening methods, these adhesives contribute to overall vehicle lightweighting by reducing the number of parts and simplifying assembly processes. Lightweighting is directly linked to extended driving range and improved energy efficiency in EVs.
- In EV battery assembly, specific adhesives such as thermally conductive and flame-retardant types play vital roles in securing battery cells, preventing thermal runaway, and ensuring waterproofing and dustproofing. This ensures the safety and long-term performance of the battery system.

Background & Context

The automotive industry is undergoing a once-in-a-century transformation driven by the "CASE" trends: Connected, Autonomous, Shared, and Electric. For EVs, battery pack safety, efficiency, and lightweighting are paramount, while HMI advancements are directly linked to improved information delivery and usability for drivers and passengers. Addressing these new requirements necessitates advanced material solutions like adhesives, as traditional fastening methods such like welding or screwing alone are proving insufficient.

Strategic Significance & Outlook

TESA's advanced automotive adhesives will increasingly play a critical role in the evolution of the automotive industry. As EV battery technology continues to innovate, in-vehicle HMIs become more sophisticated, and autonomous vehicles become widespread, there will be an escalating demand for adhesives with superior functionality, reliability, and manufacturing efficiency. TESA aims to remain a core partner in supporting the safety, performance, and sustainability of next-generation vehicles by addressing these technological challenges.

Source: https://www.tesa.com/en/industry/markets/automotive

#16 KAIST Develops Smartphone-Controlled Adhesive Microneedle Electronic Medicine for Remote Pain Management

Published September 13, 2026 Ground News (Yonhap News Agency) South Korea

OVERVIEW

A KAIST-led research team, in collaboration with the Korea Institute of Oriental Medicine, has developed an adhesive microneedle electronic medicine for smartphone-controlled remote pain management. This innovative patch adheres to the skin and allows for wireless regulation of therapeutic delivery, marking a significant advance in medical adhesive applications for drug delivery and health monitoring. The technology promises enhanced patient convenience and personalized at-home treatment, reducing the need for frequent clinical visits.

IN DEPTH

Key Findings

A research team at KAIST, in collaboration with the Korea Institute of Oriental Medicine, has successfully developed an adhesive microneedle electronic medicine capable of remote control via a smartphone. This groundbreaking technology enables a patch to adhere to the skin, facilitating wireless drug delivery and health monitoring for pain management. This advancement signifies a major leap in medical adhesive applications, offering patients unprecedented convenience and access to personalized care from their homes.

Technical and Clinical Details

The developed electronic medicine utilizes an adhesive patch embedded with an array of ultra-fine microneedles. These microneedles minimize skin irritation while efficiently delivering therapeutic agents directly into the body. This targeted approach offers a significant advantage over traditional oral medications or injections by potentially reducing systemic side effects. The system integrates wireless control, allowing users to precisely adjust dosage and timing of medication through a dedicated smartphone application. This real-time adjustability enables highly personalized pain management tailored to individual patient needs. While specific communication protocols were not detailed, it is likely based on common wireless technologies like Bluetooth for user-friendly operation. Furthermore, the patch is anticipated to incorporate embedded biosensors for continuous monitoring of pain levels and other physiological parameters, creating a feedback loop for optimized treatment. The adhesive component is designed using medical-grade materials, ensuring prolonged and stable adherence while mitigating allergic reactions.

Background and Industry Context

Chronic pain affects a vast global population, driving high demand for effective and convenient pain management solutions. Existing treatment modalities often present challenges such as medication compliance issues and the necessity for frequent clinic visits, imposing a significant burden on patients. This new technology addresses these limitations, particularly benefiting elderly individuals and those in remote areas by improving healthcare accessibility. The medical adhesive market is rapidly expanding, with applications ranging from diagnostics to therapeutics and health monitoring. The convergence of advanced adhesives with smart patches and wearable devices is creating new market segments, positioning this development as a key innovation. This Korean-led research underscores the country's strong capabilities in medical technology innovation.

Future Outlook

Beyond pain management, this adhesive microneedle electronic medicine holds promise for broader applications in drug delivery systems for other diseases and as a continuous biosignal monitoring device. Future integrations with AI-driven personalized medicine platforms could establish it as a core component of advanced, self-contained healthcare ecosystems. While further clinical trials and regulatory approvals are required for market entry, its realization is expected to invigorate the mobile healthcare market and accelerate the shift towards patient-centric care models. Continued miniaturization of the device and reduction in manufacturing costs would pave the way for wider adoption globally, transforming how chronic conditions are managed.

Source: https://ground.news/article/pain-can-be-remotely-managed-via-smartphone-development-of-adhesive-microneedle-electronic-medicine_e49016

Collected: September 18, 2026 | Automated Research System (Gemini API)

#17 Samsung Electro-Mechanics and Qualcomm Jointly Develop Organic Bridge Technology for 2.1D AI Semiconductor Packaging

Published September 14, 2026 The Elec South Korea

OVERVIEW

Samsung Electro-Mechanics and Qualcomm are collaboratively developing an advanced "organic bridge" technology for 2.1D packaging in AI semiconductors. This innovation utilizes organic materials, akin to PCBs, instead of silicon to interconnect multiple dies within a single package, offering a competitive alternative to Intel's EMIB. The organic bridge facilitates ultrafine circuitry, significantly boosting I/O density and bandwidth crucial for next-generation AI processing.

IN DEPTH

Key Findings

Samsung Electro-Mechanics and Qualcomm are jointly developing a pioneering “organic bridge” technology for advanced 2.1D packaging of AI semiconductors. This innovative approach replaces traditional silicon interposers with organic materials, similar to those found in printed circuit boards (PCBs), to connect multiple semiconductor dies within a single package. The technology promises a significant boost in I/O (input/output) density and data bandwidth, addressing critical bottlenecks in high-performance AI processing.

Technical and Clinical Details

The organic bridge technology is being developed to overcome the cost and manufacturing complexities associated with silicon-based bridges. By leveraging the flexibility and ease of processing inherent in organic materials, this technology enables the creation of ultra-fine circuitry on an organic layer, facilitating high-density electrical connections between chips. This potentially allows for the fabrication of larger bridges, integrating more dies efficiently and increasing the overall I/O count of the package. Organic materials can also offer advantageous thermal expansion coefficients compared to silicon, which can help in mitigating stress between dissimilar materials. Samsung Electro-Mechanics aims to apply this organic bridge technology to 2.1D packaging, essential for enhancing AI semiconductor performance, thereby contributing to the increased processing power of data centers and edge AI devices. This development positions the organic bridge as a strong alternative to silicon bridges like Intel’s Embedded Multi-die Interconnect Bridge (EMIB), intensifying competition in the advanced packaging sector.

Background and Industry Context

The rapid advancement of AI necessitates semiconductor capabilities that can process immense amounts of data at ever-increasing speeds. Consequently, advanced packaging techniques, such as 2.5D and 3D integration, have become paramount for integrating multiple chips into a single package. Interconnect technologies, particularly for efficiently linking High Bandwidth Memory (HBM) and high-performance computing cores, are crucial determinants of AI semiconductor performance. While silicon interposers have been widely used in conventional 2.5D packaging, they face challenges related to high manufacturing costs and size limitations. Organic bridge technology offers a cost-effective solution to these issues, providing greater design flexibility and manufacturing process adaptability. The collaboration between Samsung Electro-Mechanics and Qualcomm is a strategic move, combining Samsung Electro-Mechanics' expertise in advanced packaging with Qualcomm's prowess in AI chip design, to establish a leading position in the next-generation AI semiconductor market.

Future Outlook

The organic bridge technology is poised to significantly enhance AI semiconductor performance and cost-efficiency, accelerating the adoption of AI applications across various sectors including data centers, edge AI, and automotive industries. As this technology matures and is implemented, it will enable the design of more complex and higher-performing AI chips, potentially resolving one of the current major bottlenecks in semiconductor manufacturing. Further optimization of organic material choices and manufacturing processes could lead to even greater performance improvements and cost reductions in the future. If this technology scales to mass production, it is expected to influence the packaging strategies of competitors like Intel and TSMC, thereby fostering broader technological innovation across the industry.

Source: https://www.thelec.net/news/articleView.html?idxno=13907

Collected: September 18, 2026 | Automated Research System (Gemini API)

#18 Non-Woven Adhesives Market Grows; Bostik Expands APAO Production, Henkel Co-Develops Bio-Based Hot Melt

Published September 16, 2026 SNS Insider India

OVERVIEW

This article is an overview of a market research report published by SNS Insider. The non-woven adhesives market is experiencing growth, primarily driven by increasing demand from hygiene product manufacturers. Bostik expanded its APAO adhesive production capacity with a new manufacturing line in 2026, targeting elastic attachment applications. Additionally, Henkel partnered with a leading manufacturer in 2026 to co-develop a bio-based hot-melt adhesive for sustainable baby care product lines, demonstrating a strong focus on eco-friendly formulations.

IN DEPTH

This article is an overview of a market research report published by SNS Insider.

Report Overview

This report provides a detailed analysis of the current market size, share, and growth trends of the non-woven adhesives market from 2026 to 2035. It emphasizes that increasing demand from the hygiene products industry is a primary driver of market growth.

Key Findings

The non-woven adhesives market is experiencing steady growth, predominantly propelled by heightened demand from manufacturers of hygiene products. Adhesives for non-wovens are critical in products such as disposable diapers, feminine hygiene products, and adult incontinence products, enhancing comfort, reliability, and manufacturing efficiency. Bostik, a key player in the market, responded to this rising demand by expanding its production capacity for APAO (Amorphous Polyalphaolefin) adhesives for elastic attachment applications with a new manufacturing line in 2026. This strategic move aims to stabilize product supply and maintain or expand its market share. Furthermore, in response to growing environmental consciousness, Henkel partnered with a leading manufacturer in 2026 to co-develop a bio-based hot-melt adhesive specifically for sustainable baby care product lines. This initiative highlights a strong market trend towards environmentally friendly and sustainable adhesive solutions, reflecting the proactive stance of companies in their development efforts.

About the Publisher

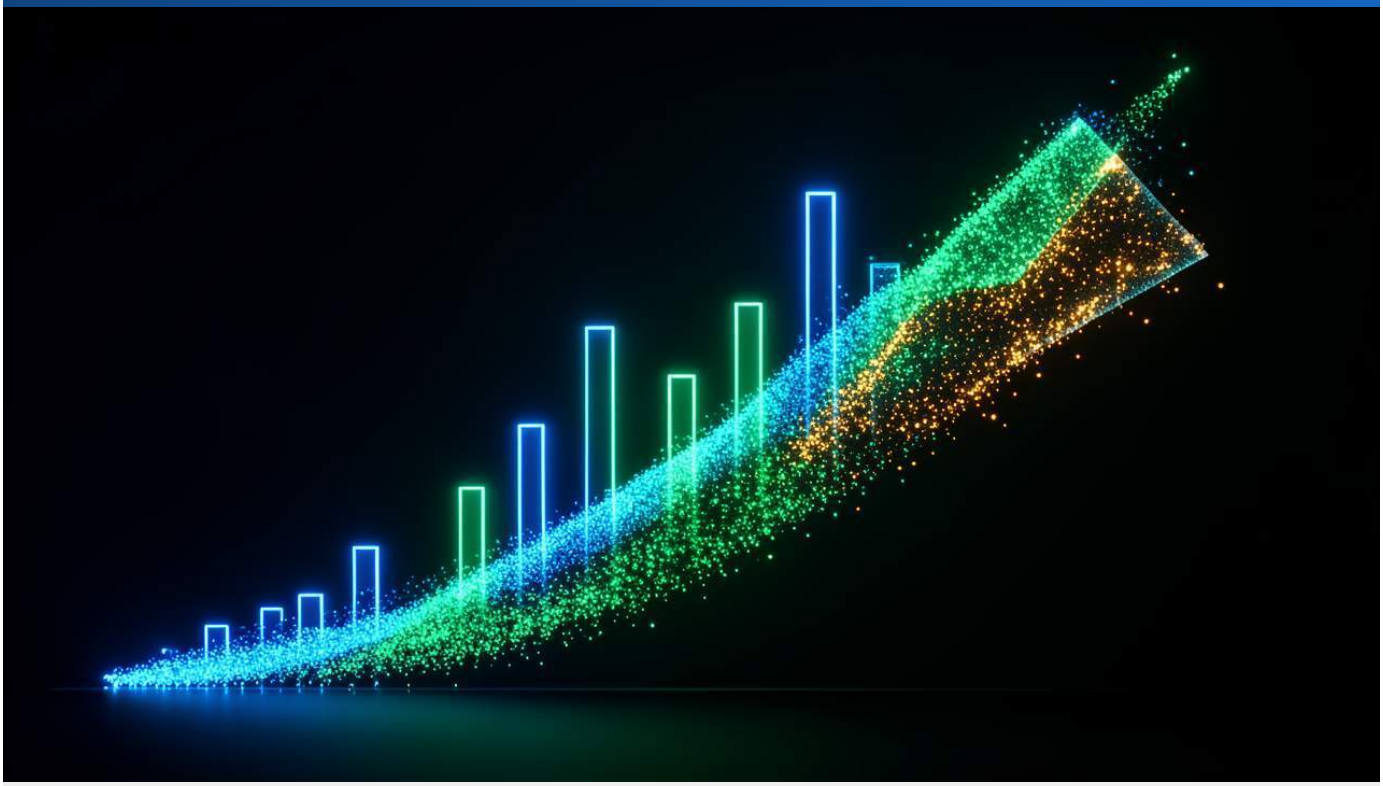
SNS Insider is a company that provides market research reports and business intelligence covering a wide range of industries. They assist businesses in making strategic decisions through data-driven insights and analysis.

Source: https://www.snsinsider.com/reports/non-woven-adhesives-market-11124

Collected: September 18, 2026 | Automated Research System (Gemini API)

#19 Gel-Based Cooling Pad Market Poised for Growth Through 2035, Driven by Biopharma Cold Chain and EV Demand

Published September 17, 2026 IndexBox Global



OVERVIEW

The global gel-based cooling pads market is projected for substantial growth through 2035, primarily fueled by the expanding biopharma cold chain, consumer electronics, and electric vehicle (EV) battery pack applications. Innovation is concentrated on developing gel formulations with superior thermal conductivity to meet stringent thermal management and safety requirements. Despite competition from other thermal interface materials, regulatory pressures for improved battery safety are a key growth driver.

IN DEPTH

Key Findings

The gel-based cooling pads market is set for significant expansion through 2035, with demand particularly strong from the biopharmaceutical cold chain, consumer electronics, and custom-shaped pads for EV battery packs. A major focus of innovation is on developing gel formulations that offer enhanced thermal conductivity, crucial for efficient heat dissipation and ensuring the stable performance of sensitive components.

Technical / Clinical Details

Growth in this sector is intrinsically linked to two major technological trends: the increasing miniaturization and power density of electronic devices, and the imperative for robust thermal management in EV battery systems. For biopharma, precise temperature control during transport is critical, making custom gel pads ideal for maintaining efficacy. In electronics, higher thermal conductivity gels facilitate more effective heat transfer from components to heat sinks, preventing performance degradation and extending device lifespan. For EV batteries, these pads play a vital role in thermal runaway prevention, a critical safety concern, by distributing and dissipating heat across the battery modules.

Background & Context

Historically, thermal management has relied on various materials, but gel-based solutions offer flexibility and conformability, making them suitable for complex geometries and delicate components. The increasing regulatory scrutiny on battery safety, particularly in the automotive sector, is compelling manufacturers to invest in advanced thermal interface materials. While competing with phase change materials (PCMs), graphite sheets, and liquid cooling solutions, gel-based pads carve out a niche due to their ease of application, cost-effectiveness for certain volumes, and adaptability.

Strategic Significance & Outlook

The market’s trajectory underscores the broader trend of thermal management becoming a central design consideration, not merely an afterthought. For manufacturers in electronics and automotive, selecting high-performance gel-based cooling pads can be a differentiating factor in product reliability and safety. Investment in R&D for next-generation gel chemistries will be paramount for market players to gain a competitive edge, focusing on materials with even higher thermal conductivity, greater durability, and environmental sustainability. This segment's growth reflects its integral role in enabling the continued advancement of high-performance computing, advanced electronics, and sustainable mobility solutions.

Source: https://www.indexbox.io/blog/gel-based-cooling-pads-market-forecast-to-2035-driven-by-biopharma-cold-chain-expansion/

Collected: September 18, 2026 | Automated Research System (Gemini API)

#20 Penn State and Kurt J. Lesker Company Form Atomic-Scale Processing Hub for Semiconductors and Quantum Tech

Published September 10, 2026 Penn State USA

OVERVIEW

Penn State University and Kurt J. Lesker Company have established a strategic partnership to accelerate advanced atomic-scale processing methods crucial for semiconductors, advanced packaging, quantum, and photonic technologies. This collaboration aims to create a center of excellence focused on precise material control at the atomic level, driving innovation and talent development. The initiative is critical for overcoming materials challenges in next-generation electronic devices.

IN DEPTH

Key Findings

Penn State University and the Kurt J. Lesker Company have forged a strategic partnership to accelerate the development of advanced atomic-scale processing methods, critical for leading-edge applications in semiconductors, advanced packaging, quantum computing, and photonic technologies. This collaboration establishes a “center of excellence” dedicated to advancing techniques like atomic layer deposition (ALD) and atomic layer etching (ALE), thereby solidifying U.S. leadership in these crucial technological domains.

Technical / Clinical Details

The joint initiative leverages Penn State's robust research infrastructure with Kurt J. Lesker Company's state-of-the-art equipment and technical expertise. The focus areas include a comprehensive suite of advanced thin-film deposition and processing techniques, such as electron beam evaporation, thermal evaporation, sputtering, plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), and atomic layer etching (ALE). This synergistic approach enables the creation of complex multilayer structures and precise material control at the atomic scale, foundational for enhancing the performance of next-generation devices. Specific contributions are anticipated in semiconductor miniaturization, high-density packaging, improved quantum bit stability, and the realization of low-loss photonic circuits.

Background & Context

The rapid advancements in modern microelectronics, quantum information science, and photonics are profoundly dependent on breakthroughs in materials science. Precise control over materials at the atomic level is the linchpin determining device performance, reliability, and energy efficiency. Penn State boasts a long-standing reputation for excellence in materials science, while the Kurt J. Lesker Company is an industry leader in vacuum technology and thin-film equipment. This partnership is deemed essential for addressing the formidable technical challenges in this field and for ensuring the United States maintains and strengthens its global competitiveness in these strategically vital technologies.

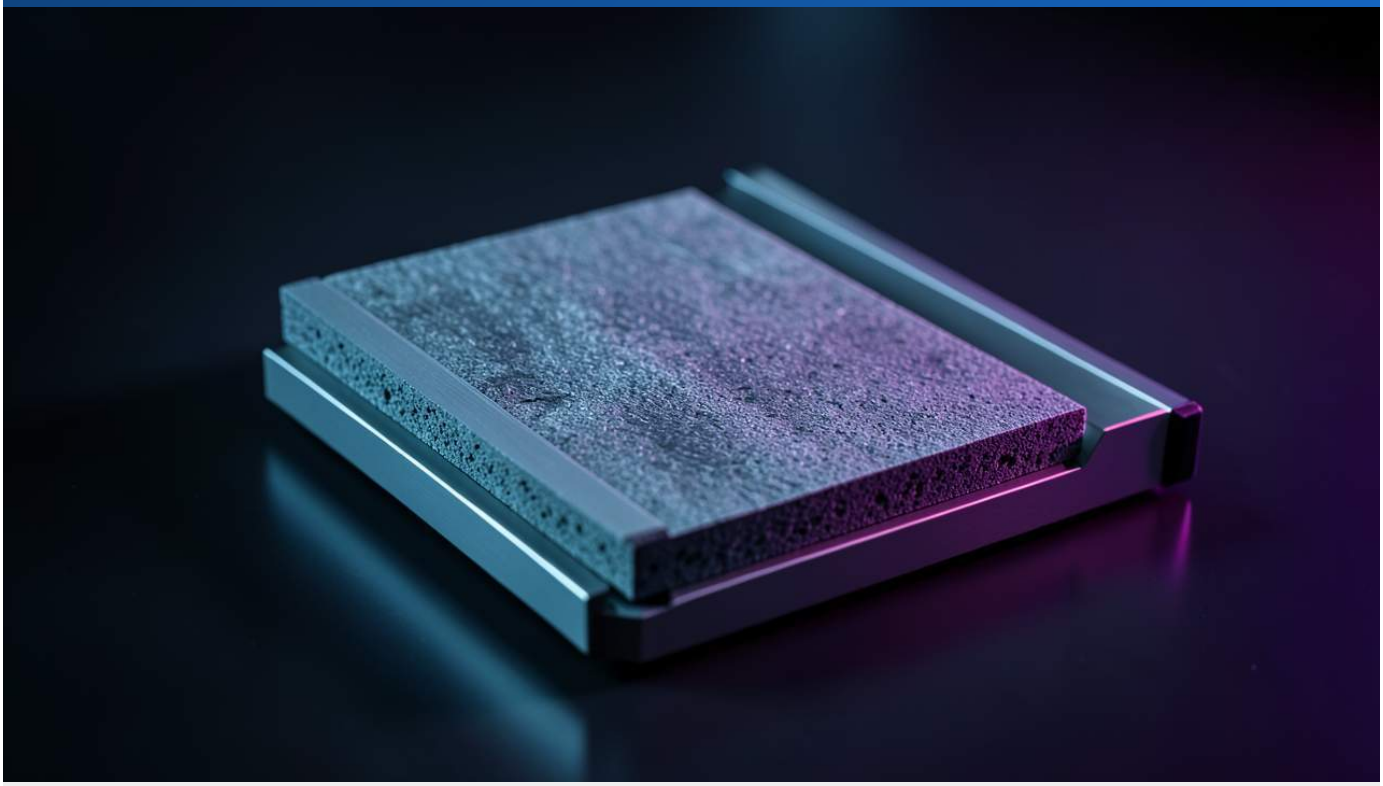
Strategic Significance & Outlook

This academic-industrial partnership exemplifies a model for accelerating the translation of research findings into commercial applications. Furthermore, it is expected to provide invaluable educational programs and training opportunities for the next generation of scientists and engineers. Such initiatives will expedite the development of novel manufacturing processes, optimize existing technologies, and ultimately lead to the market introduction of high-performance, energy-efficient electronic components, driving technological innovation across a broad spectrum of industrial sectors. The focus on atomic-scale precision positions the collaboration at the forefront of materials engineering, offering solutions that will impact everything from consumer electronics to advanced defense systems.

Source: https://www.psu.edu/news/materials-research-institute/story/penn-state-kurt-j-lesker-company-partner-advance-atomic-scale

#21 NovoLINC Unveils MaxLINC, Achieving Industry-Leading 0.7 mm²•K/W Thermal Resistance for Multi-Kilowatt AI Chips

Published September 17, 2026 PR Newswire (NovoLINC) Unknown



OVERVIEW

NovoLINC has launched MaxLINC, an advanced thermal interface material (TIM) designed for high-performance AI computing, achieving an industry-leading thermal resistance as low as 0.7 mm²•K/W. This new TIM offers over 20% cooling energy savings for AI servers compared to current products, effectively addressing the critical thermal bottleneck in multi-kilowatt AI accelerators. NovoLINC is expanding operations to support the growing demand and commercialization of MaxLINC.

IN DEPTH

Key Findings

NovoLINC has announced the launch of MaxLINC, an advanced thermal interface material (TIM) engineered specifically for high-performance AI computing, achieving an industry-leading thermal resistance as low as 0.7 mm²•K/W. This breakthrough product is capable of delivering over 20% cooling energy savings for AI servers compared to current industry offerings, thereby resolving a critical thermal bottleneck faced by multi-kilowatt AI accelerators.

Technical / Clinical Details

MaxLINC features a proprietary material design that ensures exceptionally high thermal conductivity and superior interfacial contact properties. The thermal resistance value of 0.7 mm²•K/W signifies its unparalleled efficiency in transferring heat from high-power components, such as CPUs and GPUs, to their respective heatsinks. This capability allows AI chips to operate at higher clock frequencies and maintain optimal junction temperatures, leading to enhanced stability, improved performance, and extended operational lifespans. The material's superior thermal performance directly translates into significant reductions in power consumption for cooling systems, which is a major operational cost for data centers, especially given the exponential increase in power density of high-output AI chips.

Background & Context

The rapid advancements in artificial intelligence (AI) and high-performance computing (HPC) have led to a dramatic surge in processor power consumption and heat generation. For multi-kilowatt AI accelerators in particular, thermal management has emerged as a primary bottleneck limiting both performance and reliability. Traditional thermal interface materials have struggled to efficiently dissipate such extreme heat loads, often leading to system throttling, reduced lifespan, and increased risk of failure. MaxLINC’s introduction provides a much-needed solution to this pressing industry challenge, enabling the design and deployment of next-generation AI infrastructure.

Strategic Significance & Outlook

The deployment of MaxLINC is set to establish a new benchmark in AI chip cooling technology, significantly boosting the performance and energy efficiency of data centers and edge AI devices. NovoLINC is actively expanding its operations to meet the anticipated demand and facilitate the broad commercialization of this industry-leading TIM. MaxLINC is expected to be widely adopted across all applications requiring critical thermal management, including AI supercomputers, cloud servers, and autonomous driving systems. Its ability to enable more powerful and efficient AI hardware positions it as a foundational technology supporting the continued exponential growth and advancement of AI.

Source: https://www.prnewswire.com/news-releases/novolinc-launches-maxlinc-achieving-industry-leading-0-7-mmkw-thermal-resistance-for-multi-kilowatt-ai-chips-302882340.html

#22 KAIST Engineers E. coli to Produce Glucose-Based Biodegradable Hot-Melt Adhesives, Outperforming Petroleum Counterparts

Published September 17, 2026 Mirage News (referencing KAIST) South Korea

OVERVIEW

KAIST researchers have developed a glucose-based adhesive as an alternative to petroleum-derived hot-melt adhesives by genetically engineering *Escherichia coli* to produce novel aromatic polyhydroxyalkanoate (PHA) polymers. This bio-based adhesive demonstrates promising adhesive performance and thermal properties suitable for applications in packaging, furniture, electronics, and automobiles. The successful production of two new adhesive materials from glucose, particularly polymers with 24–34 mol% 4HB showing excellent adhesive performance, marks a significant advance in sustainable material solutions.

IN DEPTH

Key Findings

Researchers at KAIST (Korea Advanced Institute of Science and Technology) have successfully developed a glucose-based adhesive that serves as a sustainable alternative to petroleum-derived hot-melt adhesives. This innovation was achieved by engineering *Escherichia coli* to produce novel aromatic polyhydroxyalkanoate (PHA) polymers. The resulting bio-based adhesive exhibits promising adhesive performance and thermal properties, making it suitable for a wide range of applications including packaging, furniture, electronics, and automobiles.

Technical / Clinical Details

The research team initially engineered *E. coli* to produce 4-hydroxybutyrate (4HB), an aromatic monomer. By feeding glucose to these modified bacteria, they efficiently synthesized PHA copolymers incorporating 4HB and other monomers. Notably, polymers containing 24–34 mol% of 4HB demonstrated excellent adhesive performance, closely matching or even surpassing that of conventional petroleum-based hot-melt adhesives. This bio-synthetic process offers a significantly lower environmental footprint compared to traditional petrochemical manufacturing, enabling the production of adhesives from renewable resources. This contributes to reduced energy consumption and CO2 emissions throughout the adhesive's lifecycle, enhancing overall sustainability.

Background & Context

Hot-melt adhesives are extensively used across numerous industries, including packaging, woodworking, and electronics assembly, due to their rapid curing and strong bonding capabilities. However, the vast majority of these adhesives are derived from petroleum, raising significant environmental concerns regarding resource depletion and pollution. With a global push towards reducing plastic waste and transitioning to sustainable materials, the development of high-performance, biodegradable adhesives from renewable sources has become a critical imperative. KAIST's research provides an innovative biotechnological approach to address this pressing challenge.

Strategic Significance & Outlook

The development of this glucose-based, bio-derived adhesive represents a crucial step forward in accelerating environmentally conscious product development. With its superior adhesive performance and thermal properties, it holds the potential to replace existing petroleum-based hot-melt adhesives, significantly improving sustainability in the manufacturing of packaging materials, furniture, electronic components, and automotive interiors. Future research will likely focus on optimizing production costs and scaling up to large-scale manufacturing, which will further facilitate the market penetration of bio-based adhesives. This innovation is expected to make a substantial contribution to the transition towards a circular economy and the realization of industries with reduced environmental impact.

Source: https://www.miragenews.com/kaist-creates-glucose-based-adhesive-alternative-1745846/

Collected: September 18, 2026 | Automated Research System (Gemini API)

#23 Tata Electronics Invests $3 Billion in India's First Semiconductor Packaging Facility, Partners with Besi to Boost Advanced Packaging

Published September 17, 2026 Tata Electronics India

OVERVIEW

Tata Electronics announced a $3 billion investment in India's first indigenous semiconductor packaging facility in Jagiroad, Assam, and a strategic partnership with advanced packaging equipment provider Besi. This collaboration aims to significantly enhance India's advanced packaging capabilities by leveraging Besi's cutting-edge technologies. The initiative is set to accelerate technology readiness and foster innovation within India's burgeoning semiconductor ecosystem, strengthening its global supply chain position.

IN DEPTH

Key Findings

Tata Electronics has announced a significant investment of $3 billion to establish India's first indigenous semiconductor packaging facility in Jagiroad, Assam. Concurrently, the company has formed a strategic partnership with Besi (BE Semiconductor Industries N.V.), a leading provider of advanced packaging equipment and technologies. This dual initiative aims to substantially bolster India's advanced packaging capabilities within its rapidly developing semiconductor ecosystem.

Technical / Clinical Details

The core of this partnership involves integrating Besi's state-of-the-art advanced packaging equipment and processes, including die bonding, flip-chip, and surface-mount technologies (SMT), into Tata Electronics' new facility. Besi's technologies are renowned for enabling high-precision and high-yield semiconductor device production, from wafer processing to final packaging. This collaboration will specifically accelerate the development of fine-pitch interconnects and advanced thermal management solutions, which are crucial for high-density integrated chips used in AI and high-performance computing (HPC) applications. By doing so, India will establish the capability to manufacture and package complex semiconductor devices domestically, enhancing its position in the global supply chain.

Background & Context

Semiconductors form the backbone of the modern economy, with their importance growing exponentially across sectors like AI, 5G, and IoT. The Indian government, as part of its "Make in India" initiative, has prioritized establishing domestic semiconductor manufacturing capabilities as a national strategic imperative. Currently, India heavily relies on imported semiconductors, which poses geopolitical risks and supply chain vulnerabilities. The partnership between Tata Electronics and Besi is a pivotal step towards overcoming this dependency and building a self-reliant semiconductor ecosystem within India. Besi's extensive experience globally, including a strong presence in the Asia-Pacific region, makes it an ideal partner for this technological leap.

Strategic Significance & Outlook

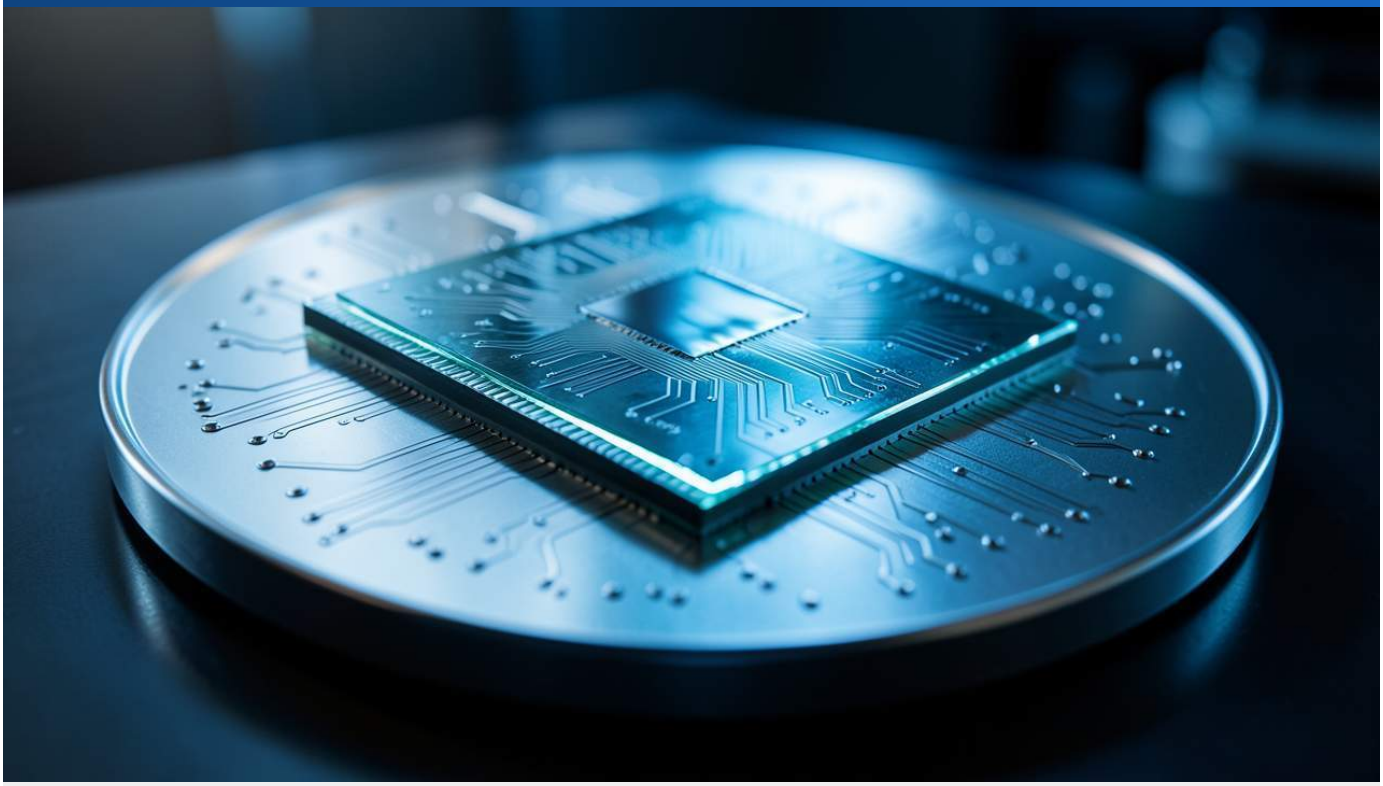
This $3 billion investment and strategic alliance with Besi represent a landmark development for India's semiconductor industry. The new facility is expected to create hundreds of thousands of jobs, fostering further investment in related supply chain companies and research institutions. In the long term, it aims to establish India as a key hub for advanced packaging technology, significantly strengthening the country's role in the global semiconductor supply chain. This move is essential for India to maintain competitiveness in the future digital economy and enhance its geopolitical autonomy, reducing reliance on external semiconductor manufacturing capabilities.

Source: https://www.tataelectronics.com/w/tata-electronics-and-besi-enter-strategic-partnership-to-strengthen-advanced-packaging-capabilities

Collected: September 18, 2026 | Automated Research System (Gemini API)

#24 Taiyo Holdings Achieves First 700nm CD Three-Layer RDL Formation on 12-Inch Wafers with New FPIM Series for Advanced Semiconductor Packaging

Published September 10, 2026 Morningstar (Taiyo Holdings Co. Ltd.) Japan



OVERVIEW

Taiyo Holdings has launched its "FPIM Series" next-generation semiconductor-packaging material, achieving the industry's first three-layer Redistribution Layer (RDL) formation with a 700-nm critical dimension (CD) on 12-inch wafers. Developed in collaboration with imec since October 2022, this material is optimized for dual damascene processes essential for fine-pitch wiring in advanced semiconductor packaging. The breakthrough was presented at the 11th IEEE Electronics System-Integration Technology Conference, pushing the boundaries of high-density chip interconnects.

IN DEPTH

Key Findings

Taiyo Holdings Co. Ltd. has unveiled its "FPIM Series," a next-generation semiconductor-packaging material that has achieved the world's first three-layer Redistribution Layer (RDL) formation with a 700-nanometer critical dimension (CD) on 12-inch wafers. This groundbreaking material is specifically designed for dual damascene processes, which are crucial for realizing fine-pitch wiring in advanced semiconductor packaging applications.

Technical / Clinical Details

The "FPIM Series" material enables the formation of extremely fine wiring patterns in advanced packaging technologies such as Fan-Out Wafer Level Packaging (FOWLP). The successful achievement of a 700nm CD three-layer RDL allows for high-density, high-performance chip interconnections that were previously challenging with conventional packaging technologies. RDLs play a vital role in establishing electrical connections between the chip and the external package, and their miniaturization directly translates to increased signal transmission speeds and reduced package sizes. This material has been developed through a collaborative research effort with imec, a world-leading research and innovation hub in nanoelectronics and digital technologies, since October 2022. The synergy between imec’s advanced process capabilities and Taiyo Holdings’ material expertise was instrumental in this achievement. The detailed findings were presented at the 11th IEEE Electronics System-Integration Technology Conference, where its efficacy was validated by industry experts.

Background & Context

The rapid advancements in AI, 5G, and high-performance computing (HPC) demand semiconductor chips with higher performance, greater integration, and lower power consumption. While chip miniaturization has driven performance improvements in the past, it is approaching physical limits. Consequently, advanced packaging technologies, which efficiently connect multiple chips and components without further shrinking chip dimensions, have become the new frontier for the semiconductor industry. The miniaturization of RDLs is an indispensable technology for these advanced packaging methods, particularly FOWLP and 2.5D/3D packaging, enabling high-performance data processing and efficient power delivery.

Strategic Significance & Outlook

The "FPIM Series" is expected to make a significant contribution to the development of high-performance semiconductors used in next-generation smartphones, data center servers, and autonomous vehicles. The 700nm CD three-layer RDL formation technology pushes the current limits of semiconductor packaging performance, enabling further chip density and speed enhancements. Taiyo Holdings plans to continue deepening its collaboration with imec, leveraging this foundational technology to drive further innovations in semiconductor packaging materials. This strategic move is anticipated to further strengthen Japan’s technological leadership in material science within the global semiconductor supply chain, providing critical enablers for future digital advancements.

Source: https://www.morningstar.com/news/pr-newswire/20260910hk44704/taiyo-holdings-launches-next-generation-semiconductor-packaging-material-fpim-series-achieving-its-first-three-layer-rdl-formation-with-700-nm-cd-on-12-inch-wafers

Collected: September 18, 2026 | Automated Research System (Gemini API)

#25 TESA Unveils Innovative Adhesive Solutions to Meet Demands of Miniaturized and Complex Electronic Devices

Published September 16, 2026 TESA Germany

OVERVIEW

TESA is showcasing its innovative electronic adhesive solutions engineered for bonding, mounting, sealing, cushioning, shielding, and encapsulation in increasingly small and complex electronic devices. These solutions enable precise application at high production rates while ensuring reliable performance and product quality across diverse applications, including smartphones, displays, and wearables. TESA underscores its pivotal role in developing cutting-edge adhesives that address the evolving challenges of the electronics industry.

IN DEPTH

Key Findings

TESA is actively providing innovative adhesive solutions designed to meet the rigorous demands of increasingly miniaturized and complex electronic devices. These advanced adhesives facilitate multiple critical functions—including bonding, mounting, sealing, cushioning, shielding, and encapsulation—thereby enhancing both the reliability and production efficiency of high-performance electronics.

Technical & Clinical Details

TESA's electronic adhesive solutions are characterized by their capability for precise application at high production rates. This portfolio includes ultra-thin tapes, specialized thermally curing adhesives, and custom die-cut components. These solutions ensure consistent performance and product quality across a wide spectrum of applications, from display-equipped devices like smartphones and tablets to wearables, smart home devices, and automotive electronics. For instance, TESA offers customized products that address complex requirements such as securing curved displays, safely mounting batteries, protecting sensitive electronic components from moisture and dust, and providing electromagnetic shielding. This contributes directly to improving device durability and reducing failure rates, which are paramount in today's competitive electronics market.

Background & Context

The electronics market is in a perpetual state of evolution, driven by the relentless pursuit of miniaturization, enhanced performance, and diversified design. Consequently, internal component layouts are becoming denser, requiring adhesives that offer not only traditional bonding but also advanced functionalities such as thermal conductivity, electrical insulation, shock resistance, and shielding properties. TESA, leveraging its extensive experience in adhesive technology and strong R&D capabilities, has developed products that meet these stringent demands. This technological leadership is crucial for electronic device manufacturers to manage trade-offs among design flexibility, manufacturing costs, and product reliability, which are constant challenges in the industry.

Strategic Significance & Outlook

TESA's innovative adhesive solutions are positioned as foundational technologies supporting the future evolution of the electronics industry. Especially in rapidly developing sectors such as microelectronics, flexible devices, and IoT devices, adhesive performance can dictate the overall success or failure of a product. Therefore, the role of technology leaders like TESA is becoming increasingly critical. Through continuous research and development, the company is expected to continue addressing new challenges posed by next-generation electronic devices, ensuring its continued relevance and leadership in this dynamic market.

Source: https://www.tesa.com/en/industry/markets/electronics

Collected: September 18, 2026 | Automated Research System (Gemini API)

#26 3M Launches Cooling Film Reflecting Over 85% Solar Radiation, Cutting Vehicle Interior Temperatures by up to 10°F Without Energy Input

Published September 15, 2026 Simply Wall St News USA

OVERVIEW

3M has introduced its 3M Cooling Film, a roof-applied heat management product for vehicles that reflects over 85% of solar radiation, reducing interior temperatures by up to 10°F (approx. 5.6°C) without consuming additional energy. This innovation targets last-mile fleets, refrigerated trucks, trailers, and passenger rail, offering a critical solution to high cooling costs and cargo protection challenges. The launch underpins 3M's turnaround strategy, focusing on novel product innovation and operational efficiency to drive sustainable growth and market leadership.

IN DEPTH

Key Findings

3M has unveiled its new 3M Cooling Film, a groundbreaking heat management product designed for vehicle roofs, capable of reflecting over 85% of solar radiation. This innovative film significantly lowers interior temperatures by up to 10°F (approximately 5.6°C) without requiring any additional energy input, presenting a transformative solution for the transport sector grappling with high cooling costs and the imperative of cargo protection.

Technical and Application Details

- **High Reflectivity:** The 3M Cooling Film achieves its exceptional performance by reflecting more than 85% of incident solar radiation, dramatically mitigating heat build-up within vehicle cabins and cargo areas. This efficiency is superior to many existing passive cooling solutions.
- **Energy-Free Operation:** As a passive thermal management technology, the film operates without drawing power, fuel, or external energy, leading directly to reduced operational costs for vehicle operators. This makes it a versatile solution for electric, hybrid, and conventional internal combustion engine vehicles.
- **Targeted Markets:** Primary applications include last-mile delivery fleets, refrigerated trucks, trailers, and passenger rail vehicles, where stringent temperature control is essential. Industries such as food and beverage, pharmaceuticals, and logistics stand to benefit significantly from enhanced product integrity and cost efficiency.

Background and Industry Context

The transportation industry faces persistent pressures from escalating fuel prices, tightening environmental regulations, and the growing importance of maintaining cold chain integrity, particularly in last-mile logistics. Conventional refrigeration systems in vehicles are energy-intensive, contributing substantially to both operating expenses and carbon emissions. The 3M Cooling Film offers a straightforward, cost-effective, and highly efficient answer to these challenges through a simple film application process.

This product launch is strategically aligned with 3M's ongoing business transformation initiatives. The company is committed to leveraging new product innovation and operational efficiencies to enhance profitability and strengthen its competitive position. The introduction of the cooling film represents a significant milestone in this strategy, especially as global demand for sustainable and energy-efficient solutions continues to surge.

Future Outlook

The market introduction of the 3M Cooling Film is poised to redefine energy efficiency standards in the transportation sector. It offers a triple benefit of reduced operational costs, lower environmental impact, and improved cargo quality, which is highly appealing to vehicle manufacturers and fleet operators. For 3M, this product is expected to become a substantial revenue driver in a high-growth market, potentially influencing its stock performance positively by demonstrating concrete progress in its innovation and sustainability goals.

Source: https://simplywall.st/stocks/us/capital-goods/nyse-mmm/3m/news/cooling-film-launch-could-matter-for-3m-stock-mmm

Collected: September 18, 2026 | Automated Research System (Gemini API)

#27 Tyndall National Institute Unveils Three Papers at ESTC 2026 Advancing Photonic Packaging and Chiplet Integration

Published September 16, 2026　Tyndall National Institute　アイルランド

OVERVIEW

Researchers from Tyndall National Institute presented three pivotal papers at ESTC 2026, showcasing significant innovations in photonic packaging, co-packaged optics, and chiplet integration technologies. Dr. Sharon Butler demonstrated scalable manufacturing for healthcare and sensing with a co-packaged bio-imaging system integrating hybrid lasers on a glass interposer. Concurrently, Dr. Arun Kumar Malik introduced silicon interposer technology, exploring a standardized 2.5D chiplet integration framework for high-density electrical interconnections, marking a breakthrough in next-generation semiconductor design.

IN DEPTH

Key Findings

Researchers from Tyndall National Institute presented three significant papers at the European Semiconductor Technology Conference (ESTC) 2026, highlighting advanced innovations in photonic packaging, co-packaged optics, and chiplet integration technologies. These presentations contribute substantially to improving performance and manufacturing efficiency for next-generation electronics and photonics systems, particularly demonstrating breakthroughs in medical bio-imaging systems and high-performance computing semiconductor packaging.

Technical / Clinical Details

- **Co-Packaged Bio-Imaging System (Dr. Sharon Butler):**
  - Dr. Butler's presentation focused on the development of a co-packaged bio-imaging system utilizing hybrid laser integration on a glass interposer. This system integrates optical devices and electronic circuits within the same package, leading to miniaturization, enhanced performance, and improved energy efficiency.
  - This technology holds immense promise for diverse applications in medical diagnostics, environmental sensing, and life science research. Its demonstrated scalable manufacturing capability paves the way for future mass production, leveraging glass interposers for their superior optical properties and electrical isolation, ideal for high-density optoelectronic integration.
- **Silicon Interposer Technology for 2.5D Chiplet Integration (Dr. Arun Kumar Malik):**
  - Dr. Malik's research detailed silicon interposer technology for advanced chiplet-based packaging. This foundational technology enables the high-density integration of multiple chiplets—small semiconductor dies with different functionalities—within a single package.
  - His work explores a standardized 2.5D chiplet integration framework to facilitate high-density electrical interconnections, promising enhanced processing capabilities, faster data transfer rates, and reduced power consumption. This technology is critical for supporting future computing demands, including AI chips, high-performance data centers, and edge computing.

Background & Context

As the limits of Moore's Law become increasingly apparent, advanced packaging technologies have gained paramount importance for achieving system-level performance improvements in the semiconductor industry. Specifically, co-packaged optics (CPO) and chiplet technologies, which integrate multiple diverse functionalities, are considered key to expanding data bandwidth and enhancing energy efficiency. The research by Tyndall National Institute directly contributes to the advancement of these cutting-edge technologies.

Photonic packaging enables the seamless integration of electronic and optical signals, addressing bottlenecks in data centers and communication networks. Meanwhile, chiplet integration offers the flexibility and cost efficiency to combine chips fabricated on different process nodes or by various foundries, thereby accelerating the development of application-specific integrated circuits (ASICs).

Strategic Significance & Outlook

The achievements presented by Tyndall National Institute are expected to have a profound impact on the future of the semiconductor and photonics sectors. The scalable co-packaged bio-imaging system, in particular, could drive the miniaturization and performance enhancement of medical diagnostic devices, leading to the creation of novel healthcare solutions. Furthermore, the 2.5D chiplet integration framework is poised to significantly boost the performance of AI processors and data centers, making it an indispensable technology for the evolving digital infrastructure. Tyndall's efforts reinforce Ireland's position as a critical hub for semiconductor technology innovation in Europe.

Source: https://www.tyndall.ie/news/tyndall-researchers-showcase-advanced-packaging-innovation-through-three-published-papers-at-estc-2026/

Collected: September 18, 2026 | Automated Research System (Gemini API)

#28 Researchers Develop Wafer-Scale Bonded Active Photonics Interposer: Pioneering Low-Loss, High-Bandwidth Optoelectronic Integration

Published September 17, 2026 EurekAlert! USA

OVERVIEW

Researchers have developed a wafer-scale bonded active photonics interposer that integrates photonic devices with electronic circuits at the wafer level, enabling low-loss, high-bandwidth communication with mass production scalability. This technology leverages through-silicon vias and advanced wafer-bonding techniques to overcome traditional integration challenges related to scalability, yield, alignment, and thermal management. This breakthrough significantly advances optoelectronic integration in microchips, paving the way for next-generation high-performance computing and communication systems.

IN DEPTH

Key Findings

Researchers have successfully developed a wafer-scale bonded active photonics interposer, a significant breakthrough that dramatically enhances the integration of optical and electronic components within microchips. This innovative technology directly bonds photonic devices with electronic circuits at the wafer level, resolving critical challenges inherent in conventional integration methods such as scalability, yield, alignment precision, and thermal management. The result is the achievement of low-loss, high-bandwidth communication between optoelectronic components, establishing a clear pathway for mass production.

Technical / Clinical Details

- **Wafer-Level Bonding:** The core of this technology lies in bonding entire wafers containing photonic devices and electronic circuits, rather than packaging individual chips. This approach significantly improves alignment accuracy, streamlines manufacturing processes, and enhances overall yield rates.
- **Leveraging Through-Silicon Vias (TSVs):** Through-silicon vias are vertical electrical connections that penetrate silicon wafers, enabling high-density 3D integration. In this interposer, TSVs establish robust electrical links between optoelectronic components, shortening signal paths and thereby boosting performance and efficiency.
- **Low-Loss, High-Bandwidth Communication:** The intimate integration of light and electronics minimizes signal loss during data transmission while achieving extremely high bandwidths. This is crucial for applications demanding rapid data processing, such as data centers, AI processors, and high-performance computing (HPC) systems.
- **Scalability and Thermal Management:** Wafer-level manufacturing inherently offers excellent scalability, enabling cost-effective mass production. Furthermore, the advanced bonding techniques optimize heat dissipation between devices, effectively addressing thermal management challenges that typically arise during high-performance operation.

Background & Context

Modern microchips are approaching the fundamental limits of their processing capabilities, with electronic signal speed and power consumption increasingly becoming bottlenecks. To overcome these limitations, optoelectronic integration—the merging of photonics (light) with electronics—has emerged as a key area of focus. Traditional optoelectronic integration methods, which involve manufacturing separate optical and electronic components and then assembling them, have been constrained by costs, complexity, and performance limitations.

The wafer-scale bonded active photonics interposer has the potential to fundamentally transform this landscape. Silicon photonics is an attractive option for the semiconductor industry due to its compatibility with existing CMOS manufacturing processes. This new technology maximizes the potential of silicon photonics, contributing to advancements in data communication speeds and energy efficiency, and thereby laying the groundwork for next-generation computing systems.

Strategic Significance & Outlook

The development of this wafer-scale bonded active photonics interposer marks a paradigm shift in microchip design. It promises to enable revolutionary advancements across various fields, including reduced power consumption in data centers, accelerated processing speeds for AI training models, and expanded bandwidth for optical communication networks. Furthermore, this technology holds the potential to open doors to new application areas such as miniaturized high-performance sensors, advanced medical diagnostic devices, and even quantum computing, positioning it as a crucial foundational technology that will accelerate the growth of the entire semiconductor industry.

Source: https://www.eurekalert.org/news-releases/1144463