

TROY TECHNICAL

SEMICONDUCTOR BACK-END WEEKLY REPORT

October 10 - October 16, 2026 | Issue 2026-W41

**Package performance, process yield, test
coverage and qualified capacity**

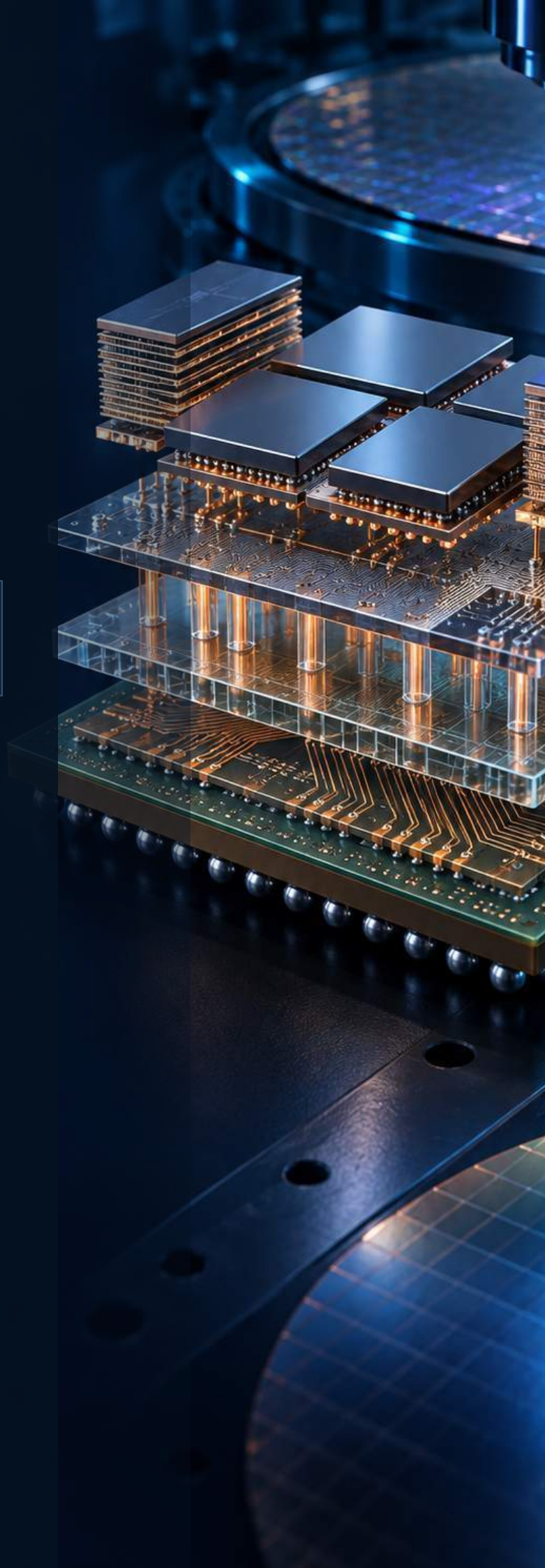
20

ANALYZED ARTICLES

10

PRIORITY THEMES

Issued 2026-10-16 | English edition | fixed approved cover artwork



Semiconductor Back-End: the boundary moved from isolated claims to qualification evidence

20 English articles were reviewed independently from the Japanese edition. Ten themes are retained for management decisions.

SIGNAL 01 | BUSINESS / RULES

ASE PowerSiPTM: 3D SiP for AI Vertical Power Delivery Specs

Primary-source report: ASE has expanded its PowerSiPTM platform with a 3D System-in-Package (SiP) solution that enables vertically integrated voltage regulator modules (VRMs).

SIGNAL 02 | BUSINESS / RULES

Japan-U.S. Semiconductor Project: New York Plant Timeline and Costs

Collected report (not independently verified): Japan and the United States have agreed to implement a semiconductor manufacturing project in New York State with an initial estimated cost of 10 billion USD.

SIGNAL 03 | SYSTEM / ADOPTION

ERS electronic: Automated 310mm Panel-Level Packaging System Specs

Collected report (not independently verified): ERS electronic has launched a fully automated panel-level packaging (PLP) system for 310×310mm substrates that integrates bonding, debonding, and detaping.

SIGNAL 04 | SYSTEM / ADOPTION

Evatec CLUSTERLINE 310: Panel-Level Packaging for 310mm Formats

Collected report (not independently verified): Evatec has delivered its first CLUSTERLINE 310 system to a global IDM for advanced packaging on 310×310mm panel formats.

DECISION

Focus this week's management attention on package performance, process yield, test coverage and qualified capacity. Move only when the linked evidence can be reproduced under your own operating conditions.

THREE MANAGEMENT MOVES

- 1. Buyers: compare architectures using thermal, electrical, yield, repair and supply evidence.
- 2. Suppliers: co-develop materials, bonding, inspection and reliability windows with customers.
- 3. Executives: track yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EVIDENCE DISCIPLINE

FACT states what the collected English source reports. BUSINESS READ and ACTION are editorial interpretations. UNKNOWN lists information that the source file does not establish. A linked article is not treated as independent confirmation of every claim.

Five numbers or evidence anchors that require conditions

>=50% A07	SOURCE-BOUND CONDITION ASE claimed parasitic routing-loss reduction
310x310 mm A05	SOURCE-BOUND CONDITION ERS supported panel format; reported
450 nm A12	SOURCE-BOUND CONDITION Hybrid-bonding research pitch; reported
RM396M A06	SOURCE-BOUND CONDITION Unisem plant expansion; reported investment
OPEN A07	SOURCE-BOUND CONDITION Application-specific thermal and joint reliability, reproducibility and deployment terms remain unproven. Published claims are not customer-qualified performance.
HOW TO USE THESE NUMBERS Each value is shown with the condition stated in the collected English article. Do not compare values across different test methods, device sizes, operating temperatures or commercial stages without normalizing those conditions.	

Where the value chain moved

Each stage combines one leading theme and one supporting theme. The report treats handoffs as evidence transfers, not decorative arrows.

1 Materials P01/P06 Primary-source report: ASE has expanded its PowerSiPTM platform with a 3D System-in-Package (SiP) solution that enables vertically integrated voltage regulator modules (VRMs).	2 Bonding & assembly P02/P07 Collected report (not independently verified): Japan and the United States have agreed to implement a semiconductor manufacturing project in New York State with an initial estimated cost of 10 billion USD.	3 Advanced package P03/P08 Collected report (not independently verified): ERS electronic has launched a fully automated panel-level packaging (PLP) system for 310×310mm substrates that integrates bonding, debonding, and detaping.	4 Test & inspection P04/P09 Collected report (not independently verified): Evatec has delivered its first CLUSTERLINE 310 system to a global IDM for advanced packaging on 310×310mm panel formats.	5 Volume supply P05/P10 Collected report (not independently verified): Hybrid bonding enables interconnect pitches below 10um, with Applied Materials and imec/EV group demonstrating pitches of 450nm and 200nm respectively.
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EVIDENCE REQUIRED AT EACH HANDOFF

Materials to Bonding & assembly	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Bonding & assembly to Advanced package	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Advanced package to Test & inspection	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Test & inspection to Volume supply	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.

COMMON CONTROL POINT

No theme moves to a commercial commitment until a named owner has reproduced the relevant evidence and documented yield, warpage, thermal cycling, test time, capacity, cost and qualification.

Priority map: maturity and next decision locus



REPRODUCIBLE POSITIONING RULE
Horizontal position uses five discrete stages: Research, Prototype, Joint evaluation, Product adoption and Scale. The vertical bands classify the next decision locus: Tech / process, System / adoption, or Business / rules (including supply systems). Article-title cues take precedence; the overview is used only when the title is silent. These are categories, not impact ranks. Bubble diameter reflects the editorial score.

For legibility, scores of 18 or below use an 18-pt bubble diameter; underlying scores are unchanged.

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P01

ASE PowerSiPTM: 3D SiP for AI Vertical Power Delivery Specs

A07 | Business / rules | Product adoption

2026-10-14

FACT

Primary-source report: ASE has expanded its PowerSiPTM platform with a 3D System-in-Package (SiP) solution that enables vertically integrated voltage regulator modules (VRMs). This architecture can reduce parasitic routing losses by 50% or more, addressing the extreme power demands of AI data centers and high-performance computing.

WHY IT MATTERS

In practical terms, ASE PowerSiPTM needs separate tests of power-delivery loss and thermal and joint reliability before the result becomes an adoption case.

BUSINESS READ

For ASE PowerSiPTM, compare power-delivery loss and thermal and joint reliability under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare ASE PowerSiPTM on power-delivery loss against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific thermal and joint reliability, reproducibility and deployment terms remain unproven. Published claims are not customer-qualified performance.

EDITORIAL SCORE 19/25 | MATURITY 4/5 | DECISION LOCUS: BUSINESS / RULES

P02

Japan-U.S. Semiconductor Project: New York Plant Timeline and Costs

A04 | Business / rules | Joint evaluation

2026-10-15

FACT

Collected report (not independently verified): Japan and the United States have agreed to implement a semiconductor manufacturing project in New York State with an initial estimated cost of 10 billion USD. The project focuses on expanding production capacity for mature-node semiconductors to strengthen economic security and supply chain resilience.

WHY IT MATTERS

In practical terms, Japan-U.S. Semiconductor Project needs separate tests of interface function and aging and process window before the result becomes an adoption case.

BUSINESS READ

For Japan-U.S. Semiconductor Project, compare interface function and aging and process window under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare Japan-U.S. Semiconductor Project on interface function against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific aging and process window, reproducibility and deployment terms remain unproven. Confirm the original primary record.

EDITORIAL SCORE 16/25 | MATURITY 3/5 | DECISION LOCUS: BUSINESS / RULES

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P03

ERS electronic: Automated 310mm Panel-Level Packaging System Specs

A05 | System / adoption | Prototype

2026-10-12

FACT

Collected report (not independently verified): ERS electronic has launched a fully automated panel-level packaging (PLP) system for 310×310mm substrates that integrates bonding, debonding, and detaping. The platform achieves a throughput of 13 panels per hour, reducing handling risks and transit time by eliminating inter-tool transfers.

WHY IT MATTERS

In practical terms, ERS electronic needs separate tests of panel warpage and bonding and inspection yield before the result becomes an adoption case.

BUSINESS READ

For ERS electronic, compare panel warpage and bonding and inspection yield under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare ERS electronic on panel warpage against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific bonding and inspection yield, reproducibility and deployment terms remain unproven. Confirm the original primary record.

EDITORIAL SCORE 15/25 | MATURITY 2/5 | DECISION LOCUS: SYSTEM / ADOPTION

P04

Evatec CLUSTERLINE 310: Panel-Level Packaging for 310mm Formats

A10 | System / adoption | Prototype

2026-10-13

FACT

Collected report (not independently verified): Evatec has delivered its first CLUSTERLINE 310 system to a global IDM for advanced packaging on 310×310mm panel formats. The tool integrates degas, etch, and PVD technologies to support next-generation chip manufacturing, specifically for glass and highly outgassing organics.

WHY IT MATTERS

In practical terms, Evatec CLUSTERLINE 310 needs separate tests of panel warpage and bonding and inspection yield before the result becomes an adoption case.

BUSINESS READ

For Evatec CLUSTERLINE 310, compare panel warpage and bonding and inspection yield under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare Evatec CLUSTERLINE 310 on panel warpage against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific bonding and inspection yield, reproducibility and deployment terms remain unproven. Confirm the original primary record.

EDITORIAL SCORE 15/25 | MATURITY 2/5 | DECISION LOCUS: SYSTEM / ADOPTION

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P05

Hybrid Bonding: Technical Process, Performance and 2026 Roadmap

A12 | Tech / process | Prototype

2026-10-14

FACT

Collected report (not independently verified): Hybrid bonding enables interconnect pitches below 10um, with Applied Materials and imec/EV group demonstrating pitches of 450nm and 200nm respectively. By eliminating solder bridging and underfill gaps, the technology improves signal bandwidth and heat transfer for high-performance 2.5D/3D packaging. This process is critical for high-layer-count HBM stacks and 224Gbps+ optical engines.

WHY IT MATTERS

In practical terms, Hybrid Bonding needs separate tests of bonding yield and warpage before the result becomes an adoption case.

BUSINESS READ

For Hybrid Bonding, compare bonding yield and warpage under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare Hybrid Bonding on bonding yield against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific warpage, reproducibility and deployment terms remain unproven. Confirm the original primary record.

EDITORIAL SCORE 15/25 | MATURITY 2/5 | DECISION LOCUS: TECH / PROCESS

P06

Intel EMIB and Foveros: Advanced Packaging Roadmaps and Specs

A15 | System / adoption | Prototype

2026-10-14

FACT

Collected report (not independently verified): Intel is scaling its chiplet strategy through the evolution of EMIB and Foveros to enable system-in-packages (SiPs) up to 12 reticles in size. The roadmap focuses on reducing bump pitches to 25 µm and integrating glass-core substrates to support massive AI accelerators and HBM4-class memory.

WHY IT MATTERS

In practical terms, Intel EMIB and Foveros needs separate tests of bonding yield and warpage before the result becomes an adoption case.

BUSINESS READ

For Intel EMIB and Foveros, compare bonding yield and warpage under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare Intel EMIB and Foveros on bonding yield against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific warpage, reproducibility and deployment terms remain unproven. Confirm the original primary record.

EDITORIAL SCORE 15/25 | MATURITY 2/5 | DECISION LOCUS: SYSTEM / ADOPTION

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P07

ZEISS SMT: Inspection and Metrology for Advanced Packaging

A16 | Tech / process | Prototype

2026-10-15

FACT

Collected report (not independently verified): ZEISS Semiconductor Manufacturing Technology (SMT) has introduced the NLX and DUNE systems to address inspection and wafer bow challenges in advanced packaging. These tools, alongside EUV photomask solutions, enable the production of complex chiplet architectures and High-NA-EUV lithography at scale.

WHY IT MATTERS

In practical terms, ZEISS SMT needs separate tests of bonding yield and warpage before the result becomes an adoption case.

BUSINESS READ

For ZEISS SMT, compare bonding yield and warpage under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare ZEISS SMT on bonding yield against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific warpage, reproducibility and deployment terms remain unproven. Confirm the original primary record.

EDITORIAL SCORE 15/25 | MATURITY 2/5 | DECISION LOCUS: TECH / PROCESS

P08

Unisem: RM396 million Gopeng plant expansion for AI packaging

A06 | Business / rules | Product adoption

2026-10-09

FACT

Collected report (not independently verified): Unisem (M) Bhd is investing RM396 million in the second phase of its Gopeng, Perak facility to increase capacity for wafer bumping and post-bump services. This expansion targets the growing demand for advanced chip packaging in AI, data centers, and high-performance computing.

WHY IT MATTERS

In practical terms, Unisem needs separate tests of bonding yield and warpage before the result becomes an adoption case.

BUSINESS READ

For Unisem, compare bonding yield and warpage under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare Unisem on bonding yield against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific warpage, reproducibility and deployment terms remain unproven. Confirm the original primary record.

EDITORIAL SCORE 17/25 | MATURITY 4/5 | DECISION LOCUS: BUSINESS / RULES

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P09

IJM Corporation: RM1.23 Billion AT&S Semiconductor Facility Timeline

A13 | Business / rules | Product adoption

2026-10-12

FACT

Collected report (not independently verified): IJM Corporation has secured a RM1.23 billion contract to construct semiconductor manufacturing facilities for AT&S Austria Technologie & Systemtechnik in Kedah's Kulim Hi-Tech Park. The project involves building high-end IC substrate and PCB production capacity to support data center processors for clients including AMD.

WHY IT MATTERS

In practical terms, IJM Corporation needs separate tests of interface function and aging and process window before the result becomes an adoption case.

BUSINESS READ

For IJM Corporation, compare interface function and aging and process window under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare IJM Corporation on interface function against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific aging and process window, reproducibility and deployment terms remain unproven. Confirm the original primary record.

EDITORIAL SCORE 17/25 | MATURITY 4/5 | DECISION LOCUS: BUSINESS / RULES

P10

FCS and CKST: Glass Substrate Equipment Distribution for AI Chips

A18 | System / adoption | Joint evaluation

2026-10-09

FACT

Collected report (not independently verified): FCS Precision Industry Co., Ltd. has secured exclusive distribution rights for China Korea Smart Technology (CKST) equipment in Taiwan and Southeast Asia. The partnership focuses on glass substrate equipment for next-generation AI chips and high-performance computing (HPC) advanced packaging.

WHY IT MATTERS

In practical terms, FCS and CKST needs separate tests of bonding yield and warpage before the result becomes an adoption case.

BUSINESS READ

For FCS and CKST, compare bonding yield and warpage under the same application conditions. Request source protocols before extrapolating to customer use. This is an editorial inference.

ACTION

Within 30 days, R&D and quality should compare FCS and CKST on bonding yield against a baseline; deliver an acceptance and stop-rule sheet.

UNKNOWN

Application-specific warpage, reproducibility and deployment terms remain unproven. Confirm the original primary record.

EDITORIAL SCORE 16/25 | MATURITY 3/5 | DECISION LOCUS: SYSTEM / ADOPTION

Playbook and 0-5 year roadmap

STAKEHOLDER	NOW 0-30 DAYS	NEXT 1-12 MONTHS	LATER 1-5 YEARS
Operating companies	compare architectures using thermal, electrical, yield, repair and supply evidence	Run production-like qualification with explicit acceptance and stop criteria.	Build a portfolio and architecture that can absorb technology and supplier changes.
Materials, equipment and technology suppliers	co-develop materials, bonding, inspection and reliability windows with customers	Create shared reliability, process-window and failure-analysis data with customers.	Standardize interfaces, traceability, lifecycle support and recovery services.
Trading, investment and legal teams	Map yield, warpage, thermal cycling, test time, capacity, cost and qualification.	Contract for capacity, quality, change notice, liability, alternatives and exit.	Diversify regional, technical and customer concentration risk.

ROADMAP

NOW 0-30 DAYS Evidence ledger Owner: Strategy + quality Deliverable: claim, source, condition, owner	NOW 0-30 DAYS Risk screen Owner: Procurement + legal Deliverable: unknowns, alternatives, stop	NEXT 1-12 MONTHS Joint qualification Owner: R&D + supplier Deliverable: process window and failure data
NEXT 1-12 MONTHS Commercial gate Owner: Business + finance Deliverable: unit economics and capacity	LATER 1-5 YEARS Platform strategy Owner: Executive team Deliverable: portfolio and interface roadmap	LATER 1-5 YEARS Service layer Owner: Operations + channel Deliverable: monitoring, maintenance and recovery

GO / NO-GO GATES

GATE	OWNER	REQUIRED EVIDENCE	NO-GO CONDITION
G1 Evidence	Quality	Source, test conditions and reproducibility	No traceable evidence
G2 Integration	R&D	Interface, process window and failure analysis	Cannot meet system conditions
G3 Commercial	Business	Capacity, total cost, contract and alternatives	Economics or supply cannot be supported
G4 Lifecycle	Operations	Monitoring, maintenance, change notice and exit	No accountable operating plan

ANALYZED ARTICLES | ITEMS 01-10

Every title and URL is displayed in full. URLs wrap without shortening and remain clickable. A verified-reference label means the translated HTML did not retain its original source URL.

ID	FULL ARTICLE TITLE	FULL SOURCE / VERIFIED REFERENCE URL - CLICKABLE
A01	Micron HBM Roadmap: AATT2 Opening and 2027 Capacity Status	https://finance.biggo.com/news/b82e06b8-3991-4a72-8281-d310d2d97660
A02	Hanmi Semiconductor: HBM4 Packaging Equipment and 2027 Roadmap	https://wisevoter.com/world/us/ca/san-francisco/2026/10/14/hanmi-semiconductor-unveiled-hbm4-equipment
A03	ASE Technology Holding: Advanced Packaging Roadmap and 2027 Timeline	https://techsoda.substack.com/p/dr-change-column-16-packaging-takes
A04	Japan-U.S. Semiconductor Project: New York Plant Timeline and Costs	https://www.meti.go.jp/english/press/2026/10/20261015001.html
A05	ERS electronic: Automated 310mm Panel-Level Packaging System Specs	https://www.semiconductor-digest.com/ers-introduces-automated-310mm-panel-level-packaging-system/
A06	Unisem: RM396 million Gopeng plant expansion for AI packaging	https://theedgemalaysia.com/node/821171
A07	ASE PowerSiPTM: 3D SiP for AI Vertical Power Delivery Specs	https://www.aseglobal.com/press-room/ase-expands-powersip-platform-for-next-generation-ai-power-delivery
A08	Samsung: \$9.15 bn semiconductor investment and Vietnam roadmap	https://manufacturing.economictimes.indiatimes.com/news/hi-tech/samsung-plans-9-15-bn-semiconductor-investment-with-nearly-6-bn-earmarked-for-vietnam/134885720
A09	NXP Semiconductors: \$250M EIB Global Loan for Malaysia Expansion	https://news.fundsforngos.org/2026/10/16/eib-global-finances-nxp-250-million-malaysia-semiconductors/
A10	Evatec CLUSTERLINE 310: Panel-Level Packaging for 310mm Formats	https://chiplet-marketplace.com/insights/news/evatec-clusterline-310-advanced-packaging-small-panel-formats

ANALYZED ARTICLES | ITEMS 11-20

Every title and URL is displayed in full. URLs wrap without shortening and remain clickable. A verified-reference label means the translated HTML did not retain its original source URL.

ID	FULL ARTICLE TITLE	FULL SOURCE / VERIFIED REFERENCE URL - CLICKABLE
A11	Bac Ninh: Vietnam's Semiconductor Hub Roadmap and FDI Projects	https://www.thestar.com.my/business/business-news/2026/10/16/bac-ninh-eyes-vietnams-semiconductor-hub-status
A12	Hybrid Bonding: Technical Process, Performance and 2026 Roadmap	https://www.3dincites.com/2026/10/why-hybrid-bonding-is-hard-to-perfect/
A13	IJM Corporation: RM1.23 Billion AT&S Semiconductor Facility Timeline	https://theedgemalaysia.com/node/821536
A14	Bridge Technology: Next-Gen Large-Format Packaging Roadmap 2026	https://www.thelec.net/news/articleView.html?idxno=14567
A15	Intel EMIB and Foveros: Advanced Packaging Roadmaps and Specs	https://www.tomshardware.com/tech-industry/semiconductors/analyzing-intels-emib-and-foveros-advanced-packaging-roadmaps-how-intel-plans-to-scale-chips-in-every-direction
A16	ZEISS SMT: Inspection and Metrology for Advanced Packaging	https://metrology.news/zeiss-advances-inspection-and-metrology-for-next-generation-semiconductor-manufacturing/
A17	CIT ASEDep: Single-Crystal Copper Deposition for AI Packaging	https://www.donga.com/en/article/all/20261015/6420046/1
A18	FCS and CKST: Glass Substrate Equipment Distribution for AI Chips	https://www.adsalecprj.com/en/news/article_details/90309.html
A19	Samsung Electro-Mechanics: 100mm Glass Substrate Testing Roadmap	https://www.digitimes.com/news/a20261008VL220/semco-glass-substrate-testing-expansion.html
A20	Intel Advanced Packaging: EMIB-T and Foveros Roadmap to 2028	https://finance.biggo.com/news/03f6f05f-928f-44ea-a48e-4414bad68127

Scope: retrieving a source does not independently validate performance, cost or clinical utility. The claim ledger distinguishes announcements, papers and secondary reporting. Material published before the reporting week is continuing context, not a new event. Editorial inferences and actions are not investment or medical advice.

Semiconductor_BackEnd — Selected Articles

Date: 2026-10-18

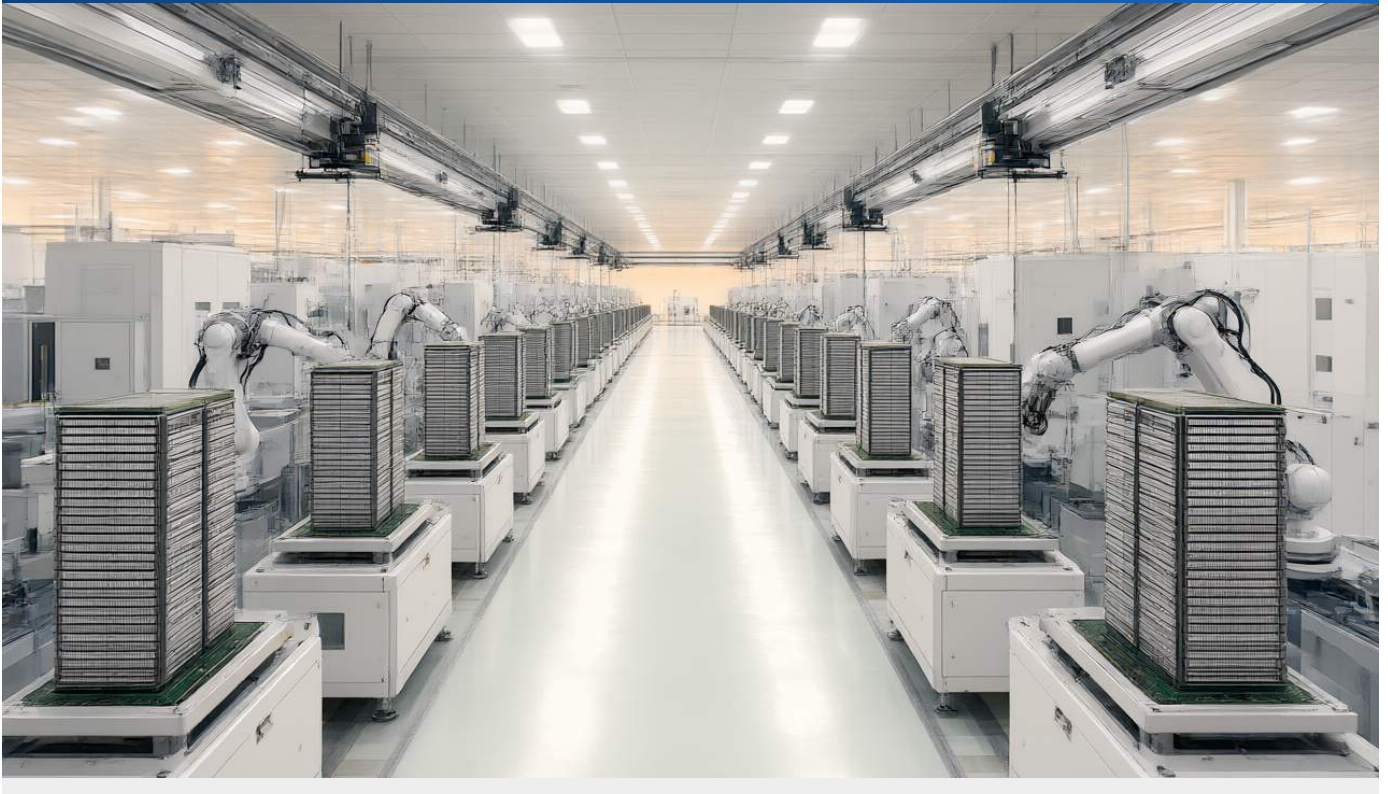
Articles: 20

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- #06 Unisem: RM396 million Gopeng plant expansion for AI packaging
- #07 ASE PowerSiP™: 3D SiP for AI Vertical Power Delivery Specs
- #08 Samsung: \$9.15 bn semiconductor investment and Vietnam roadmap
- #09 NXP Semiconductors: \$250M EIB Global Loan for Malaysia Expansion
- #10 Evatec CLUSTERLINE 310: Panel-Level Packaging for 310mm Formats
- #11 Bac Ninh: Vietnam's Semiconductor Hub Roadmap and FDI Projects
- #12 Hybrid Bonding: Technical Process, Performance and 2026 Roadmap
- #13 IJM Corporation: RM1.23 Billion AT&S Semiconductor Facility Timeline
- #14 Bridge Technology: Next-Gen Large-Format Packaging Roadmap 2026
- #15 Intel EMIB and Foveros: Advanced Packaging Roadmaps and Specs
- #16 ZEISS SMT: Inspection and Metrology for Advanced Packaging
- #17 CIT ASEDep: Single-Crystal Copper Deposition for AI Packaging
- #18 FCS and CKST: Glass Substrate Equipment Distribution for AI Chips
- #19 Samsung Electro-Mechanics: 100mm Glass Substrate Testing Roadmap
- #20 Intel Advanced Packaging: EMIB-T and Foveros Roadmap to 2028

#01 Micron HBM Roadmap: AATT2 Opening and 2027 Capacity Status

Published October 15, 2026 BigGo Finance Taiwan



OVERVIEW

Micron has inaugurated its Advanced Assembly and Test Taiwan 2 (AATT2) facility in Taichung, with HBM capacity for 2027 already fully sold out. The company is accelerating its global supply chain across Taiwan, Singapore, and Japan to meet generative AI demand, with HBM growth expected to outpace the broader DRAM industry through 2028.

Key Findings

Micron Technology has officially opened the Advanced Assembly and Test Taiwan 2 (AATT2) facility in Taichung. Micron President and COO Manish Bhatia confirmed that the facility's HBM capacity for 2027 is already fully sold out. The company expects HBM growth to continue exceeding that of the general DRAM industry through 2028, driven by the requirements of generative AI and data center customers.

Technical Details

The AATT2 plant transitioned from a traditional spring factory into a fully automated advanced packaging facility. The production process focuses on the challenges of stacking multiple DRAM layers, specifically regarding interconnects, thermal management, and quality control. Micron's global HBM strategy involves a distributed manufacturing model:

- **Taiwan:** AATT2 focuses on advanced packaging and testing, leveraging a local workforce of approximately 12,000 people in Taichung.
- **Singapore:** An advanced HBM packaging plant is expected to contribute capacity starting in 2027.
- **Japan:** A new cleanroom at the Hiroshima plant, involving a ¥1.5 trillion investment (with up to ¥536 billion in subsidies from the Ministry of Economy, Trade and Industry), will manufacture DRAM for HBM4 using the 1 γ process node, with shipments expected in 2028.

Background and Context

The AATT2 facility moved from groundbreaking in September of last year to volume production in approximately one year. This acceleration reflects a shift in the semiconductor industry where technological generations now advance roughly every 12 months, and AI model benefits are realized by customers within 12 to 18 months. Micron's cumulative investment in Taiwan has surpassed NT\$1.6 trillion.

Significance and Outlook

The rapid expansion of HBM capacity and production ramp speed has become the primary competitive battleground for memory manufacturers. To support this, the Taiwanese government has provided new subsidies under the A+ Industrial Innovation R&D Program to accelerate HBM investment and capacity expansion, while assisting local precision manufacturing suppliers to enter the high-tech industry chain.

Reference technology guide: High Bandwidth Memory (HBM): <https://troy-technical.com/semiconductor-back-end-term-hbm/>

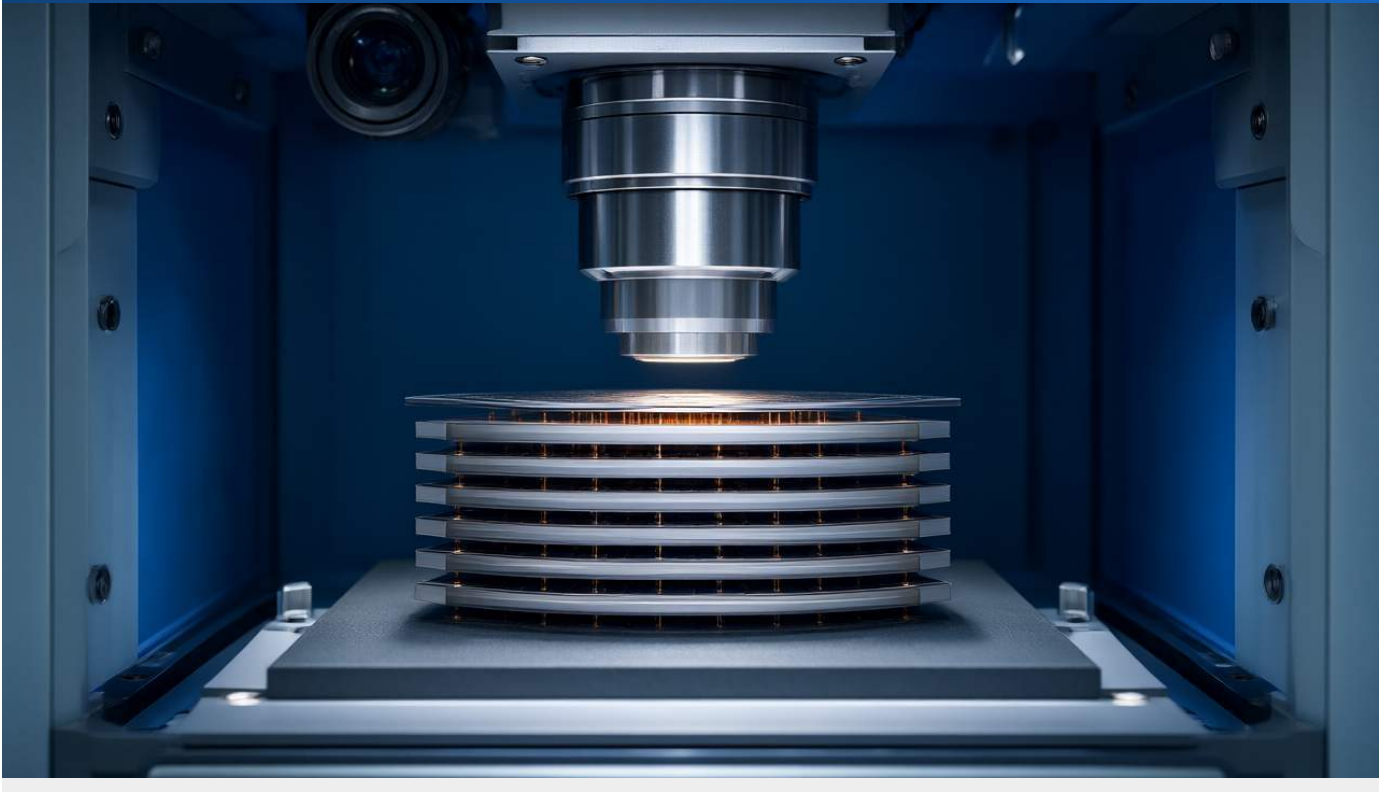
Reference technology guide: Semiconductor Test: <https://troy-technical.com/semiconductor-back-end-term-test/>

Source: <https://finance.biggo.com/news/b82e06b8-3991-4a72-8281-d310d2d97660>

Collected: October 17, 2026 | Automated Research System (AI)

#02 Hanmi Semiconductor: HBM4 Packaging Equipment and 2027 Roadmap

Published October 14, 2026 Wisevoter USA



OVERVIEW

Hanmi Semiconductor debuted five specialized packaging models for HBM4 production at Semicon West 2026 to address AI semiconductor manufacturing bottlenecks. The suite includes TC and FC Bonders designed for high-precision stacking and 2.5D integration. These advancements aim to optimize the production pipeline for high-performance GPUs and CPUs.

Key Findings

Hanmi Semiconductor introduced a new suite of packaging equipment at Semicon West 2026, held at the Moscone Center in San Francisco from October 13-15, 2026. The company debuted five specialized models specifically designed to support the mass production of HBM4 memory chips and optimize the assembly of next-generation AI semiconductors.

Technical Details

The newly introduced equipment lineup consists of the following:

- TC Bonder 4: Dedicated for HBM4 production.
- 2.5D TC Bonders: Three units.
- FC Bonders: Two units.

These tools utilize heat and pressure to facilitate high-precision bonding and stacking of memory chips. Furthermore, the company showcased 2.5D packaging technology that employs silicon interposers to integrate HBM, CPUs, and GPUs into a single high-performance package. Hanmi also demonstrated its Micro Saw & Vision Placement process—a technology developed in 2021—which automates the sequence of cutting, cleaning, drying, inspection, sorting, and loading.

Background & Context

As a leading manufacturer of semiconductor back-end process equipment, Hanmi Semiconductor is positioning itself to challenge existing foundry market providers. The launch of these specific bonders responds to a surge in demand for sophisticated manufacturing technology as global memory manufacturers ramp up HBM4 production, particularly within the United States.

Significance & Outlook

Packaging technology currently represents the primary bottleneck for the capacity and speed of AI hardware production. The increased availability of specialized assembly equipment may reduce production bottlenecks, potentially lowering costs for data centers and developers of high-performance AI hardware.

Looking forward, Hanmi Semiconductor has scheduled the release of the Wide TC Bonder for 2027. This upcoming rollout is identified as a key signal for when high-volume HBM4 production may reach its next phase of maturity.

Reference technology guide: High Bandwidth Memory (HBM): <https://troy-technical.com/semiconductor-back-end-term-hbm/>

Reference technology guide: Die Stacking: <https://troy-technical.com/semiconductor-back-end-term-stacking/>

Reference technology guide: Interposers: <https://troy-technical.com/semiconductor-back-end-term-interposer/>

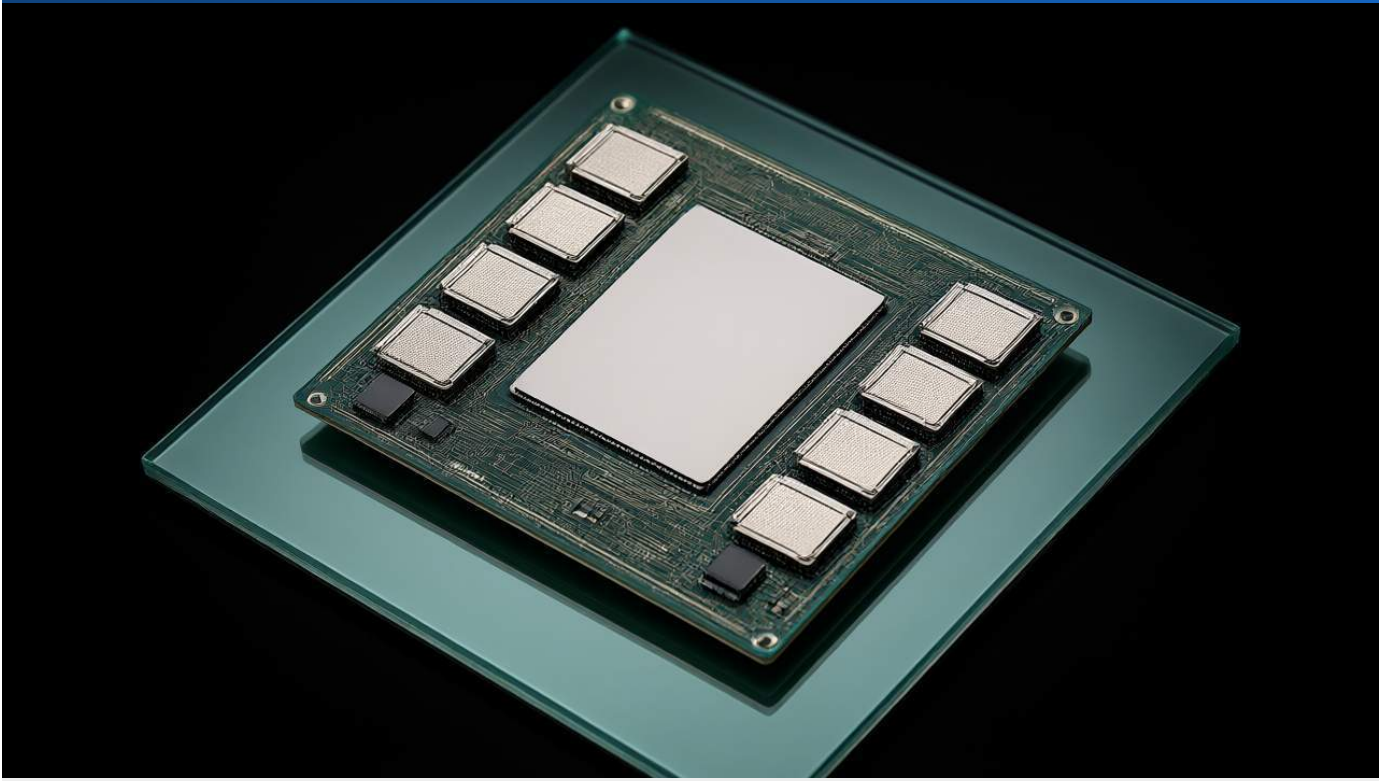
Reference company guide: Hanmi Semiconductor: <https://troy-technical.com/semiconductor-back-end-company-hanmi/>

Source: <https://wisevoter.com/world/us/ca/san-francisco/2026/10/14/hanmi-semiconductor-unveiled-hbm4-equipment>

Collected: October 17, 2026 | Automated Research System (AI)

#03 ASE Technology Holding: Advanced Packaging Roadmap and 2027 Timeline

Published October 15, 2026 TechSoda USA



OVERVIEW

ASE has transitioned from traditional OSAT services to advanced packaging, with advanced packaging revenue growing from NT\$18.8 billion in 2024 to NT\$50.2 billion in 2025. The company is now implementing panel-level packaging and CPO to address AI computing bottlenecks. This shift moves packaging from a supporting role to a primary determinant of system performance.

Key Findings

ASE has significantly expanded its footprint in the advanced packaging sector, increasing its share of the semiconductor assembly and test business from 6% in 2024 to 13% in 2025. In 2024, ASE accounted for US\$18.54 billion of the US\$41.56 billion total revenue generated by the world's top ten OSAT companies. For the full year 2025, ASE's total revenue grew 8.4% to NT\$645.4 billion, driven by a 17.8% increase in packaging revenue and a 31.8% increase in testing revenue.

Technical Details

ASE's technical strategy is centered on the VIPack platform, which integrates several advanced frameworks:

- **FOCoS (Fan-Out Chip-on-Substrate):** Uses redistribution layers to integrate ASICs, chiplets, and HBM.
- **FOCoS-Bridge:** Incorporates localized silicon bridges to increase interconnect density between dies.
- **CPO (Co-packaged Optics):** Integrates optical components closer to compute silicon to overcome bandwidth and power constraints in AI data centers.
- **Panel-Level Packaging:** In 2026, ASE introduced an automated 310mm × 310mm panel-level packaging line to replace round wafers for large packages, with mass production scheduled for the first half of 2027.

Background and Context

The traditional semiconductor value chain separated IC design, foundry manufacturing, and OSAT packaging. However, as Moore's Law scaling from 7nm down to 2nm becomes increasingly expensive, AI accelerators now require the integration of GPUs, ASICs, and multiple HBM stacks. This has shifted the industry toward 2.5D and 3D packaging, where chips are placed on the same interconnect structure or stacked vertically to enable high-speed communication.

Significance and Outlook

The integration of ASE and Siliconware Precision Industries (SPIL) under a joint holding company since 2018 provided the scale and R&D synergies necessary to lead the OSAT market. As packaging now determines overall system performance, ASE is moving toward system-level engineering, combining chiplet architectures and optical communications to meet the computing demands of AI.

Reference technology guide: Semiconductor Test: <https://troy-technical.com/semiconductor-back-end-term-test/>

Reference technology guide: Chiplets: <https://troy-technical.com/semiconductor-back-end-term-chiplet/>

Reference technology guide: High Bandwidth Memory (HBM): <https://troy-technical.com/semiconductor-back-end-term-hbm/>

Reference company guide: ASE Group: <https://troy-technical.com/semiconductor-back-end-company-ase-group/>

Reference company guide: SPIL: <https://troy-technical.com/semiconductor-back-end-company-spil/>

Source: <https://techsoda.substack.com/p/dr-change-column-16-packaging-takes>

Collected: October 17, 2026 | Automated Research System (AI)

#04 Japan-U.S. Semiconductor Project: New York Plant Timeline and Costs

Published October 15, 2026 Ministry of Economy, Trade and Industry (METI) Japan Japan



OVERVIEW

Japan and the United States have agreed to implement a semiconductor manufacturing project in New York State with an initial estimated cost of 10 billion USD. The project focuses on expanding production capacity for mature-node semiconductors to strengthen economic security and supply chain resilience.

Key Findings

Japan and the United States concurred on October 14 (U.S. time) to launch a semiconductor manufacturing project in New York State. This initiative represents the first project under the Japan-U.S. Strategic Investment Initiative. The initial estimated total project cost is approximately 10 billion USD (approximately 1.6 trillion JPY), with construction scheduled to begin by the end of 2026. Future expansions of production facilities could potentially increase the total investment to approximately 21 billion USD.

Technical Details

The project targets the expansion of production capacity for mature-node semiconductors. These components are identified as essential for several critical sectors, including:

- Automobiles
- Industrial machinery
- Smartphones
- AI data centers

Background & Context

The project is a result of coordination efforts and Consultation Committee meetings following the announcement of the Strategic Investment Initiative in September 2025. The initiative is designed to build a resilient semiconductor supply chain in a strategically important area for economic security.

Significance & Outlook

The project is expected to create business opportunities for Japanese companies across the supply chain. Several firms have expressed interest in participating:

- **Manufacturing Equipment:** Tokyo Electron Ltd. and SCREEN Holdings Co., Ltd.
- **Materials and Components:** TOKYO OHKA KOGYO CO., LTD.
- **Product Procurement:** Renesas Electronics Corporation

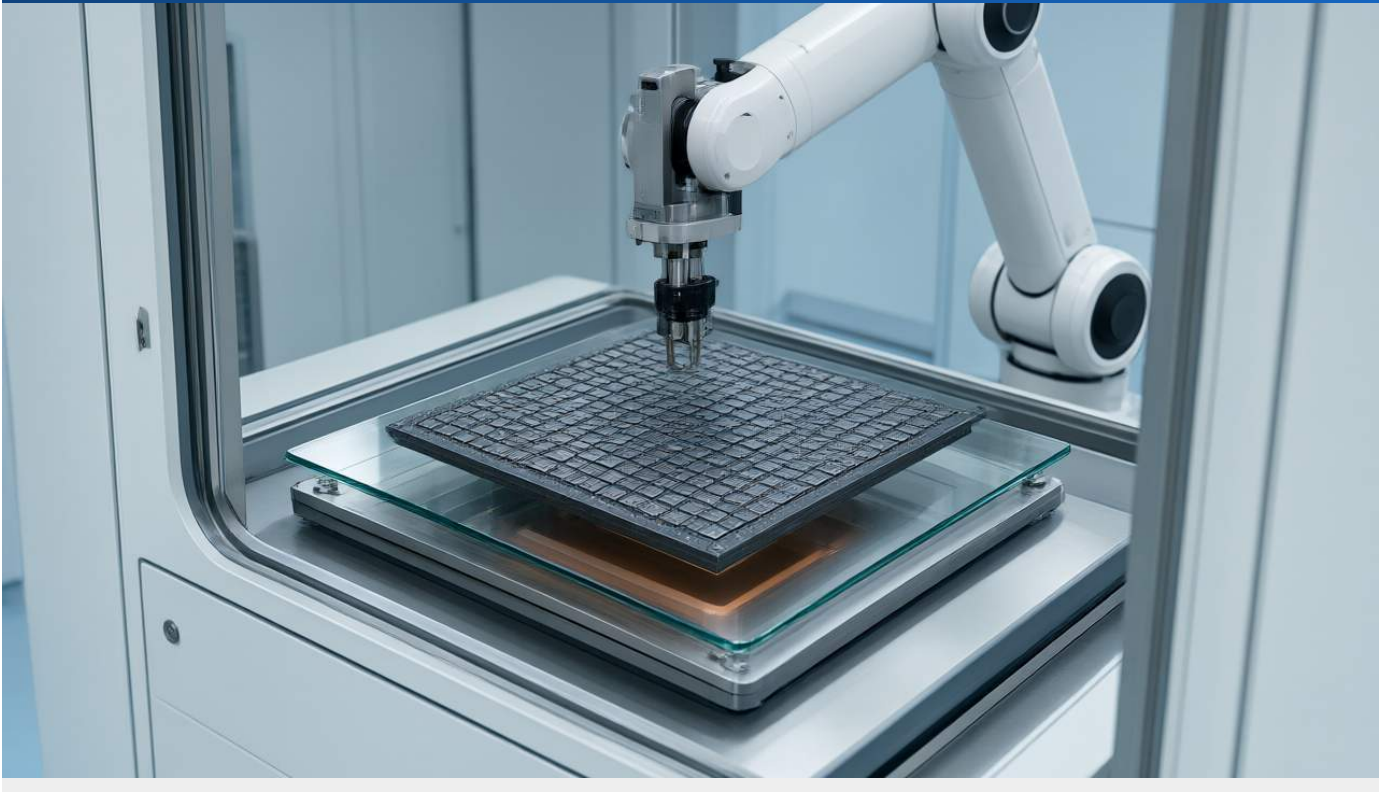
Additionally, the initiative is expected to benefit small and medium enterprises. Specifically, Fujikin Incorporated and Kusakawa Seiki Co., Ltd. have expressed interest in supplying manufacturing equipment, materials, and components. Japan intends to maintain close cooperation with the United States to ensure the prompt and smooth implementation of the facility.

Source: <https://www.meti.go.jp/english/press/2026/10/20261015001.html>

Collected: October 17, 2026 | Automated Research System (AI)

#05 ERS electronic: Automated 310mm Panel-Level Packaging System Specs

Published October 12, 2026 Semiconductor Digest Germany



OVERVIEW

ERS electronic has launched a fully automated panel-level packaging (PLP) system for 310×310mm substrates that integrates bonding, debonding, and detaping. The platform achieves a throughput of 13 panels per hour, reducing handling risks and transit time by eliminating inter-tool transfers. This system targets the growing demand for backside processing in 3D IC, HBM, and 2.5D IC packaging.

Key Findings

ERS electronic has introduced an automated panel-level packaging (PLP) system designed for 310×310mm substrates. The system consolidates three thermally critical process steps—temporary carrier bonding, debonding, and detaping—into a single automated platform. The first unit has already been delivered to a leading semiconductor manufacturer for integration into its production line.

Technical Details

The system operates at a throughput of 13 panels per hour. By integrating three traditionally separate processes into one platform, the machine allows panels to move between internal process modules rather than between separate machines. This architecture eliminates the need for inter-tool transfers, which typically introduce handling steps, transit time, and the risk of substrate damage without requiring changes to the existing fab layout.

Background and Context

The system was developed and manufactured at ERS's Advanced Packaging facility in Barbing, Germany. The development leverages 55 years of thermal management expertise and over 30 years of machine-building capability, supplemented by the 2024 integration of a semiconductor specialist equipment engineering team. ERS is an early adopter of this technology, having shipped its first commercial panel-level tool to Fraunhofer IZM in Berlin in 2018.

Significance and Outlook

The 310×310mm panel format is gaining industry traction due to its ability to significantly improve substrate area utilization compared to 300mm circular wafers. According to Yole Group, the panel-level packaging segment is projected to grow at a compound annual growth rate (CAGR) of over 40% over the next five years. As dual-carrier bonding and debonding workflows become increasingly critical for 3D IC, HBM, and 2.5D IC packaging, this integrated platform aims to improve process consistency, yield, and throughput for manufacturers.

Reference technology guide: Bonding: <https://troy-technical.com/semiconductor-back-end-term-bonding/>

Reference technology guide: Panel-Level Packaging (PLP): <https://troy-technical.com/semiconductor-back-end-term-plp/>

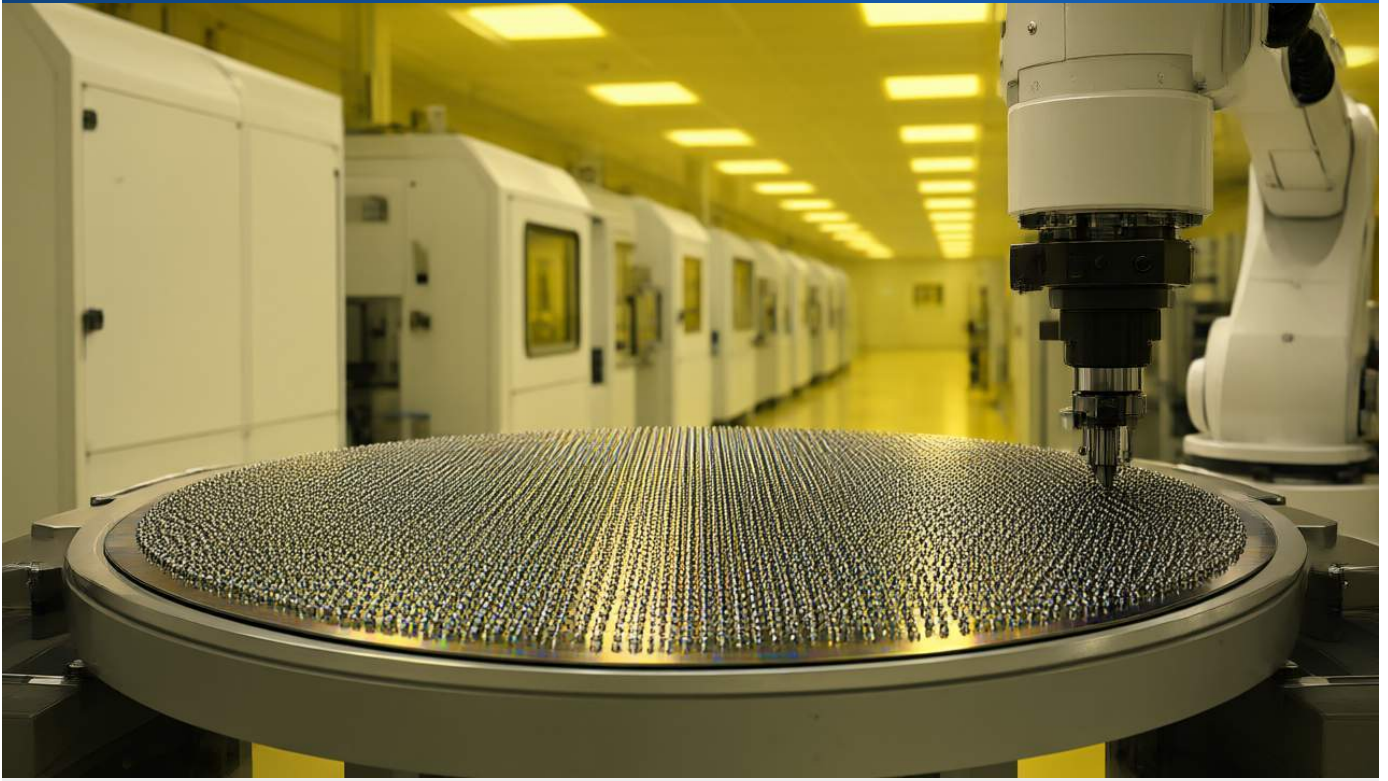
Reference technology guide: High Bandwidth Memory (HBM): <https://troy-technical.com/semiconductor-back-end-term-hbm/>

Source: <https://www.semiconductor-digest.com/ers-introduces-automated-310mm-panel-level-packaging-system/>

Collected: October 17, 2026 | Automated Research System (AI)

#06 Unisem: RM396 million Gopeng plant expansion for AI packaging

Published October 09, 2026 The Edge Malaysia Malaysia



OVERVIEW

Unisem (M) Bhd is investing RM396 million in the second phase of its Gopeng, Perak facility to increase capacity for wafer bumping and post-bump services. This expansion targets the growing demand for advanced chip packaging in AI, data centers, and high-performance computing.

Key Findings

Unisem (M) Bhd and its subsidiary are allocating RM396 million to expand their semiconductor manufacturing plant in Gopeng, Perak. The investment is designed to capture increasing demand for advanced packaging used in artificial intelligence (AI), data centers, and high-performance computing.

Technical Details

The second phase of expansion focuses on increasing manufacturing capacity for wafer bumping and post-bump services. The project includes the following components:

- **Infrastructure:** Construction of a new production facility with a built-up area of approximately 40,000 sq m, costing an estimated RM196 million.
- **Operational Allocation:** Half of the new facility will be leased to Unisem Advanced Technologies Sdn Bhd, a wholly owned subsidiary, to expand wafer-bumping operations.
- **Equipment:** An additional RM200 million is allocated for necessary equipment and facility preparation works.

Background & Context

This project follows an earlier investment in the Gopeng facility that began construction in March 2022. The first phase, initially estimated at RM300 million, was intended to double the production capacity of existing operations in Ipoh. Chairman and group managing director John Chia Sin Tet stated in April that the group had invested RM600 million in the Gopeng plant as part of a nearly RM1 billion capital expenditure plan over three years.

Significance & Outlook

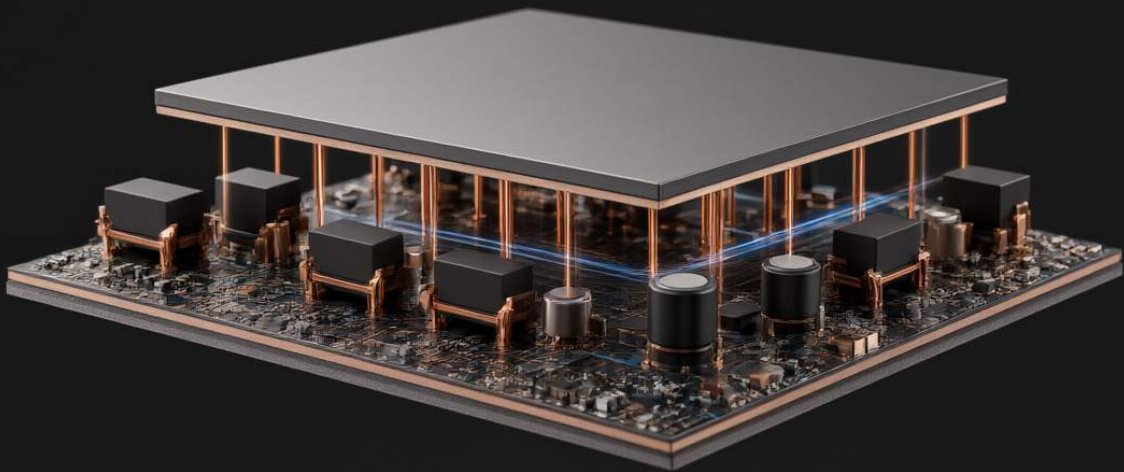
The expansion will be funded through a combination of bank borrowings and internally generated funds, though specific proportions are not yet determined. While the group does not expect the project to materially affect earnings for the current financial year, it is expected to contribute positively once operational. CIMB Securities noted in September that Gopeng Phase 2 could drive the company's next leg of growth by supporting additional advanced packaging and wafer-bumping capacity. As of Friday's midday break, Unisem shares were at RM4.36, representing a market capitalization of RM7.48 billion.

Source: <https://theedgemalaysia.com/node/821171>

Collected: October 17, 2026 | Automated Research System (AI)

#07 ASE PowerSiP™: 3D SiP for AI Vertical Power Delivery Specs

Published October 14, 2026 ASE Technology Holding USA



OVERVIEW

ASE has expanded its PowerSiP™ platform with a 3D System-in-Package (SiP) solution that enables vertically integrated voltage regulator modules (VRMs). This architecture can reduce parasitic routing losses by 50% or more, addressing the extreme power demands of AI data centers and high-performance computing.

Key Findings

ASE has introduced a 3D System-in-Package (SiP) solution within its PowerSiP™ platform to enable vertically integrated voltage regulator modules (VRMs). By positioning voltage regulation directly beneath the processor, this vertical architecture reduces parasitic routing losses by 50% or more compared to traditional lateral architectures. The solution is available now for use in AI data centers and high-performance computing (HPC) applications.

Technical Details

The PowerSiP™ vertical integration toolbox utilizes several advanced packaging technologies to overcome density and thickness constraints in space-constrained compute trays:

- Double-sided connected capacitors positioned between coreless substrates.
- Solder-free, substrate-less cap array modules with exposed terminals for PCB or embedded substrate solutions.
- High-aspect-ratio 4:1 copper pin integration to lower packaging impedance.
- Single- or double-sided molding for high-density integration of active and passive components.

Background and Context

The shift toward vertical power delivery is driven by the scaling performance of AI processors. Modern high-performance AI SoCs can exceed kilowatt-level power consumption and require peak currents greater than 1,000 amps at sub-volt levels. In traditional lateral architectures, electricity must travel across the PCB, through interconnects and package substrates, leading to significant routing losses. Reducing the physical distance between the VRM and the processor is critical to minimizing these losses.

Significance and Outlook

The expansion of the PowerSiP™ platform provides a flexible toolbox for developing compact, highly integrated VRMs for next-generation GPUs, TPUs, and custom ASICs. As AI infrastructure moves toward more heterogeneous and modular compute architectures, system-level power efficiency becomes a defining challenge. ASE's approach addresses the stringent space and performance requirements of AI at scale by shortening the high-current transmission path, translating directly into system-level power savings.

Reference technology guide: System-in-Package (SiP): <https://troy-technical.com/semiconductor-back-end-term-sip/>

Reference technology guide: Package Substrates: <https://troy-technical.com/semiconductor-back-end-term-package-substrate/>

Reference technology guide: Chiplets: <https://troy-technical.com/semiconductor-back-end-term-chiplet/>

Reference company guide: ASE Group: <https://troy-technical.com/semiconductor-back-end-company-ase-group/>

Source: <https://www.aseglobal.com/press-room/ase-expands-powersip-platform-for-next-generation-ai-power-delivery>

#08 Samsung: \$9.15 bn semiconductor investment and Vietnam roadmap

Published October 12, 2026 ET Manufacturing India



OVERVIEW

Samsung is planning a total semiconductor investment of \$9.15 bn, with nearly \$6 bn allocated specifically for Vietnam. This investment focuses on expanding memory chip testing facilities and the production of flip-chip ball grid array substrates.

Key Findings

Samsung has outlined a semiconductor investment plan totaling \$9.15 bn. A significant portion of this capital, nearly \$6 bn, is earmarked for operations in Vietnam. This strategic allocation underscores a major expansion of the company's manufacturing and testing footprint in the region.

Technical Details

The investment is directed toward specific high-tech semiconductor processes and infrastructure. Key technical focuses include:

- **Memory Chip Testing:** Expansion of facilities dedicated to the testing of memory chips to ensure quality and performance standards.
- **Substrate Production:** Investment in flip-chip ball grid array (FCBGA) substrates, which are critical components for connecting semiconductor dies to printed circuit boards.

Background & Context

The operational expansion is centered around the Yen Binh Industrial Park. By concentrating these resources in Vietnam, Samsung is integrating its specialized testing and substrate production into the local industrial landscape. This move is designed to strengthen the overall Vietnam semiconductor ecosystem, moving beyond simple assembly to more complex backend semiconductor processes.

Significance & Outlook

The commitment of nearly \$6 bn to a single region indicates a long-term shift in Samsung's supply chain strategy. By enhancing the capabilities of the Yen Binh Industrial Park and investing in flip-chip ball grid array substrates, the company aims to stabilize its production pipeline for memory products. For investors and researchers, this represents a significant scaling of semiconductor infrastructure in Southeast Asia, specifically targeting the critical testing and packaging phases of the semiconductor lifecycle.

Reference technology guide: Semiconductor Test: <https://troy-technical.com/semiconductor-back-end-term-test/>

Reference technology guide: Flip Chip: <https://troy-technical.com/semiconductor-back-end-term-flipchip/>

Reference company guide: Samsung Electronics: <https://troy-technical.com/semiconductor-back-end-company-samsung-electronics/>

Source: <https://manufacturing.economictimes.indiatimes.com/news/hi-tech/samsung-plans-9-15-bn-semiconductor-investment-with-nearly-6-bn-earmarked-for-vietnam/134885720>

Collected: October 17, 2026 | Automated Research System (AI)

#09 NXP Semiconductors: \$250M EIB Global Loan for Malaysia Expansion

Published October 16, 2026 fundsforNGOs News USA



OVERVIEW

NXP Semiconductors is receiving a \$250 million loan from EIB Global to expand semiconductor assembly, packaging, and testing capacity at its facility near Kuala Lumpur. The project, scheduled for completion by 2030, aims to create over 1,000 jobs and strengthen global supply chain resilience for automotive and industrial chips.

Key Findings

EIB Global, the international development arm of the European Investment Bank Group, is providing a \$250 million loan to NXP Semiconductors. This financing is dedicated to expanding the company's manufacturing footprint in Malaysia, specifically focusing on a plant located near Kuala Lumpur. The initiative is expected to be completed by 2030 and is projected to create more than 1,000 jobs within the region.

Technical Details

The investment targets the back-end of the semiconductor production process. Specifically, the funds will boost capacity for:

- Semiconductor assembly
- Packaging
- Testing

These operations are critical for converting semiconductor wafers into packaged chips ready for integration into end products. The expanded capacity will support the production of chips used in automotive sectors, industrial equipment, and smart-home devices.

Background & Context

The financing was announced on 13 October 2026 during the European Union–Malaysia business forum in Kuala Lumpur. This move aligns with the EU's "Global Gateway" strategy, which seeks to mobilize international investments and build partnerships in digital technologies. From a strategic standpoint, the European Investment Bank intends to reinforce Europe's semiconductor supply chains and improve resilience against global supply challenges by diversifying NXP's global manufacturing operations.

Significance & Outlook

For the semiconductor industry, this expansion represents a strategic shift toward diversifying manufacturing footprints to mitigate supply chain risks. Beyond capacity increases, the project emphasizes the transfer of technology and know-how to Malaysia. NXP leadership indicates that the investment will support regional skills development and strengthen the overall resilience of the semiconductor supply chain. For development stakeholders, the project serves as a model for using development finance to link private-sector industrial capacity building with workforce development and high-value employment.

Reference technology guide: Semiconductor Test: <https://troy-technical.com/semiconductor-back-end-term-test/>

Source: <https://news.fundsforngos.org/2026/10/16/eib-global-finances-nxp-250-million-malaysia-semiconductors/>

Collected: October 17, 2026 | Automated Research System (AI)

#10 Evatec CLUSTERLINE 310: Panel-Level Packaging for 310mm Formats

Published October 13, 2026 Evatec Switzerland



OVERVIEW

Evatec has delivered its first CLUSTERLINE 310 system to a global IDM for advanced packaging on 310×310mm panel formats. The tool integrates degas, etch, and PVD technologies to support next-generation chip manufacturing, specifically for glass and highly outgassing organics.

Key Findings

Evatec has completed the delivery of the first dedicated CLUSTERLINE 310 tool designed for panel level packaging on 310×310mm formats. The system was delivered to a leading global IDM to support next-generation chip manufacturing. This delivery marks the start of a pipeline of global customer orders, with additional deliveries scheduled for the coming months.

Technical Details

The CLUSTERLINE 310 is engineered to handle specific material challenges and architectural requirements, including:

- **Integrated Technologies:** The tool combines degas, etch, and PVD technologies.
- **Material Compatibility:** It is specifically designed for the processing of glass and highly outgassing organics.
- **Application Scope:** The solution supports various architectures, ranging from Fan-Out Panel-Level Packaging (FOPLP) to CoPoS.
- **Performance Goals:** The system is designed to provide the process uniformities and process yield necessary for scaling production.

Background & Context

Evatec has spent the last 8 years as a market leader in packaging solutions for larger panels up to 650mm. Through this experience, the company identified cost benefits associated with manufacturing on larger package sizes for High Performance Computing (HPC) and AI applications. The development of the CLUSTERLINE 310 leverages this existing engineering and process know-how to address emerging customer requests for a dedicated 310mm solution.

Significance & Outlook

The introduction of the CLUSTERLINE 310 allows customers to scale up production with lower initial tool investment costs compared to larger formats. Additionally, the platform includes built-in flexibility to support evolving technology roadmaps. Evatec positions this tool as a production solution for the rapidly growing market segment of advanced packaging for AI and HPC.

Reference technology guide: Panel-Level Packaging (PLP): <https://troy-technical.com/semiconductor-back-end-term-plp/>

Reference technology guide: Glass Substrates: <https://troy-technical.com/semiconductor-back-end-term-glass-substrate/>

Reference technology guide: Fan-Out & Wafer-Level Packaging: <https://troy-technical.com/semiconductor-back-end-term-fanout/>

Source: <https://chiplet-marketplace.com/insights/news/evatec-clusterline-310-advanced-packaging-small-panel-formats>

#11 Bac Ninh: Vietnam's Semiconductor Hub Roadmap and FDI Projects

Published October 15, 2026 The Star ベトナム



OVERVIEW

Bac Ninh is positioning itself as Vietnam's national center for semiconductor manufacturing by leveraging a US\$52bil FDI base and strategic industrial infrastructure. The province is integrating high-tech manufacturing and workforce development to move deeper into the global semiconductor value chain.

Key Findings

Bac Ninh is pursuing status as a national semiconductor hub, utilizing its strategic location linking Hanoi, Hai Phong, Hung Yen, and Thai Nguyen. The province has already attracted over 3,600 foreign direct investment (FDI) projects with total registered capital exceeding US\$52bil from the United States, South Korea, Japan, and the European Union.

Technical Details and Project Pipeline

Several large-scale semiconductor and electronics projects are currently driving the region's industrial expansion:

- **Victory Giant Technology:** A semiconductor equipment plant in VSIP Bac Ninh II Industrial Park with a US\$900mil investment. Operations began in 2Q26, with an annual production capacity of 62 million units and an estimated production value exceeding US\$400mil.
- **Seojin Vietnam Co, Ltd:** A subsidiary of South Korea's Seojin System Group implementing eight projects at Song Khe – Noi Hoang Industrial Park totaling over US\$900mil. In early 2026, the group added a plant for semiconductor products and high-tech energy storage systems.
- **Micro Commercial Components:** A US\$90mil project at Yen Phong I Industrial Park that began trial operations in 1Q25.
- **HongKong Fingu Development Company Limited:** A project at Yen Phong II-C Industrial Park producing semiconductor chips, automotive sensors, and communications equipment for 2G, 3G, 4G, and 5G circuits.

Background and Context

The province's ecosystem is anchored by the presence of major corporations including Samsung, Canon, Foxconn, Goertek, and Amkor. To support double-digit economic growth, Bac Ninh has identified three key pillars: digital, transport, and industrial infrastructure. This includes the development of free trade zones, logistics centers, and high-tech industrial parks.

Significance and Outlook

To sustain this growth, Bac Ninh is focusing on the "university-oriented urban area" to attract reputable educational institutions. The province is implementing a cooperation model between the state, enterprises, and educational institutions to align vocational training with the specific workforce needs of the semiconductor industry.

Reference technology guide: Semiconductor Test: <https://troy-technical.com/semiconductor-back-end-term-test/>

Reference company guide: Samsung Electronics: <https://troy-technical.com/semiconductor-back-end-company-samsung-electronics/>

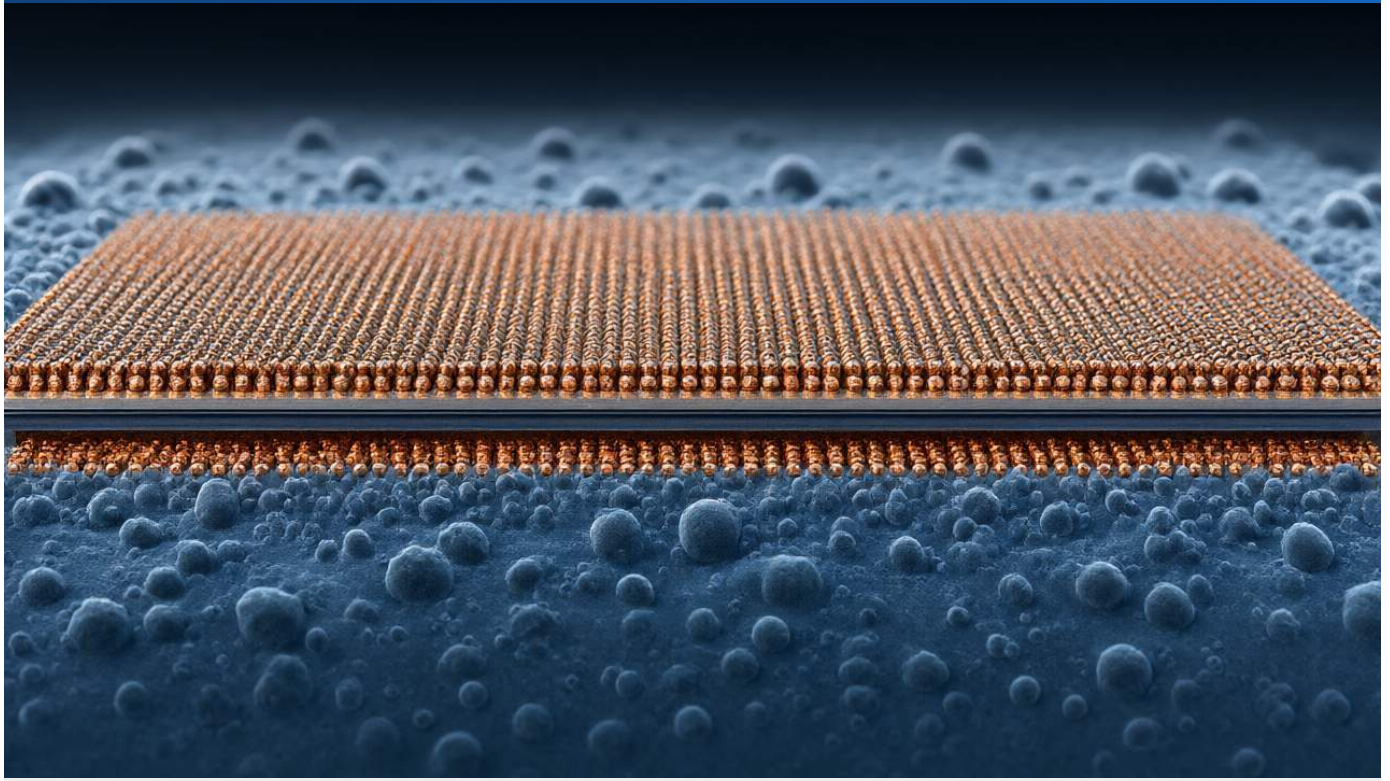
Reference company guide: Amkor Technology: <https://troy-technical.com/semiconductor-back-end-company-amkor/>

Source: <https://www.thestar.com.my/business/business-news/2026/10/16/bac-ninh-eyes-vietnams-semiconductor-hub-status>

Collected: October 17, 2026 | Automated Research System (AI)

#12 Hybrid Bonding: Technical Process, Performance and 2026 Roadmap

Published October 14, 2026 IMAPS 3D InCites Content Platform USA



OVERVIEW

Hybrid bonding enables interconnect pitches below 10um, with Applied Materials and imec/EV group demonstrating pitches of 450nm and 200nm respectively. By eliminating solder bridging and underfill gaps, the technology improves signal bandwidth and heat transfer for high-performance 2.5D/3D packaging. This process is critical for high-layer-count HBM stacks and 224Gbps+ optical engines.

Key Findings

Hybrid bonding significantly increases interconnect density compared to conventional bump limits. At ECTC 2026, Applied Materials demonstrated a 450nm pitch with 98% yield across 20M interconnects, while imec/EV group achieved a 200nm pitch with less than 40nm overlay for 300mm Wafer to Wafer (W2W) bonding. These advancements allow for interconnect pitches as low as 1um, far surpassing the 20um limit of Cu Pillars or the 50um limit of C4 bumps.

Technical Details

The process involves both direct Cu-Cu and dielectric bonding, using either organic polymers or inorganic dielectrics (Si_xO_y , $\text{Si}_x\text{O}_y\text{N}_z$, $\text{Si}_x\text{C}_y\text{N}_z$). There are three primary implementation methods:

- **Die to Die (D2D):** Bonds two individual dies; limited throughput.
- **Die to Wafer (D2W):** Places known-good die on a wafer via room temperature oxide bonds; offers flexibility but increases processing time.
- **Wafer to Wafer (W2W):** Bonds two wafers simultaneously; cost-efficient for simple 2-hi stacks like compute-DRAM or CMOS imagers, though it compounds yield loss.

A critical technical requirement is CMP uniformity. While a controlled Cu recess is necessary to prevent oxide separation during expansion, over-dishing or under-dishing of the copper can lead to bond failures.

Background and Context

Cu-Cu Hybrid bonding was invented between 2004-2005, combining embedded metal bonds with ZIBond (direct oxide-to-oxide bond). Sony has used the technology in high-volume production for CMOS image sensors since 2015. The IP landscape has seen significant shifts, including Tessera Technologies' acquisition of Ziptronix and DTS. Recently, Adeia Inc. settled a patent infringement suit against AMD's 3D V-Cache processors in March 2026 via a multi-year license agreement.

Significance and Outlook

Hybrid bonding reduces vertical interconnect height and thermal interface resistance by eliminating the underfill gap. While more expensive than Thermocompression bonding (TCB) due to stringent processing requirements, it is essential for high-performance interfaces, including high-density chiplet bridges and 224Gbps+ EIC/PIC-based optical engines.

Reference technology guide: Hybrid Bonding: <https://troy-technical.com/semiconductor-back-end-term-hybrid-bonding/>

Reference technology guide: High Bandwidth Memory (HBM): <https://troy-technical.com/semiconductor-back-end-term-hbm/>

Reference technology guide: Bridges & EMIB: <https://troy-technical.com/semiconductor-back-end-term-bridge/>

Reference company guide: AMD: <https://troy-technical.com/semiconductor-back-end-company-amd/>

Reference company guide: Applied Materials: <https://troy-technical.com/semiconductor-back-end-company-applied-materials/>

Source: <https://www.3dincites.com/2026/10/why-hybrid-bonding-is-hard-to-perfect/>

Collected: October 17, 2026 | Automated Research System (AI)

#13 IJM Corporation: RM1.23 Billion AT&S Semiconductor Facility Timeline

Published October 12, 2026 (No explicit source, appears to be a business news portal)

Malaysia



OVERVIEW

IJM Corporation has secured a RM1.23 billion contract to construct semiconductor manufacturing facilities for AT&S Austria Technologie & Systemtechnik in Kedah's Kulim Hi-Tech Park. The project involves building high-end IC substrate and PCB production capacity to support data center processors for clients including AMD.

Key Findings

IJM Construction Sdn Bhd, a wholly owned subsidiary of IJM Corporation Bhd, has accepted a letter of award for the design and construction of semiconductor manufacturing facilities for AT&S Malaysia. The contract is valued at RM1.23 billion. Construction is scheduled to begin in the fourth quarter of 2026 and is expected to reach completion by the fourth quarter of 2027.

Technical Details

The 14-month project scope encompasses design development, procurement, construction, testing, and commissioning. The physical infrastructure consists of three primary structures:

- A four-storey production building targeted for LEED Gold certification.
- A three-storey central utility building.
- A single-storey wastewater treatment facility.

Technical requirements include the installation of cleanrooms, process utilities, mechanical and electrical systems, and civil and structural works. To optimize delivery speed, the project will utilize Industrialised Building System (IBS) precast components.

Background & Context

AT&S Malaysia is a subsidiary of the Vienna-listed AT&S, a manufacturer of integrated circuit (IC) substrates and high-end printed circuit boards (PCBs). The group's Kulim campus began high-volume production of IC substrates for Advanced Micro Devices Inc (AMD) in 2025, primarily for data center processors. AT&S previously invested €1.7 billion in the first phase of the campus, which opened in January 2024. The company has further announced plans to invest between €1.5 billion and €2 billion (approximately RM7 billion to RM9.3 billion) to expand operations, including the construction of new facilities for advanced PCBs and IC substrate cores.

Significance & Outlook

This contract follows RM909.5 million in semiconductor and medical technology projects secured by IJM Construction in August 2026. The award brings IJM Construction's total outstanding order book to RM10.6 billion. According to CEO Datuk Lee Chun Fai, the project demonstrates the company's ability to manage technically complex semiconductor facilities that require high coordination of engineering systems and cleanroom environments under demanding timelines.

Reference technology guide: Semiconductor Test: <https://troy-technical.com/semiconductor-back-end-term-test/>

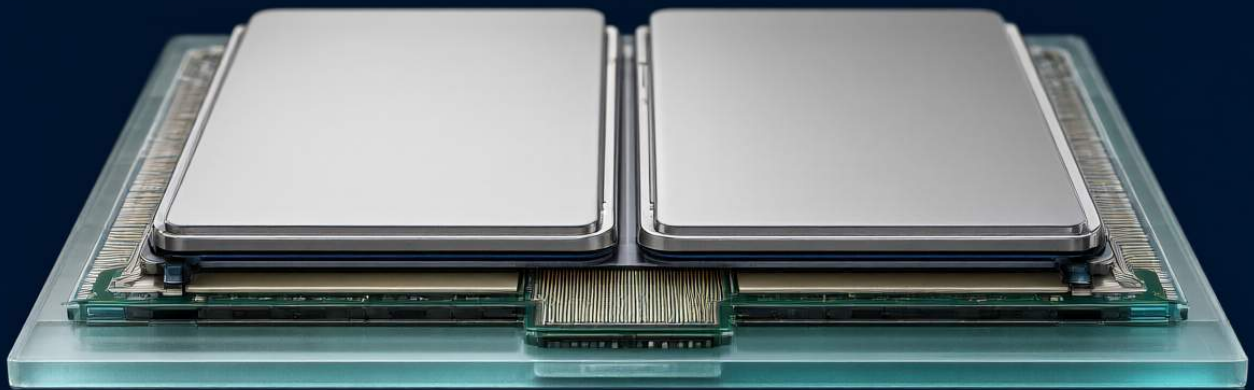
Reference company guide: AMD: <https://troy-technical.com/semiconductor-back-end-company-amd/>

Source: <https://theedgemalaysia.com/node/821536>

Collected: October 17, 2026 | Automated Research System (AI)

#14 Bridge Technology: Next-Gen Large-Format Packaging Roadmap 2026

Published October 13, 2026 The Elec Inc. USA



OVERVIEW

SEMI reports that bridge technology will lead the next generation of large-format semiconductor packaging to overcome the manufacturing constraints of silicon interposers. This shift is driven by the increasing size of AI server packages, which now exceed 100-by-100 mm.

Key Findings

Bridge technology is set to drive the next generation of large-format semiconductor packaging, according to Beth Keser, vice president of SEMI's Advanced Packaging and Heterogeneous Integration (APHI) technology community. This transition is necessary because traditional silicon interposers face significant production constraints as package dimensions increase to meet the demands of AI semiconductors.

Technical Details

Bridge packaging embeds small dies—typically made of silicon—into a flip-chip ball-grid-array (FC-BGA) substrate. Unlike traditional 2.5D packaging, which mounts multiple chips (such as GPUs and HBM) on a single large silicon interposer, bridge structures place high-density wiring only where specifically required between chips.

The industry is exploring both silicon and organic bridge materials:

- **Silicon Bridges:** Intel has used its Embedded Multi-die Interconnect Bridge (EMIB) since 2017. TSMC utilizes CoWoS-L, which embeds local silicon bridges in a redistribution-layer (RDL) interposer, starting with Nvidia's Blackwell platform. OSAT providers ASE and Amkor Technology are developing FoCoS-B and S-Connect, respectively.
- **Organic Bridges:** Samsung Electro-Mechanics and Qualcomm are developing an approach using photosensitive dielectric (PID) for RDLs. Additionally, Shinko Electric Industries is developing integrated Thin film High density Organic Package (i-THOP) for products requiring lower costs than through-silicon-via (TSV) bridges.

Background & Context

The shift is driven by the physical limitations of 300-mm circular silicon wafers. When rectangular packages grow to 100-by-100 mm or larger, the number of interposers per wafer drops to four or fewer due to edge waste. This is critical as AI server packages have expanded from previous CPU sizes of 45-by-45 mm to current dimensions exceeding 100-by-100 mm and reaching 120-by-120 mm.

Significance & Outlook

The rapid growth of package sizes is also accelerating the timeline for glass substrates. Keser noted that the expected adoption date for glass substrates has moved up from 2030 to approximately 2028, with one or two leading companies likely to adopt the technology first.

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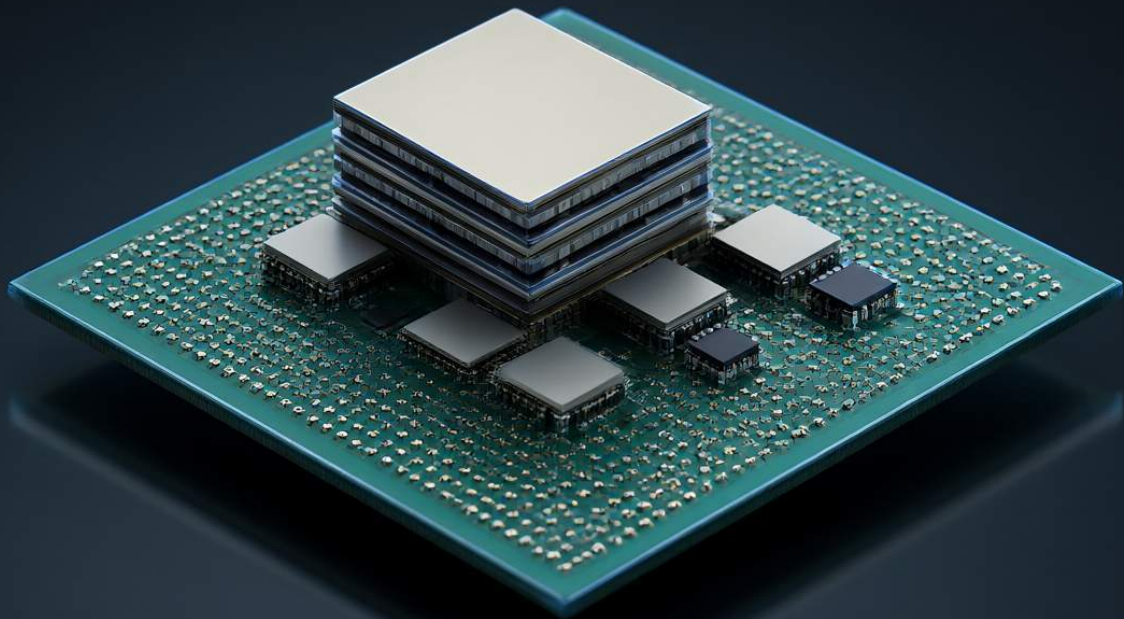
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Collected: October 17, 2026 | Automated Research System (AI)

#15 Intel EMIB and Foveros: Advanced Packaging Roadmaps and Specs

Published October 14, 2026 Tom's Hardware USA



OVERVIEW

Intel is scaling its chiplet strategy through the evolution of EMIB and Foveros to enable system-in-packages (SiPs) up to 12 reticles in size. The roadmap focuses on reducing bump pitches to 25 μm and integrating glass-core substrates to support massive AI accelerators and HBM4-class memory.

Key Findings

Intel is advancing its multi-chiplet strategy by evolving Embedded Multi-die Interconnect Bridge (EMIB) and Foveros technologies to create larger, more efficient system-in-packages (SiPs). The company's ultimate objective is to build SiPs the size of 12 reticles using EMIB and Foveros Direct 3D. This transition allows Intel to deliver performance enhancements cost-efficiently while scaling chips in every direction.

Technical Details of EMIB Evolution

EMIB has transitioned from a simple alternative to silicon interposers to a sophisticated system for high-density die-to-die connectivity. Key technical milestones include:

- **Bump Pitch Reduction:** First-layer-interconnect (FLI) bump pitch has decreased from 55 μm to 45 μm , with future targets of 36 μm and eventually 25 μm to increase shoreline density.
- **EMIB-M:** Incorporates metal-insulator-metal (MIM) capacitors to improve power delivery and suppress voltage fluctuations.
- **EMIB-T:** Adds through-silicon vias (TSVs) to enable vertical power travel, reducing impedance and noise. This is critical for multi-kilowatt SiPs and HBM4-class memory.
- **Physical Scaling:** Package sizes have grown from 4X reticle (80×80 mm) to 8X reticles (120×120 mm), with future 12X SiPs planned for 120×180 mm packages.

Background and Context

Intel began its advanced packaging journey in 2017 with Stratix 10 FPGAs and Kaby Lake-G CPUs. Following challenges with initial 10nm process technology, the company shifted toward a multi-chiplet strategy. Today, EMIB and Foveros are no longer separate technologies but complementary building blocks used across most of Intel's recent client and data center CPU products, including Xeon 6 'Granite Rapids'.

Significance and Outlook

The integration of glass-core substrates is expected to be a major advancement for EMIB, providing better stability and reduced warpage for enormous packages. Intel states that EMIB-T is on track for mass production in 2027, with yields and reliability meeting targets. According to CEO Lip Bu Tan, the technology is essential for advanced AI silicon solutions that are not possible with current mainstream offerings.

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Reference technology guide: System-in-Package (SiP): <https://troy-technical.com/semiconductor-back-end-term-sip/>

Reference technology guide: Bridges & EMIB: <https://troy-technical.com/semiconductor-back-end-term-bridge/>

Reference company guide: Intel: <https://troy-technical.com/semiconductor-back-end-company-intel/>

Source: <https://www.tomshardware.com/tech-industry/semiconductors/analyzing-intels-emib-and-foveros-advanced-packaging-roadmaps-how-intel-plans-to-scale-chips-in-every-direction>

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#16 ZEISS SMT: Inspection and Metrology for Advanced Packaging

Published October 15, 2026 (No explicit source, appears to be a company news release repost)
Germany



OVERVIEW

ZEISS Semiconductor Manufacturing Technology (SMT) has introduced the NLX and DUNE systems to address inspection and wafer bow challenges in advanced packaging. These tools, alongside EUV photomask solutions, enable the production of complex chiplet architectures and High-NA-EUV lithography at scale.

Key Findings

ZEISS SMT is expanding its portfolio to support next-generation semiconductor manufacturing, focusing on advanced packaging and critical lithography processes. The company has introduced the ZEISS NLX and ZEISS DUNE systems to manage the increased complexity of chip architectures, specifically where multiple chips or chiplets are integrated into compact spaces.

Technical Details: Advanced Packaging

- **ZEISS NLX:** A non-destructive inspection system designed for 300-millimeter wafers. It allows manufacturers to visualize internal structures in chip packages, such as connections between stacked dies, to detect defects early. It is compatible with both process development and high-volume production.
- **ZEISS DUNE:** A metrology system that measures and individually corrects wafer bow. By managing wafer topography, the system helps avoid yield losses in downstream processing and prepares wafers for bonding processes.

Technical Details: Lithography and Photomasks

To ensure stable lithography, ZEISS SMT provides specialized photomask solutions. The ZEISS AIMS EUV 3.0 inspects photomasks under optical conditions that mirror those of the wafer scanner, allowing for the detection of critical defects before production. This system supports both Low-NA-EUV and High-NA-EUV lithography and triples mask throughput.

Complementing this is the ZEISS MeRiT system, which enables the targeted repair of the smallest defects on photomasks, providing a final qualification step following the AIMS EUV process.

Significance and Outlook

According to Christoph Henschel, President of ZEISS Semiconductor Manufacturing Optics, the next generation of manufacturing relies on the precise interaction of complex process steps rather than isolated technology leaps. Axel Christian, President of ZEISS North America, emphasizes that as manufacturing becomes more demanding, photomask quality becomes increasingly critical. By combining optical systems, process control, and advanced packaging solutions, ZEISS SMT intends to help customers bring future chip generations into production reliably and productively.

Reference technology guide: Chiplets: <https://troy-technical.com/semiconductor-back-end-term-chiplet/>

Source: <https://metrology.news/zeiss-advances-inspection-and-metrology-for-next-generation-semiconductor-manufacturing/>

Collected: October 17, 2026 | Automated Research System (AI)

#17 CIT ASEDep: Single-Crystal Copper Deposition for AI Packaging

Published October 15, 2026 (No explicit source, appears to be a press release repost) South Korea



OVERVIEW

CIT has introduced ASEDep, a manufacturing solution for semiconductor packaging substrates that utilizes single-crystal copper deposition. The technology aims to overcome the limitations of conventional copper to enable ultra-flat, ultra-thin package cores for AI semiconductors.

Key Findings

CIT has developed a semiconductor packaging substrate manufacturing solution called ASEDep. This technology is designed to break through the limitations associated with conventional copper used in AI semiconductor packaging by implementing a single-crystal copper deposition process.

Technical Details

The ASEDep solution utilizes ASE technology to bond copper and insulators into a single-crystal structure. This process enables the production of the CuFlat-PKGCore, a copper flat package core specifically designed for AI semiconductor packages. According to the technical specifications provided, the copper in these cores is deposited to an ultra-flat and ultra-thin state, addressing the physical constraints of traditional packaging materials.

Background and Context

The development of ASEDep addresses the increasing demands of AI semiconductor packaging, where conventional copper deposition methods have faced limitations. To support the production of these substrates, CIT has established a single-crystal copper substrate production facility. The company's efforts in this field have recently gained recognition, as CIT won the Grand Prize at FLY ASIA, providing the company a platform to showcase its technology in Silicon Valley.

Significance and Outlook

By transitioning from conventional copper to a single-crystal structure, CIT's ASEDep provides a pathway toward thinner and flatter package cores. This advancement is critical for the scaling and performance requirements of next-generation AI semiconductor packaging, where substrate flatness and material properties directly impact the efficiency of the final package. The integration of the CuFlat-PKGCore into AI hardware represents a shift toward higher precision in substrate manufacturing.

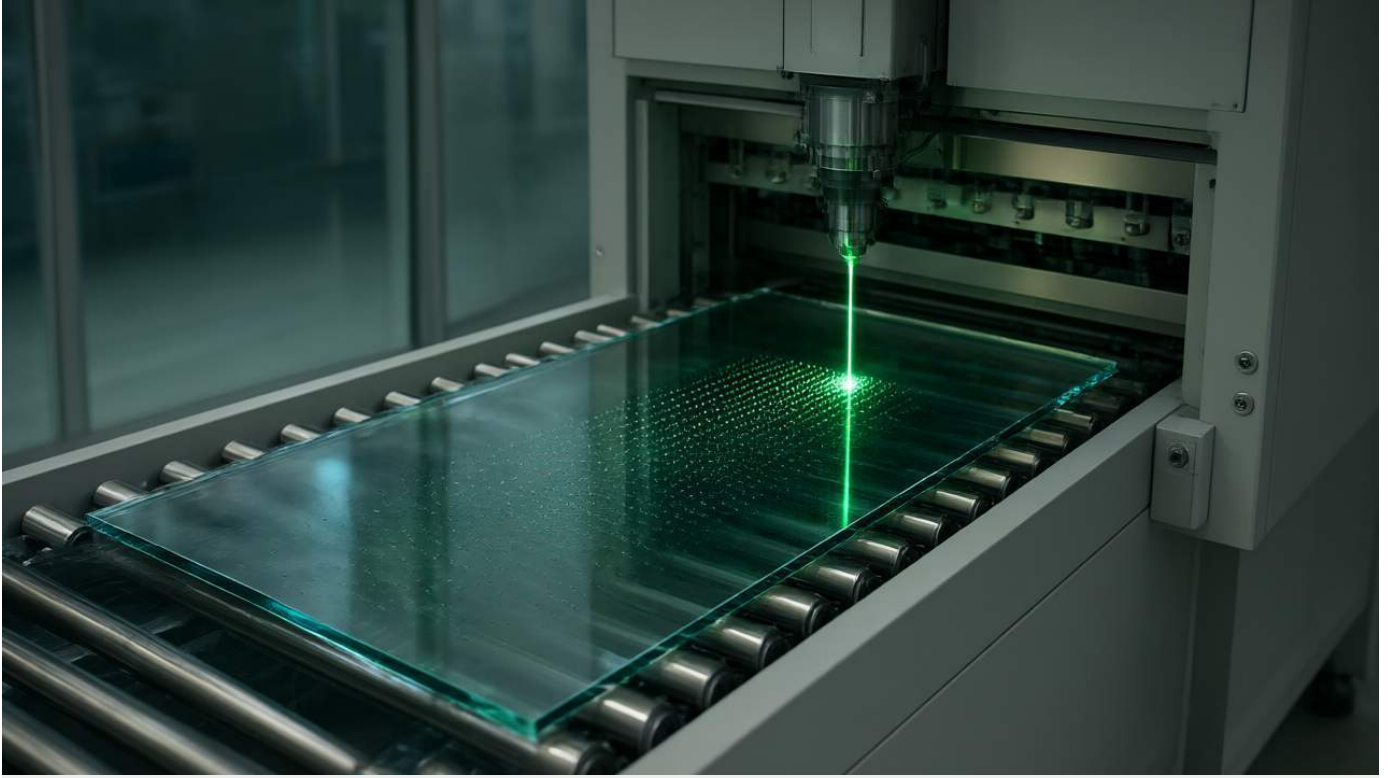
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Collected: October 17, 2026 | Automated Research System (AI)

#18 FCS and CKST: Glass Substrate Equipment Distribution for AI Chips

Published October 09, 2026 CPRJAdsale Plastics Network Taiwan



OVERVIEW

FCS Precision Industry Co., Ltd. has secured exclusive distribution rights for China Korea Smart Technology (CKST) equipment in Taiwan and Southeast Asia. The partnership focuses on glass substrate equipment for next-generation AI chips and high-performance computing (HPC) advanced packaging.

Key Findings

FCS Precision Industry Co., Ltd. and Korea-based China Korea Smart Technology (CKST) have entered a strategic cooperation agreement. Under this exclusive distribution agreement, FCS will provide CKST's glass substrate equipment to customers in Taiwan and Southeast Asia, targeting the PCB, IC substrate, and semiconductor packaging and testing sectors.

Technical Details

The collaboration introduces three primary categories of equipment designed for advanced semiconductor packaging:

- **Advanced VP Vertical Plating Equipment:** Utilizes proprietary control technology to maintain plating deviation within 3%.
- **High-Speed VCP Vertical Continuous Plating Equipment:** Engineered for large-scale mass production efficiency.
- **High-Performance SPP Panel-Level Plating Equipment:** Provides a comprehensive solution covering TGV via filling through mass-production plating applications.

These systems leverage CKST's expertise in glass substrate TGV, VP, VCP, and advanced packaging, combined with FCS's capabilities in precision manufacturing, automation integration, and system integration.

Background & Context

The shift toward glass substrates is driven by the limitations of conventional organic substrates, such as ABF, which face thermal stress and warpage challenges as package sizes increase for large language models and AI computing. Glass substrates offer high rigidity, low warpage, and strong high-frequency electrical performance, making them a viable solution for next-generation AI and HPC packaging, despite ongoing mass-production technical challenges.

Significance & Outlook

This partnership is part of a dual-track semiconductor growth strategy for FCS. While the distribution of CKST equipment serves as one growth engine, FCS is simultaneously investing NT\$200 million to establish an AI manufacturing base and advanced MLPC (Multilayer Solid Capacitor) production line. This second initiative targets the demand for high-power, high-voltage, and low-ESR components in GPU accelerator cards, AI servers, and automotive electronics, addressing a market of approximately six billion units annually through import-substitution.

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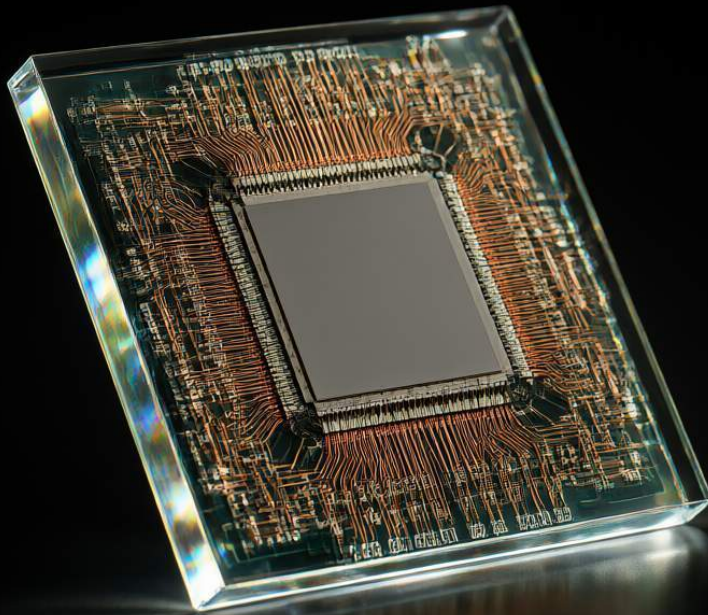
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Source: https://www.adsalecprj.com/en/news/article_details/90309.html

Collected: October 17, 2026 | Automated Research System (AI)

#19 Samsung Electro-Mechanics: 100mm Glass Substrate Testing Roadmap

Published October 10, 2026 digitimes Taiwan



OVERVIEW

Samsung Electro-Mechanics (Semco) has transitioned its 100mm glass substrates from initial reliability testing to package-level verification. This phase utilizes customer chips to validate the technology, marking a step toward the commercialization of next-generation packaging.

Key Findings

Samsung Electro-Mechanics (Semco) has reportedly completed the initial reliability testing phase for its 100mm glass substrates. The company has now progressed to package-level verification, a critical stage in the development cycle that involves integrating actual customer chips to ensure functional compatibility and performance.

Technical Details

The current technical focus is centered on the 100mm glass substrate format. Having passed the preliminary reliability benchmarks, the verification process has shifted from isolated material testing to a system-level approach. By employing customer chips in the package-level testing, Semco is evaluating how the glass substrate performs as a foundation for active semiconductor components in a real-world packaging configuration.

Background & Context

Glass substrates are being developed as a next-generation alternative to traditional packaging materials. The transition from initial reliability tests to package-level verification indicates that the material has met basic durability and stability requirements, allowing the company to move toward the final stages of technical validation required for industry adoption.

Significance & Outlook

The move to package-level verification using customer chips represents significant progress toward the commercialization of this packaging technology. By validating the substrates with actual hardware, Semco is bridging the gap between laboratory reliability and commercial viability, positioning the 100mm glass substrate for future deployment in high-performance packaging applications.

Source: <https://www.digitimes.com/news/a20261008VL220/semco-glass-substrate-testing-expansion.html>

#20 Intel Advanced Packaging: EMIB-T and Foveros Roadmap to 2028

Published October 15, 2026 BigGo Finance USA



OVERVIEW

Intel is scaling its EMIB and Foveros packaging platforms to achieve 12x reticle-size system-in-package (SiP) by 2028 to compete with TSMC's CoWoS. Key advancements include the mass production of EMIB-T next year and the introduction of copper-to-copper hybrid bonding in Foveros Direct 3D.

Key Findings

Intel is transitioning its advanced packaging from high-end processor support to a core strategy for the AI chip market. The company targets 12x reticle-size SiPs on 120×180mm packages by 2028, utilizing glass-core substrates for improved stability and lower warpage. CEO Lip-Bu Tan noted during the August 2026 earnings call that customer interest in EMIB-T is very high, with production capacity ramping planned for 2027.

Technical Details: EMIB and Foveros

The EMIB (Embedded Multi-die Interconnect Bridge) roadmap focuses on shrinking interconnect pitches from 55 microns to 45, then 36, and eventually 25 microns. Functional iterations include EMIB-M, which integrates metal-insulator-metal (MIM) capacitors, and EMIB-T, which employs through-silicon vias (TSVs) for vertical power delivery to support HBM4-class memory and multi-kilowatt SiPs.

The Foveros family is positioned against TSMC's CoWoS with three 2.5D variants:

- **Foveros-S:** Uses a silicon interposer; currently supports up to 4x reticle size.
- **Foveros-R:** Uses fan-out redistribution layer (RDL) technology; mass production planned for 2027.
- **Foveros-B:** Combines RDL with localized silicon bridges.

These variants target sub-25-micron pitches and bump densities increasing from 772 to 1,600 connections per square millimeter, with interconnect power of 0.15 pJ/bit.

Foveros Direct 3D and Hybrid Bonding

Foveros Direct 3D replaces solder with copper-to-copper hybrid bonding, achieving interconnect pitches below 10 microns. This technology enables densities up to 10,000 connections per square millimeter and reduces interconnect power to below 0.05 pJ/bit. The Xeon 6+ "Clearwater Forest" processor is the first mass-produced product to utilize this bonding for Intel 18A compute dies.

Significance and Outlook

By evolving toward finer pitches and larger package sizes, Intel aims to capture spillover orders resulting from TSMC's CoWoS supply constraints. The move toward glass substrates and hybrid bonding is critical for reducing latency and improving heat dissipation in vertically stacked logic circuits.

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Reference technology guide: System-in-Package (SiP): <https://troy-technical.com/semiconductor-back-end-term-sip/>

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Collected: October 17, 2026 | Automated Research System (AI)