TROY TECHNICAL

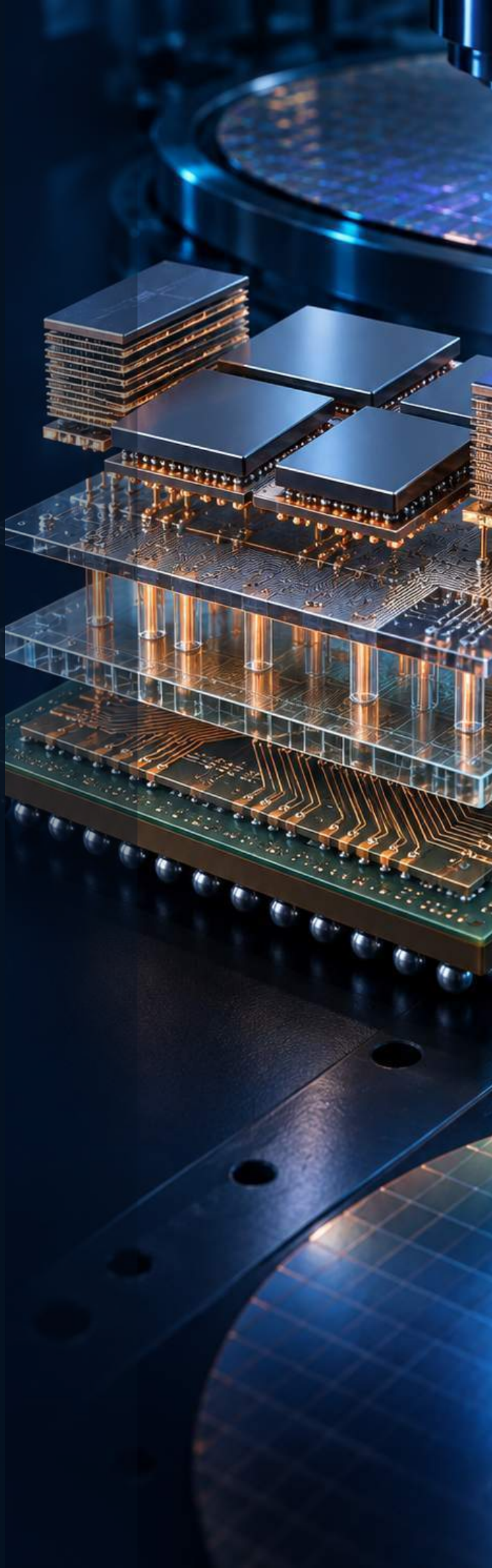
SEMICONDUCTOR BACK-END WEEKLY REPORT

October 24 - October 30, 2026 | Issue 2026-W43

Package performance, process yield, test coverage and qualified capacity

9	9
ANALYZED ARTICLES	PRIORITY THEMES

Issued 2026-10-30 | English edition | fixed approved cover artwork



Semiconductor Back-End: the boundary moved from isolated claims to qualification evidence

9 English articles were reviewed independently from the Japanese edition. Ten themes are retained for management decisions.

SIGNAL 01 | MATERIALS

ASE and SPIL: AMD Venice PLP Roadmap and Broadcom Joint Venture

ASE has showcased a panel-level packaging (PLP) solution for AMD's Venice server processors, targeting initial production in Q1 2027.

SIGNAL 02 | BONDING & ASSEMBLY

Lam and imec: 3D Integration and High-NA EUV Roadmap for AI

Lam Research and imec are collaborating to accelerate the transition of 3D integration and advanced patterning technologies from the lab to high-volume manufacturing.

SIGNAL 03 | ADVANCED PACKAGE

Glass Substrate Packaging: 510x515mm Size and Warpage Constraints

Panel-level glass substrates are shifting toward a 510x515mm standard to increase area utilization from 45-65% to over 81% compared to 300mm wafers.

SIGNAL 04 | TEST & INSPECTION

Hunan Titan Future: China's First 12-Inch Polycrystalline SiC Substrate

Hunan Titan Future Technology has developed China's first 12-inch polycrystalline silicon carbide (SiC) substrate featuring thermal conductivity exceeding 280 W/(m·K).

DECISION

Focus this week's management attention on package performance, process yield, test coverage and qualified capacity. Move only when the linked evidence can be reproduced under your own operating conditions.

THREE MANAGEMENT MOVES

1. Buyers: compare architectures using thermal, electrical, yield, repair and supply evidence.
2. Suppliers: co-develop materials, bonding, inspection and reliability windows with customers.
3. Executives: track yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EVIDENCE DISCIPLINE

FACT states what the collected English source reports. BUSINESS READ and ACTION are editorial interpretations. UNKNOWN lists information that the source file does not establish. A linked article is not treated as independent confirmation of every claim.

Five numbers or evidence anchors that require conditions

$400 million
A04

SOURCE-BOUND CONDITION
Simultaneously, SPIL received approval for a $400 million joint venture with Broadcom in Singapore to produce advanced PLP substrates for CPO applications by 2028.

510x
A08

SOURCE-BOUND CONDITION
Panel-level glass substrates are shifting toward a 510x515mm standard to increase area utilization from 45-65% to over 81% compared to 300mm wafers.

280 W
A09

SOURCE-BOUND CONDITION
Hunan Titan Future Technology has developed China's first 12-inch polycrystalline silicon carbide (SiC) substrate featuring thermal conductivity exceeding 280 W/(m·K).

200mm
A07

SOURCE-BOUND CONDITION
The research team successfully produced 200mm-class glass substrate specimens and demonstrated precise Through Glass Via (TGV) formation on 100mm-class substrates.

510mm
A03

SOURCE-BOUND CONDITION
By replacing circular wafers with rectangular panels up to 515×510mm, manufacturers can increase processing area by more than 3.5 times compared to 300mm wafers.

HOW TO USE THESE NUMBERS
Each value is shown with the condition stated in the collected English article. Do not compare values across different test methods, device sizes, operating temperatures or commercial stages without normalizing those conditions.

Where the value chain moved

Each stage combines one leading theme and one supporting theme. The report treats handoffs as evidence transfers, not decorative arrows.

1

Materials

P01/P06

ASE has showcased a panel-level packaging (PLP) solution for AMD's Venice server processors, targeting initial production in.

2

Bonding & assembly

P02/P07

Lam Research and imec are collaborating to accelerate the transition of 3D integration and advanced patterning technologies.

3

Advanced package

P03/P08

Panel-level glass substrates are shifting toward a 510x515mm standard to increase area utilization from 45-65% to over 81%.

4

Test & inspection

P04/P09

Hunan Titan Future Technology has developed China's first 12-inch polycrystalline silicon carbide (SiC) substrate featuring.

5

Volume supply

P05/P01

Micron plans to integrate wafer bonding and High-NA EUV lithography into its next-generation DRAM to enable vHBM and vEIM.

EVIDENCE REQUIRED AT EACH HANDOFF

Materials to Bonding & assembly	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Bonding & assembly to Advanced package	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Advanced package to Test & inspection	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Test & inspection to Volume supply	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.

COMMON CONTROL POINT

No theme moves to a commercial commitment until a named owner has reproduced the relevant evidence and documented yield, warpage, thermal cycling, test time, capacity, cost and qualification.

Priority map: maturity and next decision locus



P01	ASE and SPIL: AMD Venice PLP Roadmap and Broadcom Joint Venture Tech / process | cue: no system/business cue
P02	Lam and imec: 3D Integration and High-NA EUV Roadmap for AI System / adoption | cue: Integration
P03	Glass Substrate Packaging: 510x515mm Size and Warpage Constraints Business / rules | cue: standard
P04	Hunan Titan Future: China's First 12-Inch Polycrystalline SiC Substrate Tech / process | cue: no system/business cue
P05	Micron DRAM Roadmap: Wafer Bonding and High-NA EUV for 2028 System / adoption | cue: integrate
P06	Photosensitive Crystallizable Glass: KICET's TGV Process for Semiconductors Tech / process | cue: no system/business cue
P07	CoPoS Packaging: TSMC and Samsung's Shift to Panel-Level RDL System / adoption | cue: integration
P08	GIST Glass Substrates: Low-Dielectric Material for AI Chips Tech / process | cue: no system/business cue
P09	AI Chip Packaging: CoWoS-L vs EMIB-T Roadmap through 2028 System / adoption | cue: adopters

REPRODUCIBLE POSITIONING RULE

Horizontal position uses five discrete stages: Research, Prototype, Joint evaluation, Product adoption and Scale. The vertical bands classify the next decision locus: Tech / process, System / adoption, or Business / rules (including supply systems). Article-title cues take precedence; the overview is used only when the title is silent. These are categories, not impact ranks. Bubble diameter reflects the editorial score.

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P01 ASE and SPIL: AMD Venice PLP Roadmap and Broadcom Joint Venture

A04 | Materials | Product adoption

Date not stated

FACT

ASE has showcased a panel-level packaging (PLP) solution for AMD's Venice server processors, targeting initial production in Q1 2027. Simultaneously, SPIL received approval for a $400 million joint venture with Broadcom in Singapore to produce advanced PLP substrates for CPO applications by 2028.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P01.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 21/25 | MATURITY 4/5 | DECISION LOCUS: TECH / PROCESS

P02 Lam and imec: 3D Integration and High-NA EUV Roadmap for AI

A10 | Bonding & assembly | Joint evaluation

Date not stated

FACT

Lam Research and imec are collaborating to accelerate the transition of 3D integration and advanced patterning technologies from the lab to high-volume manufacturing. The partnership focuses on solving process challenges for advanced packaging, next-generation memory, and angstrom-era logic devices to meet AI-driven demands for bandwidth and density.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P02.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 3/5 | DECISION LOCUS: SYSTEM / ADOPTION

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P03 Glass Substrate Packaging: 510x515mm Size and Warpage Constraints

A08 | Advanced package | Research

Date not stated

FACT

Panel-level glass substrates are shifting toward a 510x515mm standard to increase area utilization from 45-65% to over 81% compared to 300mm wafers. However, scaling is limited by a "warpage wall" where warpage displacement increases with the square of the side length ($w \propto L2$), creating a trade-off between cost efficiency and yield.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P03.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | DECISION LOCUS: BUSINESS / RULES

P04 Hunan Titan Future: China's First 12-Inch Polycrystalline SiC Substrate

A09 | Test & inspection | Pilot

Date not stated

FACT

Hunan Titan Future Technology has developed China's first 12-inch polycrystalline silicon carbide (SiC) substrate featuring thermal conductivity exceeding 280 W/(m·K). Designed for AI computing chips and advanced packaging, the substrate addresses heat dissipation challenges in high-power semiconductor operations.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P04.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 2/5 | DECISION LOCUS: TECH / PROCESS

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P05 Micron DRAM Roadmap: Wafer Bonding and High-NA EUV for 2028

A02 | Volume supply | Scale-up

Date not stated

FACT

Micron plans to integrate wafer bonding and High-NA EUV lithography into its next-generation DRAM to enable vHBM and vEIM mass production by 2028. The strategy prioritizes the optimization of 6F2 cells over 4F2 to balance memory density with manufacturing cost and complexity.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P05.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 5/5 | DECISION LOCUS: SYSTEM / ADOPTION

P06 Photosensitive Crystallizable Glass: KICET's TGV Process for Semiconductors

A07 | Materials | Product adoption

Date not stated

FACT

The Korea Institute of Ceramic Technology (KICET) has developed a photosensitive crystallizable glass material to enable the domestic production of next-generation semiconductor substrates. The research team successfully produced 200mm-class glass substrate specimens and demonstrated precise Through Glass Via (TGV) formation on 100mm-class substrates.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P06.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 4/5 | DECISION LOCUS: TECH / PROCESS

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P07 CoPoS Packaging: TSMC and Samsung's Shift to Panel-Level RDL

A03 | Bonding & assembly | Research

Date not stated

FACT

The industry is shifting from CoWoS to CoPoS (Chip-on-Panel-on-Substrate) to overcome area utilization limits in GPU and HBM integration. By replacing circular wafers with rectangular panels up to 515×510mm, manufacturers can increase processing area by more than 3.5 times compared to 300mm wafers.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P07.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

P08 GIST Glass Substrates: Low-Dielectric Material for AI Chips

A05 | Advanced package | Pilot

Date not stated

FACT

Researchers at the Gwangju Institute of Science and Technology (GIST) have developed a low-dielectric aluminoborosilicate glass material to replace polymer-based organic substrates in AI semiconductors. This technology addresses heat-induced warping and signal attenuation in high-frequency data transmission.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P08.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 2/5 | DECISION LOCUS: TECH / PROCESS

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P09 AI Chip Packaging: CoWoS-L vs EMIB-T Roadmap through 2028

A01 | Test & inspection | Research

Date not stated

FACT

AI chip package sizes are expanding toward and beyond the reticle limit to accommodate increasing compute and memory bandwidth demands. TSMC's CoWoS-L is expected to remain the mainstream solution through 2028, while Intel's EMIB-T emerges as a high-density alternative for specific adopters.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P09.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

Playbook and 0-5 year roadmap

STAKEHOLDER	NOW | 0-30 DAYS	NEXT | 1-12 MONTHS	LATER | 1-5 YEARS
Operating companies	compare architectures using thermal, electrical, yield, repair and supply evidence	Run production-like qualification with explicit acceptance and stop criteria.	Build a portfolio and architecture that can absorb technology and supplier changes.
Materials, equipment and technology suppliers	co-develop materials, bonding, inspection and reliability windows with customers	Create shared reliability, process-window and failure-analysis data with customers.	Standardize interfaces, traceability, lifecycle support and recovery services.
Trading, investment and legal teams	Map yield, warpage, thermal cycling, test time, capacity, cost and qualification.	Contract for capacity, quality, change notice, liability, alternatives and exit.	Diversify regional, technical and customer concentration risk.

ROADMAP

NOW | 0-30 DAYS
Evidence ledger
Owner: Strategy + quality
Deliverable: claim, source, condition, owner

NOW | 0-30 DAYS
Risk screen
Owner: Procurement + legal
Deliverable: unknowns, alternatives, stop

NEXT | 1-12 MONTHS
Joint qualification
Owner: R&D + supplier
Deliverable: process window and failure data

NEXT | 1-12 MONTHS
Commercial gate
Owner: Business + finance
Deliverable: unit economics and capacity

LATER | 1-5 YEARS
Platform strategy
Owner: Executive team
Deliverable: portfolio and interface roadmap

LATER | 1-5 YEARS
Service layer
Owner: Operations + channel
Deliverable: monitoring, maintenance and recovery

GO / NO-GO GATES

GATE	OWNER	REQUIRED EVIDENCE	NO-GO CONDITION
G1 Evidence	**Quality**	Source, test conditions and reproducibility	No traceable evidence
G2 Integration	**R&D**	Interface, process window and failure analysis	Cannot meet system conditions
G3 Commercial	**Business**	Capacity, total cost, contract and alternatives	Economics or supply cannot be supported
G4 Lifecycle	**Operations**	Monitoring, maintenance, change notice and exit	No accountable operating plan

ANALYZED ARTICLES | ITEMS 01-10

Every title and URL is displayed in full. URLs wrap without shortening and remain clickable. A verified-reference label means the translated HTML did not retain its original source URL.

ID	FULL ARTICLE TITLE	FULL SOURCE / VERIFIED REFERENCE URL - CLICKABLE
A01	AI Chip Packaging: CoWoS-L vs EMIB-T Roadmap through 2028	https://finance.biggo.com/news/4eb5b699-fd87-4922-8d26-0463a5d2360e
A02	Micron DRAM Roadmap: Wafer Bonding and High-NA EUV for 2028	https://xenospectrum.com/en/micron-dram-bonding-vertical-memory/
A03	CoPoS Packaging: TSMC and Samsung's Shift to Panel-Level RDL	https://eu.36kr.com/en/p/4042012488962946
A04	ASE and SPIL: AMD Venice PLP Roadmap and Broadcom Joint Venture	https://www.blocktempo.com/ase-amd-venice-panel-level-packaging-powertech-broadcom-singapore-plant/
A05	GIST Glass Substrates: Low-Dielectric Material for AI Chips	https://www.mt.co.kr/index.php/en/future/2026/10/25/2026101915054962909
A07	Photosensitive Crystallizable Glass: KICET's TGV Process for Semiconductors	https://www.fnnews.com/news/202610291026456501
A08	Glass Substrate Packaging: 510x515mm Size and Warpage Constraints	https://finance.sina.com.cn/wm/2026-10-27/doc-iniwrzht4588328.shtml
A09	Hunan Titan Future: China's First 12-Inch Polycrystalline SiC Substrate	https://www.trendforce.com/news/2026/10/29/news-chinas-first-12-inch-polycrystalline-silicon-carbide-substrate-unveiled/
A10	Lam and imec: 3D Integration and High-NA EUV Roadmap for AI	https://www.electronicsweekly.com/news/business/lam-and-imec-pursue-3-d-integration-2026-10/

Semiconductor_BackEnd — Selected Articles

Date: 2026-10-31

Articles: 9

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#09 Hunan Titan Future: China's First 12-Inch Polycrystalline SiC Substrate

#10 Lam and imec: 3D Integration and High-NA EUV Roadmap for AI

#01 AI Chip Packaging: CoWoS-L vs EMIB-T Roadmap through 2028

Published October 28, 2026 BigGo Finance

OVERVIEW

AI chip package sizes are expanding toward and beyond the reticle limit to accommodate increasing compute and memory bandwidth demands. TSMC's CoWoS-L is expected to remain the mainstream solution through 2028, while Intel's EMIB-T emerges as a high-density alternative for specific adopters.

IN DEPTH

Key Findings

AI chip packaging is shifting toward larger sizes to integrate more Chiplets and HBM. Nvidia's Blackwell GPU has reached approximately 3.3x the reticle limit, with the next-generation Rubin platform expected to reach 4x. TSMC's CoWoS-L is projected to remain the dominant advanced packaging solution through 2028 due to its technical maturity and yield advantages, although Intel's EMIB-T is positioning itself as a competitive alternative.

Technical Details

TSMC utilizes three CoWoS variants: CoWoS-S (large-area silicon interposer), CoWoS-R (redistribution layer/RDL), and CoWoS-L. CoWoS-L combines these by embedding local silicon interconnect (LSI) dies within the RDL. This allows high-density routing only where needed (e.g., SoC-to-HBM), reducing cost and complexity compared to full silicon interposers. TSMC mass-produced 3.5x reticle CoWoS-L in 2024 and plans to mass-produce a 5.5x reticle solution in 2026.

Intel's EMIB-T embeds small silicon bridges in the package substrate rather than using a full interposer. The "T" upgrade adds through-silicon vias (TSVs) for vertical power delivery. At ECTC 2026, Intel presented a solution with a 25-micrometer first-layer interconnect bump pitch and a package size of 120mm x 120mm, supporting over 9 reticle areas of chips and 12Gb/s HBM4e.

Background and Context

Package sizes have grown steadily; TSMC's CoWoS silicon interposers evolved from 1.5x reticle size (1,287 square millimeters) in 2016 to 3.3x (2,831 square millimeters) today. Equipment is adapting to this trend, such as HANMI Semiconductor's FC Bonder 75, which supports 75mm x 75mm packaging compared to the conventional 20mm x 20mm. High-end GPU shipments for Nvidia are expected to grow 30% year-on-year in 2026, while AMD will push MI400 and MI450 in the second half of 2026.

Significance and Outlook

Adoption patterns are diverging by provider. Nvidia, AMD, and Meta (MTIA 400) already use CoWoS-L, with Microsoft and AWS expected to adopt it in 2027. Conversely, Google is expected to adopt EMIB-T in 2027, and AWS is currently testing EMIB technology.

Reference technology guide: CoWoS: https://troy-technical.com/semiconductor-back-end-term-cowos/

Reference technology guide: High Bandwidth Memory (HBM): https://troy-technical.com/semiconductor-back-end-term-hbm/

Reference technology guide: Interconnects: https://troy-technical.com/semiconductor-back-end-term-interconnect/

Reference company guide: TSMC: https://troy-technical.com/semiconductor-back-end-company-tsmc/

Reference company guide: NVIDIA: https://troy-technical.com/semiconductor-back-end-company-nvidia/

Reference company guide: Intel: https://troy-technical.com/semiconductor-back-end-company-intel/

Source: https://finance.biggo.com/news/4eb5b699-fd87-4922-8d26-0463a5d2360e

Collected: October 31, 2026 | Automated Research System (AI)

#02 Micron DRAM Roadmap: Wafer Bonding and High-NA EUV for 2028

Published October 26, 2026 Xenospectrum USA

OVERVIEW

Micron plans to integrate wafer bonding and High-NA EUV lithography into its next-generation DRAM to enable vHBM and vEIM mass production by 2028. The strategy prioritizes the optimization of 6F² cells over 4F² to balance memory density with manufacturing cost and complexity.

IN DEPTH

Key Findings

Micron is targeting 2028 for the mass production of the first generation of vHBM, which stacks memory on compute chips, and vEIM, designed for AI inference on edge devices. To achieve this, the company is pursuing a dual-track strategy: shrinking DRAM memory cells while simultaneously advancing packaging technologies to shorten data paths between memory and compute chips.

Technical Details

Micron's roadmap outlines a progression of manufacturing generations:

- **1γ (1-gamma):** Current production generation utilizing EUV lithography.
- **1δ (1-delta):** Planned for volume ramp-up in the second half of 2027, targeting a bit-density improvement in the mid-20% range over 1γ. This will serve as the foundation for HBM5, vHBM, and vEIM.
- **1ε (1-epsilon):** Under development; planned introduction of wafer bonding.
- **ζÅ:** Early development stage; planned adoption of High-NA EUV lithography (increasing numerical aperture from 0.33 to 0.55).
- **ηÅ:** Technology exploration stage; focused on new materials.

Background & Context

Micron has decided to skip the $4F^2$ cell architecture, despite 20 years of research, citing excessive complexity and cost. Instead, the company will continue improving the existing $6F^2$ cell and developing 3D DRAM. Regarding peripheral circuits, Micron is exploring wafer bonding to decouple the manufacturing of memory cells and peripheral circuits. This approach addresses the constraint where peripheral circuits must otherwise withstand high-temperature heat treatments (550–600°C) required for memory cell fabrication.

Significance & Outlook

By separating the production of peripheral circuits and memory cells via wafer bonding, Micron seeks to optimize manufacturing conditions for each component and improve overall performance. While High-NA EUV improves resolution to form finer patterns, wafer bonding addresses the physical arrangement and scaling of circuits. These combined efforts aim to extend conventional DRAM scaling and restructure memory architecture specifically for AI workloads.

Reference technology guide: Bonding: https://troy-technical.com/semiconductor-back-end-term-bonding/

Source: https://xenospectrum.com/en/micron-dram-bonding-vertical-memory/

#03 CoPoS Packaging: TSMC and Samsung's Shift to Panel-Level RDL

Published October 26, 2026 36Kr Europe China

OVERVIEW

The industry is shifting from CoWoS to CoPoS (Chip-on-Panel-on-Substrate) to overcome area utilization limits in GPU and HBM integration. By replacing circular wafers with rectangular panels up to 515×510mm, manufacturers can increase processing area by more than 3.5 times compared to 300mm wafers.

IN DEPTH

Key Findings

CoPoS is emerging as a successor to CoWoS to address the limitations of traditional wafer-level packaging as GPU and HBM integration scales. According to analysis from Infomarket CEO Yong-woon Kang, TSMC is advancing R&D in this direction, and Samsung Electro-Mechanics is also exploring related technologies. The transition shifts the processing carrier from a circular wafer to a rectangular panel, significantly reducing edge area loss.

Technical Details

The CoPoS workflow utilizes an organic redistribution layer (RDL) as the interposer structure. The process follows these stages:

- **RDL Fabrication:** Ultra-fine circuits (approximately 2 microns linewidth) are fabricated on a temporary glass carrier.
- **Chip Mounting:** GPU chips (approx. 26×33mm) and HBM stacks (approx. 11×12mm) are mounted on the RDL with a micro-bump pitch of 25 to 40 microns and alignment accuracy of ±1 to 2 microns.
- **Encapsulation:** Molding compound encapsulates the chips and RDL for mechanical strength.
- **Dicing and Connection:** The glass carrier is stripped, and the panel is diced into independent packaged units (69 to 90mm square) before being connected to the organic packaging substrate.

Crucially, the glass in current CoPoS solutions serves as a temporary carrier; the final RDL interposer remains an organic material structure.

Equipment Requirements

The shift to panel sizes expanding from 310×310mm to 515×510mm drives demand for specific hardware:

- **40mm-class TC thermal compression bonders:** Used for the initial mounting of GPU and HBM stacks.

- **MSVP (Micro SAW & VISION PLACEMENT) systems:** Integrated systems for dicing, cleaning, inspection, and placement of the molded panels.
- **120mm-class TC bonders:** Used for the final connection between the packaged unit and the substrate.

Significance and Outlook

The transition to CoPoS allows for a processing area more than 3.5 times larger than a 300mm wafer. Future growth in equipment demand is expected to align with the development of glass interposers and glass core substrates.

Reference technology guide: CoPoS: https://troy-technical.com/semiconductor-back-end-term-copos/

Reference technology guide: Redistribution Layer (RDL): https://troy-technical.com/semiconductor-back-end-term-rdl/

Reference technology guide: Interposers: https://troy-technical.com/semiconductor-back-end-term-interposer/

Reference company guide: TSMC: https://troy-technical.com/semiconductor-back-end-company-tsmc/

Reference company guide: Samsung Electronics: https://troy-technical.com/semiconductor-back-end-company-samsung-electronics/

Source: https://eu.36kr.com/en/p/4042012488962946

#04 ASE and SPIL: AMD Venice PLP Roadmap and Broadcom Joint Venture

Published October 29, 2026 Blocktempo Taiwan

OVERVIEW

ASE has showcased a panel-level packaging (PLP) solution for AMD's Venice server processors, targeting initial production in Q1 2027. Simultaneously, SPIL received approval for a $400 million joint venture with Broadcom in Singapore to produce advanced PLP substrates for CPO applications by 2028.

IN DEPTH

Key Findings

ASE has demonstrated a panel-level packaging (PLP) solution specifically designed for AMD's next-generation Venice server processors. Initial production is targeted for the first quarter of 2027, likely starting at a limited scale at ASE's Kaohsiung facility. In a separate development, Taiwan's Investment Commission approved a $400 million investment by SPIL to establish XCIP TECHNOLOGIES PTE. LTD. in Singapore, a joint venture with Broadcom focused on PLP advanced packaging, assembly, and final testing.

Technical Details

The Venice solution utilizes second-generation Fan-Out Embedded Bridge (FOEB) technology developed through collaboration between ASE, SPIL, and AMD. The technical advantages of transitioning from circular wafers to square panels are as follows:

- **Substrate Dimensions:** ASE uses a 310 x 310 mm square panel.
- **Capacity Increase:** A single panel can accommodate 25 Venice interposers, compared to 22 on a traditional 300 mm circular wafer, representing a 14% increase.
- **Scaling Advantage:** The advantage of square panels increases with interposer size. For an interposer 9.5 times the reticle size, a panel can hold 9 units, whereas a wafer can only hold 4.

Background & Context

Venice is AMD's sixth-generation EPYC processor. While AMD previously announced that Venice has begun production ramp-up using TSMC's 2nm process, the PLP packaging implementation will follow in early 2027. Regarding the Singapore venture, Broadcom is expected to hold a majority stake and lead the facility, while SPIL will handle operations and mass production. This plant focuses on additive fine-line redistribution layer (RDL) technology for PLP substrates, targeting Co-Packaged Optics (CPO) requirements.

Significance & Outlook

The Singapore plant is expected to break ground as early as late 2026, with mass production slated for 2028. The production timelines for ASE and SPIL (2027–2028) align closely with reported plans for TSMC's CoPoS packaging. This shift toward PLP reflects a strategic move to increase AI chip output and reduce costs as interposer sizes grow.

Reference technology guide: Interposers: https://troy-technical.com/semiconductor-back-end-term-interposer/

Reference technology guide: Panel-Level Packaging (PLP): https://troy-technical.com/semiconductor-back-end-term-plp/

Reference technology guide: Fan-Out & Wafer-Level Packaging: https://troy-technical.com/semiconductor-back-end-term-fanout/

Reference company guide: ASE Group: https://troy-technical.com/semiconductor-back-end-company-ase-group/

Reference company guide: AMD: https://troy-technical.com/semiconductor-back-end-company-amd/

Reference company guide: SPIL: https://troy-technical.com/semiconductor-back-end-company-spil/

Source: https://www.blocktempo.com/ase-amd-venice-panel-level-packaging-powertech-broadcom-singapore-plant/

#05 GIST Glass Substrates: Low-Dielectric Material for AI Chips

Published October 25, 2026 Money Today (mt.co.kr) South Korea

OVERVIEW

Researchers at the Gwangju Institute of Science and Technology (GIST) have developed a low-dielectric aluminoborosilicate glass material to replace polymer-based organic substrates in AI semiconductors. This technology addresses heat-induced warping and signal attenuation in high-frequency data transmission.

IN DEPTH

Key Findings

Kim Bok-hyun and a research team at the GIST Advanced Photonics Research Institute have developed a specialized low-dielectric glass material designed specifically for high-performance semiconductor packaging. Unlike repurposed display glass, this material is engineered from the ground up to optimize signal transmission and thermal stability for AI semiconductors.

Technical Details

The team improved the composition of aluminoborosilicate glass—consisting of silicon dioxide, boron oxide, and aluminum oxide—to achieve a balance of physical properties. The primary technical goals were the reduction of the dielectric constant (Dk) and the dielectric loss factor (Df), which is critical as data transmission frequencies reach 10–20 gigahertz (GHz) or higher.

- **Signal Integrity:** Lowering Dk and Df reduces signal attenuation, noise, and heat generation during high-speed data travel over copper wiring.
- **Thermal Management:** The material is engineered to expand and contract at levels comparable to silicon chips, mitigating the risk of warping or cracks at junctions.
- **Processability:** The glass is designed to withstand high-temperature manufacturing processes, including drilling and wiring formation.

Background & Context

Current semiconductor packages primarily rely on polymer-based organic substrates (such as blue or green PCBs). However, as AI semiconductors integrate multiple computing chips and high-bandwidth memory (HBM) into single packages, power consumption and package size increase. This leads to "warpage," where heat causes the organic substrate to bend, and signal attenuation that degrades overall system performance.

Significance & Outlook

By replacing organic substrates with this specialized glass, AI semiconductors can achieve higher power efficiency and improved performance. Beyond electrical improvements, the research team intends to expand this technology into "optical interconnects," utilizing the glass substrate to create internal pathways for light to replace traditional copper wiring to further reduce power consumption.

Reference technology guide: Glass Substrates: https://troy-technical.com/semiconductor-back-end-term-glass-substrate/

Reference technology guide: Interconnects: https://troy-technical.com/semiconductor-back-end-term-interconnect/

Reference technology guide: High Bandwidth Memory (HBM): https://troy-technical.com/semiconductor-back-end-term-hbm/

Source: https://www.mt.co.kr/index.php/en/future/2026/10/25/2026101915054962909

Collected: October 31, 2026 | Automated Research System (AI)

#07 Photosensitive Crystallizable Glass: KICET's TGV Process for Semiconductors

Published October 29, 2026 Financial News (파이낸셜뉴스) South Korea

OVERVIEW

The Korea Institute of Ceramic Technology (KICET) has developed a photosensitive crystallizable glass material to enable the domestic production of next-generation semiconductor substrates. The research team successfully produced 200mm-class glass substrate specimens and demonstrated precise Through Glass Via (TGV) formation on 100mm-class substrates.

IN DEPTH

Key Findings

The Korea Institute of Ceramic Technology (KICET), in collaboration with HAS, Korea Aerospace University, and LX Glass, has developed a photosensitive crystallizable glass material and the associated processing technology required for next-generation semiconductor packaging. The team successfully fabricated large-area glass substrate specimens with a diameter of 200mm and verified the ability to form precise micro-holes (Through Glass Vias, or TGV) on 100mm-class substrates of the same material.

Technical Details

The developed photosensitive crystallizable glass is a specialized material that selectively forms crystals in areas exposed to ultraviolet (UV) light and subsequent heat treatment. The technical process encompasses the entire production chain, including:

- Raw material blending and glass substrate fabrication.
- UV irradiation and thermal treatment to induce selective crystallization.
- Chemical etching to remove the crystallized portions, allowing for the precise creation of multiple micro-holes (TGV).

This method addresses the critical challenge of creating uniform, precise micro-holes in glass, which is traditionally difficult due to the material's fragility and the precision required for vertical interconnects.

Background and Context

Glass substrates serve as the base for mounting and connecting semiconductor chips. Compared to conventional plastic-based substrates, glass offers a smoother surface and lower thermal deformation. These properties are advantageous for creating denser, smaller circuits and reducing electrical signal loss. However, the commercialization of glass substrates has been hindered by the material's susceptibility to impact and the difficulty of achieving precise TGV processing.

Significance and Outlook

By securing the technology to design and manufacture photosensitive crystallizable glass, KICET has established a technical foundation for the localization of semiconductor packaging materials. Dr. Han Yun-su of KICET stated that the team intends to further refine large-area fabrication and micro-processing technologies to facilitate the industrial application and domestic production of next-generation semiconductor packaging materials.

Reference technology guide: Glass Substrates: https://troy-technical.com/semiconductor-back-end-term-glass-substrate/

Reference technology guide: Vias: https://troy-technical.com/semiconductor-back-end-term-via/

Source: https://www.fnnews.com/news/202610291026456501

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#08 Glass Substrate Packaging: 510x515mm Size and Warpage Constraints

Published October 27, 2026　21ic電子網（新浪財経転載）　China

OVERVIEW

Panel-level glass substrates are shifting toward a 510x515mm standard to increase area utilization from 45-65% to over 81% compared to 300mm wafers. However, scaling is limited by a "warpage wall" where warpage displacement increases with the square of the side length ($w \propto L^2$), creating a trade-off between cost efficiency and yield.

IN DEPTH

Key Findings

The industry is converging on the 510x515mm panel size, adopted by TSMC, Innolux, and Vogher, as it allows the reuse of mature G8.5 generation display production lines. While larger panels reduce costs and address capacity gaps—such as the estimated 300,000 to 400,000 unit shortage for CoWoS in 2026—they introduce exponential risks in warpage and yield. Consequently, AI chips with tight RDL requirements (1-10μm) remain on more conservative sizes, while PMIC and RF chips (10-20μm) are targeted for larger panels exceeding 600mm.

Technical Details: The Warpage Wall

Warpage is driven by the difference in coefficients of thermal expansion (CTE) between materials: silicon (~2.6 ppm/°C), copper (16-17 ppm/°C), and organic dielectric layers (30-60 ppm/°C). According to thin-plate mechanics, warpage displacement (w) is proportional to the square of the characteristic length (L^2). Increasing a panel from 300mm to 600mm quadruples the warpage driving force, which can lead to focus errors in stepper exposure machines and mechanical handling failures.

To mitigate this, the industry employs three strategies:

- **Material:** Using low-CTE glass (3.2 to 7.2 ppm/°C) to match silicon, though this increases brittleness and costs by 30-50%.
- **Structure:** Implementing symmetrical routing (e.g., TSMC's CoPoS) to cancel out local stress.
- **Process:** Utilizing air gaps, stress buffer layers, or "chip-after" RDL sequences to reduce thermal stress.

Industry Roadmap and Adopters

TSMC's CoPoS roadmap targets mass production between 2028 and 2029, with 510mm as a mid-term goal. Intel is pursuing a more aggressive 510x515mm route with 24-layer glass cores. In China, BOE has invested 993 million yuan in a test line with a monthly capacity of 1,000 pieces, while Vogher reports a TGV monthly capacity of 10,000 pieces based on the 510x515mm size. Other players include Samsung Electro-Mechanics (415x510mm) and Rapidus (600x600mm).

Significance and Outlook

The transition from circular wafers to square panels is a strategic move to solve capacity shortages for AI GPUs, such as the Nvidia Rubin generation. However, because total panel yield is the product of individual hole yields, increasing the area exponentially increases the risk of failure. The upper limit of panel size is effectively defined by the limit of warpage control.

Reference technology guide: Coefficient of Thermal Expansion (CTE): https://troy-technical.com/semiconductor-back-end-term-cte/

Reference technology guide: CoWoS: https://troy-technical.com/semiconductor-back-end-term-cowos/

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Reference company guide: Intel: https://troy-technical.com/semiconductor-back-end-company-intel/

Source: https://finance.sina.com.cn/wm/2026-10-27/doc-iniwrzht4588328.shtml

Collected: October 31, 2026 | Automated Research System (AI)

#09 Hunan Titan Future: China's First 12-Inch Polycrystalline SiC Substrate

Published October 29, 2026 TrendForce News China

OVERVIEW

Hunan Titan Future Technology has developed China's first 12-inch polycrystalline silicon carbide (SiC) substrate featuring thermal conductivity exceeding 280 W/(m·K). Designed for AI computing chips and advanced packaging, the substrate addresses heat dissipation challenges in high-power semiconductor operations.

IN DEPTH

Key Findings

Hunan Titan Future Technology has developed the first 12-inch polycrystalline silicon carbide (SiC) substrate in China. The product is currently in the stage of sample validation and small-batch trial production, having already completed validation by leading companies.

Technical Details

The substrate is engineered specifically for thermal management rather than epitaxial growth for power devices. Key technical specifications and applications include:

- **Thermal Performance:** Thermal conductivity exceeds 280 W/(m·K).
- **Primary Function:** Acts as a heat-conducting base within semiconductor packaging structures to alleviate heat buildup during high-power chip operation.
- **Target Applications:** AI computing chips and advanced packaging.
- **Alternative Uses:** The substrate can serve as a carrier for crystal growth and a base for high-temperature semiconductor processing.

Background and Context

The technology is based on research from the Powder Metallurgy Research Institute at Central South University, with a core team comprising several doctoral graduates from the institution. Titan Future previously developed domestic 6-inch and 8-inch polycrystalline SiC substrates.

The company is expanding its manufacturing footprint across three locations:

- **Changsha:** Serves as the technology development and application incubation center.
- **Xiamen:** Planned annual capacity of 500,000 composite SiC substrates.
- **Jinhu, Jiangsu:** A new integrated manufacturing base for high-purity, high-density SiC components and polycrystalline substrates broke ground on September 28.

Significance and Outlook

The Jinhu facility will produce high-performance SiC components and tantalum carbide (TaC)-coated products. Once fully operational, this site is expected to reach an annual production capacity of 200,000 units, generating CNY 600 million in annual sales and contributing CNY 30 million in tax revenue.

Source: https://www.trendforce.com/news/2026/10/29/news-chinas-first-12-inch-polycrystalline-silicon-carbide-substrate-unveiled/

#10 Lam and imec: 3D Integration and High-NA EUV Roadmap for AI

Published October 28, 2026 Electronics Weekly UK

OVERVIEW

Lam Research and imec are collaborating to accelerate the transition of 3D integration and advanced patterning technologies from the lab to high-volume manufacturing. The partnership focuses on solving process challenges for advanced packaging, next-generation memory, and angstrom-era logic devices to meet AI-driven demands for bandwidth and density.

IN DEPTH

Key Findings

Lam and imec have entered a collaboration to accelerate manufacturing readiness for 3D integration technologies. By combining Lam's deposition and etch capabilities with imec's integration infrastructure, the partnership aims to scale heterogeneous integration and advanced packaging across the industry. Additionally, the two organizations are collaborating on the application of Lam's Aether dry resist platform to address the requirements of high-NA EUV lithography.

Technical Details

Joint research in 3D integration covers several critical process areas:

- Thick dielectric deposition, asymmetric stress compensation, bevel deposition, and plasma dicing.
- Process validation for advanced packaging and future memory architectures.
- Future 3D memory technologies, including new charge-trap materials, precision multilayer deposition, high-aspect-ratio channel etch, deep memory contacts, and low-resistivity interconnects.

Regarding logic devices, the collaboration focuses on enhancing the resolution, sensitivity, depth of focus, and stochastic defectivity of the Aether dry resist platform using imec's high-NA EUV environment. This includes exploring ruthenium direct metal etch for advanced interconnects at aggressive pitches. Joint research has already demonstrated single-exposure high-NA EUV patterning for sub-20 nm ruthenium direct metal etch interconnects, achieving 100% electrical yield for fork structures and over 90% for meander structures at a 20nm pitch.

Background & Context

The push toward 3D integration and high-NA EUV is driven by AI workloads that require increased memory density and bandwidth. As the industry moves toward angstrom-era nodes, high-NA EUV is necessary for smaller features and higher transistor density, though it requires simultaneous innovations in resists, mask design, patterning, and materials.

Significance & Outlook

The Aether platform, alongside Lam's Akara etch systems and Striker ALD portfolio, provides a path toward reducing multi-patterning complexity and improving manufacturability. These innovations are intended to enable the gate-all-around (GAA) and complementary FET (CFET) architectures expected to power future generations of AI computing.

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Reference technology guide: Bridges & EMIB: https://troy-technical.com/semiconductor-back-end-term-bridge/

Reference company guide: Lam Research: https://troy-technical.com/semiconductor-back-end-company-lam-research/

Source: https://www.electronicsweekly.com/news/business/lam-and-imec-pursue-3-d-integration-2026-10/

Collected: October 31, 2026 | Automated Research System (AI)