TROY TECHNICAL

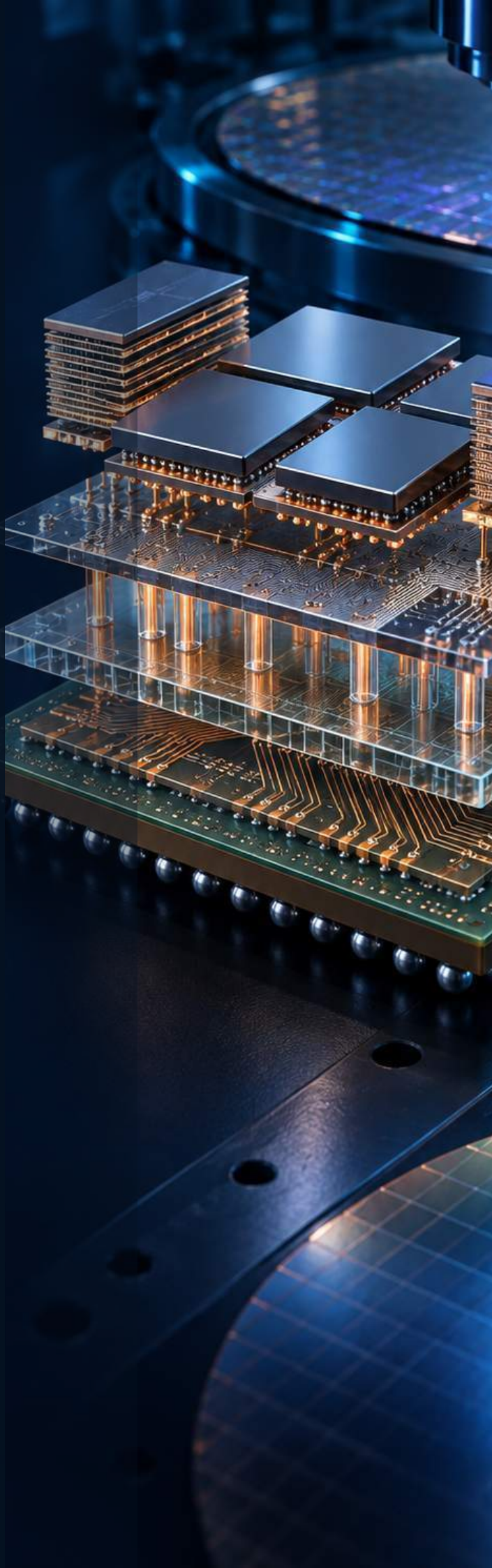
SEMICONDUCTOR BACK-END WEEKLY REPORT

October 31 - November 6, 2026 | Issue 2026-W44

Package performance, process yield, test coverage and qualified capacity

10	10
ANALYZED ARTICLES	PRIORITY THEMES

Issued 2026-11-06 | English edition | fixed approved cover artwork



Semiconductor Back-End: the boundary moved from isolated claims to qualification evidence

10 English articles were reviewed independently from the Japanese edition. Ten themes are retained for management decisions.

SIGNAL 01 | MATERIALS

ACM Research: Ultra ECP ap-p 310 x 310 mm Tool Specs and Shipment

ACM Research has shipped its first 310 × 310 mm Ultra ECP ap-p panel-level horizontal electroplating production tool to a customer in Asia outside mainland China.

SIGNAL 02 | BONDING & ASSEMBLY

SK Hynix HBM4: Yield rates and DRAM supply expansion

SK Hynix has achieved an industry-leading yield rate in the mid-60% range for its sixth-generation high-bandwidth memory (HBM4). This development coincides with the company's efforts to expand its DRAM supply to meet AI-driven demand.

SIGNAL 03 | ADVANCED PACKAGE

NVIDIA Rubin GPU: Revised HBM4 and NVLink Shipping Specs 2026

NVIDIA has revised the final shipping specifications for its Rubin GPU, reducing HBM4 memory bandwidth by 11% and NVLink bandwidth by 17% while increasing scale-out networking bandwidth.

SIGNAL 04 | TEST & INSPECTION

Intel EMIB Packaging: Wafer Utilization and AI Chip Roadmap

Intel is positioning its interposer-free EMIB and EMIB-T packaging as high-efficiency alternatives to TSMC's CoWoS, claiming over 90% wafer utilization. Major U.S.

DECISION

Focus this week's management attention on package performance, process yield, test coverage and qualified capacity. Move only when the linked evidence can be reproduced under your own operating conditions.

THREE MANAGEMENT MOVES

1. Buyers: compare architectures using thermal, electrical, yield, repair and supply evidence.
2. Suppliers: co-develop materials, bonding, inspection and reliability windows with customers.
3. Executives: track yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EVIDENCE DISCIPLINE

FACT states what the collected English source reports. BUSINESS READ and ACTION are editorial interpretations. UNKNOWN lists information that the source file does not establish. A linked article is not treated as independent confirmation of every claim.

Five numbers or evidence anchors that require conditions

310 mm
A07

SOURCE-BOUND CONDITION
ACM Research has shipped its first 310 × 310 mm Ultra ECP ap-p panel-level horizontal electroplating production tool to a customer in Asia outside mainland China.

60%
A03

SOURCE-BOUND CONDITION
SK Hynix has achieved an industry-leading yield rate in the mid-60% range for its sixth-generation high-bandwidth memory (HBM4).

11%
A06

SOURCE-BOUND CONDITION
NVIDIA has revised the final shipping specifications for its Rubin GPU, reducing HBM4 memory bandwidth by 11% and NVLink bandwidth by 17% while increasing scale-out networking bandwidth.

90%
A01

SOURCE-BOUND CONDITION
Intel is positioning its interposer-free EMIB and EMIB-T packaging as high-efficiency alternatives to TSMC's CoWoS, claiming over 90% wafer utilization.

P05
A05

SOURCE-BOUND CONDITION
Qualcomm has validated its High Bandwidth Compute (HBC) stacked memory architecture, demonstrating over five times the energy efficiency (bandwidth-per-watt) of HBM4 in initial tests.

HOW TO USE THESE NUMBERS
Each value is shown with the condition stated in the collected English article. Do not compare values across different test methods, device sizes, operating temperatures or commercial stages without normalizing those conditions.

Where the value chain moved

Each stage combines one leading theme and one supporting theme. The report treats handoffs as evidence transfers, not decorative arrows.

1

Materials

P01/P06

ACM Research has shipped its first 310 × 310 mm Ultra ECP ap-p panel-level horizontal electroplating production tool to a.

2

Bonding & assembly

P02/P07

SK Hynix has achieved an industry-leading yield rate in the mid-60% range for its sixth-generation high-bandwidth memory.

3

Advanced package

P03/P08

NVIDIA has revised the final shipping specifications for its Rubin GPU, reducing HBM4 memory bandwidth by 11% and NVLink.

4

Test & inspection

P04/P09

Intel is positioning its interposer-free EMIB and EMIB-T packaging as high-efficiency alternatives to TSMC's CoWoS, claiming.

5

Volume supply

P05/P10

Qualcomm has validated its High Bandwidth Compute (HBC) stacked memory architecture, demonstrating over five times the energy.

EVIDENCE REQUIRED AT EACH HANDOFF

Materials to Bonding & assembly	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Bonding & assembly to Advanced package	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Advanced package to Test & inspection	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Test & inspection to Volume supply	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.

COMMON CONTROL POINT

No theme moves to a commercial commitment until a named owner has reproduced the relevant evidence and documented yield, warpage, thermal cycling, test time, capacity, cost and qualification.

Priority map: maturity and next decision locus



P01	ACM Research: Ultra ECP ap-p 310 x 310 mm Tool Specs and Shipment System / adoption | cue: Shipment
P02	SK Hynix HBM4: Yield rates and DRAM supply expansion Tech / process | cue: no system/business cue
P03	NVIDIA Rubin GPU: Revised HBM4 and NVLink Shipping Specs 2026 System / adoption | cue: system
P04	Intel EMIB Packaging: Wafer Utilization and AI Chip Roadmap System / adoption | cue: adopting
P05	Qualcomm HBC Memory: Architecture and Dragonfly AI250 Timeline System / adoption | cue: integrated
P06	Silicon Bridge: NNFC's First Public Nanofab Process for AI Chips Business / rules | cue: infrastructure
P07	Intel EMIB-T vs TSMC CoWoS: AI Packaging Roadmaps to 2029 Business / rules | cue: supply chain
P08	Fraunhofer IPMS: Chiplet Integration and Memory Tech for 2026 System / adoption | cue: Integration
P09	Nippon Sheet Glass TGV: Specs and Advantages for 5G/6G Substrates Tech / process | cue: no system/business cue
P10	Eco-Optical: TGV Glass Substrate Inspection and Sensing Specs System / adoption | cue: system

REPRODUCIBLE POSITIONING RULE

Horizontal position uses five discrete stages: Research, Prototype, Joint evaluation, Product adoption and Scale. The vertical bands classify the next decision locus: Tech / process, System / adoption, or Business / rules (including supply systems). Article-title cues take precedence; the overview is used only when the title is silent. These are categories, not impact ranks. Bubble diameter reflects the editorial score.

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P01 ACM Research: Ultra ECP ap-p 310 x 310 mm Tool Specs and Shipment

A07 | Materials | Pilot

2026-11-03

FACT

ACM Research has shipped its first 310 × 310 mm Ultra ECP ap-p panel-level horizontal electroplating production tool to a customer in Asia outside mainland China. The system supports multiple plating materials and is designed to meet the complex packaging requirements driven by AI. This shipment marks the transition of ACM's panel-level technology from R&D to scale production.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P01.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 21/25 | MATURITY 2/5 | DECISION LOCUS: SYSTEM / ADOPTION

P02 SK Hynix HBM4: Yield rates and DRAM supply expansion

A03 | Bonding & assembly | Research

2026-11-05

FACT

SK Hynix has achieved an industry-leading yield rate in the mid-60% range for its sixth-generation high-bandwidth memory (HBM4). This development coincides with the company's efforts to expand its DRAM supply to meet AI-driven demand.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P02.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | DECISION LOCUS: TECH / PROCESS

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P03 NVIDIA Rubin GPU: Revised HBM4 and NVLink Shipping Specs 2026

A06 | Advanced package | Research

2026-10-31

FACT

NVIDIA has revised the final shipping specifications for its Rubin GPU, reducing HBM4 memory bandwidth by 11% and NVLink bandwidth by 17% while increasing scale-out networking bandwidth. These changes directly impact the Vera Rubin NVL72 rack-scale system, shifting the performance balance toward larger scale-out deployments.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P03.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

P04 Intel EMIB Packaging: Wafer Utilization and AI Chip Roadmap

A01 | Test & inspection | Research

2026-11-05

FACT

Intel is positioning its interposer-free EMIB and EMIB-T packaging as high-efficiency alternatives to TSMC's CoWoS, claiming over 90% wafer utilization. Major U.S. tech firms including Google and Amazon are reportedly adopting the technology for custom AI chips as package sizes and HBM counts scale.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P04.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P05 Qualcomm HBC Memory: Architecture and Dragonfly AI250 Timeline

A05 | Volume supply | Research

2026-11-02

FACT

Qualcomm has validated its High Bandwidth Compute (HBC) stacked memory architecture, demonstrating over five times the energy efficiency (bandwidth-per-watt) of HBM4 in initial tests. This technology will be integrated into the Dragonfly AI250 data center AI accelerators, with sampling scheduled to begin in 2027.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P05.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

P06 Silicon Bridge: NNFC's First Public Nanofab Process for AI Chips

A02 | Materials | Research

2026-11-04

FACT

The National NanoFab Center (NNFC) has implemented a test fabrication process for silicon bridges, a critical technology for AI semiconductor chiplet connectivity. The process integrates 1µm fine wiring and Through-Silicon Vias (TSV) on 8-inch wafers, providing a public infrastructure for domestic industry and academia to verify advanced packaging.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P06.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 1/5 | DECISION LOCUS: BUSINESS / RULES

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P07 Intel EMIB-T vs TSMC CoWoS: AI Packaging Roadmaps to 2029

A09 | Bonding & assembly | Research

2026-11-02

FACT

Intel's EMIB-T is emerging as a viable alternative to TSMC's CoWoS as supply bottlenecks for AI chip packaging increase. While CoWoS remains the choice for high-bandwidth requirements, EMIB-T offers a scalable silicon bridge architecture that could diversify the supply chain for logic chips and custom ASICs.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P07.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 1/5 | DECISION LOCUS: BUSINESS / RULES

P08 Fraunhofer IPMS: Chiplet Integration and Memory Tech for 2026

A04 | Advanced package | Research

2026-11-03

FACT

Fraunhofer IPMS is advancing 2.5D and Quasi-Monolithic Integration (QMI) for chiplets alongside low-power ferroelectric memory. These developments, to be showcased at SEMICON Europa 2026, aim to reduce power consumption and increase manufacturing flexibility for European semiconductor firms.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P08.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P09 Nippon Sheet Glass TGV: Specs and Advantages for 5G/6G Substrates

A08 | Test & inspection | Research

2026-11-04

FACT

Nippon Sheet Glass showcased a Through Glass Via (TGV) substrate at CEATEC 2026 featuring a custom alkali-free low-dielectric glass composition. The technology reduces energy loss and improves mechanical durability, positioning it as a potential alternative to silicon substrates for high-frequency circuits.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P09.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 1/5 | DECISION LOCUS: TECH / PROCESS

P10 Eco-Optical: TGV Glass Substrate Inspection and Sensing Specs

A10 | Volume supply | Research

2026-11-02

FACT

Eco-Optical received the "2026 Annual Glass Substrate TGV Excellent Enterprise Award" for its technical contributions to Through Glass Via (TGV) process inspection. The company's intelligent autofocus system enables sub-micron tracking precision to resolve imaging challenges in advanced glass substrate packaging.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P10.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 18/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

Playbook and 0-5 year roadmap

STAKEHOLDER	NOW | 0-30 DAYS	NEXT | 1-12 MONTHS	LATER | 1-5 YEARS
Operating companies	compare architectures using thermal, electrical, yield, repair and supply evidence	Run production-like qualification with explicit acceptance and stop criteria.	Build a portfolio and architecture that can absorb technology and supplier changes.
Materials, equipment and technology suppliers	co-develop materials, bonding, inspection and reliability windows with customers	Create shared reliability, process-window and failure-analysis data with customers.	Standardize interfaces, traceability, lifecycle support and recovery services.
Trading, investment and legal teams	Map yield, warpage, thermal cycling, test time, capacity, cost and qualification.	Contract for capacity, quality, change notice, liability, alternatives and exit.	Diversify regional, technical and customer concentration risk.

ROADMAP

NOW | 0-30 DAYS
Evidence ledger
Owner: Strategy + quality
Deliverable: claim, source, condition, owner

NOW | 0-30 DAYS
Risk screen
Owner: Procurement + legal
Deliverable: unknowns, alternatives, stop

NEXT | 1-12 MONTHS
Joint qualification
Owner: R&D + supplier
Deliverable: process window and failure data

NEXT | 1-12 MONTHS
Commercial gate
Owner: Business + finance
Deliverable: unit economics and capacity

LATER | 1-5 YEARS
Platform strategy
Owner: Executive team
Deliverable: portfolio and interface roadmap

LATER | 1-5 YEARS
Service layer
Owner: Operations + channel
Deliverable: monitoring, maintenance and recovery

GO / NO-GO GATES

GATE	OWNER	REQUIRED EVIDENCE	NO-GO CONDITION
G1 Evidence	**Quality**	Source, test conditions and reproducibility	No traceable evidence
G2 Integration	**R&D**	Interface, process window and failure analysis	Cannot meet system conditions
G3 Commercial	**Business**	Capacity, total cost, contract and alternatives	Economics or supply cannot be supported
G4 Lifecycle	**Operations**	Monitoring, maintenance, change notice and exit	No accountable operating plan

ANALYZED ARTICLES | ITEMS 01-10

Every title and URL is displayed in full. URLs wrap without shortening and remain clickable. A verified-reference label means the translated HTML did not retain its original source URL.

ID	FULL ARTICLE TITLE	FULL SOURCE / VERIFIED REFERENCE URL - CLICKABLE
A01	Intel EMIB Packaging: Wafer Utilization and AI Chip Roadmap	https://www.trendforce.com/news/2026/11/05/news-intel-reportedly-touts-90-wafer-utilization-with-interposer-free-emib-eyes-70-bridges-per-future-ai-chip/
A02	Silicon Bridge: NNFC's First Public Nanofab Process for AI Chips	https://www.joongangenews.com/news/articleView.html?idxno=561178
A03	SK Hynix HBM4: Yield rates and DRAM supply expansion	https://www.digitimes.com/news/a20261105PD211/sk-hynix-hbm4-dram-hbm-capacity.html
A04	Fraunhofer IPMS: Chiplet Integration and Memory Tech for 2026	https://www.eenewseurope.com/en/fraunhofer-ipms-advances-chiplet-integration-and-low-power-memory/
A05	Qualcomm HBC Memory: Architecture and Dragonfly AI250 Timeline	https://www.servethehome.com/qualcomm-validates-hbc-stacked-memory-ahead-of-2027-dragonfly-ai250-sampling/
A06	NVIDIA Rubin GPU: Revised HBM4 and NVLink Shipping Specs 2026	https://www.servethehome.com/nvidia-updates-rubin-gpu-specs-as-first-production-hardware-arrives/
A07	ACM Research: Ultra ECP ap-p 310 x 310 mm Tool Specs and Shipment	https://www.semiconductor-digest.com/acm-research-announces-shipment-of-its-first-310-x-310-mm-ultra-ecp-ap-p-panel-level-horizontal-electroplating-production-tool/
A08	Nippon Sheet Glass TGV: Specs and Advantages for 5G/6G Substrates	https://monoist.itmedia.co.jp/mn/articles/2611/04/news015.html
A09	Intel EMIB-T vs TSMC CoWoS: AI Packaging Roadmaps to 2029	https://technews.tw/2026/11/02/cowos-supply-bottlenecks-intel-emib-t-alternative-packaging/
A10	Eco-Optical: TGV Glass Substrate Inspection and Sensing Specs	https://www.gongkong.com/news/202611/454355.html

Semiconductor_BackEnd — Selected Articles

Date: 2026-11-08

Articles: 10

Table of Contents

#01 Intel EMIB Packaging: Wafer Utilization and AI Chip Roadmap

#02 Silicon Bridge: NNFC's First Public Nanofab Process for AI Chips

#03 SK Hynix HBM4: Yield rates and DRAM supply expansion

#04 Fraunhofer IPMS: Chiplet Integration and Memory Tech for 2026

#05 Qualcomm HBC Memory: Architecture and Dragonfly AI250 Timeline

#06 NVIDIA Rubin GPU: Revised HBM4 and NVLink Shipping Specs 2026

#07 ACM Research: Ultra ECP ap-p 310 x 310 mm Tool Specs and Shipment

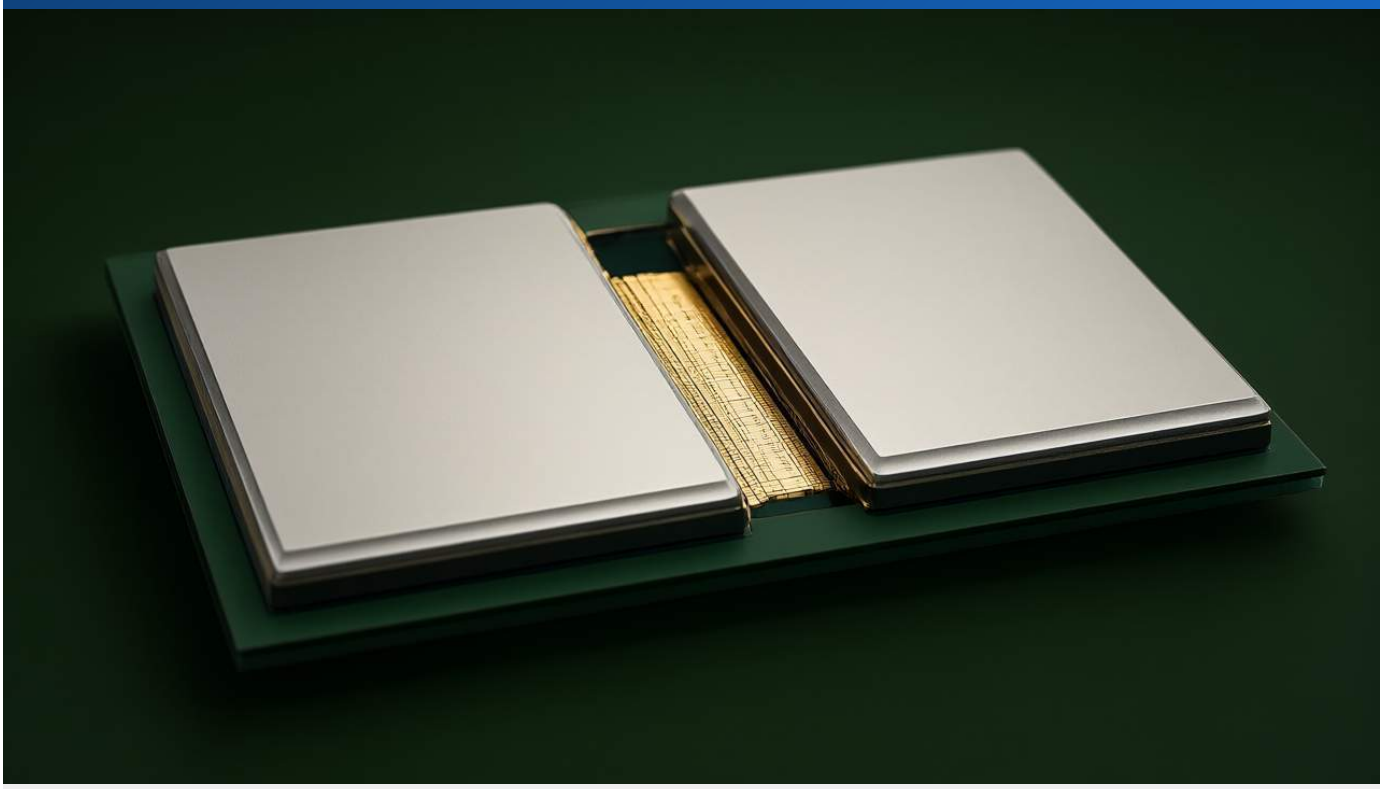
#08 Nippon Sheet Glass TGV: Specs and Advantages for 5G/6G Substrates

#09 Intel EMIB-T vs TSMC CoWoS: AI Packaging Roadmaps to 2029

#10 Eco-Optical: TGV Glass Substrate Inspection and Sensing Specs

#01 Intel EMIB Packaging: Wafer Utilization and AI Chip Roadmap

Published November 05, 2026 TrendForce Taiwan



OVERVIEW

Intel is positioning its interposer-free EMIB and EMIB-T packaging as high-efficiency alternatives to TSMC's CoWoS, claiming over 90% wafer utilization. Major U.S. tech firms including Google and Amazon are reportedly adopting the technology for custom AI chips as package sizes and HBM counts scale.

IN DEPTH

Key Findings

Intel reports that its Embedded Multi-die Interconnect Bridge (EMIB) technology achieves silicon wafer utilization of over 90%, significantly higher than the roughly 60% utilization seen in interposer-based designs. This efficiency is driven by the use of small, localized silicon bridges rather than a full-size interposer. Additionally, EMIB-T, which integrates through-silicon vias (TSVs) for power delivery, is gaining traction among major U.S. technology companies.

Technical Details and Roadmap

Intel's roadmap for AI chip packages shows a trajectory of increasing size and complexity:

- **2026 Commercialization:** Packages up to 120 × 120 mm, integrating 12 HBM stacks and more than 20 EMIB bridges.
- **Current Development:** Targets of at least 120 × 180 mm, featuring 16 or more HBM stacks and at least 38 bridges.
- **Future Vision:** Packages reaching 240 × 240 mm, integrating over 32 HBM stacks and more than 70 EMIB bridges.

Adoption and Supply Chain

Industry sources indicate that Google’s TPU v9 lineup may adopt EMIB-T for the HumuFish and TriggerFish models, while the WhaleFish model is expected to use TSMC’s CoWoS-L. Amazon is also reportedly planning to use EMIB-T for its custom AI chips. To support this ecosystem, Taiwanese foundry UMC manufactures EMIB silicon bridges using mature 12-inch wafer processes at its facilities in Taiwan and Singapore.

Competitive Landscape

TSMC is pursuing similar scaling via CoWoS technology. In 2026, CoWoS-L is expected to support a 5.5X reticle-size package with four chiplets and 12 HBM stacks. By 2028, this is projected to scale to 14X, accommodating 20 chiplets and 20 HBM stacks. Meanwhile, reports indicate Intel's EMIB substrate yields have hit 45%, with suppliers targeting 60% by 1Q27.

Reference technology guide: Bridges & EMIB: https://troy-technical.com/semiconductor-back-end-term-bridge/

Reference technology guide: High Bandwidth Memory (HBM): https://troy-technical.com/semiconductor-back-end-term-hbm/

Reference technology guide: CoWoS: https://troy-technical.com/semiconductor-back-end-term-cowos/

Reference company guide: TSMC: https://troy-technical.com/semiconductor-back-end-company-tsmc/

Reference company guide: Intel: https://troy-technical.com/semiconductor-back-end-company-intel/

Source: https://www.trendforce.com/news/2026/11/05/news-intel-reportedly-touts-90-wafer-utilization-with-interposer-free-emib-eyes-70-bridges-per-future-ai-chip/

Collected: November 07, 2026 | Automated Research System (AI)

#02 Silicon Bridge: NNFC's First Public Nanofab Process for AI Chips

Published November 04, 2026 중앙이코노미뉴스 South Korea



OVERVIEW

The National NanoFab Center (NNFC) has implemented a test fabrication process for silicon bridges, a critical technology for AI semiconductor chiplet connectivity. The process integrates 1㎛ fine wiring and Through-Silicon Vias (TSV) on 8-inch wafers, providing a public infrastructure for domestic industry and academia to verify advanced packaging.

IN DEPTH

Key Findings

The National NanoFab Center (NNFC) has successfully implemented a test fabrication process for "silicon bridges," marking the first time this capability has been available in a South Korean public nanofab. This infrastructure allows for the high-speed connection of multiple semiconductor chips, enabling domestic companies, universities, and research institutes to develop and verify advanced packaging technologies locally.

Technical Details

The NNFC Advanced Packaging Development Center research team developed the process based on 8-inch wafers. The technical specifications include:

- **Fine Wiring:** Copper wiring with a line width and spacing of approximately 1 micrometer (㎛), stacked in multiple layers to enable high-density electrical connections between chiplets.
- **Vertical Connectivity:** Integration of Through-Silicon Via (TSV) technology, which creates vertical conductive paths through the silicon to connect the top and bottom layers.
- **Integrated Structure:** The silicon bridge combines horizontal connectivity via fine wiring and vertical connectivity via TSV within a single structure.
- **Additional Components:** The process includes the fabrication of copper bumps for electrical contact and capacitors to stabilize power supply and reduce voltage fluctuations during high-speed operations.
- **Standardization:** The design incorporates concepts from the Universal Chiplet Interconnect Express (UCIe) international standard to ensure technical compatibility between chiplets from different manufacturers.

Background & Context

Silicon bridges act as data conduits between chiplets in a modular architecture. Rather than manufacturing a single large chip, the chiplet approach combines smaller, specialized chips (such as logic and memory) into one package. This increases design flexibility and is essential for AI semiconductors that require the rapid transfer of massive amounts of data.

Significance & Outlook

Previously, research into advanced packaging required significant costs to secure the necessary production equipment and process technology. By providing this public infrastructure, NNFC aims to support the entire lifecycle from initial R&D to prototype production and performance verification. This is expected to strengthen the competitiveness of the domestic semiconductor ecosystem, specifically for AI semiconductors and high-performance computing.

Reference technology guide: Chiplets: https://troy-technical.com/semiconductor-back-end-term-chiplet/

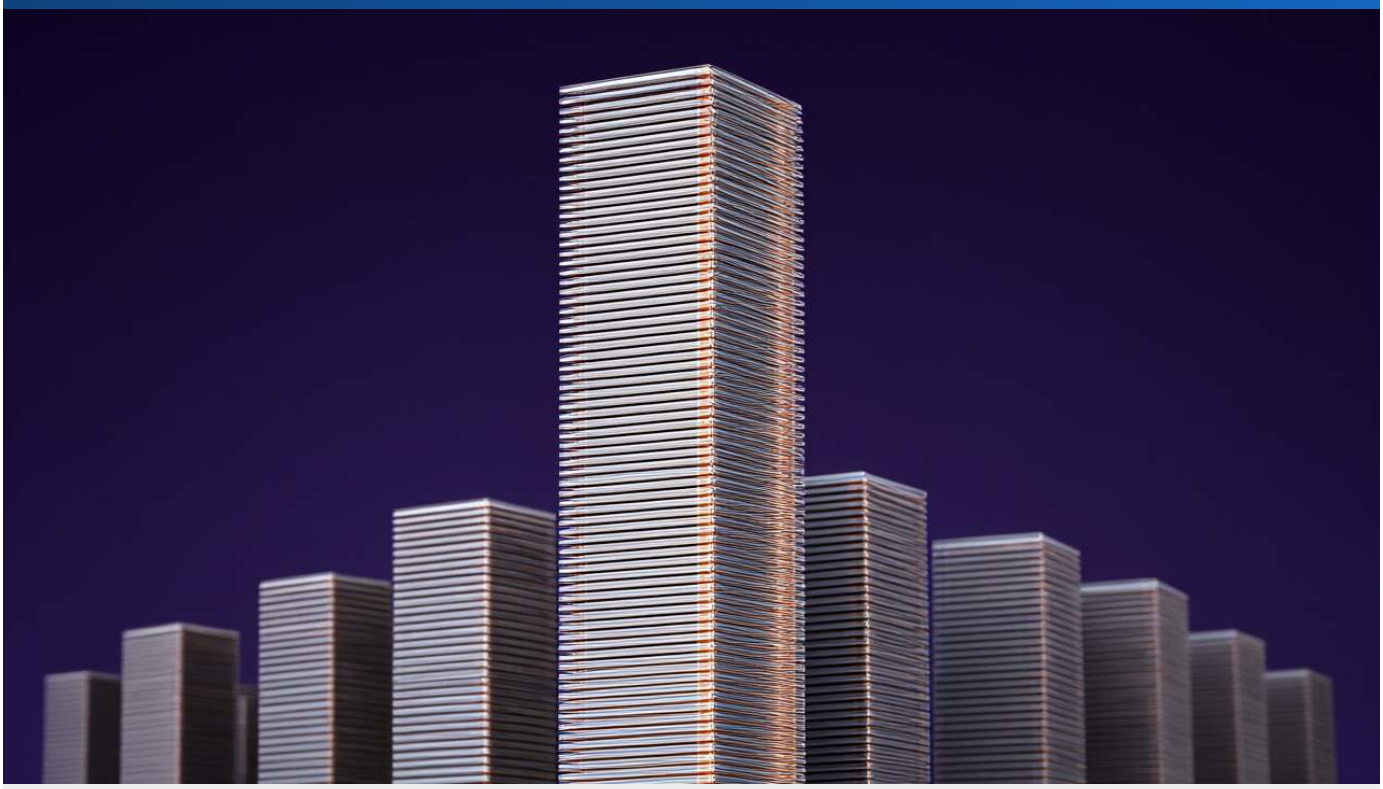
Reference technology guide: Bridges & EMIB: https://troy-technical.com/semiconductor-back-end-term-bridge/

Reference technology guide: Through-Silicon Via (TSV): https://troy-technical.com/semiconductor-back-end-term-tsv/

Source: https://www.joongangenews.com/news/articleView.html?idxno=561178

#03 SK Hynix HBM4: Yield rates and DRAM supply expansion

Published November 05, 2026 DIGITIMES Taiwan



OVERVIEW

SK Hynix has achieved an industry-leading yield rate in the mid-60% range for its sixth-generation high-bandwidth memory (HBM4). This development coincides with the company's efforts to expand its DRAM supply to meet AI-driven demand.

IN DEPTH

Key Findings

SK Hynix has reportedly reached a yield rate in the mid-60% range for its sixth-generation high-bandwidth memory (HBM4), marking the highest yield currently seen in the industry. Alongside these yield improvements, the company is expanding its DRAM supply.

Technical Details

The report focuses on the production efficiency of HBM4, noting that the mid-60% yield represents a significant lead over other industry participants. While specific architectural changes are not detailed in the provided text, the yield rate serves as a primary indicator of the company's manufacturing maturity for this generation of memory.

Background & Context

The memory market is currently influenced by several geopolitical and industrial shifts. South Korea's SSD exports have surged by 584%, signaling a boom in AI inference. However, the landscape remains volatile due to the US midterm elections, which present both risks to AI data centers and potential opportunities via the CHIPS Act. Additionally, Beijing has limited imports of Nvidia H200 chips to accelerate its own domestic silicon push.

Significance & Outlook

SK Hynix's lead in HBM4 yield positions the company strongly within the AI hardware ecosystem. This is further supported by strategic investments, such as the SK Hynix AI arm purchasing a US$377 million stake in Penguin Solutions from SK Telecom. As the industry moves toward post-2028 AI needs—highlighted by Nvidia's OOI CPO prototype—the ability to maintain high yields on next-generation memory will be critical for scaling AI accelerators and data center infrastructure.

Reference technology guide: High Bandwidth Memory (HBM): https://troy-technical.com/semiconductor-back-end-term-hbm/

Reference company guide: SK hynix: https://troy-technical.com/semiconductor-back-end-company-sk-hynix/

Reference company guide: Samsung Electronics: https://troy-technical.com/semiconductor-back-end-company-samsung-electronics/

Reference company guide: NVIDIA: https://troy-technical.com/semiconductor-back-end-company-nvidia/

Source: https://www.digitimes.com/news/a20261105PD211/sk-hynix-hbm4-dram-hbm-capacity.html

Collected: November 07, 2026 | Automated Research System (AI)

#04 Fraunhofer IPMS: Chiplet Integration and Memory Tech for 2026

Published November 03, 2026 eeNews Europe Germany



OVERVIEW

Fraunhofer IPMS is advancing 2.5D and Quasi-Monolithic Integration (QMI) for chiplets alongside low-power ferroelectric memory. These developments, to be showcased at SEMICON Europa 2026, aim to reduce power consumption and increase manufacturing flexibility for European semiconductor firms.

IN DEPTH

Key Findings

Fraunhofer IPMS is introducing advancements in chiplet integration, silicon nitride (SiN) photonics, and hafnium oxide-based ferroelectric memory. These technologies focus on improving system performance and reducing power consumption through heterogeneous integration and energy-efficient data storage.

Technical Details

The institute's integration research focuses on two primary methods:

- **2.5D Integration:** Utilizing high-density interposers to connect separate logic, memory, and sensor chiplets into compact systems.
- **Quasi-Monolithic Integration (QMI):** Embedding chiplets into specially structured pockets within silicon wafers to enable wafer-level interconnections while maintaining modular flexibility.

In photonics, Fraunhofer IPMS has developed a silicon nitride (SiN) platform compatible with 200 mm and 300 mm wafers. This platform exhibits extremely low optical losses across wavelengths from visible light to mid-infrared, targeting applications in optical computing, quantum technologies, and photonic biosensors.

Regarding memory, the institute is developing hafnium oxide-based ferroelectric memory, including FeFET and non-volatile FRAM devices. These components operate at voltages below 1 V with nanosecond switching times, designed for edge AI, intelligent sensors, and embedded systems.

Background & Context

These developments are tied to the European APECS pilot line, a component of the EU Chips Act's Chips for Europe Initiative. Led by Research Fab Microelectronics Germany (FMD) and European partners, APECS provides industry access to advanced packaging and heterogeneous integration. Additionally, the institute utilizes the FAMES European pilot line to facilitate the transfer of these technologies into industrial applications.

Significance & Outlook

By integrating back-end process technologies into front-end fabrication, Fraunhofer IPMS aims to bridge the gap between laboratory research and commercial manufacturing. The availability of design kits, fabrication services, and technology platforms allows external partners to implement these CMOS-compatible processes into high-volume semiconductor production, enabling the creation of more powerful and energy-efficient systems.

Reference technology guide: Chiplets: https://troy-technical.com/semiconductor-back-end-term-chiplet/

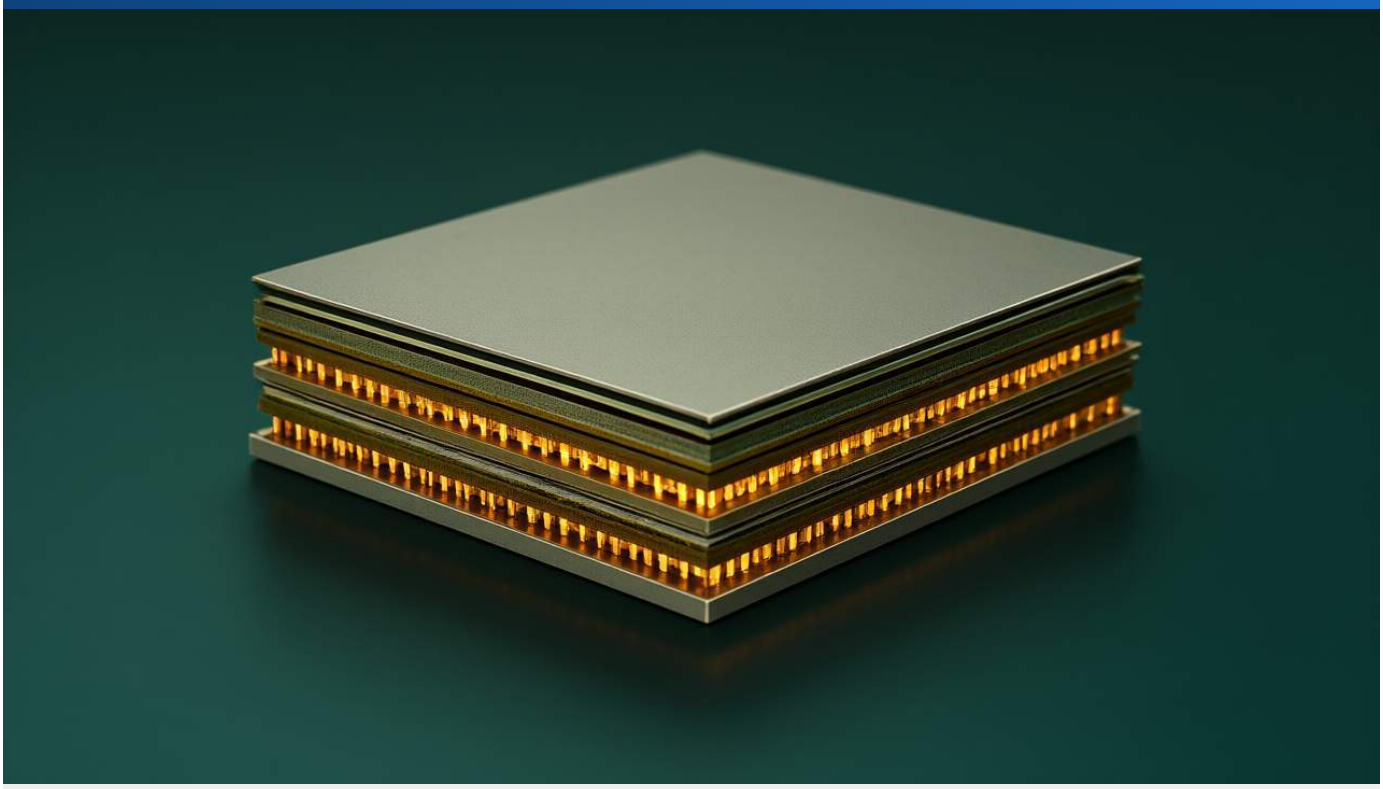
Reference technology guide: Interposers: https://troy-technical.com/semiconductor-back-end-term-interposer/

Source: https://www.eenewseurope.com/en/fraunhofer-ipms-advances-chiplet-integration-and-low-power-memory/

Collected: November 07, 2026 | Automated Research System (AI)

#05 Qualcomm HBC Memory: Architecture and Dragonfly AI250 Timeline

Published November 02, 2026 ServeTheHome USA



OVERVIEW

Qualcomm has validated its High Bandwidth Compute (HBC) stacked memory architecture, demonstrating over five times the energy efficiency (bandwidth-per-watt) of HBM4 in initial tests. This technology will be integrated into the Dragonfly AI250 data center AI accelerators, with sampling scheduled to begin in 2027.

IN DEPTH

Key Findings

Qualcomm has completed the initial validation of its High Bandwidth Compute (HBC) memory architecture. In testing conducted at its San Diego labs using a 2-layer DRAM sample stack, the company found that HBC delivers more than five times the energy efficiency, measured as bandwidth-per-watt, compared to HBM4.

Technical Details

HBC is a near-memory compute architecture that stacks multiple layers of LPDDR5X DRAM dies directly on top of a small compute die. This differs from HBM, which stacks DRAM on a base die connected to a host processor via an ultra-wide memory bus. By placing the compute die at the bottom of the stack, Qualcomm minimizes the distance data must travel, reducing energy consumption.

The architecture offers several technical advantages:

- **Cost Reduction:** By performing bandwidth-intensive operations on the compute die under the memory, the system requires less bandwidth to connect to the larger processor die. This allows the use of traditional 2D organic substrates instead of expensive advanced packaging like CoWoS or EMIB.
- **Capacity:** Because HBC utilizes LPDDR5X DRAM dies rather than the thin dies used in HBM, projected capacity is expected to exceed current HBM4 implementations.
- **Manufacturing:** While the process still requires TSVs to bond DRAM wafers, the complexity is reduced by eliminating the need for high-speed chiplet connectivity.

Background and Context

First introduced during the 2026 Investor Day, HBC is designed to balance memory capacity, performance, and production costs. Qualcomm positions HBC as a superior alternative to HBM, on-die SRAM, and off-package LPDDR by offering better bandwidth than external LPDDR and higher capacity than on-die SRAM without the associated high costs.

Significance and Outlook

The validation of HBC moves the technology toward mass production. The architecture is a central component of the Dragonfly AI250 accelerator and its successors, specifically targeting the memory bandwidth and capacity requirements of AI inference. Commercial product sampling is scheduled to start in 2027, with final shipping products expected to feature 4-layer DRAM stacks.

Reference technology guide: High Bandwidth Memory (HBM): https://troy-technical.com/semiconductor-back-end-term-hbm/

Reference technology guide: CoWoS: https://troy-technical.com/semiconductor-back-end-term-cowos/

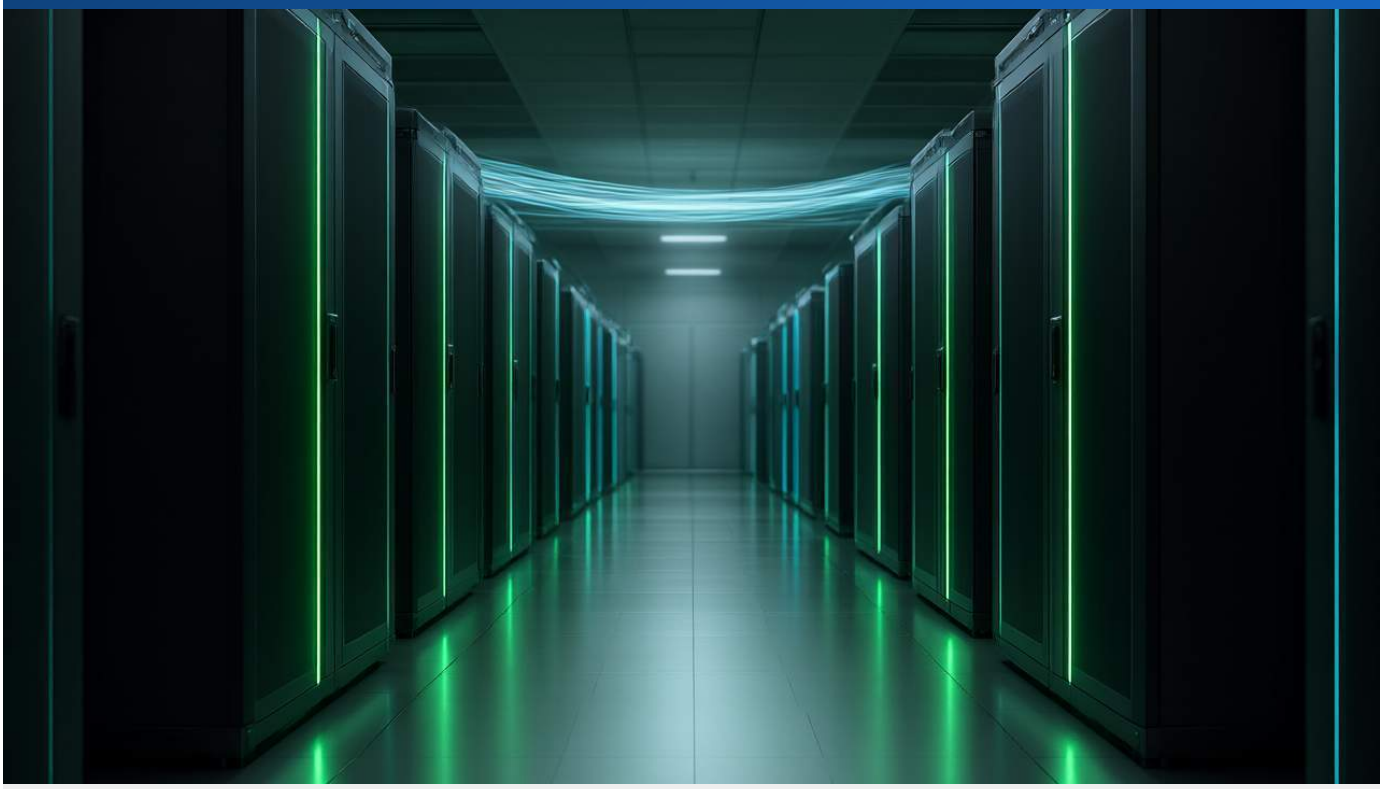
Reference technology guide: Through-Silicon Via (TSV): https://troy-technical.com/semiconductor-back-end-term-tsv/

Source: https://www.servethehome.com/qualcomm-validates-hbc-stacked-memory-ahead-of-2027-dragonfly-ai250-sampling/

Collected: November 07, 2026 | Automated Research System (AI)

#06 NVIDIA Rubin GPU: Revised HBM4 and NVLink Shipping Specs 2026

Published October 31, 2026 ServeTheHome USA



OVERVIEW

NVIDIA has revised the final shipping specifications for its Rubin GPU, reducing HBM4 memory bandwidth by 11% and NVLink bandwidth by 17% while increasing scale-out networking bandwidth. These changes directly impact the Vera Rubin NVL72 rack-scale system, shifting the performance balance toward larger scale-out deployments.

IN DEPTH

Key Findings

NVIDIA has updated the hardware shipping specifications for the Rubin GPU as production ramps up in the fourth quarter of 2026. The revised specs show a reduction in both HBM4 memory bandwidth and scale-up NVLink bandwidth, offset by an increase in scale-out networking bandwidth. Compute throughput remains unchanged at 50 PFLOPS for FP4 inference and 35 PFLOPS for FP4 training.

Technical Details

The following adjustments have been made to the Rubin GPU specifications compared to preliminary targets:

- **HBM4 Memory Bandwidth:** Reduced from 22TB/second to 19.2TB/second. This represents a data rate drop from 10.75Gbps/pin to 9.375Gbps/pin (an 11% loss).
- **NVLink Bandwidth:** Reduced from 3.6TB/second to 3.0TB/second, a 17% reduction.
- **Scale-out Networking Bandwidth:** Increased from 400GB/second to 450GB/second.

These changes propagate to the Vera Rubin NVL72 rack. Cumulative GPU memory bandwidth for the rack has dropped from 1,580TB/second to 1400TB/second, and system-wide NVLink bandwidth has decreased from 260TB/second to 216TB/second. Conversely, bidirectional networking bandwidth for the NVL72 has increased from 28.8TB/second to 32.4TB/second. GPU memory capacity remains at 20.7TB of HBM4.

Background and Context

NVIDIA previously noted that preliminary specifications were subject to change. For context, the revised 9.375Gbps/pin rate remains higher than the official HBM4 specification target of 8Gbps/pin and significantly higher than AMD's MI455X, which runs HBM4 stacks at 7.6Gbps/pin. The source suggests the downward revision may be due to challenges in memory controller speeds, stack speeds, or yields.

Significance and Outlook

While the compute hardware and CPUs are shipping at spec, the reduction in memory and NVLink bandwidth may impact the AI performance of the NVL72 rack compared to original projections. However, the boost in scale-out networking bandwidth provides a performance advantage for larger deployments that rely heavily on networking across multiple systems.

Reference technology guide: High Bandwidth Memory (HBM): https://troy-technical.com/semiconductor-back-end-term-hbm/

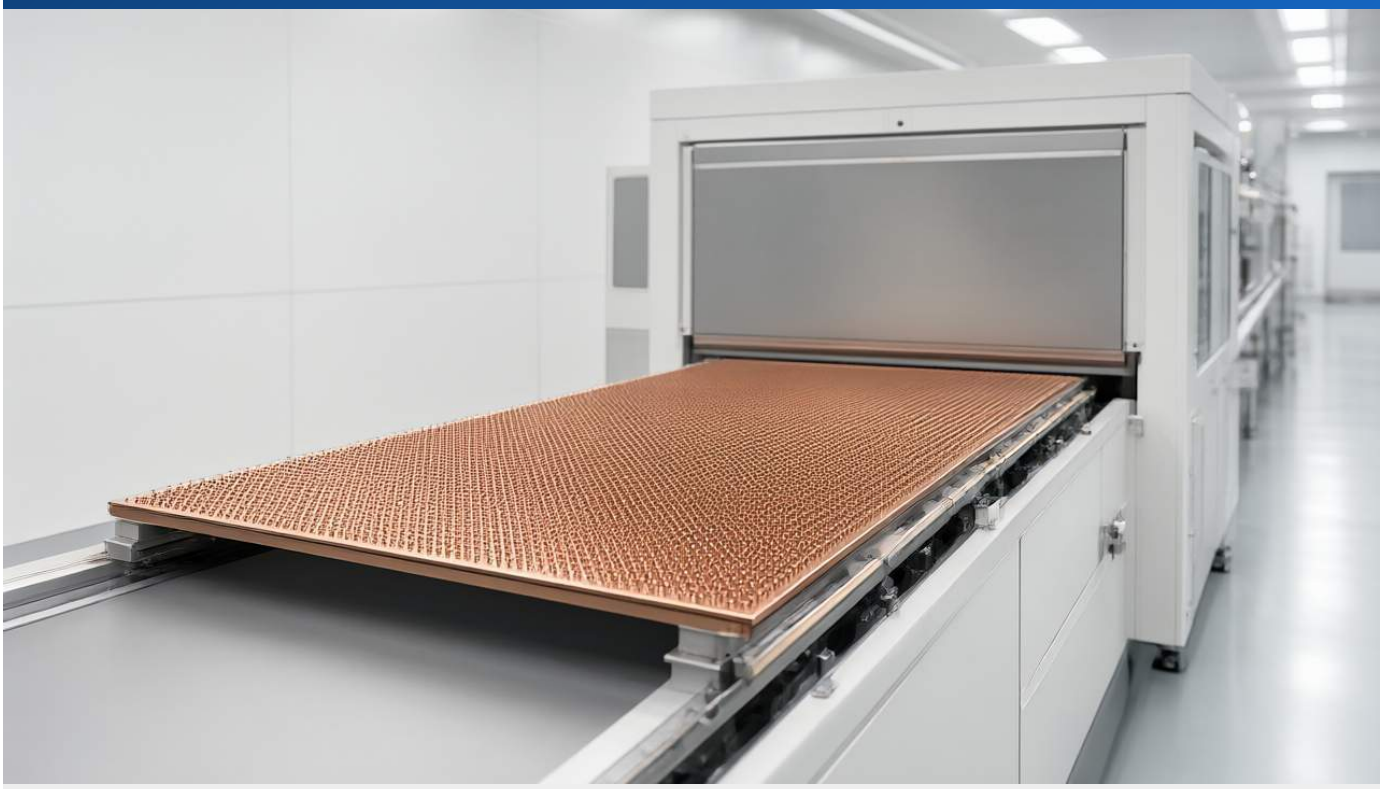
Reference company guide: NVIDIA: https://troy-technical.com/semiconductor-back-end-company-nvidia/

Reference company guide: AMD: https://troy-technical.com/semiconductor-back-end-company-amd/

Source: https://www.servethehome.com/nvidia-updates-rubin-gpu-specs-as-first-production-hardware-arrives/

#07 ACM Research: Ultra ECP ap-p 310 x 310 mm Tool Specs and Shipment

Published November 03, 2026 Semiconductor Digest USA



OVERVIEW

ACM Research has shipped its first 310 × 310 mm Ultra ECP ap-p panel-level horizontal electroplating production tool to a customer in Asia outside mainland China. The system supports multiple plating materials and is designed to meet the complex packaging requirements driven by AI. This shipment marks the transition of ACM's panel-level technology from R&D to scale production.

IN DEPTH

Key Findings

ACM Research has delivered its first 310 × 310 mm Ultra ECP ap-p panel-level horizontal electroplating production system to a customer based in Asia (excluding mainland China). This deployment follows the previous shipment of a 515 × 510 mm R&D tool, signaling the company's ability to commercialize technical breakthroughs for mass production. The tool is designed to address the industry shift toward larger substrates in advanced packaging.

Technical Details

The Ultra ECP ap-p system utilizes proprietary horizontal electroplating technology and is compatible with copper (Cu), nickel (Ni), tin-silver (SnAg), and gold (Au) plating processes. Key technical specifications include:

- **Copper Plating:** Features a high-speed plating paddle optimized for tall copper pillar applications, achieving within-die uniformity for 300-micron copper pillars at high plating rates.
- **Deposition Uniformity:** Employs patent-pending technology that synchronizes chuck rotation with a rotating rectangular electric field.
- **Hardware Reliability:** Incorporates a four-sided sealing dry contact chuck.
- **Contamination Control:** Includes in-cell rinse functionality to minimize chemical cross-contamination between different plating cells.

Background & Context

Electroplating is a critical stage in advanced packaging where plating thickness uniformity, consistency, and equipment stability directly impact product yield and manufacturing efficiency. As AI drives the need for increasingly complex packaging architectures, the industry is adopting panel-level processing to accommodate larger substrates compared to traditional wafer-level processing.

Significance & Outlook

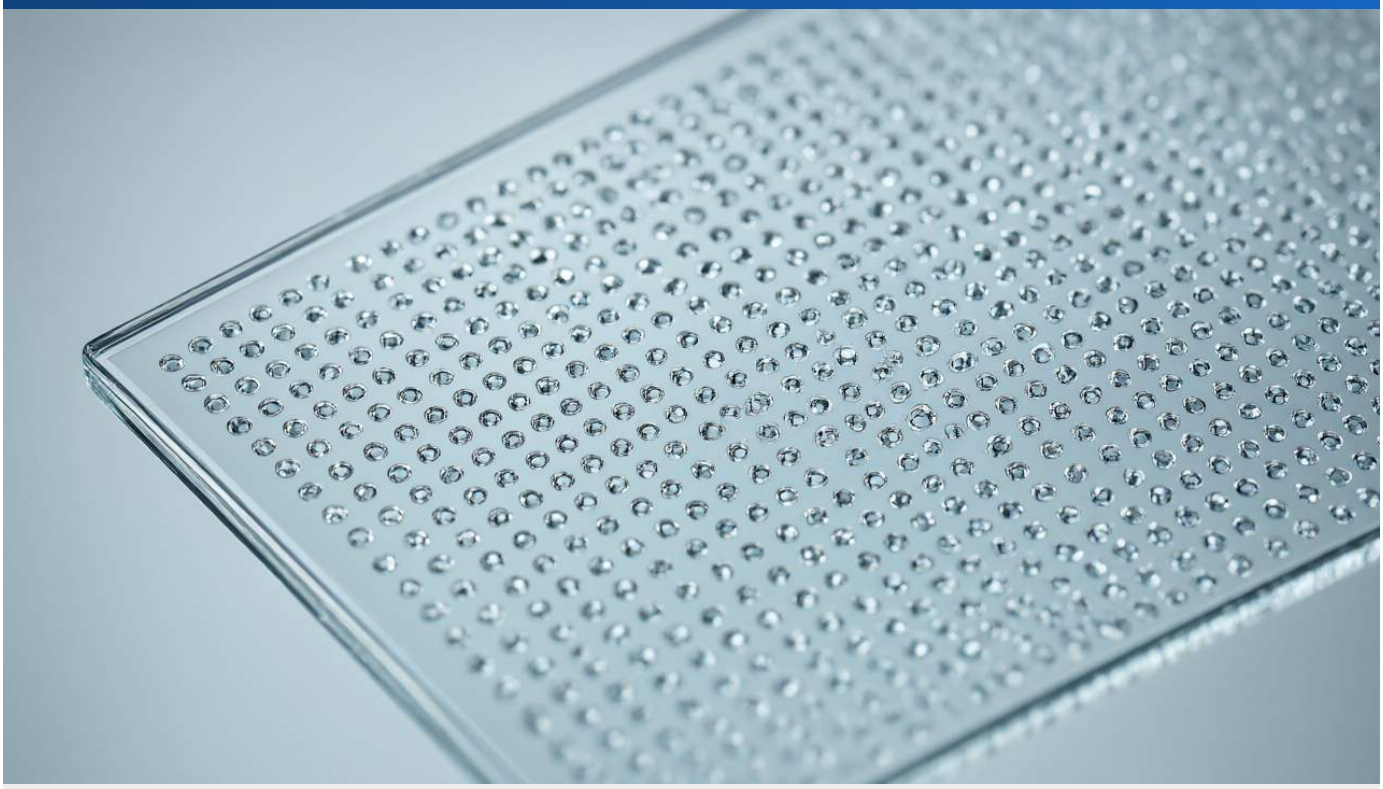
According to CEO Dr. David Wang, the shipment of the 310 × 310 mm tool is a milestone in ACM's advanced packaging efforts. The company positions its horizontal plating technology as a key enabler for next-generation semiconductor packaging across various panel sizes. ACM intends to expand its multi-product platform and global customer base to support the growth of the AI industry.

Source: https://www.semiconductor-digest.com/acm-research-announces-shipment-of-its-first-310-x-310-mm-ultra-ecp-ap-p-panel-level-horizontal-electroplating-production-tool/

Collected: November 07, 2026 | Automated Research System (AI)

#08 Nippon Sheet Glass TGV: Specs and Advantages for 5G/6G Substrates

Published November 04, 2026 MONOist Japan



OVERVIEW

Nippon Sheet Glass showcased a Through Glass Via (TGV) substrate at CEATEC 2026 featuring a custom alkali-free low-dielectric glass composition. The technology reduces energy loss and improves mechanical durability, positioning it as a potential alternative to silicon substrates for high-frequency circuits.

IN DEPTH

Key Findings

Nippon Sheet Glass presented a Through Glass Via (TGV) substrate designed for 5G and 6G communication infrastructure at CEATEC 2026. The substrate utilizes a proprietary alkali-free low-dielectric glass composition developed specifically for the company's unique processing methods, resulting in superior via processability and low dielectric properties.

Technical Details

The TGV substrate is engineered for high-frequency and power-saving electronic circuits. Its physical and electrical specifications are as follows:

- **Glass Type:** Alkali-free glass
- **Thermal Expansion Coefficient (CTE, 0–300°C):** 3.2ppm
- **Young's Modulus:** 76GPa
- **Dielectric Constant (DK):** 5.2F/m at both 1GHz and 10GHz
- **Dielectric Loss Tangent (Df):** 0.002tan at 1GHz and 0.003tan at 10GHz

The company identifies two primary competitive advantages. First, the via surfaces are extremely smooth, eliminating the micro-scratches that typically act as crack initiation points in standard TGVs, thereby increasing resistance to breakage. Second, the low dielectric constant and loss tangent minimize thermal and energy losses during operation.

Background & Context

The TGV development is complemented by other optical and material innovations showcased at the event. These include a liquid-based anti-fogging coating for automotive and surveillance cameras that creates a glass film via heat or plasma treatment, and a lens array (SLA 5EG) with lens elements reduced to a diameter of 300μm.

Significance & Outlook

Nippon Sheet Glass intends for the TGV substrate to serve as a replacement for silicon substrates in various electronic circuit boards and Micro-Electro-Mechanical Systems (MEMS) requiring high power efficiency. By combining a custom-designed glass composition with proprietary processing, the company aims to provide a more durable, low-loss alternative for next-generation high-frequency communication hardware.

Reference technology guide: Glass Substrates: https://troy-technical.com/semiconductor-back-end-term-glass-substrate/

Reference technology guide: Vias: https://troy-technical.com/semiconductor-back-end-term-via/

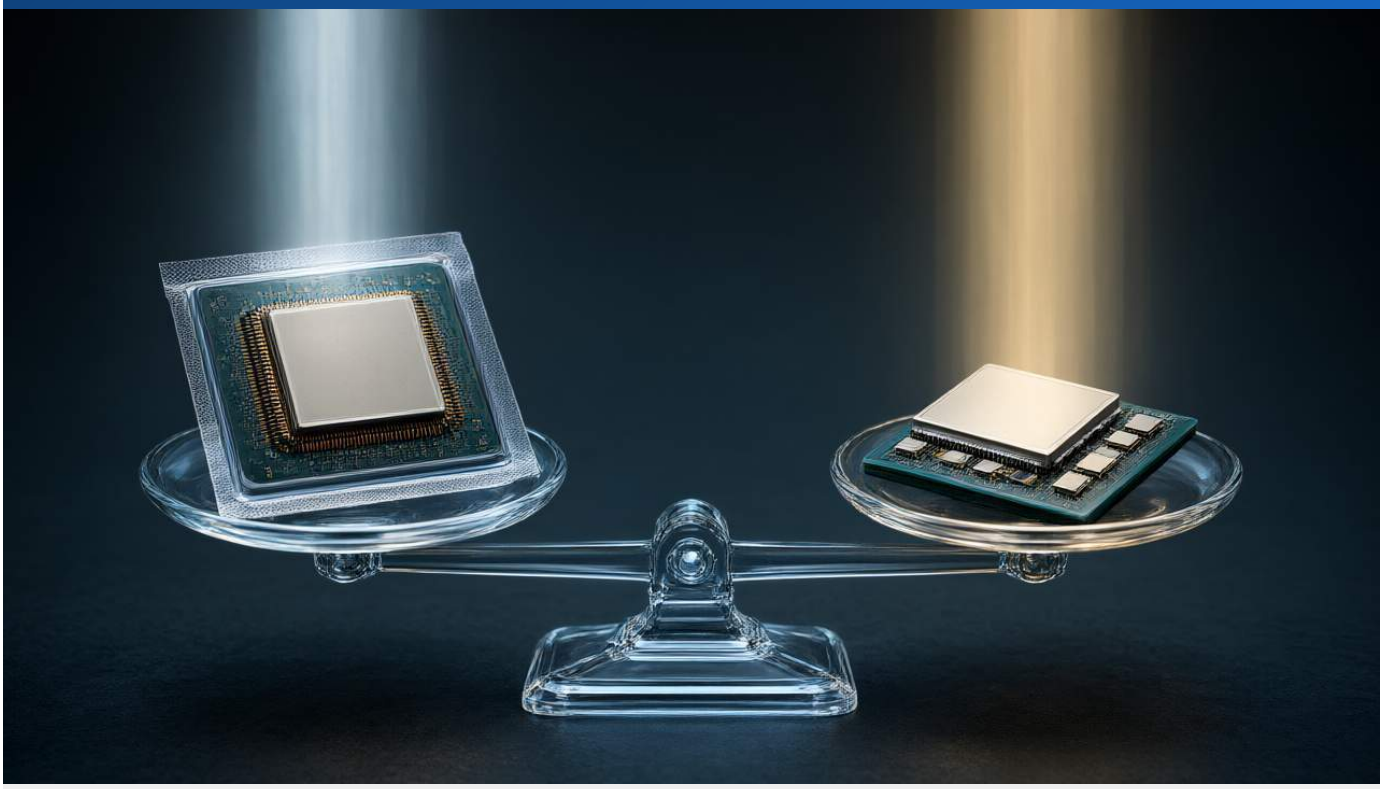
Reference technology guide: Coefficient of Thermal Expansion (CTE): https://troy-technical.com/semiconductor-back-end-term-cte/

Source: https://monoist.itmedia.co.jp/mn/articles/2611/04/news015.html

Collected: November 07, 2026 | Automated Research System (AI)

#09 Intel EMIB-T vs TSMC CoWoS: AI Packaging Roadmaps to 2029

Published November 02, 2026 TechNews 科技新報 Taiwan



OVERVIEW

Intel's EMIB-T is emerging as a viable alternative to TSMC's CoWoS as supply bottlenecks for AI chip packaging increase. While CoWoS remains the choice for high-bandwidth requirements, EMIB-T offers a scalable silicon bridge architecture that could diversify the supply chain for logic chips and custom ASICs.

IN DEPTH

Key Findings

Market research firm Prismark reports that chip designers are evaluating Intel's EMIB-T technology to mitigate supply constraints associated with TSMC's CoWoS. While the two 2.5D packaging technologies may not fully replace one another, they are expected to divide the market based on technical requirements: high-end chips requiring maximum bandwidth will likely stick with CoWoS, while certain logic chips, custom ASICs, and products with lower memory integration needs may shift to EMIB or EMIB-T.

Technical Details

The two technologies differ in their interconnect architectures. CoWoS utilizes an interposer to integrate multiple chips and High Bandwidth Memory (HBM). In contrast, EMIB embeds small silicon bridges within an organic package substrate for high-speed data transfer, avoiding the need for large-area silicon interposers.

Intel's EMIB-T roadmap shows significant scaling in package size and density:

- **2023:** 80 × 80 mm size, 12 silicon bridges, and a die-to-die pitch of 55/45 µm.
- **2026:** 120 × 120 mm size, 20 silicon bridges, and a pitch of 40 µm.
- **Post-2028:** 120 × 240 mm size, 12 to 14 reticle sizes, 40+ silicon bridges, and a pitch of 40/35 µm.
- **Long-term:** Over 240 × 240 mm size, over 40 reticle sizes, 200+ silicon bridges, and a pitch of 25 µm.

Background and Context

TSMC is also expanding CoWoS capabilities. By 2026, TSMC will have mass production capability for interposers up to 5.5 reticle sizes with yields exceeding 98%. Plans for 2028 include expanding to 14 reticle sizes to support 20 HBM units, increasing further in 2029 to over 14 reticle sizes and 24 HBM units. This coincides with the adoption of CoWoS-L for Nvidia's Blackwell and Rubin chips.

Significance and Outlook

The industry faces a critical bottleneck in advanced substrates. Prismark predicts that the area demand for advanced AI/HPC and large-size FCBGA substrates will grow at a CAGR exceeding 45% from 2025 to 2030, with demand expected to exceed supply starting in 2027. Although over 10 ABF substrate suppliers have committed to capacity expansions, supply remains tight, making the availability of alternative packaging routes like EMIB-T strategically important.

Reference technology guide: CoWoS: https://troy-technical.com/semiconductor-back-end-term-cowos/

Reference technology guide: Bridges & EMIB: https://troy-technical.com/semiconductor-back-end-term-bridge/

Reference technology guide: High Bandwidth Memory (HBM): https://troy-technical.com/semiconductor-back-end-term-hbm/

Reference company guide: Intel: https://troy-technical.com/semiconductor-back-end-company-intel/

Reference company guide: TSMC: https://troy-technical.com/semiconductor-back-end-company-tsmc/

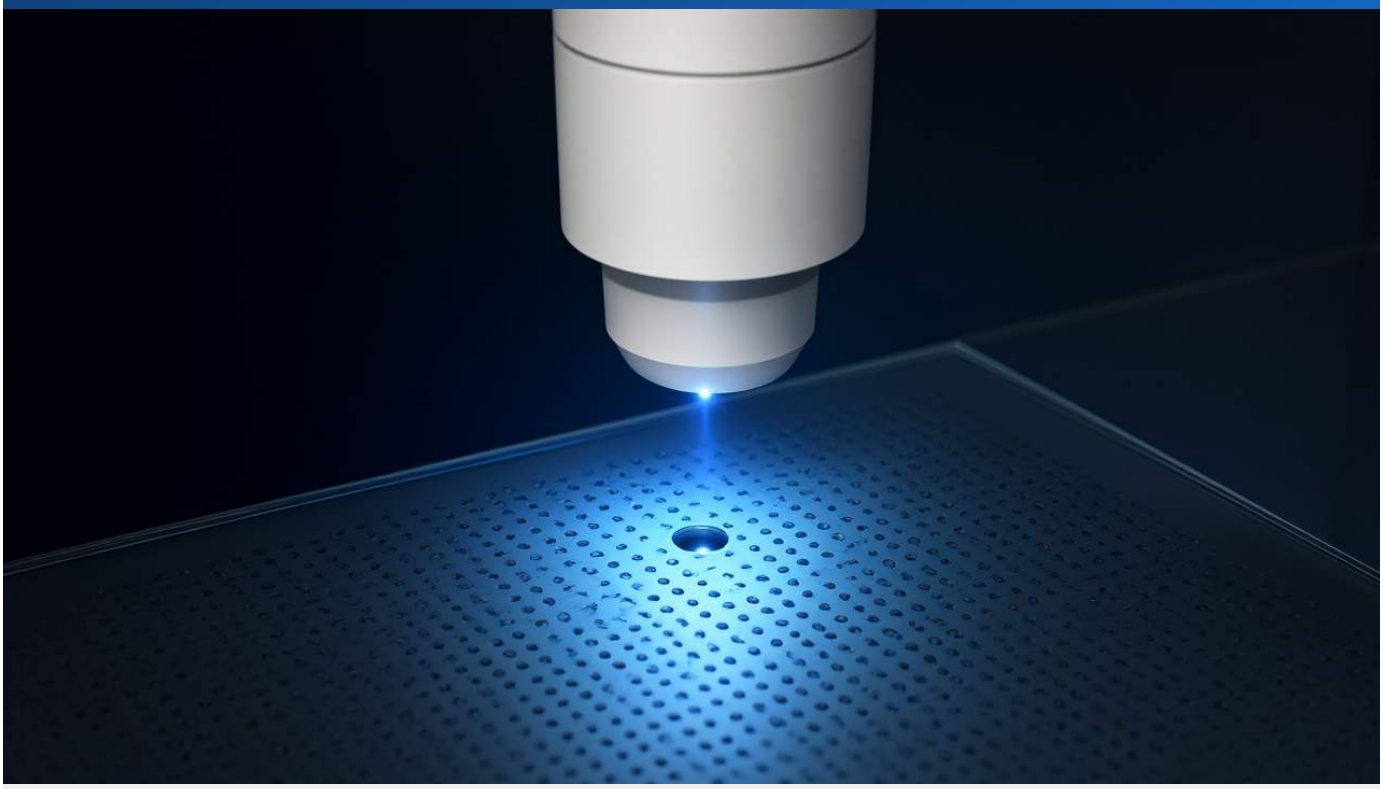
Reference company guide: NVIDIA: https://troy-technical.com/semiconductor-back-end-company-nvidia/

Source: https://technews.tw/2026/11/02/cowos-supply-bottlenecks-intel-emib-t-alternative-packaging/

Collected: November 07, 2026 | Automated Research System (AI)

#10 Eco-Optical: TGV Glass Substrate Inspection and Sensing Specs

Published November 02, 2026 中国工控網 China



OVERVIEW

Eco-Optical received the "2026 Annual Glass Substrate TGV Excellent Enterprise Award" for its technical contributions to Through Glass Via (TGV) process inspection. The company's intelligent autofocus system enables sub-micron tracking precision to resolve imaging challenges in advanced glass substrate packaging.

IN DEPTH

Key Findings

Eco-Optical has been recognized for its technical capabilities in the TGV (Through Glass Via) process inspection field, receiving the "2026 Annual Glass Substrate TGV Excellent Enterprise Award" at the 2026 Shenzhen International Touch and Display Exhibition. The company's solutions address critical inspection difficulties in advanced packaging, specifically substrate morphology fluctuations and uneven via depths.

Technical Details

To ensure clear imaging of via morphology and internal wall defects, Eco-Optical utilizes an intelligent autofocus system with the following specifications:

- **Sampling Speed:** 6.3kHz high-speed defocus sampling.
- **Precision:** Sub-micron level tracking accuracy.
- **Field of View:** Supports a maximum target surface field of 66mm.

This system dynamically compensates for height deviations in glass substrates during high-speed scanning. Additionally, the company offers a linear spectral confocal sensor featuring a coaxial optical design for zero-shadow 3D online inspection. This sensor provides sub-micron measurement precision suitable for measuring flexible circuit board morphology, curved screen edge contours, and glue path thickness.

Background and Context

The technology was showcased at the 2026 Shenzhen International Touch and Display Exhibition, an event focusing on Micro-LED, AI computing optical interconnects, and glass substrate advanced packaging. Beyond TGV, Eco-Optical's autofocus system is applicable to OLED substrate inspection, LED screen crack detection, and optical fiber end-face inspection, addressing issues related to object deformation, tilt, and defocusing caused by transparent materials.

Significance and Outlook

The implementation of these sensing solutions in glass substrate advanced packaging production lines provides stable industrial sensing support for TGV process quality control. By offering high-precision and high-stability solutions for the display and optical interconnect industries, the company aims to support quality upgrades across the supply chain, particularly in AI computing optical interconnects and new display technologies.

Reference technology guide: Glass Substrates: https://troy-technical.com/semiconductor-back-end-term-glass-substrate/

Reference technology guide: Vias: https://troy-technical.com/semiconductor-back-end-term-via/

Reference technology guide: Interconnects: https://troy-technical.com/semiconductor-back-end-term-interconnect/

Source: https://www.gongkong.com/news/202611/454355.html

Collected: November 07, 2026 | Automated Research System (AI)