TROY TECHNICAL

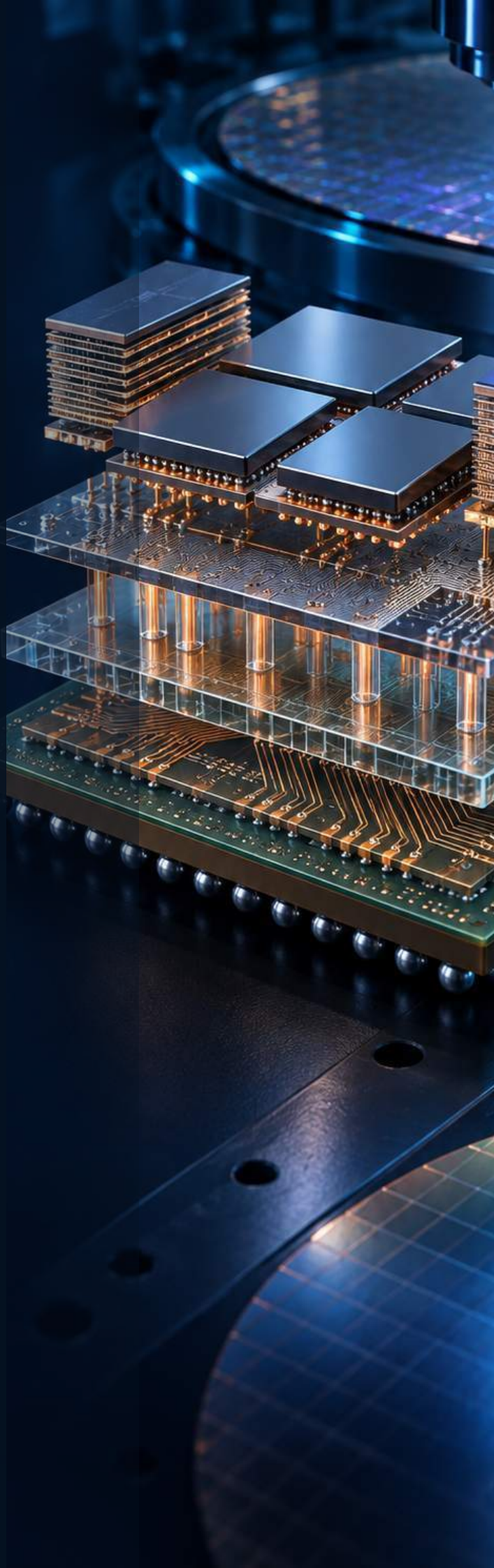
SEMICONDUCTOR BACK-END WEEKLY REPORT

November 14 - November 20, 2026 | Issue 2026-W46

Package performance, process yield, test coverage and qualified capacity

11	10
ANALYZED ARTICLES	PRIORITY THEMES

Issued 2026-11-20 | English edition | fixed approved cover artwork



Semiconductor Back-End: the boundary moved from isolated claims to qualification evidence

11 English articles were reviewed independently from the Japanese edition. Ten themes are retained for management decisions.

SIGNAL 01 | MATERIALS

Intel Foundry: 18A External Deal and Microsoft EMIB Adoption

Intel has secured its first external customer for the 18A process and named Microsoft as the first public customer for its EMIB advanced packaging technology.

SIGNAL 02 | BONDING & ASSEMBLY

Kulicke & Soffa APTURATM WSX: First FTC Panel-Level System Specs

Kulicke & Soffa has shipped the industry's first fluxless thermo-compression (FTC) bonding systems for substrate-level packaging, the APTURATM WSX, to two major customers in Taiwan.

SIGNAL 03 | ADVANCED PACKAGE

ACIR: Automotive Chiplet Interoperability Requirements for 2026

ASRA and imec have released the Automotive Chiplet Interoperability Requirement (ACIR) to enable the integration of chiplets from different providers at the system level.

SIGNAL 04 | TEST & INSPECTION

imec NanoIC: Silicon Interposer PDK Roadmap and 2027 Timeline

imec has delivered baseline flows for its silicon interposer platform within the NanoIC pilot line to enable open chiplet design in Europe.

DECISION

Focus this week's management attention on package performance, process yield, test coverage and qualified capacity. Move only when the linked evidence can be reproduced under your own operating conditions.

THREE MANAGEMENT MOVES

1. Buyers: compare architectures using thermal, electrical, yield, repair and supply evidence.
2. Suppliers: co-develop materials, bonding, inspection and reliability windows with customers.
3. Executives: track yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EVIDENCE DISCIPLINE

FACT states what the collected English source reports. BUSINESS READ and ACTION are editorial interpretations. UNKNOWN lists information that the source file does not establish. A linked article is not treated as independent confirmation of every claim.

Numbers and evidence anchors that require conditions

70%
A04

SOURCE-BOUND CONDITION
With 18A yields reportedly reaching 70%, Intel is positioning itself as a viable alternative to TSMC for hyperscalers developing custom AI silicon.

75%
A10

SOURCE-BOUND CONDITION
This shift to panel-level capability is expected to support a market for ultra high-density panel level packaging revenue growing at a CAGR exceeding 75% from 2026 through 2031.

90%
A06

SOURCE-BOUND CONDITION
Hitachi has developed agentic AI technology that reduces chiplet semiconductor design candidates by over 90% and a CMOS annealing-based system that speeds up power supply-demand planning by 20 times or more.

HOW TO USE THESE NUMBERS
Each value is shown with the condition stated in the collected English article. Do not compare values across different test methods, device sizes, operating temperatures or commercial stages without normalizing those conditions.

Where the value chain moved

Each stage combines one leading theme and one supporting theme. The report treats handoffs as evidence transfers, not decorative arrows.

1

Materials

P01/P06

Intel has secured its first external customer for the 18A process and named Microsoft as the first public customer for its.

2

Bonding & assembly

P02/P07

Kulicke & Soffa has shipped the industry's first fluxless thermo-compression (FTC) bonding systems for substrate-level.

3

Advanced package

P03/P08

ASRA and imec have released the Automotive Chiplet Interoperability Requirement (ACIR) to enable the integration of chiplets.

4

Test & inspection

P04/P09

imec has delivered baseline flows for its silicon interposer platform within the NanoIC pilot line to enable open chiplet.

5

Volume supply

P05/P10

Sikama International is developing a next-generation reflow platform for advanced panel-level packaging (PLP) scheduled for.

EVIDENCE REQUIRED AT EACH HANDOFF

Materials to Bonding & assembly	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Bonding & assembly to Advanced package	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Advanced package to Test & inspection	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.
Test & inspection to Volume supply	Transfer test conditions, acceptance criteria, failure data, owner and decision date. Recheck yield, warpage, thermal cycling, test time, capacity, cost and qualification.

COMMON CONTROL POINT

No theme moves to a commercial commitment until a named owner has reproduced the relevant evidence and documented yield, warpage, thermal cycling, test time, capacity, cost and qualification.

Priority map: maturity and next decision locus



P01	Intel Foundry: 18A External Deal and Microsoft EMIB Adoption System / adoption | cue: Adoption
P02	Kulicke & Soffa APTURATM WSX: First FTC Panel-Level System Specs System / adoption | cue: System
P03	ACIR: Automotive Chiplet Interoperability Requirements for 2026 System / adoption | cue: integration
P04	imec NanoIC: Silicon Interposer PDK Roadmap and 2027 Timeline System / adoption | cue: platform
P05	Sikama Reflow Platform: Next-Gen PLP Specs and 2027 Roadmap System / adoption | cue: Platform
P06	Lam Research: Advanced Packaging Strategies for AI Semiconductors Tech / process | cue: no system/business cue
P07	AMD EPYC Venice: 2.5D Packaging and I/O Die Architecture Tech / process | cue: no system/business cue
P08	Hitachi Agentic AI: Chiplet Design and Power Planning Efficiency System / adoption | cue: system
P09	Samsung DRAM Roadmap: Three-Track Strategy for HBM5 and LPDDR System / adoption | cue: application
P10	HBM4 Controller Partitioning: Host vs. Base Die Study (2026) System / adoption | cue: system

REPRODUCIBLE POSITIONING RULE

Horizontal position uses five discrete stages: Research, Prototype, Joint evaluation, Product adoption and Scale. The vertical bands classify the next decision locus: Tech / process, System / adoption, or Business / rules (including supply systems). Article-title cues take precedence; the overview is used only when the title is silent. These are categories, not impact ranks. Bubble diameter reflects the editorial score.

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P01 Intel Foundry: 18A External Deal and Microsoft EMIB Adoption

A04 | Materials | Research

2026-11-19

FACT

Intel has secured its first external customer for the 18A process and named Microsoft as the first public customer for its EMIB advanced packaging technology. With 18A yields reportedly reaching 70%, Intel is positioning itself as a viable alternative to TSMC for hyperscalers developing custom AI silicon.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P01.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

P02 Kulicke & Soffa APTURATM WSX: First FTC Panel-Level System Specs

A10 | Bonding & assembly | Research

2026-11-19

FACT

Kulicke & Soffa has shipped the industry's first fluxless thermo-compression (FTC) bonding systems for substrate-level packaging, the APTURATM WSX, to two major customers in Taiwan. The system enables larger-format chip-on-panel processes for AI and high-performance computing (HPC) applications. This shift to panel-level capability is expected to support a market for ultra high-density panel level packaging revenue growing at a CAGR exceeding 75% from 2026 through 2031.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P02.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P03 ACIR: Automotive Chiplet Interoperability Requirements for 2026

A03 | Advanced package | Research

Prior release 2026-11-13

FACT

ASRA and imec have released the Automotive Chiplet Interoperability Requirement (ACIR) to enable the integration of chiplets from different providers at the system level. This document establishes common architectural requirements for critical functions including safety and power management to foster a cross-manufacturer interoperable ecosystem.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P03.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 1/5 | DECISION LOCUS: SYSTEM / ADOPTION

P04 imec NanoIC: Silicon Interposer PDK Roadmap and 2027 Timeline

A09 | Test & inspection | Joint evaluation

2026-11-16

FACT

imec has delivered baseline flows for its silicon interposer platform within the NanoIC pilot line to enable open chiplet design in Europe. A dedicated Process Design Kit (PDK) is scheduled for release in early 2027, allowing designers to virtually explore high-density 2.5D packaging. This initiative provides a technical foundation for AI accelerators and high-performance computing systems.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P04.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 3/5 | DECISION LOCUS: SYSTEM / ADOPTION

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P05 Sikama Reflow Platform: Next-Gen PLP Specs and 2027 Roadmap

A11 | Volume supply | Scale-up

Prior release 2026-11-12

FACT

Sikama International is developing a next-generation reflow platform for advanced panel-level packaging (PLP) scheduled for commercial launch in 2027. The system targets critical thermal and atmospheric controls for substrates including glass and organic materials to support emerging architectures like FOPLP and TGV.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P05.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 5/5 | DECISION LOCUS: SYSTEM / ADOPTION

P06 Lam Research: Advanced Packaging Strategies for AI Semiconductors

A07 | Materials | Pilot

2026-11-16

FACT

Lam Research is leveraging its front-end manufacturing expertise to overcome the physical limits of semiconductor scaling through advanced packaging. The company focuses on 3D packaging, utilizing high-aspect-ratio TSV etching and plasma dicing to improve performance and yield for high-cost AI chips.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P06.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 20/25 | MATURITY 2/5 | DECISION LOCUS: TECH / PROCESS

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P07 AMD EPYC Venice: 2.5D Packaging and I/O Die Architecture

A05 | Bonding & assembly | Research

2026-11-16

FACT

AMD has transitioned its server CPUs to 2.5D packaging to support a bandwidth increase to 1.6 TB/s while reducing power consumption. The Venice architecture introduces a split I/O die design to accommodate the physical constraints of advanced packaging and differentiated requirements for SP7 and SP8 platforms.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P07.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 1/5 | DECISION LOCUS: TECH / PROCESS

P08 Hitachi Agentic AI: Chiplet Design and Power Planning Efficiency

A06 | Advanced package | Pilot

2026-11-16

FACT

Hitachi has developed agentic AI technology that reduces chiplet semiconductor design candidates by over 90% and a CMOS annealing-based system that speeds up power supply-demand planning by 20 times or more. These advancements aim to shorten semiconductor development cycles and stabilize complex power grids.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P08.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 2/5 | DECISION LOCUS: SYSTEM / ADOPTION

FACT is source-bound. BUSINESS READ, ACTION and UNKNOWN are explicit editorial layers.

P09 Samsung DRAM Roadmap: Three-Track Strategy for HBM5 and LPDDR

A01 | Test & inspection | Product adoption

2026-11-17

FACT

Samsung Electronics has divided its next-generation DRAM development into three distinct tracks based on product application. This strategy utilizes different cell architectures and wafer-bonding techniques to balance mass-production feasibility with high-performance requirements for HBM5 and LPDDR.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P09.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 4/5 | DECISION LOCUS: SYSTEM / ADOPTION

P10 HBM4 Controller Partitioning: Host vs. Base Die Study (2026)

A08 | Volume supply | Pilot

Prior release 2026-11-13

FACT

Researchers from the University of California, Riverside have conducted the first systematic quantitative study on partitioning HBM4 controller functions between the host and the memory base die. The study evaluates how moving complex controller functions to the base die, enabled by logic process manufacturing, impacts system architecture.

WHY IT MATTERS

The decision relevance is package performance, process yield, test coverage and qualified capacity. The signal should be tested at the application and operating-system level, not accepted from a headline alone.

BUSINESS READ

For operating companies, compare the reported change with current qualification, sourcing and product-roadmap assumptions. For suppliers, co-develop materials, bonding, inspection and reliability windows with customers.

ACTION

Within 30 days, compare architectures using thermal, electrical, yield, repair and supply evidence; record the evidence and owner against P10.

UNKNOWN

Still unproven or incompletely stated: yield, warpage, thermal cycling, test time, capacity, cost and qualification.

EDITORIAL SCORE 19/25 | MATURITY 2/5 | DECISION LOCUS: SYSTEM / ADOPTION

Playbook and 0-5 year roadmap

STAKEHOLDER	NOW | 0-30 DAYS	NEXT | 1-12 MONTHS	LATER | 1-5 YEARS
Operating companies	compare architectures using thermal, electrical, yield, repair and supply evidence	Run production-like qualification with explicit acceptance and stop criteria.	Build a portfolio and architecture that can absorb technology and supplier changes.
Materials, equipment and technology suppliers	co-develop materials, bonding, inspection and reliability windows with customers	Create shared reliability, process-window and failure-analysis data with customers.	Standardize interfaces, traceability, lifecycle support and recovery services.
Trading, investment and legal teams	Map yield, warpage, thermal cycling, test time, capacity, cost and qualification.	Contract for capacity, quality, change notice, liability, alternatives and exit.	Diversify regional, technical and customer concentration risk.

ROADMAP

NOW | 0-30 DAYS
Evidence ledger
Owner: Strategy + quality
Deliverable: claim, source, condition, owner

NOW | 0-30 DAYS
Risk screen
Owner: Procurement + legal
Deliverable: unknowns, alternatives, stop

NEXT | 1-12 MONTHS
Joint qualification
Owner: R&D + supplier
Deliverable: process window and failure data

NEXT | 1-12 MONTHS
Commercial gate
Owner: Business + finance
Deliverable: unit economics and capacity

LATER | 1-5 YEARS
Platform strategy
Owner: Executive team
Deliverable: portfolio and interface roadmap

LATER | 1-5 YEARS
Service layer
Owner: Operations + channel
Deliverable: monitoring, maintenance and recovery

GO / NO-GO GATES

GATE	OWNER	REQUIRED EVIDENCE	NO-GO CONDITION
G1 Evidence	**Quality**	Source, test conditions and reproducibility	No traceable evidence
G2 Integration	**R&D**	Interface, process window and failure analysis	Cannot meet system conditions
G3 Commercial	**Business**	Capacity, total cost, contract and alternatives	Economics or supply cannot be supported
G4 Lifecycle	**Operations**	Monitoring, maintenance, change notice and exit	No accountable operating plan

ANALYZED ARTICLES | ITEMS 01-11

Every title and URL is displayed in full. URLs wrap without shortening and remain clickable. A verified-reference label means the translated HTML did not retain its original source URL.

ID	FULL ARTICLE TITLE	FULL SOURCE / VERIFIED REFERENCE URL - CLICKABLE
A01	Samsung DRAM Roadmap: Three-Track Strategy for HBM5 and LPDDR	https://www.thelec.net/news/articleView.html?idxno=15696
A02	UCIe 4.0: Memory Connectivity and Management Specifications	https://www.electronicdesign.com/technologies/eda/article/55419127/electronic-design-ucie-40-standardizes-memory-connectivity
A03	ACIR: Automotive Chiplet Interoperability Requirements for 2026	https://www.all-electronics.de/automotive/automotive-chiplets-sollen-kompatibler-werden/2766953
A04	Intel Foundry: 18A External Deal and Microsoft EMIB Adoption	https://www.trendforce.com/news/2026/11/19/news-intel-scores-dual-foundry-wins-microsoft-named-first-emib-customer-tan-says-18a-secures-first-external-deal/
A05	AMD EPYC Venice: 2.5D Packaging and I/O Die Architecture	https://chipsandcheese.com/p/talking-venice-with-mahesh-subramony
A06	Hitachi Agentic AI: Chiplet Design and Power Planning Efficiency	https://finance.biggo.com/news/0743db9c-1a88-4d16-860f-72441620ae6b
A07	Lam Research: Advanced Packaging Strategies for AI Semiconductors	https://eetimes.itmedia.co.jp/ee/articles/2611/16/news042.html
A08	HBM4 Controller Partitioning: Host vs. Base Die Study (2026)	https://semiengineering.com/shifting-hbm4-controller-functions-closer-to-memory-uc-riverside/
A09	imec NanoIC: Silicon Interposer PDK Roadmap and 2027 Timeline	https://www.dqindia.com/semiconductors/imec-advances-europes-silicon-interposer-technology-capabilities-through-nanoic-pilot-line-paving-the-way-for-open-chiplet-design-12811834
A10	Kulicke & Soffa APTURATM WSX: First FTC Panel-Level System Specs	https://www.3dincites.com/2026/11/kulicke-soffa-accelerates-industry-shift-to-panel-level-capability-for-ai-applications/
A11	Sikama Reflow Platform: Next-Gen PLP Specs and 2027 Roadmap	https://www.3dincites.com/2026/11/sikama-develops-next-generation-reflow-platform-for-advanced-panel-level-packaging/

Semiconductor_BackEnd — Selected Articles

Date: 2026-11-21

Articles: 11

Table of Contents

#01 Samsung DRAM Roadmap: Three-Track Strategy for HBM5 and LPDDR

#02 UCIe 4.0: Memory Connectivity and Management Specifications

#03 ACIR: Automotive Chiplet Interoperability Requirements for 2026

#04 Intel Foundry: 18A External Deal and Microsoft EMIB Adoption

#05 AMD EPYC Venice: 2.5D Packaging and I/O Die Architecture

#06 Hitachi Agentic AI: Chiplet Design and Power Planning Efficiency

#07 Lam Research: Advanced Packaging Strategies for AI Semiconductors

#08 HBM4 Controller Partitioning: Host vs. Base Die Study (2026)

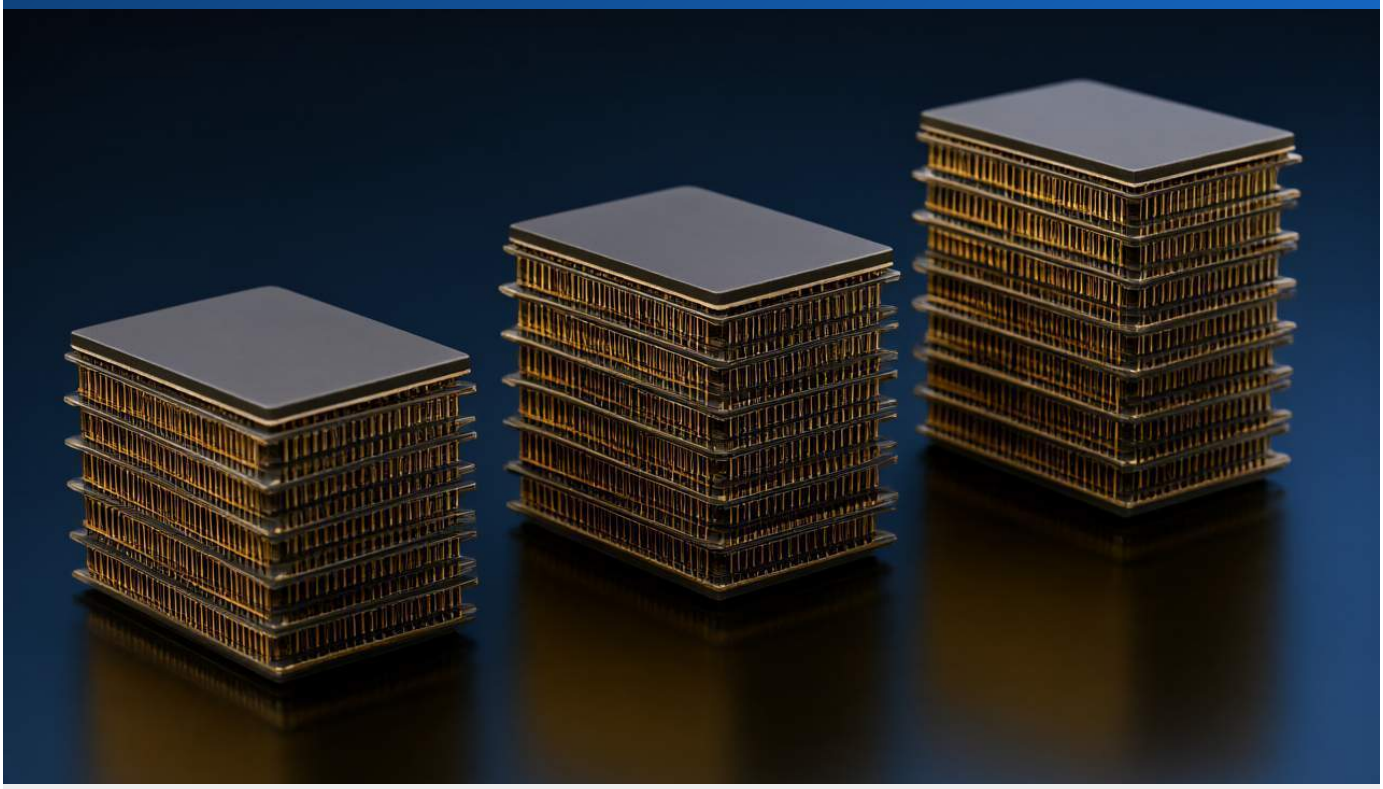
#09 imec NanoIC: Silicon Interposer PDK Roadmap and 2027 Timeline

#10 Kulicke & Soffa APTURA™ WSX: First FTC Panel-Level System Specs

#11 Sikama Reflow Platform: Next-Gen PLP Specs and 2027 Roadmap

#01 Samsung DRAM Roadmap: Three-Track Strategy for HBM5 and LPDDR

Published November 17, 2026 THE ELEC South Korea



OVERVIEW

Samsung Electronics has divided its next-generation DRAM development into three distinct tracks based on product application. This strategy utilizes different cell architectures and wafer-bonding techniques to balance mass-production feasibility with high-performance requirements for HBM5 and LPDDR.

IN DEPTH

Key Findings

Samsung Electronics has finalized a three-track development strategy for DRAM generations following D1c. The company will simultaneously develop D1d and D0A architectures, targeting transfer to mass-production lines in the second half of next year. Additionally, a third track, D0AV, is being developed for high-performance products with a target date of 2028.

Technical Details

The development tracks are differentiated by architecture and application:

- **D0A (HBM5):** This architecture separates memory cells and peripheral circuits on different wafers. Cells are fabricated using the D1b process, while core and peripheral circuits use the D1d process. The two wafers are joined via hybrid bonding, which aligns insulating layers and copper interconnects.
- **D1d (LPDDR):** This process retains the conventional $6F^2$ cell architecture, where memory cells and peripheral circuits are fabricated on a single wafer.
- **D0AV (High-Performance DRAM):** Based on a $4F^2$ cell architecture, this track targets products requiring higher performance than LPDDR.

Background and Context

Conventional DRAM uses a $6F^2$ layout (3F width by 2F height). The $4F^2$ architecture reduces dimensions to 2F to increase cell density, though this presents significant technical challenges. To address this, Samsung developed Vertical Channel Transistor (VCT) technology to position transistor channels vertically. While Samsung has secured a working die using a single-digit-nanometer process with $4F^2$ and VCT, internal concerns regarding mass-production complexity led to the current strategy.

Significance and Outlook

By applying wafer-bonding technology to conventional $6F^2$ cells first (D0A), Samsung aims to reduce development complexity before transitioning to 3D DRAM. The D0A architecture allows for higher cell density by utilizing space previously occupied by peripheral circuitry and enables independent optimization of peripheral circuits for higher performance. The D0AV track will follow approximately one year after D1d and D0A.

Reference technology guide: Bonding: https://troy-technical.com/semiconductor-back-end-term-bonding/

Reference technology guide: Interconnects: https://troy-technical.com/semiconductor-back-end-term-interconnect/

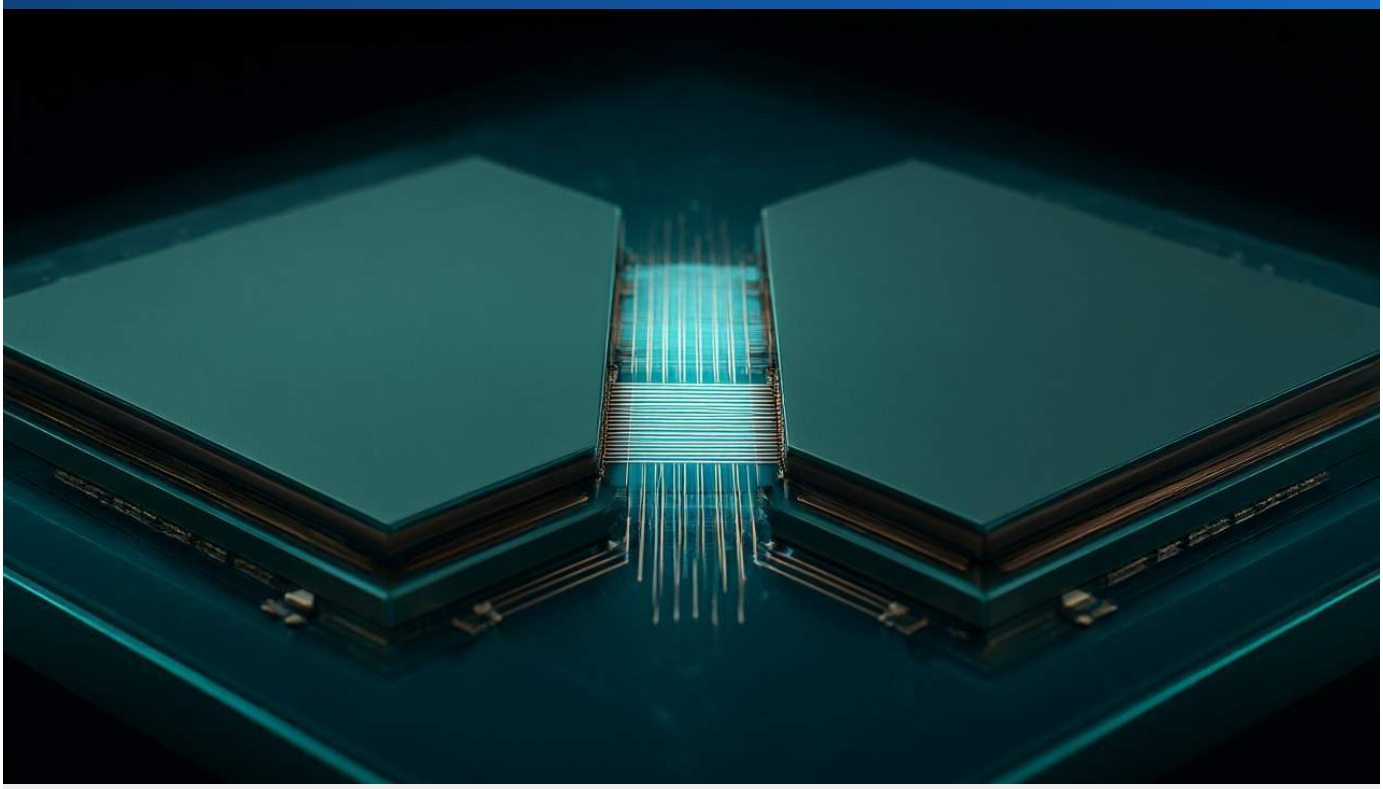
Reference company guide: Samsung Electronics: https://troy-technical.com/semiconductor-back-end-company-samsung-electronics/

Source: https://www.thelec.net/news/articleView.html?idxno=15696

Collected: November 21, 2026 | Automated Research System (AI)

#02 UCIe 4.0: Memory Connectivity and Management Specifications

Published November 16, 2026 Electronic Design USA



OVERVIEW

The UCIe Consortium has released the UCIe 4.0 specification, introducing the UCIe.mem protocol to achieve a bandwidth density of 2.5-TB/s/mm. The update improves energy efficiency by 30% to 80% and enhances secure chiplet management through the Trusted Reporting of Chiplet State (TRoCs).

IN DEPTH

Key Findings

UCIe 4.0 enhances memory and management support for chiplets, targeting a die-edge bandwidth density of approximately 2.5-TB/s/mm. The standard introduces co-optimized link profiles that increase energy efficiency by 30% to 80% at 64 GT/s. Additionally, an improved UCIe-S bump map for 48 GT/s and 64 GT/s increases shoreline bandwidth density by approximately 20% and area bandwidth density by 10%, allowing for higher bandwidth within a smaller die footprint.

Technical Details: UCIe.mem and Management

The new UCIe.mem protocol, based on the current PHY, is designed for high data efficiency, reaching up to 93.75%. It optimizes protocol encodings by packing memory requests and responses into UCIe flits (flow control units) to minimize overhead. Specifically, it can pack two memory requests or four memory responses into 16-byte slots of a 256-byte flit, reducing the need for extensive header overhead, acknowledgments, and flow-control information.

For system security and administration, UCIe 4.0 introduces the following:

- **Trusted Reporting of Chiplet State (TRoCs):** Provides secure communication of a chiplet's state to prevent spoofing attacks and manipulated state information.
- **Secure Management Channels:** Two-way channels that allow a common management subsystem to configure power and memory resources across chiplets from different sources.
- **Reliability Features:** Enhanced reset management, link-health monitoring, and optional error notifications.

Significance and Outlook

These advancements allow designers to either achieve higher bandwidth in a given footprint or reallocate package resources for other system requirements. The inclusion of enhanced management and error notification features is particularly critical for functional-safety applications in the aviation and automotive sectors, where strict safety and reliability standards must be met.

Reference technology guide: Chiplets: https://troy-technical.com/semiconductor-back-end-term-chiplet/

Source: https://www.electronicdesign.com/technologies/eda/article/55419127/electronic-design-ucie-40-standardizes-memory-connectivity

Collected: November 21, 2026 | Automated Research System (AI)

#03 ACIR: Automotive Chiplet Interoperability Requirements for 2026

Published November 13, 2026 all-electronics Germany



OVERVIEW

ASRA and imec have released the Automotive Chiplet Interoperability Requirement (ACIR) to enable the integration of chiplets from different providers at the system level. This document establishes common architectural requirements for critical functions including safety and power management to foster a cross-manufacturer interoperable ecosystem.

IN DEPTH

Key Findings

The Advanced SoC Research for Automotive (ASRA) and imec introduced the "Automotive Chiplet Interoperability Requirement" (ACIR) on November 12, 2026. Presented during the eighth Autonomous Edge Chiplet Forum (AECF) in Japan, the ACIR document supplements existing standards by defining shared architectural requirements. The primary goal is to allow independently developed chiplets from various vendors to function together within a single overall system.

Technical Details

The ACIR focuses on the capabilities that interoperable automotive chiplets must support, though the specific technical implementation remains the responsibility of individual providers. The requirements cover several critical system-level functions:

- Error and system management, including a uniform infrastructure for error reporting to ensure predictable reactions.
- Boot sequences and energy management.
- Functional safety.
- Common specifications for die-to-die communication.

The first version of the ACIR is available for public download at acir.imec-int.com, and the organizations are seeking feedback from the industry.

Background & Context

The AECF event featured 16 keynotes and 140 registered participants, involving ASRA, RISE-A, and imec. While the focus was on automotive applications, the forum also addressed chiplets for aerospace, robotics, and security applications. According to Bart Placklé, Senior Vice President Automotive at imec, partners are currently developing reference designs, IP components, concrete chiplets, and development tools.

Significance & Outlook

The ACIR serves as a framework for vehicle manufacturers and Tier-1 suppliers to formulate shared technical requirements. To achieve a cross-manufacturer interoperable ecosystem, ASRA and imec have committed to closer cooperation with other entities, including Arm with FCSA, CHASSIS, and Tenstorrent with OCA. This initiative targets a broad range of stakeholders, including semiconductor companies, software and IP providers, system integrators, and tool manufacturers.

Reference technology guide: Chiplets: https://troy-technical.com/semiconductor-back-end-term-chiplet/

Source: https://www.all-electronics.de/automotive/automotive-chiplets-sollen-kompatibler-werden/2766953

#04 Intel Foundry: 18A External Deal and Microsoft EMIB Adoption

Published November 19, 2026 TrendForce Taiwan



OVERVIEW

Intel has secured its first external customer for the 18A process and named Microsoft as the first public customer for its EMIB advanced packaging technology. With 18A yields reportedly reaching 70%, Intel is positioning itself as a viable alternative to TSMC for hyperscalers developing custom AI silicon.

IN DEPTH

Key Findings

Intel has achieved two major milestones in its foundry business: securing the first external customer for its 18A process and partnering with Microsoft for Embedded Multi-die Interconnect Bridge (EMIB) technology. Microsoft will utilize EMIB for its custom Azure silicon. Additionally, CEO Lip-Bu Tan reported that 18A yields have climbed to 70%, a significant improvement from the "horrible" yields observed when Tan took over in March 2025.

Technical Details

The 18A deal specifically involves 18A-P, an upgraded process node that entered risk production in June, according to Intel technology chief Pushkar Ranade. Regarding packaging, Intel's EMIB technology is gaining traction among AI chip developers. Beyond Microsoft, reports indicate that MediaTek is utilizing EMIB-T for Google’s ninth-generation TPU, with mass production targeted for 1Q28. Analyst Ming-Chi Kuo suggests that all Google TPU generations from v9 (Humufish and Triggerfish) and v10 (Quillfish) onward are expected to adopt EMIB-T.

Background & Context

These developments occur as AI-driven demand exceeds TSMC’s CoWoS capacity, prompting hyperscalers to seek alternative suppliers. While the first 18A customer remains unidentified, speculation includes NVIDIA, Apple, and various hyperscalers. Microsoft is a primary candidate, as previous reports from October 2025 suggested Intel would manufacture the Maia 2 AI processor using 18A/18A-P. The Microsoft partnership also encompasses a multi-year Xeon supply agreement and joint development on Compute Express Link (CXL).

Significance & Outlook

The recovery of 18A yields and the acquisition of high-profile customers provide momentum for Intel's five-year strategy to challenge TSMC's foundry dominance. The adoption of EMIB and EMIB-T by major players like Microsoft and Google indicates a shift in the advanced packaging landscape, as Intel moves from internal production to serving the broader AI silicon market.

Reference technology guide: CoWoS: https://troy-technical.com/semiconductor-back-end-term-cowos/

Reference technology guide: Interconnects: https://troy-technical.com/semiconductor-back-end-term-interconnect/

Reference technology guide: Package Substrates: https://troy-technical.com/semiconductor-back-end-term-package-substrate/

Reference company guide: Intel: https://troy-technical.com/semiconductor-back-end-company-intel/

Reference company guide: TSMC: https://troy-technical.com/semiconductor-back-end-company-tsmc/

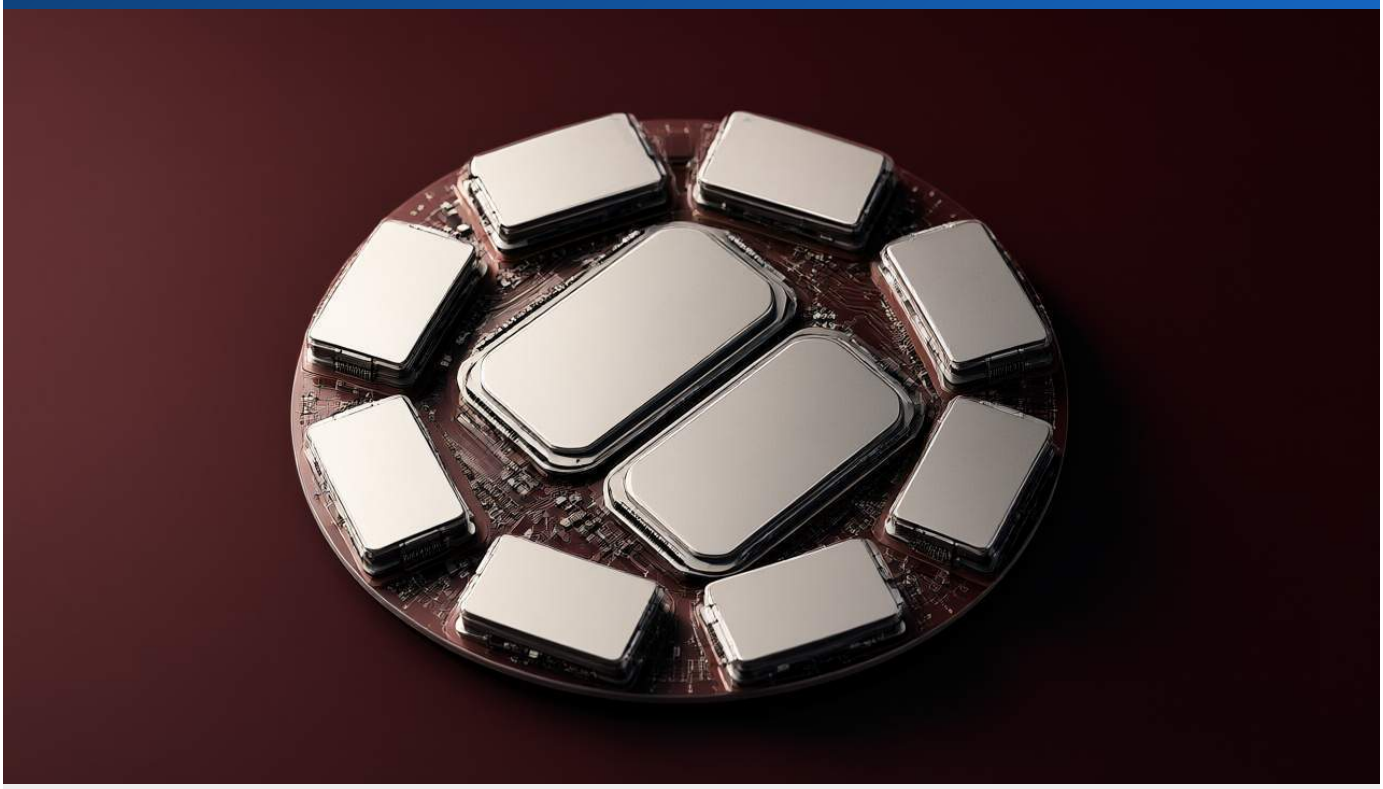
Reference company guide: NVIDIA: https://troy-technical.com/semiconductor-back-end-company-nvidia/

Source: https://www.trendforce.com/news/2026/11/19/news-intel-scores-dual-foundry-wins-microsoft-named-first-emib-customer-tan-says-18a-secures-first-external-deal/

Collected: November 21, 2026 | Automated Research System (AI)

#05 AMD EPYC Venice: 2.5D Packaging and I/O Die Architecture

Published November 16, 2026 Chips and Cheese USA



OVERVIEW

AMD has transitioned its server CPUs to 2.5D packaging to support a bandwidth increase to 1.6 TB/s while reducing power consumption. The Venice architecture introduces a split I/O die design to accommodate the physical constraints of advanced packaging and differentiated requirements for SP7 and SP8 platforms.

IN DEPTH

Key Findings

AMD's Venice processors utilize 2.5D packaging to handle a data movement requirement of 1.6 TB/s. This shift was driven by power efficiency; using conventional packaging for this level of bandwidth would have consumed approximately 10–15% of the total SoC power budget. To facilitate this, AMD has moved away from a single I/O die to a split I/O die configuration.

Technical Details

The transition to 2.5D packaging introduced strict physical constraints, requiring shorter die-to-die connections and precise matching of die widths at the interface. To provide sufficient perimeter for CCD connections and I/O beachfront, AMD implemented the following:

- **Mirrored I/O Design:** The SoC uses two identical I/O die designs, with one rotated 180 degrees. While this results in some area overhead due to the duplication of functional blocks like the root of trust, it simplifies design.
- **Fabric Topology:** The mirrored design is engineered to operate as a single domain in NPS1 configurations to maintain quality of service, bandwidth, and latency.
- **Platform Differentiation:** AMD developed distinct I/O dies for the SP7 and SP8 platforms. The SP7 I/O die is optimized for higher compute and memory bandwidth. In contrast, the SP8 I/O die provides 128 PCIe lanes per socket and half the memory channels of SP7, targeting lower core counts (up to 96 for Zen 6 and 128 for Zen 6c).

Background & Context

In previous generations, AMD utilized standard packaging and GMI links, which were sufficient when data movement was under 700 GB/s. The move to 2.5D packaging allows for low-power, high-bandwidth, and low-latency links, which mitigates the latency and power penalties associated with splitting the I/O die.

Significance & Outlook

The adoption of a tiled approach to I/O and compute allows AMD to scale SoCs to larger core counts and differentiate products for different enterprise market requirements. AMD indicates that tiled approaches will become increasingly advantageous as SoC core counts continue to scale.

Reference technology guide: Chiplets: https://troy-technical.com/semiconductor-back-end-term-chiplet/

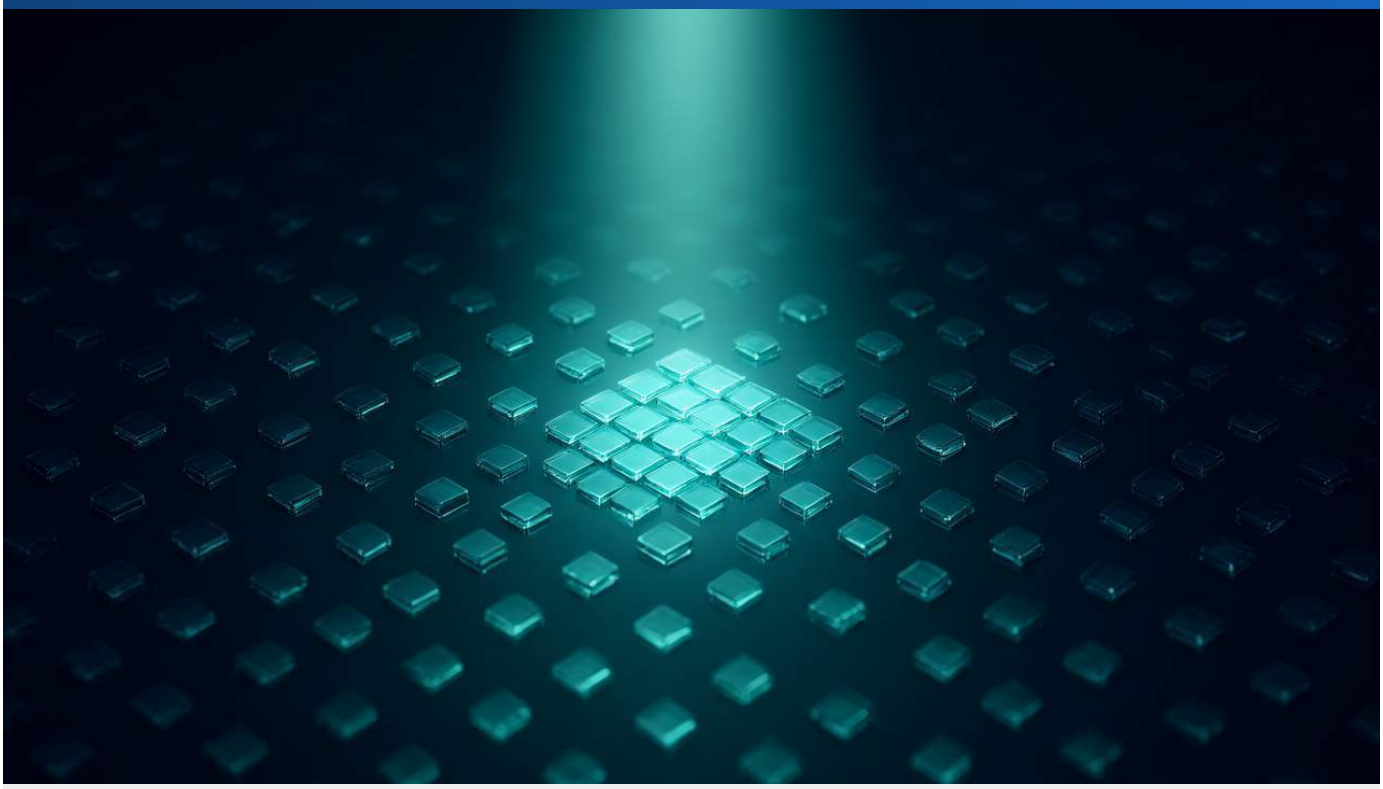
Reference company guide: AMD: https://troy-technical.com/semiconductor-back-end-company-amd/

Source: https://chipsandcheese.com/p/talking-venice-with-mahesh-subramony

Collected: November 21, 2026 | Automated Research System (AI)

#06 Hitachi Agentic AI: Chiplet Design and Power Planning Efficiency

Published November 16, 2026 BigGo Finance Japan



OVERVIEW

Hitachi has developed agentic AI technology that reduces chiplet semiconductor design candidates by over 90% and a CMOS annealing-based system that speeds up power supply-demand planning by 20 times or more. These advancements aim to shorten semiconductor development cycles and stabilize complex power grids.

IN DEPTH

Key Findings

Hitachi has introduced two primary technological advancements focused on optimization. In semiconductor design, the company utilized agentic AI to reduce the number of design candidates for chiplet packages by more than 90%. Simultaneously, in the power sector, Hitachi combined CMOS annealing with AI and mathematical optimization to generate large-scale power supply-demand plans in 60 minutes—a process that previously took over a day using conventional mathematical optimization methods, representing a speedup of 20 times or more.

Technical Details

The chiplet design foundation integrates agentic AI for automated candidate narrowing with high-speed physical analysis technology. Designers input requirements in natural language, and the system automatically suggests chip combinations, layouts, and package structures while considering component procurement availability. This allows for rapid evaluation of electrical, thermal, and stress characteristics to minimize rework.

The power planning technology utilizes CMOS annealing, a method based on the Ising model that operates at room temperature and handles over 100,000 variables. For generator startup and shutdown planning (SCUC), CMOS annealing narrows promising candidates, which are then iteratively refined using AI, mathematical optimization, and power grid analysis to evaluate reserve capacity, output ramp rates, and operating costs.

Background & Context

Chiplet semiconductors, which combine small chips into a single device, are increasingly used in autonomous driving, edge AI, and industrial IoT. However, the complexity of layout and wiring often leads to lengthy early-stage design phases. In the power sector, the rise of data centers and renewable energy has increased the complexity of power grids, making traditional computation for 500+ generators difficult.

Significance & Outlook

These technologies support Hitachi's "IWIM" social infrastructure intelligence platform and are intended for deployment within the "Lumada 3.0" solution. While verification shows significant lead-time reductions in the semiconductor supply chain and cost suppression in power grids, Hitachi has not yet disclosed the timing for commercialization or actual system application.

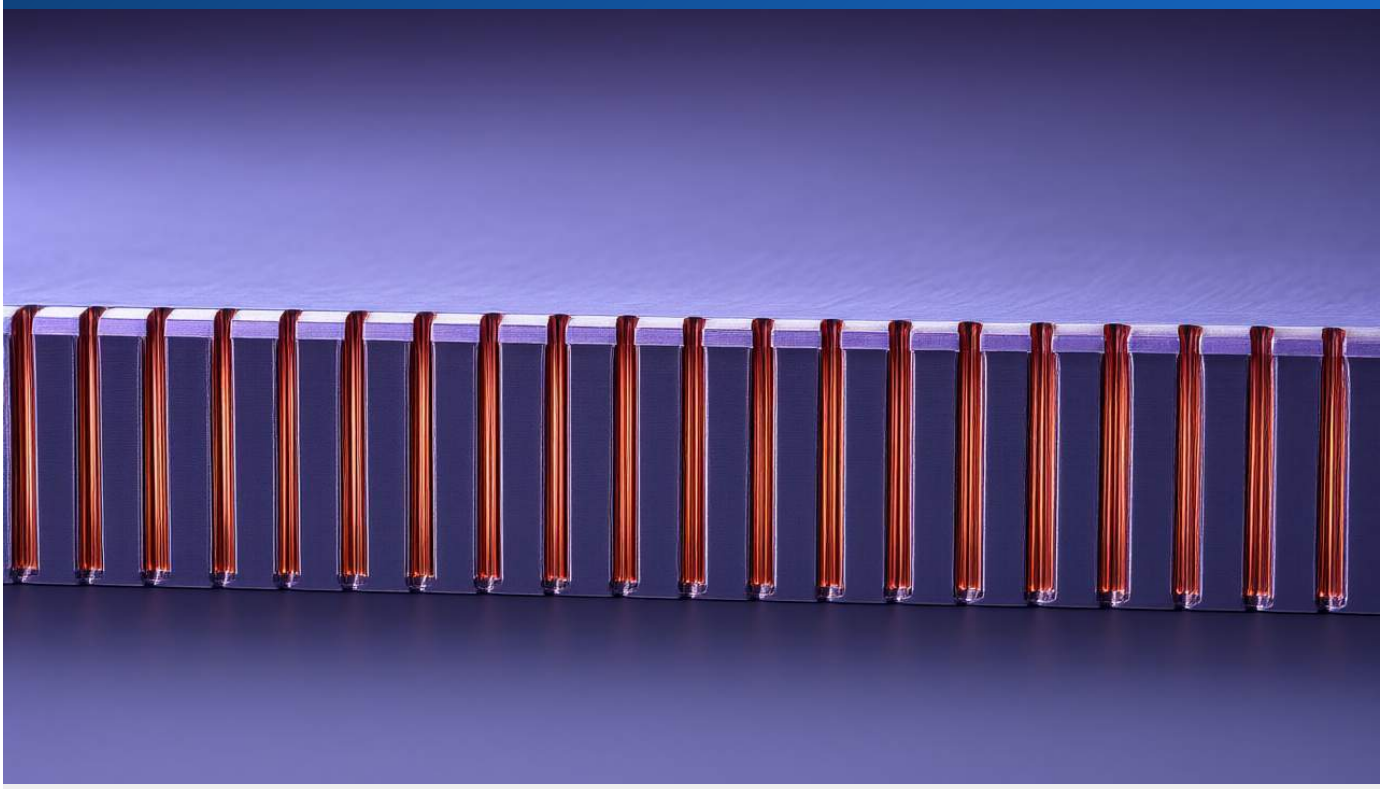
Reference technology guide: Chiplets: https://troy-technical.com/semiconductor-back-end-term-chiplet/

Source: https://finance.biggo.com/news/0743db9c-1a88-4d16-860f-72441620ae6b

Collected: November 21, 2026 | Automated Research System (AI)

#07 Lam Research: Advanced Packaging Strategies for AI Semiconductors

Published November 16, 2026 EE Times Japan Japan



OVERVIEW

Lam Research is leveraging its front-end manufacturing expertise to overcome the physical limits of semiconductor scaling through advanced packaging. The company focuses on 3D packaging, utilizing high-aspect-ratio TSV etching and plasma dicing to improve performance and yield for high-cost AI chips.

IN DEPTH

Key Findings

Lam Research has identified advanced packaging as the critical "partner" to overcome the physical limitations of traditional semiconductor miniaturization. During a media briefing held on November 10, 2026, the company detailed its strategy to apply large-scale production technologies from front-end processes—specifically wet processing, deposition, and etching—to the advanced packaging sector.

Technical Details: 3D Packaging and TSV

A primary focus of Lam's evolution is the shift from horizontal to Z-axis (3D) packaging. This approach involves stacking chips vertically and connecting them via Through-Silicon Vias (TSV). To achieve high performance, Lam addresses two critical technical challenges:

- **TSV Etching:** To meet the requirements for high-aspect ratios of 15:1 or greater, Lam utilizes advanced etching technology that employs high-speed cycle counts to ensure high-precision control.
- **Plasma Dicing:** To replace traditional blade-based methods, Lam employs plasma dicing. This technology significantly reduces particles and increases die strength by more than 1.5 times compared to conventional methods.

Background and Context

The push toward advanced packaging is driven by the rapid development of AI, which has led to an explosion in data processing requirements. While performance was historically improved through miniaturization, the industry is now facing physical limits. These constraints, combined with the need for larger memory capacity, wider bandwidth, and the management of increased power consumption and heat generation, necessitate a shift in architectural approach.

Significance and Outlook

According to Chee Ping Lee, Managing Director of Advanced Packaging Strategic Marketing at Lam, the precision of the dicing process directly impacts the bottom line. Because AI semiconductors are extremely expensive, the increase in yield provided by plasma dicing and high-precision TSV etching provides direct economic value to manufacturers.

Reference technology guide: Through-Silicon Via (TSV): https://troy-technical.com/semiconductor-back-end-term-tsv/

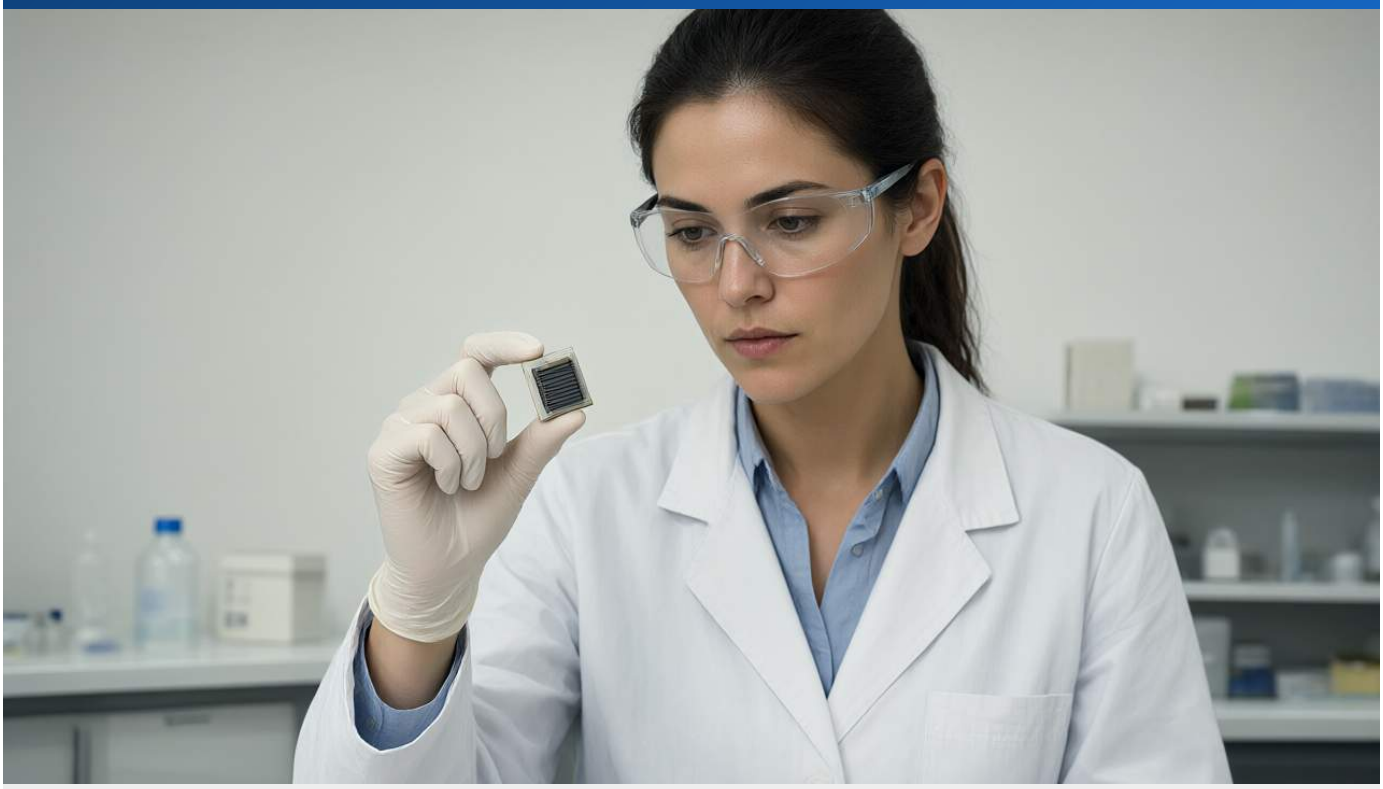
Reference company guide: Lam Research: https://troy-technical.com/semiconductor-back-end-company-lam-research/

Source: https://eetimes.itmedia.co.jp/ee/articles/2611/16/news042.html

Collected: November 21, 2026 | Automated Research System (AI)

#08 HBM4 Controller Partitioning: Host vs. Base Die Study (2026)

Published November 13, 2026 Semiconductor Engineering USA



OVERVIEW

Researchers from the University of California, Riverside have conducted the first systematic quantitative study on partitioning HBM4 controller functions between the host and the memory base die. The study evaluates how moving complex controller functions to the base die, enabled by logic process manufacturing, impacts system architecture.

IN DEPTH

Key Findings

Tharunya Yogananda and Wantong Li of the University of California, Riverside have presented a quantitative analysis of function-level controller placement for HBM4. The research explores the trade-offs of shifting controller responsibilities from the host side to the HBM base die on a silicon interposer.

Technical Details

The study focuses on the partitioning of the memory controller into its main functions. The researchers evaluated four specific placement configurations to determine the optimal distribution of tasks:

- A complete host-side controller.
- A complete base die controller.
- Intermediate placements where maintenance functions are moved to the base die.
- Intermediate placements where scheduling functions are moved to the base die.

Background & Context

This architectural shift is made possible by advancements in HBM4, where the base die of the memory stack can be manufactured using a logic process. This capability allows the base die to accommodate more complex controller functions in closer proximity to the DRAM than was possible in previous generations.

Significance & Outlook

By analyzing the placement of maintenance and scheduling functions, this research provides a framework for optimizing the interface between the host and HBM4. The findings are detailed in the technical paper titled “Beyond Host-Side Control: HBM Controller Partitioning Across Host and HBM Base Dies,” published in November 2026 (arXiv:2611.10930).

Reference technology guide: High Bandwidth Memory (HBM): https://troy-technical.com/semiconductor-back-end-term-hbm/

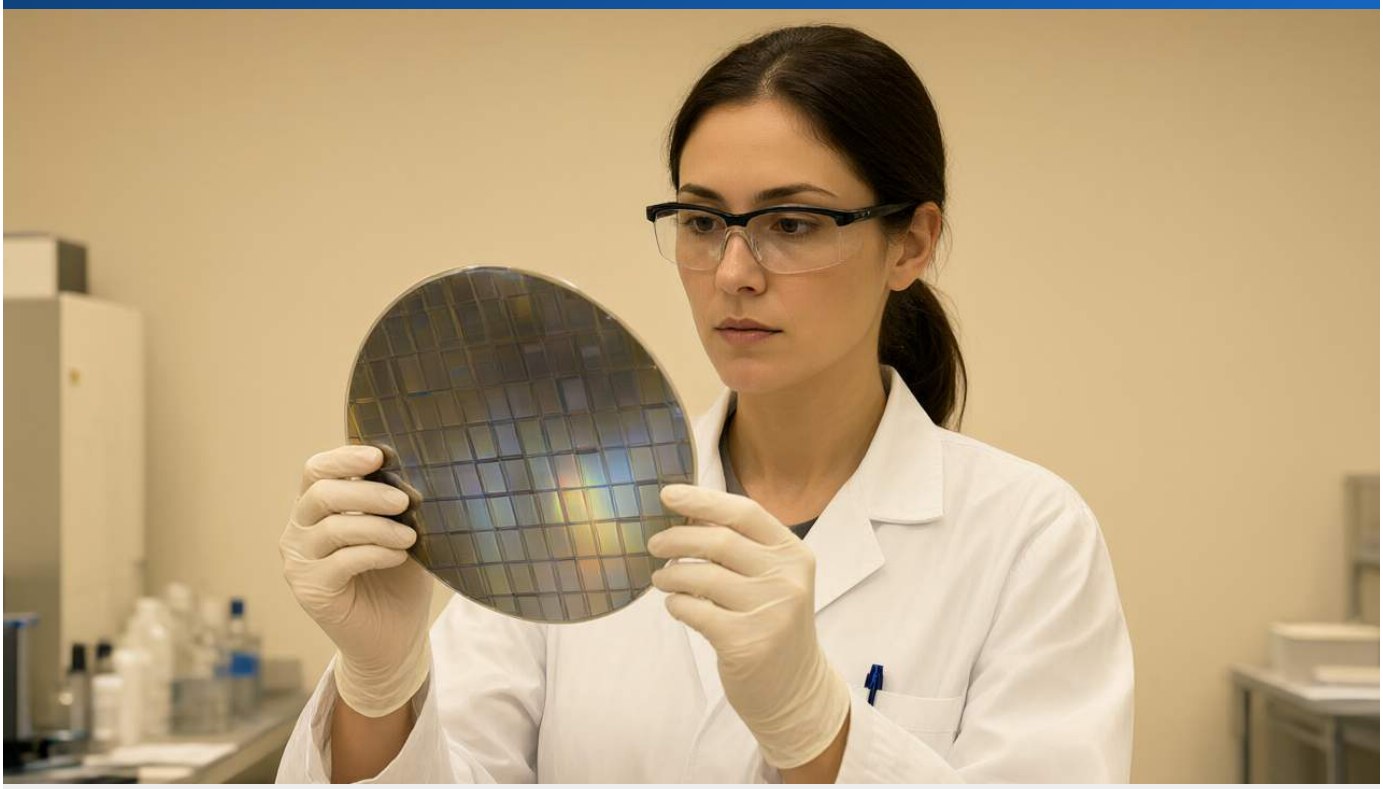
Reference technology guide: Interposers: https://troy-technical.com/semiconductor-back-end-term-interposer/

Source: https://semiengineering.com/shifting-hbm4-controller-functions-closer-to-memory-uc-riverside/

Collected: November 21, 2026 | Automated Research System (AI)

#09 imec NanoIC: Silicon Interposer PDK Roadmap and 2027 Timeline

Published November 16, 2026　DQ (Dataquest)　ベルギー



OVERVIEW

imec has delivered baseline flows for its silicon interposer platform within the NanoIC pilot line to enable open chiplet design in Europe. A dedicated Process Design Kit (PDK) is scheduled for release in early 2027, allowing designers to virtually explore high-density 2.5D packaging. This initiative provides a technical foundation for AI accelerators and high-performance computing systems.

IN DEPTH

Key Findings

imec has achieved a milestone in the NanoIC pilot line by delivering the baseline flows for its silicon interposer platform. This development serves as the technical foundation for a dedicated silicon interposer Process Design Kit (PDK) slated for release in early 2027. The PDK will enable universities, start-ups, and fabless companies to utilize industry-standard EDA environments from Cadence and Synopsys to virtually explore chiplet integration.

Technical Details

The silicon interposer platform is designed to act as a high-density routing layer beneath dies, facilitating connections between compute chiplets, high-bandwidth memory, and specialized components. Key technical specifications include:

- Support for microbump pitches down to 20 µm.
- Integration of through-silicon vias (TSVs).
- Multiple metal routing layers for 2.5D packaging.

This technology is one of three advanced interconnect solutions being developed within NanoIC, alongside die-to-wafer hybrid bonding for ultra-dense connections and fine-pitch RDL interposers for cost-efficient integration.

Background & Context

The shift toward chiplet architectures is driven by the rising performance requirements of AI, where system efficiency depends on the bandwidth and energy consumption of the connections between specialized dies. The NanoIC pilot line is jointly funded by the Chips Joint Undertaking via the European Union’s Digital Europe and Horizon Europe programs, with participation from Belgium (Flanders), France, Germany, Finland, Ireland, and Romania.

Significance & Outlook

By providing a common technology foundation and accessible PDKs, imec aims to allow researchers and companies to experiment with different interconnect approaches and evaluate future system architectures. The long-term goal of the NanoIC project is to transition from virtual exploration via PDKs to the production of physical silicon demonstrators on the pilot line. This infrastructure is intended to prepare European strategic markets for next-generation automotive, physical AI, and advanced computing systems.

Reference technology guide: Interposers: https://troy-technical.com/semiconductor-back-end-term-interposer/

Reference technology guide: Chiplets: https://troy-technical.com/semiconductor-back-end-term-chiplet/

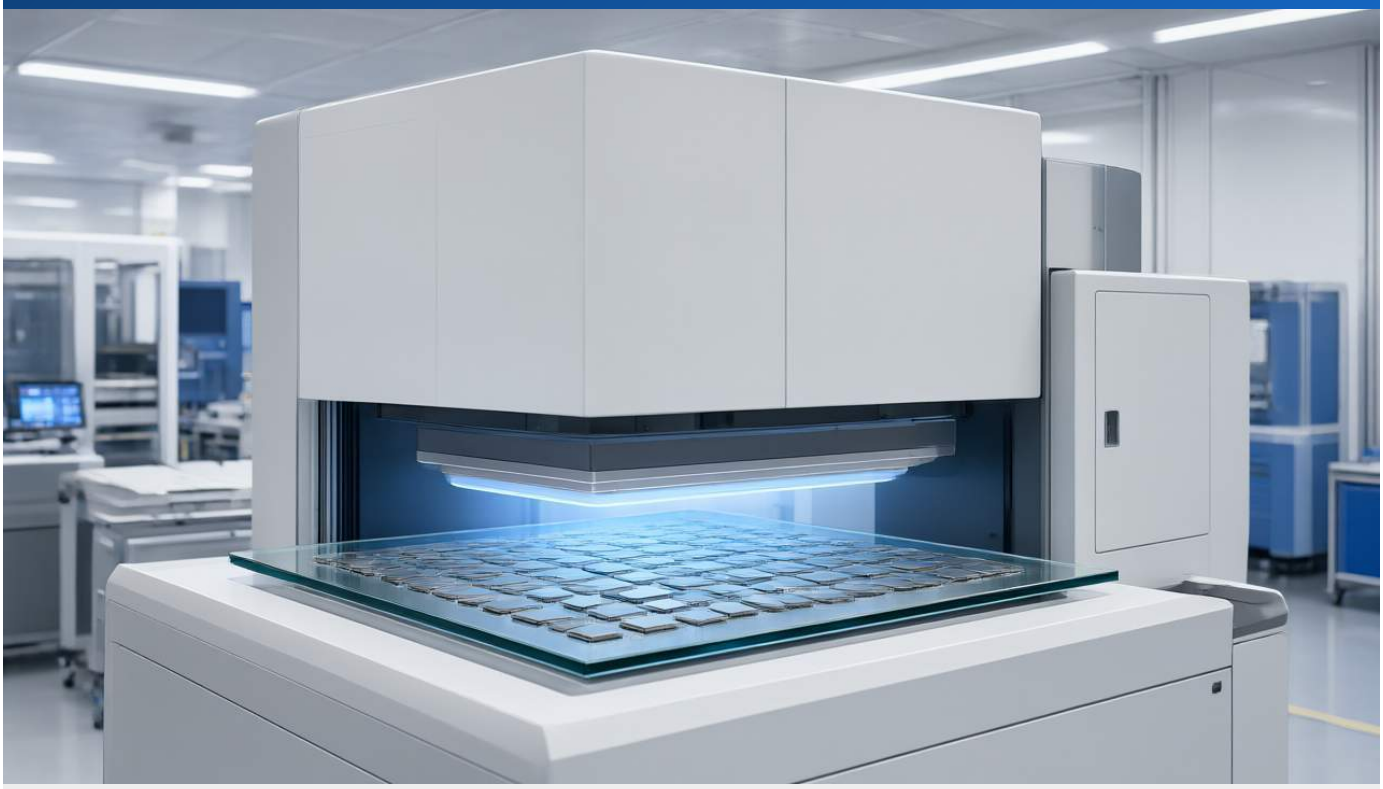
Reference technology guide: Through-Silicon Via (TSV): https://troy-technical.com/semiconductor-back-end-term-tsv/

Source: https://www.dqindia.com/semiconductors/imec-advances-europes-silicon-interposer-technology-capabilities-through-nanoic-pilot-line-paving-the-way-for-open-chiplet-design-12811834

Collected: November 21, 2026 | Automated Research System (AI)

#10 Kulicke & Soffa APTURA™ WSX: First FTC Panel-Level System Specs

Published November 19, 2026　IMAPS 3D InCites（Kulicke & Soffa発表）　USA



OVERVIEW

Kulicke & Soffa has shipped the industry's first fluxless thermo-compression (FTC) bonding systems for substrate-level packaging, the APTURA™ WSX, to two major customers in Taiwan. The system enables larger-format chip-on-panel processes for AI and high-performance computing (HPC) applications. This shift to panel-level capability is expected to support a market for ultra high-density panel level packaging revenue growing at a CAGR exceeding 75% from 2026 through 2031.

IN DEPTH

Key Findings

Kulicke & Soffa (K&S) has deployed the APTURA™ WSX, the first fluxless thermo-compression (FTC) bonding platform designed for panel-level packaging. The company has shipped these systems to two major customers located in Taiwan to support the production of emerging artificial intelligence (AI) and high-performance computing (HPC) applications.

Technical Details

The APTURA™ WSX is engineered to handle the industry's largest AI packages by facilitating interposer on substrate and interposer on-panel/platform assembly. Key technical specifications and features include:

- **Bondhead Capability:** An ultra-large 180mm bondhead designed for high throughput and production efficiency.
- **Bonding Technology:** A dual-fluxless bonding process that combines plasma and formic acid to reduce oxides.
- **Process Capability:** Extension of K&S's existing FTC leadership from fine-pitch chip on wafer production to larger-format chip on panel processes.

Background & Context

The transition to panel-level formats is driven by the requirements of AI and HPC, which necessitate larger dies and larger packages. K&S's FTC technology is already utilized in high-volume manufacturing for advanced heterogeneous compute applications, providing control, reliability, and cleanliness.

Significance & Outlook

The shift toward larger format, high-precision, panel-based solutions is intended to improve system-level performance and production efficiency. According to data from Yole Group's Panel Level Packaging 2026 report, the served available market for ultra high-density panel level packaging revenue is projected to grow at a CAGR exceeding 75% between 2026 and 2031. By scaling its proven high-volume manufacturing process to the panel level, K&S provides a path for customers to implement next-generation AI and HPC packaging architectures.

Reference technology guide: Interposers: https://troy-technical.com/semiconductor-back-end-term-interposer/

Reference technology guide: Bonding: https://troy-technical.com/semiconductor-back-end-term-bonding/

Reference technology guide: Panel-Level Packaging (PLP): https://troy-technical.com/semiconductor-back-end-term-plp/

Source: https://www.3dincites.com/2026/11/kulicke-soffa-accelerates-industry-shift-to-panel-level-capability-for-ai-applications/

Collected: November 21, 2026 | Automated Research System (AI)

#11 Sikama Reflow Platform: Next-Gen PLP Specs and 2027 Roadmap

Published November 12, 2026　IMAPS 3D InCites（Sikama発表）　USA



OVERVIEW

Sikama International is developing a next-generation reflow platform for advanced panel-level packaging (PLP) scheduled for commercial launch in 2027. The system targets critical thermal and atmospheric controls for substrates including glass and organic materials to support emerging architectures like FOPLP and TGV.

IN DEPTH

Key Findings

Sikama International has announced a next-generation reflow platform designed for advanced semiconductor and panel-level packaging. Building upon the existing UP1200 technology, which supports 310 × 310 mm panels, the new platform is engineered to accommodate larger formats and a diverse range of substrate materials, including silicon, ceramic, organic, and glass.

Technical Specifications

The platform is being developed to meet specific performance targets critical for next-generation packaging:

- Temperature uniformity of ±2°C across the panel substrate.
- Process atmosphere control with oxygen levels below 10 ppm O_2.
- Vibration levels 10x lower than conventional competitive reflow solutions.
- Power consumption reduced by 50% compared to competitive models.
- Support for high thermal-mass processing and precise control over heating, cooling, and thermal profiles.

Background and Context

The shift toward larger square and rectangular panels is driving new thermal processing requirements. Specifically, technologies such as Fan-Out Panel-Level Packaging (FOPLP), Chip-on-Panel-on-Substrate (CoPoS), glass core substrates, and Through-Glass Via (TGV) architectures require enhanced mechanical stability and warpage control. While current support exists for 310 × 310 mm formats, the industry roadmap is moving toward larger standardized sizes, including approximately 510 × 515 mm and 600 × 600 mm.

Significance and Outlook

Rather than scaling existing ovens, Sikama is developing a new architecture specifically for these emerging panel-level requirements. This approach focuses on the intersection of thermal efficiency, atmosphere management, and transport technologies to handle increasingly demanding substrates. The company is working directly with customers to align the platform's flexibility with evolving technology roadmaps. Commercial introduction is planned for 2027, with further specifications and the official product name to be released during the development process.

Reference technology guide: Panel-Level Packaging (PLP): https://troy-technical.com/semiconductor-back-end-term-plp/

Reference technology guide: CoPoS: https://troy-technical.com/semiconductor-back-end-term-copos/

Reference technology guide: Fan-Out & Wafer-Level Packaging: https://troy-technical.com/semiconductor-back-end-term-fanout/

Source: https://www.3dincites.com/2026/11/sikama-develops-next-generation-reflow-platform-for-advanced-panel-level-packaging/

Collected: November 21, 2026 | Automated Research System (AI)