SEMICONDUCTOR FRONT-END · PART 2-4

Wafers Beyond Silicon
Growing crystals that resist the usual rules

Silicon can be melted and pulled into a large single crystal. Many other useful semiconductor materials are less cooperative. Silicon carbide does not provide a convenient stoichiometric melt under normal growth conditions. Gallium nitride decomposes before ordinary melt growth becomes practical. Gallium arsenide and indium phosphide lose volatile constituents unless the process contains them. This lesson follows the different solutions, explains why larger wafers remain difficult, and connects crystal growth to power electronics, optical communications and the raw-material supply chain.

Semiconductor Front-End Series · Part 2-4 · Intermediate introduction · Helpful background: Lessons 1-2 and 2-1 · English edition prepared 7 November 2026

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How to read this lesson

Begin with the main text. The shaded physics boxes add optional detail and worked estimates. Figures are conceptual and not to scale. Numbered links lead to the supporting sources.

What you will learn

- Explain why each material needs a different growth strategy rather than a simple copy of silicon's CZ process.
- Describe the principles and limitations of SiC vapour growth, GaAs/InP melt growth and three routes towards bulk GaN substrates.
- Distinguish a commercial wafer from a sample or demonstration, and raw-material production share from wafer-market share.

1. Three ideas to keep in mind

- **The material's phase behaviour sets the problem.** Some compounds decompose; others lose a volatile element. A usable growth process must preserve the required composition as well as the crystal structure.
- **There is no single replacement for silicon's growth method.** SiC can grow by vapour transport; GaAs and InP use carefully contained melts; GaN can grow from vapour, supercritical ammonia or a flux solution. Growth rate, diameter and defects must be controlled together.
- **Technical progress and commercial availability are different measures.** A larger experimental wafer does not establish high-volume supply. Prices, capital investment, customer qualification and concentrated raw-material production all influence what can actually reach a device factory.

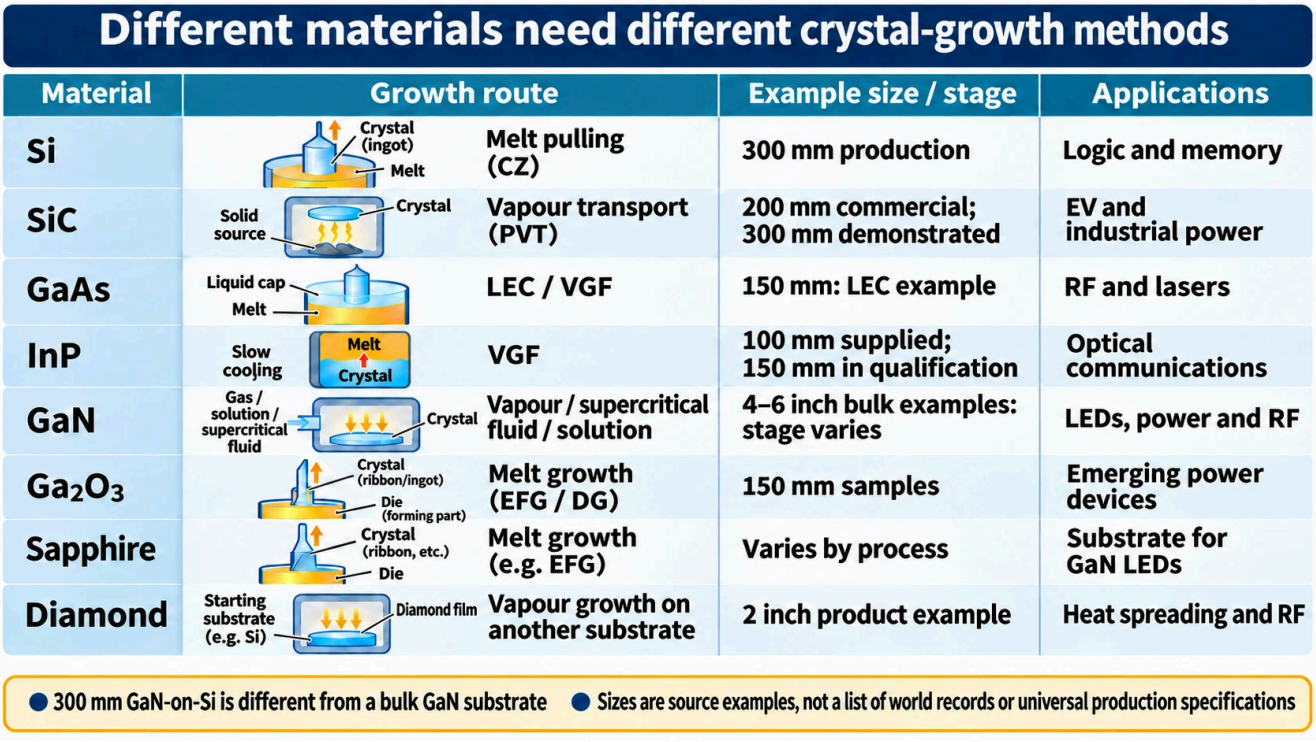


Figure 1 **A map of materials, growth routes and development stages** (schematic)

Reading the figure: size does not establish production readiness

A supplied product, a customer-qualification wafer, a sample and a research demonstration can have the same diameter but very different commercial significance. A 300 mm GaN-on-Si wafer is silicon carrying a GaN film; it is not a 300 mm bulk GaN crystal. The figures below retain the dates and contexts of their sources.

2. How a material melts determines how it can be grown

Silicon melts at about **1,414°C**, and a seed can guide crystallisation as a boule is pulled from the liquid. A compound containing two elements may behave differently: heating need not produce a liquid of the same composition. One constituent may escape into the gas phase, or the solid may decompose before a useful melt is obtained Explanation .

Keeping the composition, not just controlling temperature

Melting ice gives liquid water without changing its chemical formula. For a compound semiconductor, a volatile constituent can leave the heated material and change what remains. A temperature profile that works perfectly for silicon is therefore not enough.

Material	Growth challenge	Representative response
SiC	No stoichiometric Si:C = 1:1 liquid at atmospheric pressure in the cited description [1]	Vapour transport to a seed
GaN	Decomposes under ordinary-pressure conditions rather than providing a convenient melt [10]	Vapour, supercritical-fluid or solution growth
GaAs and InP	High arsenic or phosphorus vapour pressure [6]	Encapsulation, pressure and controlled solidification
β-Ga_2O_3	Can be melt-grown, but requires temperatures around 1,800°C [15]	EFG and alternative melt-feeding methods
Sapphire, Al_2O_3	Melting point about 2,053°C [17]	High-temperature melt growth

A NIST thermodynamic assessment calculated conditions for GaN melting at roughly **4.9 GPa of nitrogen pressure**, about 50,000 atmospheres [10]. High-pressure phase behaviour is a research question; other work has discussed decomposition even at very high pressure. The practical conclusion here is narrower: ordinary silicon-style melt pulling is not a convenient industrial route for bulk GaN Explanation .

Those differences help explain why substrate cost and available diameter vary so widely between materials.

3. Silicon carbide: move material through the vapour

- **PVT growth inside a graphite crucible**

A widely used route for SiC is **physical vapour transport, PVT**, also called seeded sublimation or the modified Lely method. A graphite crucible contains SiC source powder and a SiC seed. The source region is slightly hotter, within a representative **2,000–2,500°C** range [1].

The source produces vapour species including **Si_2C, SiC_2 and Si**. Material reaches the cooler seed region and is incorporated into the growing crystal. The cited process uses reduced-pressure argon, with nitrogen added when n-type material is required [1] Reported . The gas does not consist only of intact SiC molecules, and there is no bulk SiC melt being pulled upwards.

Slow growth changes the economics

An ICSCRM 2024 presentation describes commercial sublimation growth at approximately **0.2–0.4 mm per hour** [2]. Mitsubishi Electric also identifies slow growth and residual dislocations as important challenges relative to silicon [1].

DISCO illustrates wafer extraction from a **150 mm diameter, 20 mm thick** SiC ingot [7]. Growing 20 mm at 0.2–0.4 mm/h would take **about 50–100 hours** Calculation . That covers growth alone; heating, cooling and wafer processing add time. Even a relatively short boule can therefore tie up a growth system for days.



According to its Commons description, the grown silicon carbide crystal has been rounded for wafer processing, with a flat on part of the side. It is a short ingot rather than the long silicon boule familiar from CZ growth.
Photo: LaMèreVeille / Wikimedia Commons / CC BY-SA 4.0. Existing article image retained.

The right composition can still produce the wrong stacking sequence

SiC has several **polytypes**: the chemistry is the same, but the atomic layers follow different repeating sequences. Familiar examples are **3C, 4H and 6H**. Small energy differences make competing stacking arrangements possible, and growth conditions influence which form appears. Mitsubishi Electric describes commercial power-device substrates as predominantly **n-type 4H-SiC** [3] Reported .

A usable boule therefore requires more than a supply of silicon and carbon. The process must maintain the intended stacking sequence as the crystal grows Explanation .

Defects can affect devices long after growth

Mitsubishi Electric's defect discussion gives examples of **1–10 micropipes/cm²** and dislocation densities around **10^3–10^4/cm²** [4]. A micropipe is a hollow-core defect associated with a large screw dislocation. These are examples from the cited material, not current specifications or best achievable values for every supplier. Diameter, defect category and product grade all matter.

How a defect can expand when a device carries current

A **basal-plane dislocation, BPD**, can be associated with partial dislocations bounding a stacking fault. The cited explanation follows this sequence [4]:

1. A substrate defect can propagate into the epitaxial layer, including the voltage-supporting drift region.
2. Bipolar conduction supplies both electrons and holes, which can recombine at relevant defects.
3. Recombination releases energy that assists partial-dislocation motion and stacking-fault expansion.
4. The expanded fault can impede conduction and increase resistance.

The concern is not that every electric current makes every defect grow. The mechanism involves the relevant defects and carrier injection. Suitable **buffer layers** and epitaxial process design can greatly reduce BPDs entering the drift region [4]. A substrate defect can thus become a later reliability problem, making growth quality part of device engineering Explanation .

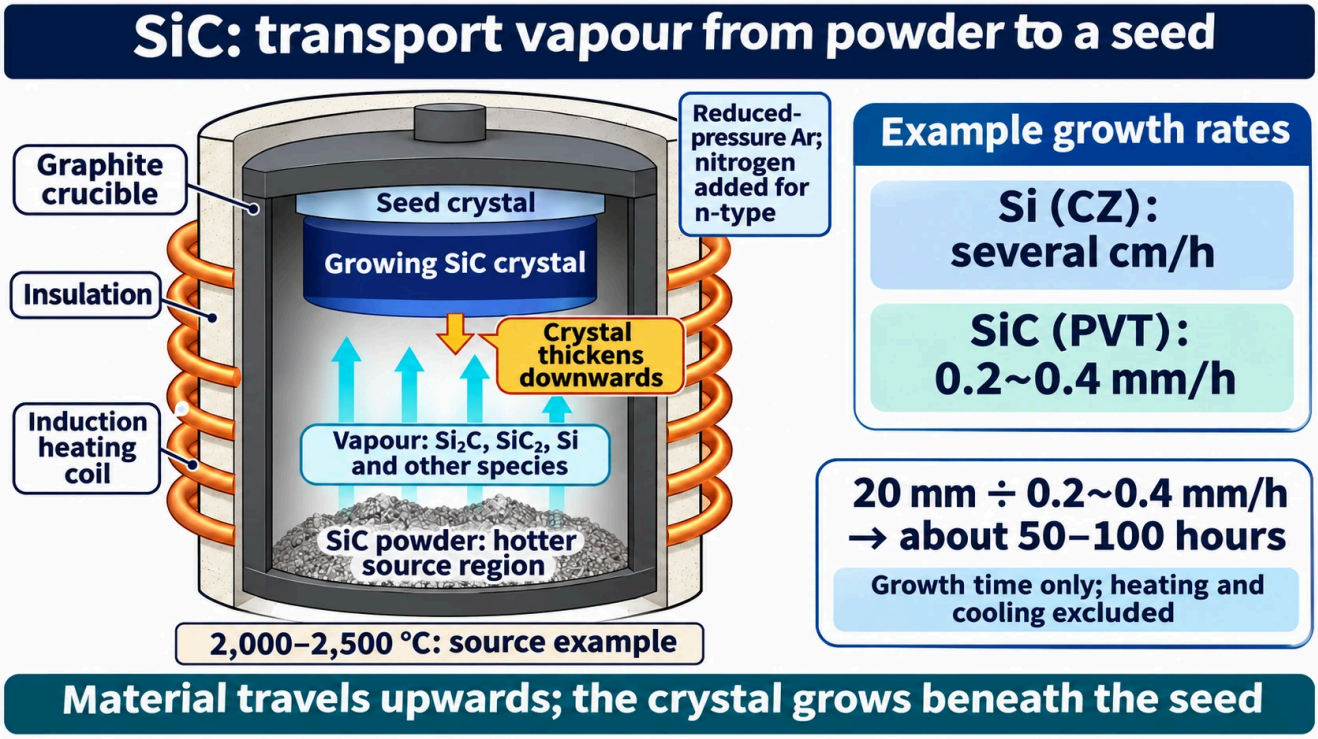


Figure 2 **Source vapour travels upwards; the SiC crystal thickens below the seed** (schematic)

Reading the figure

Blue arrows show material transport, while the short amber arrow marks the direction in which the crystal becomes thicker. These are different directions. The 50–100 hour estimate excludes heating and cooling, and the growth-rate comparison is illustrative rather than a scale drawing.

Hardness makes wafer extraction difficult too

SiC is hard enough to be used as an abrasive, which makes slicing and finishing demanding [5]. In DISCO's **150 mm diameter, 20 mm thick ingot / 350 µm wafer** example, conventional wire sawing takes around **3.1 hours per wafer**, or roughly **100 hours per ingot**, and loses about **180 µm per wafer** as kerf. The company identifies these as general values based on user interviews [7].

Laser-assisted separation creates a modified layer at the required depth and uses it to release a wafer. DISCO reports approximately **10 minutes per wafer**, around **80 µm material loss**, and about **1.4 times as many wafers from an ingot** for its example [7] Reported . These are supplier-specific comparisons under the stated assumptions, not guaranteed results for every material and tool.

Solution growth offers another route

SiC can also grow from a solvent. Adding metals such as titanium or chromium to a silicon melt helps dissolve carbon; SiC then crystallises on a seed. Mitsubishi Electric discusses examples at **1,500–2,000°C**, with rates of **several hundred micrometres per hour**. A benefit is that some dislocations can bend sideways and exit through the crystal's side surfaces. Faster growth and longer crystals remain development challenges [1].

This is **solution growth**, not evidence that a convenient stoichiometric SiC melt has become available at atmospheric pressure.

Prices, larger diameters and manufacturing capacity

The Japanese source describes a volatile market using dated reports:

- **TrendForce's 2024 estimate**, reported by Semiconductor Today, puts n-type SiC substrate revenue at **US$1.04 billion**, down **9%**. Reported supplier shares are **Wolfspeed 33.7%, TanKeBlue 17.3%, SICC 17.1% and Coherent 13.9%**. The same account forecasts 200 mm substrates exceeding 20% of shipments in 2030 [21]. These are market-research estimates and a forecast.
- **SemiMedia's October 2024 reporting** describes Chinese 150 mm substrate prices falling below **US$500** around mid-2024, with some overseas quotes as high as **US$850** [22]. These are historical price reports, not current quotations.
- **Wolfspeed** announced completion of its restructuring in **September 2025**, with debt reduced by about **70%** and an emphasis on installed 200 mm capacity [23]. It announced commercial availability of a 200 mm materials portfolio that month [24], and a **300 mm single-crystal SiC wafer demonstration in January 2026** [25].
- **Coherent's 300 mm SiC development**, reported in **December 2025**, included plans related to heat spreading in AI data centres [26]. A thermal-management substrate application should not be confused with qualification for power-device fabrication.

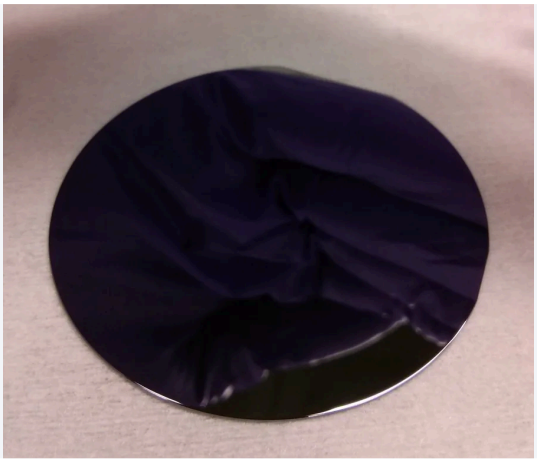
As Lesson 1-2 explained, SiC power devices can reduce conversion losses in EV inverters. Larger, less expensive substrates can help adoption, but price competition does not remove the difficulties of slow growth, defects and hard-material processing Explanation .

4. GaAs and InP: contain the volatile constituent

LEC: a liquid cap over the melt

Gallium arsenide, GaAs, can be melt-grown, but arsenic loss must be controlled. **Liquid encapsulated Czochralski, LEC**, covers the melt with liquid **boron oxide, B_2O_3**, inside a pressurised vessel. The encapsulant and atmosphere help retain composition [6].

Freiberger describes counter-rotation of seed and crucible, pressures above **0.2 MPa**, pulling rates of **5–10 mm/h** and GaAs diameters up to **150 mm** [6] Reported . These are its published process examples. The liquid cap is not a rigid lid that prevents the crystal moving: the crystal passes through it as it is pulled.



The Commons description identifies a single-crystal GaAs wafer with a (100) surface orientation. The purple reflection comes from the holder's nitrile glove, not necessarily the wafer material itself.
Photo: La2O3 / Wikimedia Commons / CC BY-SA 3.0. Existing article image retained.

VGF: solidify within the crucible

In **vertical gradient freeze, VGF**, pre-synthesised material is melted in a **pyrolytic boron nitride, pBN**, crucible. Solidification begins at a seed near the bottom, and the solid–liquid interface moves upwards as the thermal field is controlled. The crystal is not pulled out of the melt.

Freiberger describes an axial temperature gradient typically below **5 K/cm**, supporting low dislocation density [6]. AXT also uses proprietary VGF processes for **InP, GaAs and germanium** [8]. A gentle gradient reduces thermal stress, but maintaining the required interface shape and growth conditions still requires careful control Explanation .

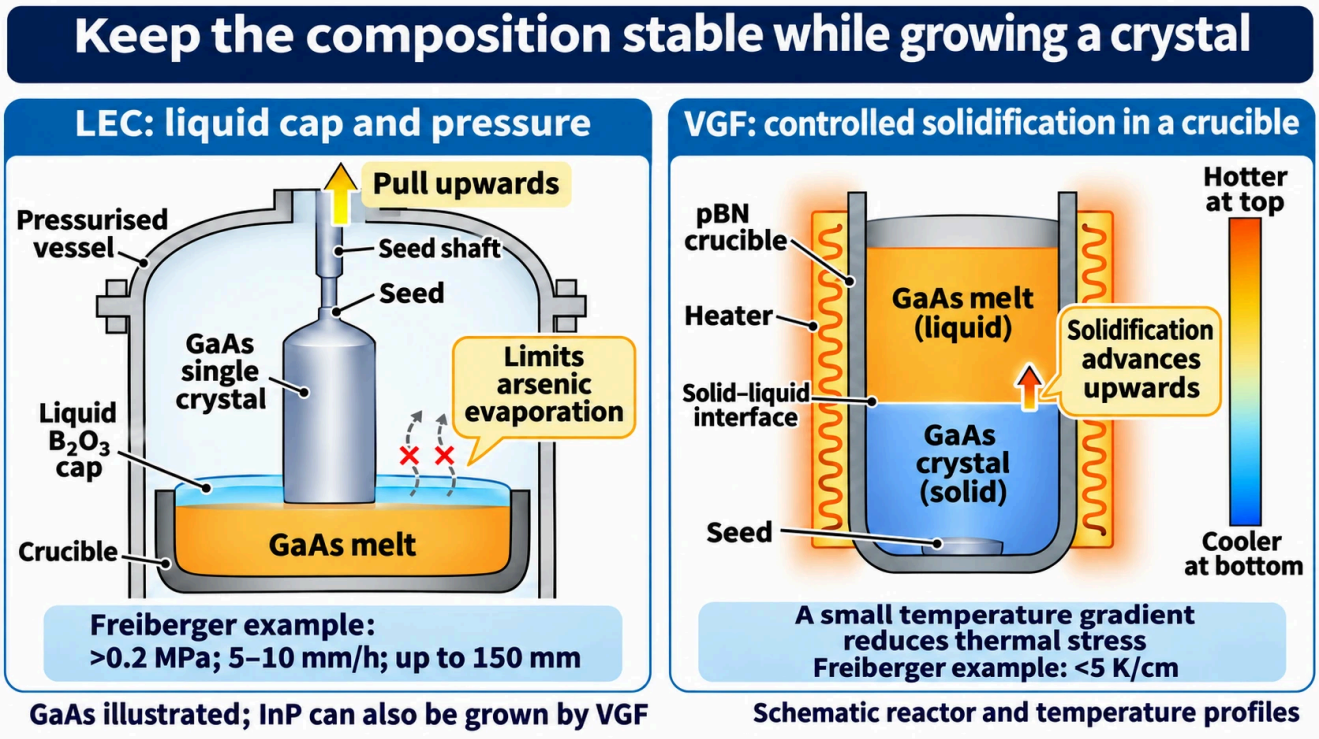


Figure 3 **LEC pulls a crystal; VGF freezes the melt in place** (schematic)

Reading the figure

Both methods manage composition and heat flow. In LEC, the liquid encapsulant limits arsenic loss during pulling. In VGF, a controlled temperature profile guides solidification inside the crucible. The apparatus and temperature profiles are schematic.

InP and the problem of twinning

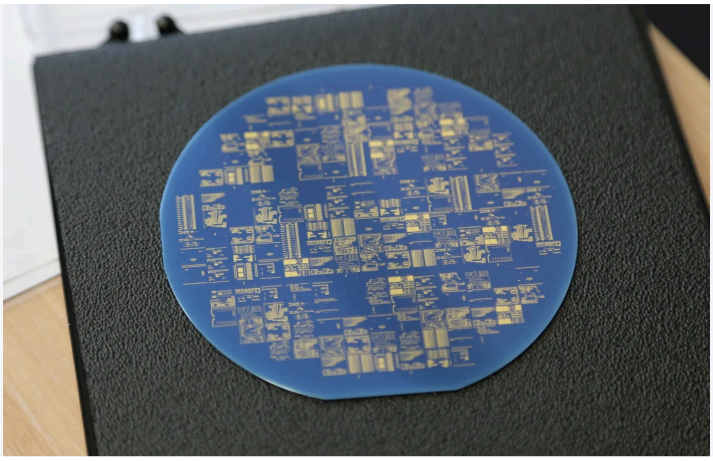
Indium phosphide, InP, is important for optical transmitters and detectors. Freiberger states that it uses VGF for InP to obtain high structural quality, and describes high-pressure synthesis to handle phosphorus vapour pressure [6].

A **twin** is a region in which crystal orientation changes across a boundary into a mirror-related arrangement. A US Air Force patent explains InP's tendency to twin in terms of low stacking-fault energy, sensitivity to interface geometry and disturbed melt convection [9]. Low stacking-fault energy makes some alternative stacking arrangements relatively inexpensive energetically. Maintaining a single crystal without unwanted twins can therefore constrain yield Explanation .

Optical communications put pressure on supply

AXT's **2025 annual filing** lists supplied InP diameters of **2, 3 and 4 inches**, with **6-inch material in prototype and customer qualification**. It describes a concentrated market with three principal suppliers, including AXT, and links demand to high-speed optical transmission in AI-related data-centre infrastructure [8]. These are the company's descriptions of its market and product stages.

In **June 2026**, **JX Advanced Metals** announced plans to invest up to **¥120 billion over four years**, aiming for InP substrate capacity **7–10 times fiscal-2025 levels** [27]. That is an investment plan, not already completed capacity.



Multiple chip designs share the wafer in a multi-project run, according to its Commons description. Patterned optical circuits and interconnect features are visible.
Photo: JonathanMarks / Wikimedia Commons / CC BY-SA 4.0. Existing article image retained.

AXT's December 2025 prospectus supplement states that China added InP substrates to export controls on **4 February 2025**, and that its Chinese subsidiary's GaAs, InP and germanium substrates require export licences [31]. This is a dated description of the company's regulatory exposure, separate from the raw-metal production statistics later in this lesson.

5. GaN: three routes to a bulk substrate, plus GaN on silicon

At ordinary pressure, GaN does not offer a convenient melt-growth route [10]. It is essential to distinguish **a GaN substrate** from **a different substrate carrying a GaN film**.

HVPE: grow thick, then separate

One route starts on another material, grows a thick GaN layer and separates it to obtain a **free-standing GaN substrate**. **Hydride vapour phase epitaxy, HVPE**, is used for rapid thick growth. A Hitachi Cable patent discusses substrate separation and the defect problems caused by mismatch with the starting material [11].

The foreign substrate provides a starting platform, but its lattice does not perfectly match GaN. Growth and separation must therefore manage defects and stress, rather than simply adding enough thickness Explanation .

Ammonothermal: crystallise from supercritical ammonia

The **ammonothermal** method uses high-pressure ammonia as a solvent, in an approach related conceptually to hydrothermal crystal growth. Nutrient dissolves in **supercritical ammonia** and material crystallises on a seed.

A NEDO announcement from **2021** describes a lower-pressure acidic ammonothermal process developed by Japan Steel Works, Mitsubishi Chemical and partners, operating around **100 MPa**, roughly half the pressure of the compared conventional approach. A demonstration facility confirmed **4-inch GaN crystal growth** [12]. This is a dated growth demonstration, not a statement that every such diameter is now a standard mass-produced substrate.

Sodium flux: use a liquid solvent

The **Na-flux method** dissolves nitrogen into a sodium–gallium solution and precipitates GaN. A **2022** Osaka University-led report describes approximately **850°C and 40 atmospheres**, using multiple seed points on sapphire to obtain a **6-inch crystal**. It reports separation from the sapphire on cooling to room temperature [13]. Again, this is a research example with its own process conditions.

GaN on Si: use silicon as the mechanical platform

Instead of making a bulk GaN substrate, engineers can grow GaN films on silicon. **Infineon's 2024 announcement** describes **300 mm power GaN technology** using existing silicon-manufacturing equipment. The company gives **2.3 times the chip count per wafer** compared with 200 mm [14]. That is a process-development announcement and a supplier's comparison, not a 300 mm bulk GaN crystal.

Lattice mismatch and thermal expansion mismatch create stress. On cooling, GaN generally wants to contract more than silicon. Being attached to the silicon prevents free contraction and can leave the GaN film under **tensile stress**, contributing to cracking [32]. Actual bow also depends on stresses introduced during growth and on the complete layer stack. Buffer-layer design and substrate thickness help manage these effects [16] Explanation .

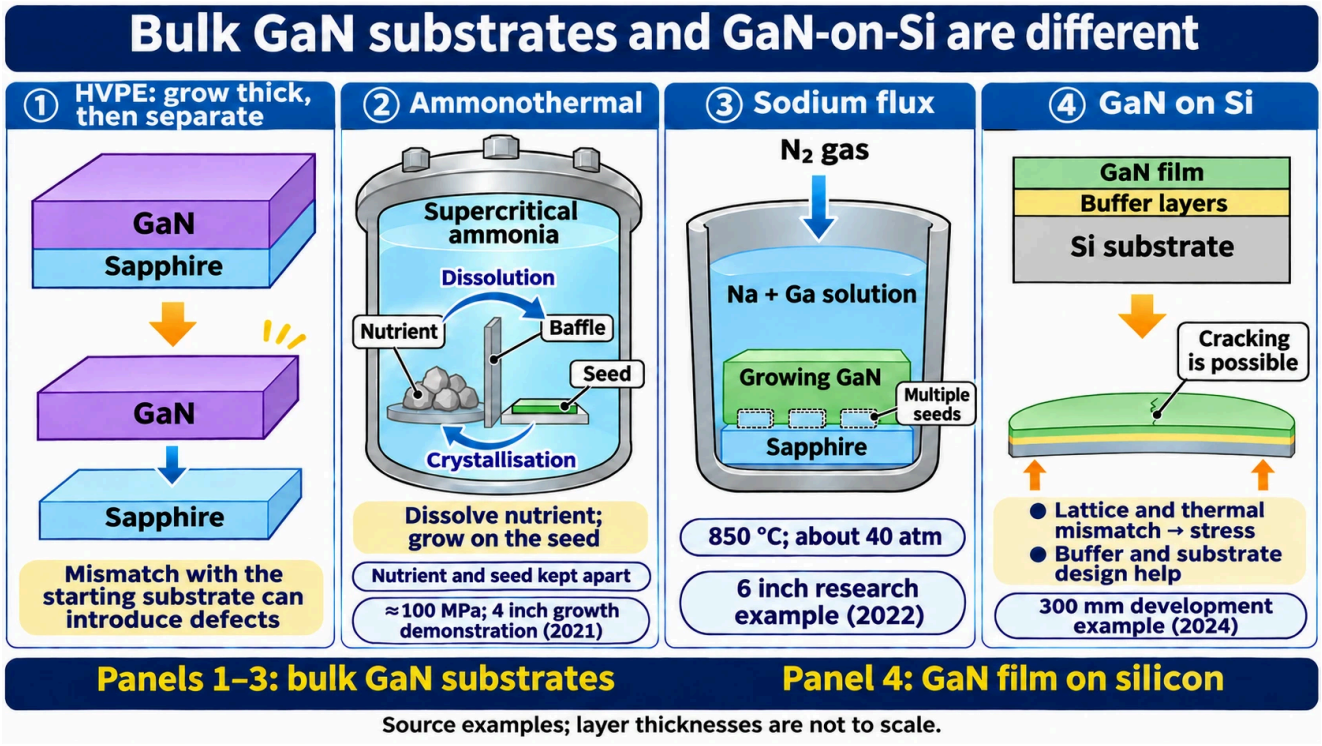


Figure 4 **Bulk GaN and GaN-on-Si solve different substrate problems** (schematic)

Reading the figure

The ammonia vessel separates nutrient and seed; it does not prescribe one universal arrangement of hot and cold zones. In GaN-on-Si, silicon remains the mechanical base. All quoted sizes and conditions are dated source examples, and the film thicknesses are exaggerated.

6. Other substrates: gallium oxide, AlN, diamond and sapphire

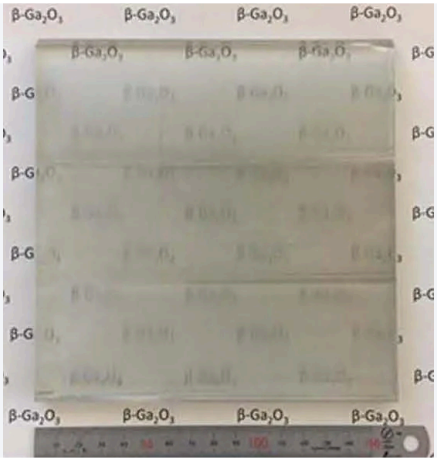
Gallium oxide: a wide-bandgap material that can be melt-grown

β-Ga_2O_3 has a wider bandgap than SiC or GaN and is being developed for power devices [18]. A notable manufacturing advantage is that crystals can be grown from a melt. A wide bandgap alone does not settle device performance or manufacturability; growth, defects, heat removal and device integration still matter Explanation .

Japan's **Novel Crystal Technology** has used **edge-defined film-fed growth, EFG**, since **2015**. Melt rises through a die and supplies the growing shaped crystal. At temperatures around **1,800°C**, the process has used costly **iridium crucibles**, making materials cost an important constraint [15].

A **December 2025 NEDO/company announcement** describes **DG growth**, feeding melt as droplets to the growing crystal. It reports a **95 mm crystal without an iridium crucible** and estimates substrate manufacturing cost at **one tenth of the compared conventional process** [15]. That is a development result and cost estimate, not a demonstrated universal cost for all future products.

March 2026 trade reporting describes the start of **150 mm EFG substrate sample shipments**, plans for **2027 epitaxial samples**, introduction of DG in full-scale production in **2029**, and a **200 mm development goal for 2035** [18]. These stages and dates should remain distinct. Melt growth may offer scale and productivity opportunities relative to SiC sublimation, but that potential is not a guaranteed commercial outcome Interpretation .

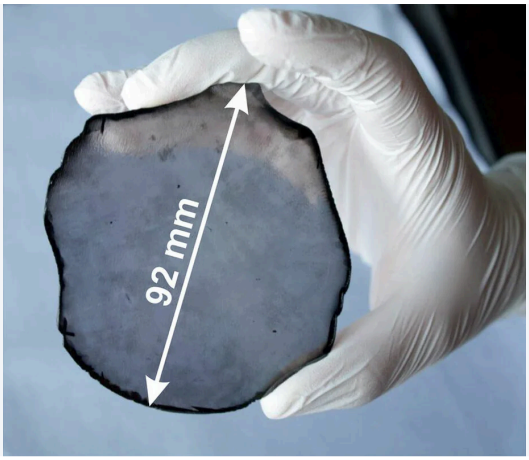


This transparent crystal is shown above a ruler in a published research figure, according to its Commons description. It illustrates the material rather than the specific product discussed above.
Image: Michael A. Mastro et al. / Wikimedia Commons / CC BY 4.0. Existing article image retained.

Aluminium nitride and diamond

AlN substrates support applications including deep-ultraviolet LEDs. **Crystal IS and Asahi Kasei announced a 4-inch AlN substrate in 2023**, alongside production of thousands of 2-inch substrates annually [19]. The demonstration diameter and established production volume are different claims.

Diamond is attractive for heat spreading and potential high-frequency semiconductor applications. **Orbray** describes growing diamond on slightly misoriented sapphire using **step-flow growth**, offers a **2-inch product example**, and discusses growth taking **more than a week**, with 4 inches as a next target [20]. A diamond heat-spreader product is not automatically equivalent to a fully qualified electronic-device substrate Explanation .



The Commons description identifies an unpolished heteroepitaxial disc, **92 mm in diameter and about 1.6 mm thick**, grown on a silicon-based substrate stack including iridium. This is work by a different research group, not an Orbray product photograph.
Image: Matthias Schreck, Stefan Gsell, Rosaria Brescia and Martin Fischer / Wikimedia Commons / CC BY-SA 4.0. Existing article image retained.

Sapphire: an important platform without being a semiconductor itself

Many blue and white LEDs begin with GaN grown on sapphire. **Sapphire is single-crystal aluminium oxide**, an insulating substrate material, rather than a semiconductor in the same sense as GaN. Kyocera lists its melting point as **2,053°C** and describes EFG production [17].



The Commons description identifies a **35 kg** synthetic sapphire crystal. Kyropoulos growth is a different melt-growth method from Kyocera's EFG example.
Photo: LaMèreVeille / Wikimedia Commons / CC BY-SA 4.0. Existing article image retained.

7. Raw materials: a different kind of concentration

Gallium and indium statistics describe different production stages

USGS's **Mineral Commodity Summaries 2026** estimates that China accounted for **99% of low-purity primary gallium production in 2025**, with worldwide output around **900 tonnes** [28]. Its indium chapter gives China about **70% of refinery production in 2025** [29].

Those are not shares of finished semiconductor wafers. High-purity refining, compound synthesis, crystal growth and wafer processing are separate stages. A country can dominate one stage without holding the same percentage at every later stage Explanation .

Gallium is recovered mainly as a by-product associated with alumina production, while indium is associated particularly with zinc processing. Output depends on recovery investment and the wider refining chain as well as semiconductor demand. Neither supply can necessarily expand immediately just because wafer demand rises.

Export licensing and destination-specific measures are separate issues

The Japanese source describes gallium export licensing introduced in **August 2023**, followed by US-specific measures in **December 2024** [28]. China's **MOFCOM Announcement No. 72 of 2025**, dated **9 November 2025**, states that paragraph 2 of Announcement No. 46 of 2024 is suspended through **27 November 2026** [30].

That statement concerns the specified destination-related measures. It does **not** mean that the broader export-licensing system was abolished. The notice's text was checked for this English edition on **7 November 2026**; readers making an actual shipment need the rules applying to its item, destination and date. The indium chapter also describes export controls introduced in **February 2025** [29].



The Commons description gives a purity of **99.999%**. Gallium supplies compounds such as GaAs, GaN and gallium oxide; it does not by itself constitute any of those wafers.
Photo: en:user:foobar / Wikimedia Commons / CC BY-SA 3.0. Existing article image retained.



A **40 g** indium ingot, according to its Commons description. Indium is one of the source elements used to make InP.
Photo: Hi-Res Images of Chemical Elements / Wikimedia Commons / CC BY 3.0. Existing article image retained.

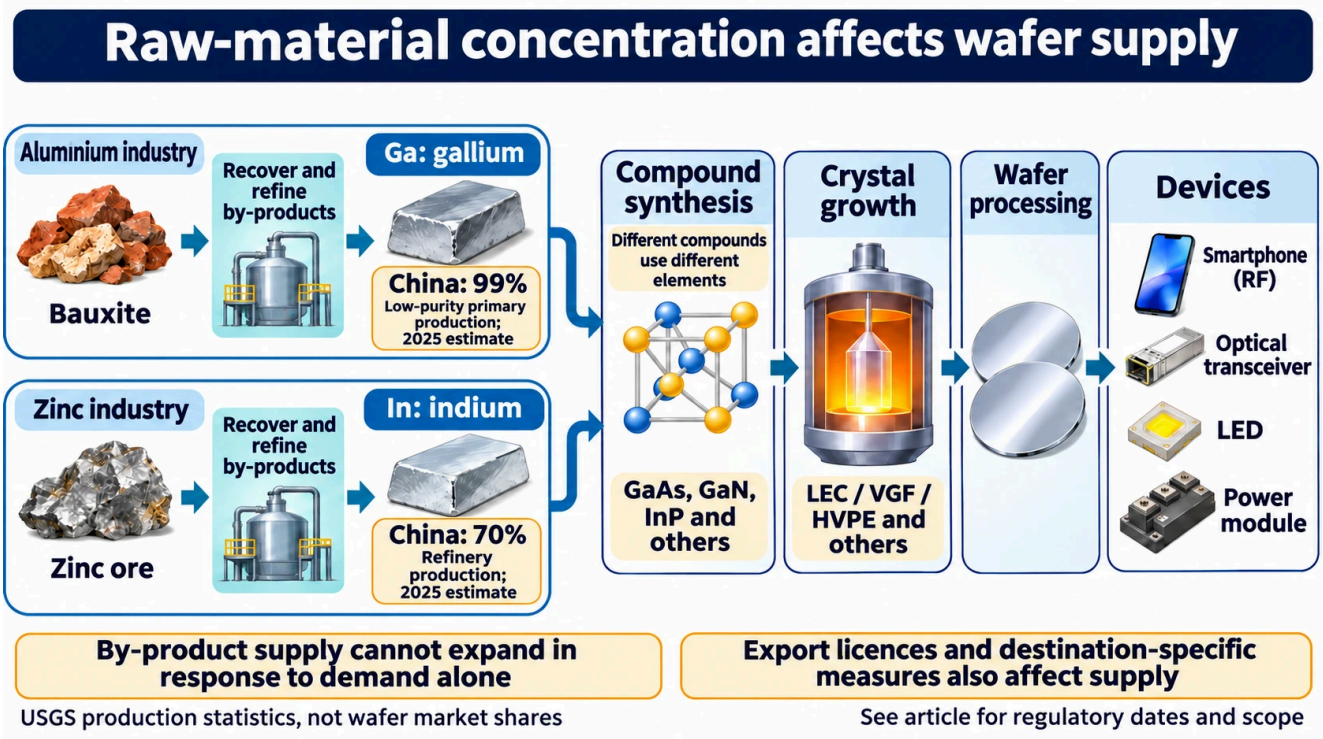


Figure 5 **From by-product recovery to a finished device** (schematic)

Reading the figure

The 99% and 70% figures refer to different USGS production categories for 2025. Gallium goes into compounds such as GaAs or GaN; indium goes into InP and other materials. The arrows do not mean that every wafer combines gallium and indium, or that those elements are used to make SiC.

8. Comparing the routes and completing Part 2

Material	Growth route	Dated size / stage example	Main difficulty or distinction
Silicon	CZ melt pulling	300 mm production	Reference case from Lesson 2-1
SiC	PVT; solution-growth alternatives	200 mm commercial; 300 mm demonstrated	Slow growth, polytypes, defects and hard-material processing
GaAs	LEC or VGF	150 mm LEC example	Contain arsenic; control stress and defects
InP	VGF in the cited supplier examples	100 mm supplied; 150 mm in qualification at AXT	Phosphorus volatility, twinning and qualification
Bulk GaN	HVPE, ammonothermal or sodium flux	4-inch demonstration, 2021; 6-inch research, 2022	Avoid ordinary melt growth; manage defects and separation
GaN on Si	GaN epitaxy on a silicon platform	300 mm development example, 2024	Not a bulk GaN substrate; lattice and thermal stress
β-Ga_2O_3	EFG; DG under development	150 mm samples; 95 mm DG demonstration	High-temperature equipment and crucible economics
Diamond	Vapour growth on another substrate	Orbray 2-inch product example	Long growth time and application-specific quality

Part 2 has followed silicon from raw materials to crystals, polished wafers, epitaxy and bonded structures, then examined the substrate industry and the alternatives to silicon. The common lesson is that a mirror-like disc can conceal a long chain of chemical, thermal and mechanical constraints.

Part 3 begins with **3-1: Cleaning**. From there, we follow the processes that create transistors and interconnects on the prepared wafer surface.

9. Check your understanding

1. Why is ordinary silicon-style melt pulling not used for SiC?

   ▼ Show answer

   Under the cited atmospheric-pressure conditions, SiC does not provide a stoichiometric 1:1 Si:C liquid. Seeded sublimation instead transports material through vapour from a hotter source to a cooler growth region. Solution growth uses a solvent and is a different route.

2. How long does 20 mm of growth take at 0.2–0.4 mm/h?

   ▼ Show answer

   About 50–100 hours: 20/0.4 = 50 and 20/0.2 = 100. This counts growth time only, excluding heating, cooling and wafer processing.

3. How can basal-plane defects increase resistance during SiC device operation?

   ▼ Show answer

   Under relevant bipolar carrier injection, electron–hole recombination can assist partial-dislocation motion and stacking-fault expansion. The expanded fault can impede conduction. Buffer and epitaxial design can reduce propagation into the drift layer.

4. Why cover the GaAs melt with liquid boron oxide in LEC growth?

   ▼ Show answer

   Arsenic has a high vapour pressure and can escape selectively. The liquid encapsulant, together with the pressurised growth environment, helps retain composition while the crystal is pulled through it.

5. Why is twinning a concern in InP?

▼ Show answer

Its low stacking-fault energy makes alternative stacking arrangements relatively easy to form. Interface geometry and melt convection can promote mirror-related regions, reducing the yield of suitable single crystal.

6. Why can GaN-on-Si crack or bow after growth?

▼ Show answer

Lattice and thermal mismatch create stress. On cooling, GaN generally wants to contract more than silicon; attachment constrains it and can leave tensile stress in the film. The full stress history and layer stack also affect bow. Buffers and substrate design help control it.

7. What manufacturing opportunity does gallium oxide offer, and what cost issue does DG address?

▼ Show answer

Gallium oxide can be melt-grown. Conventional high-temperature EFG has used costly iridium crucibles. The cited DG development feeds droplets without an iridium crucible and estimates lower cost; its demonstration, sample and planned production stages must be kept separate.

8. What do the gallium supply statistics and export notice actually describe?

▼ Show answer

The 99% figure is China's share of estimated 2025 low-purity primary gallium production, not finished wafer supply. MOFCOM's 2025 notice suspends a specified paragraph of US-related measures through 27 November 2026; it does not abolish the broader licensing system. By-product recovery also limits how quickly supply responds to demand.

10. Glossary

PVT
Physical vapour transport; source material is transported through vapour to a cooler seeded growth region.

Modified Lely method
Seeded sublimation growth widely used for SiC substrates.

Polytype
A crystal structure with the same composition but a different repeating sequence of atomic layers.

4H-SiC
A hexagonal SiC polytype with a four-layer repeat, widely used for power devices.

Micropipe
A hollow-core defect associated with a large screw dislocation in SiC.

Basal-plane dislocation
A dislocation associated with a basal plane; relevant defects can contribute to stacking-fault expansion under bipolar injection.

Stacking fault
A local interruption in the regular sequence of atomic layers.

Buffer layer
An intermediate layer used to manage defects, mismatch or stress; its function depends on the material system.

Solution growth
Crystallisation from material dissolved in a solvent.

Laser separation
Creating an internal modified layer with a laser to help release a wafer.

LEC
Liquid encapsulated Czochralski growth; a liquid cap and pressurised environment help retain volatile constituents during pulling.

VGF
Vertical gradient freeze; controlled solidification advances through a melt held in a crucible.

pBN
Pyrolytic boron nitride, used for compound-semiconductor growth crucibles.

Twin
A crystal region with a mirror-related orientation across a boundary.

Stacking-fault energy
The energetic cost of a stacking interruption; low values can favour fault or twin formation.

Free-standing substrate
A substrate consisting of the desired material itself, rather than a film supported by a foreign base.

HVPE
Hydride vapour phase epitaxy, used for relatively rapid thick growth of materials such as GaN.

Ammonothermal growth
Crystallisation using supercritical ammonia as the solvent.

Supercritical fluid
A fluid above its critical temperature and pressure, without a distinct liquid–gas boundary.

Sodium-flux growth
Growing GaN from a sodium–gallium solution that incorporates nitrogen.

GaN on Si
A wafer with GaN films on a silicon substrate, usually with buffer layers.

Thermal expansion coefficient
A measure of how dimensions change with temperature.

EFG
Edge-defined film-fed growth; melt rises through a die to feed a shaped growing crystal.

DG
A droplet-fed crystal-growth method described by Novel Crystal Technology.

Iridium
A high-melting-point precious metal used in some high-temperature growth equipment.

Step-flow growth
Growth advancing from surface steps, often introduced through a slight substrate misorientation.

By-product
A material recovered alongside the principal output of another production process.

11. Sources and further reading

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6. **Freiberger Compound Materials** — Technology: LEC and VGF — Read source
7. **DISCO** — KABRA: laser slicing of SiC ingots; Japanese product information — Read source
8. **AXT** — SEC Form 10-K, fiscal 2025: products, diameters, applications and supplier context — Read source
9. **US Air Force** — US5431125A: InP crystal growth and twinning — Read source
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23. **Wolfspeed, 29 September 2025** — Completion of restructuring; SEC Form 8-K exhibit — Read source
24. **Wolfspeed, 10 September 2025** — Commercial launch of 200mm silicon carbide materials portfolio — Read source
25. **Wolfspeed, 13 January 2026** — Wolfspeed Achieves 300mm Silicon Carbide Technology Breakthrough — Read source
26. **Semiconductor Today, 4 December 2025** — Coherent develops 300mm silicon carbide — Read source
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28. **USGS** — Mineral Commodity Summaries 2026: Gallium — Read source
29. **USGS** — Mineral Commodity Summaries 2026: Indium — Read source
30. **China's Ministry of Commerce, 9 November 2025** — Announcement No. 72 of 2025: suspension of paragraph 2 of Announcement No. 46 of 2024; original Chinese notice — Read source
31. **AXT, 29 December 2025** — SEC prospectus supplement 424B5: Chinese export controls, including InP substrates added on 4 February 2025 — Read source
32. **M. Suzuki et al.** — Mechanism of stress control for GaN growth on Si using AlN interlayers, Journal of Crystal Growth 464, 148–152, 2017 — Read source

12. Claim-to-source notes

Claim group	Basis and scope	Type
SiC phase constraint, PVT conditions, species, atmosphere and solution growth	Mitsubishi Electric [1]; representative processes and conditions	Reported
PVT growth rate of 0.2–0.4 mm/h	ICSCRM 2024 presentation [2]	Reported
Polytypes and n-type 4H power-device substrates	Mitsubishi Electric [3]	Reported
Micropipe/dislocation examples, BPD-related stacking-fault growth and buffers	Mitsubishi Electric [4]; defect values are source examples, not current universal specifications	Reported
Hard-material processing and laser-modified separation layer	Mitsubishi Electric [5]	Reported
LEC cap/pressure/rate, VGF gradient and InP growth choices	Freiberger [6]; supplier-specific examples	Reported
SiC ingot dimensions, wire/laser time and material-loss comparison	DISCO [7]; vendor example based partly on user interviews	Reported
AXT diameters, qualification stages and market description	AXT Form 10-K [8]; company description	Reported
InP substrate export controls and subsidiary exposure	AXT prospectus [31]; dated filing, not a universal shipping determination	Reported
InP twinning, stacking-fault energy and interface/convection issues	Patent [9]	Reported
GaN decomposition and calculated high-pressure melting condition	NIST assessment [10]; phase behaviour is not a production recipe	Reported
Foreign-substrate GaN and separation-related defect issues	Hitachi Cable patent [11]	Reported
Ammonothermal 100 MPa, four-inch growth	NEDO 2021 [12]; demonstration	Reported
Sodium-flux conditions and six-inch research example	JST 2022 [13]	Reported
300 mm GaN-on-Si and chip-count comparison	Infineon 2024 [14]; development announcement, not bulk GaN	Reported
GaN/Si thermal mismatch and stress control	Research paper [32] and Okmetic [16]	Reported
Gallium oxide melt growth, EFG/DG, 95 mm result and cost estimate	NEDO/company announcement [15]; development and estimated economics	Reported
Gallium oxide samples and future diameter/production plans	EE Times Japan [18]; trade reporting with dated stages	Reported
Sapphire melting point and EFG	Kyocera [17]; photograph depicts a different growth method	Reported
Four-inch AlN and established two-inch output	Asahi Kasei / Crystal IS [19]; separate claims	Reported
Diamond step-flow method, product size, growth time and next target	Orbray [20]; research photograph is not an Orbray product	Reported
SiC revenue, supplier shares and 2030 diameter forecast	TrendForce figures reported by Semiconductor Today [21]; estimates/forecast	Reported
Historical SiC prices	SemiMedia [22]; 2024 reporting, not current quotations	Reported
Wolfspeed restructuring, 200 mm launch and 300 mm demonstration	Corporate releases [23][24][25]; dates and stages retained	Reported

Claim group	Basis and scope	Type
Coherent 300 mm development and heat-spreading context	Semiconductor Today [26]; trade reporting	Reported
JX InP capacity and investment target	JX announcement [27]; investment plan	Reported
Gallium and indium production statistics	USGS [28][29]; different production-stage denominators	Reported
Suspension through 27 November 2026	MOFCOM notice [30]; specified paragraph and period only	Reported
20 mm at 0.2–0.4 mm/h gives 50–100 hours	Arithmetic using stated source inputs; heating/cooling excluded	Calculation
Commercial implications of slow growth and possible melt-growth benefits	Interpretation, not a cost guarantee or production forecast	Interpretation
Phase behaviour, stacking, thermal stress, bulk/film distinctions and supply-chain examples	General explanation; diagrams are not quantitative process simulations	Explanation

English edition prepared 7 November 2026 from the Japanese article reviewed on 6 November 2026. The technical content is rewritten for an international readership. Sizes, market figures and corporate milestones retain their source dates; they are examples, not an exhaustive survey of current specifications. Primary sources, research papers, market estimates and trade reporting are distinguished. Calculations and interpretation are labelled separately. The five Image Gen diagrams are schematics, with film thicknesses and particle sizes exaggerated where helpful. Existing photographs retain their individual credits and licences.

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