SEMICONDUCTOR FRONT-END · PART 3-9

High-Aspect-Ratio Etching Reaching the bottom of a very deep hole

A narrow opening is easy to draw on a surface. Keeping it narrow while etching many times deeper is much harder. In 3D NAND memory, a single channel hole passes through a tall stack of films; in other devices, deep features form capacitors, isolation trenches or through-silicon connections. As the feature grows, fewer useful particles reach its bottom, products become harder to remove and small errors in particle direction can distort the walls. This lesson follows those problems into the feature, then explains the Bosch process, cryogenic etching and the international ecosystem behind them.

Semiconductor Front-End Series · Part 3, Lesson 3-9 · Level ★★★
Suggested preparation: Lesson 3-8 · Updated 20 November 2026

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How to read this lesson

Reported identifies information stated in the cited source, including attributed company estimates; Calculation identifies an estimate worked out in this lesson; Outlook marks forecasts and roadmap requirements; Interpretation marks an illustrative judgement. Standard physical explanations are generally untagged. Figures are schematic and not to scale. Numbered links lead to the supporting sources.

What you will learn

- Explain why a continuous insulating charge-storage film can hold local charge at different NAND cell levels.
- Define aspect ratio and connect deep features to 3D NAND, DRAM, TSVs and MEMS.
- Explain how geometry, wall interactions and charging affect delivery to a feature's bottom.
- Distinguish the Bosch process and cryogenic silicon etching from cryogenic dielectric etching for 3D NAND.
- Understand how memory design, equipment, gases and temperature-control materials contribute to the same manufacturing challenge.

1. The idea in three steps

- **Depth divided by width sets the difficulty.** A 5 µm-deep hole only 0.1 µm wide has an aspect ratio of 50:1. Building vertically saves surface area, but makes the bottom increasingly difficult to reach.
- **The bottom does not experience the same conditions as the opening.** Oblique particles hit walls, reactive species can be consumed before arriving, and local charging can slow or deflect ions. Etch rate and profile therefore change as the feature develops.
- **Protection and removal must stay in balance.** The Bosch process alternates silicon etching with polymer protection. Cryogenic approaches use low temperature to change the surface chemistry. For tall NAND stacks, the structure can also be divided into tiers and connected afterwards.

2. Why devices need deep, narrow features

A simple ratio with demanding consequences

For a hole or trench, **aspect ratio, AR, is depth divided by width** [1]. A 40:1 feature is forty times deeper than it is wide. For a circular hole, the width is its diameter. Explanation

The cited teaching materials identify pattern transfer above 40:1 and 60:1 as demanding examples [2][5]. In a 2024 publication, Tokyo Electron described an aspect ratio of 100 as achieved in its cryogenic development and 200 in a single etch as its next objective [18]. These are dated examples and a stated goal, rather than a universal boundary between ordinary and advanced etching. Reported

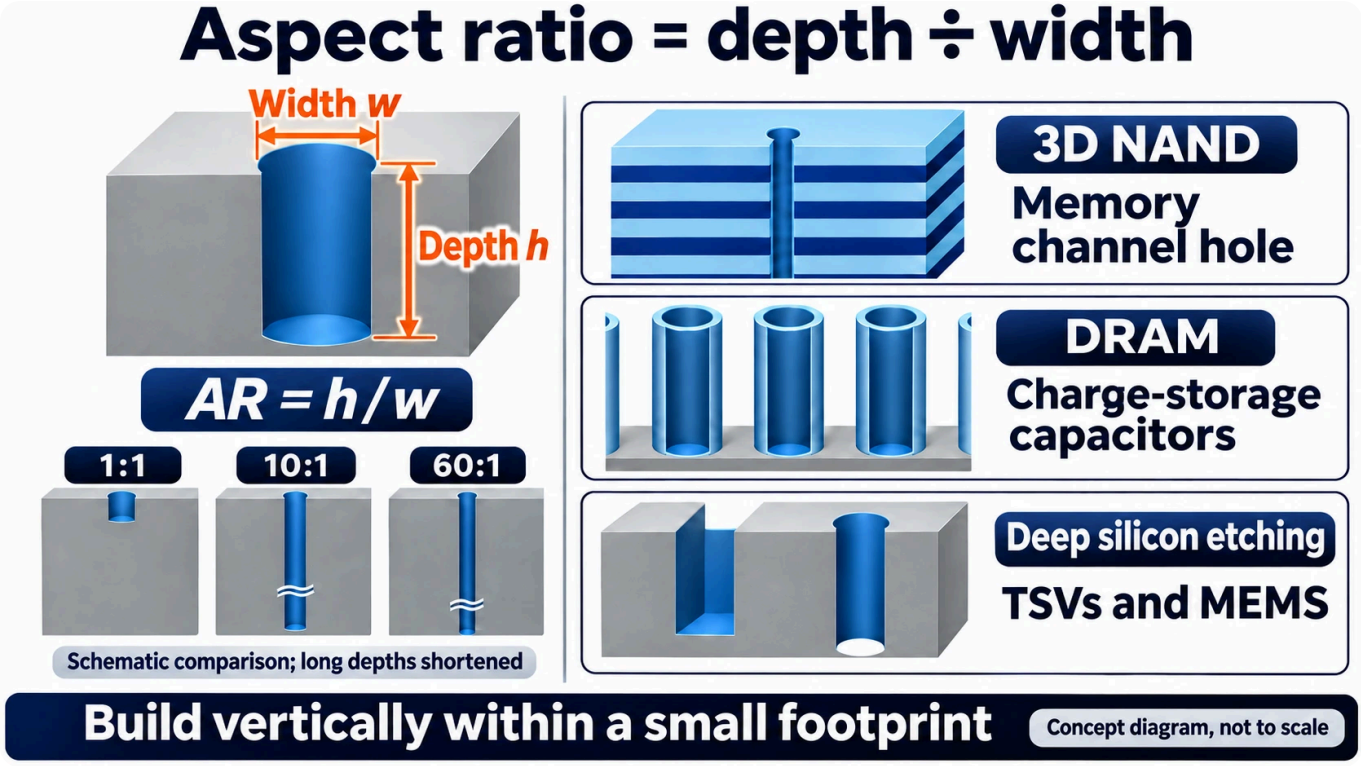


Figure 1 **Aspect ratio and three applications for deep features** (schematic)

Reading the figure

The width w spans the opening; h runs from the original surface to the bottom. The long comparison features are shortened with break marks. The application panels show different functions, not identical materials or fabrication sequences: a NAND channel hole, a DRAM capacitor and a silicon trench or via require different processes [1][11][21].

NAND stores charge, then reads the threshold

NAND flash is the non-volatile memory used in SSDs and phone storage. Its smallest storage element is a memory cell. A cell stores information by changing the charge held in a storage region isolated by dielectric. A sufficiently strong programming field transfers electrons through a thin dielectric into that region. The stored charge can remain after power is removed; erasing uses a different bias condition to reset the state. Exact voltages and erase mechanisms depend on the device. [32]

Reading does not require counting the electrons individually. Stored electrons change the transistor's threshold voltage: the gate voltage needed for appreciable channel conduction. At the same read voltage, a lower-threshold cell conducts more readily than a higher-threshold cell. In a simple single-bit example, those states represent 1 and 0. Modern multilevel cells distinguish more than two threshold ranges, so a drawing with two states is only the starting point. [32]

3D NAND: form many memory levels around one channel

Making planar cells smaller eventually leaves less stored charge and increases interaction between nearby cells. Kioxia, then Toshiba, presented its batch-processing concept in 2007. Its **punch-and-plug** explanation starts with a multilayer stack, etches many holes through it and forms the memory films and vertical semiconductor channels inside. At each gate level, the channel and charge-storage structure create a memory-cell region. [11]

The completed hole is not empty, and it is not a metal rod shorting every gate together. The cited Toshiba description includes a thin, tube-shaped polysilicon channel with an insulating fill at its centre. Around that channel are the films needed for charge storage and gate control. The radial order, moving from a wordline towards the centre, is:

1. Blocking dielectric.
2. Silicon-nitride charge-storage material.
3. Thin tunnel dielectric.
4. Polysilicon channel.
5. Insulating core. [13]

A continuous film need not behave like a conducting wire

In this charge-trap example, the nitride film runs continuously along the hole. It is not cut into a separate physical box for each gate level. That raises a natural question: why does charge stored beside one wordline not simply drain along the film into the next cell?

The nitride is an insulator containing localised electronic storage sites, called **traps**. An electron held in a trap does not move freely through the film as it would through a conducting electrode. Local charge near a selected wordline changes the channel's electrical response at that level. The dotted cell outlines in the diagram identify these controlled regions; they are not walls dividing the nitride into isolated boxes. [13]

During programming, a high voltage on the selected gate produces a field that transfers electrons from the channel through the tunnel dielectric into traps. In retention, the barriers and traps greatly restrict escape. This is controlled charge transfer under different bias conditions, rather than a claim that an insulating film can never pass charge. [32]

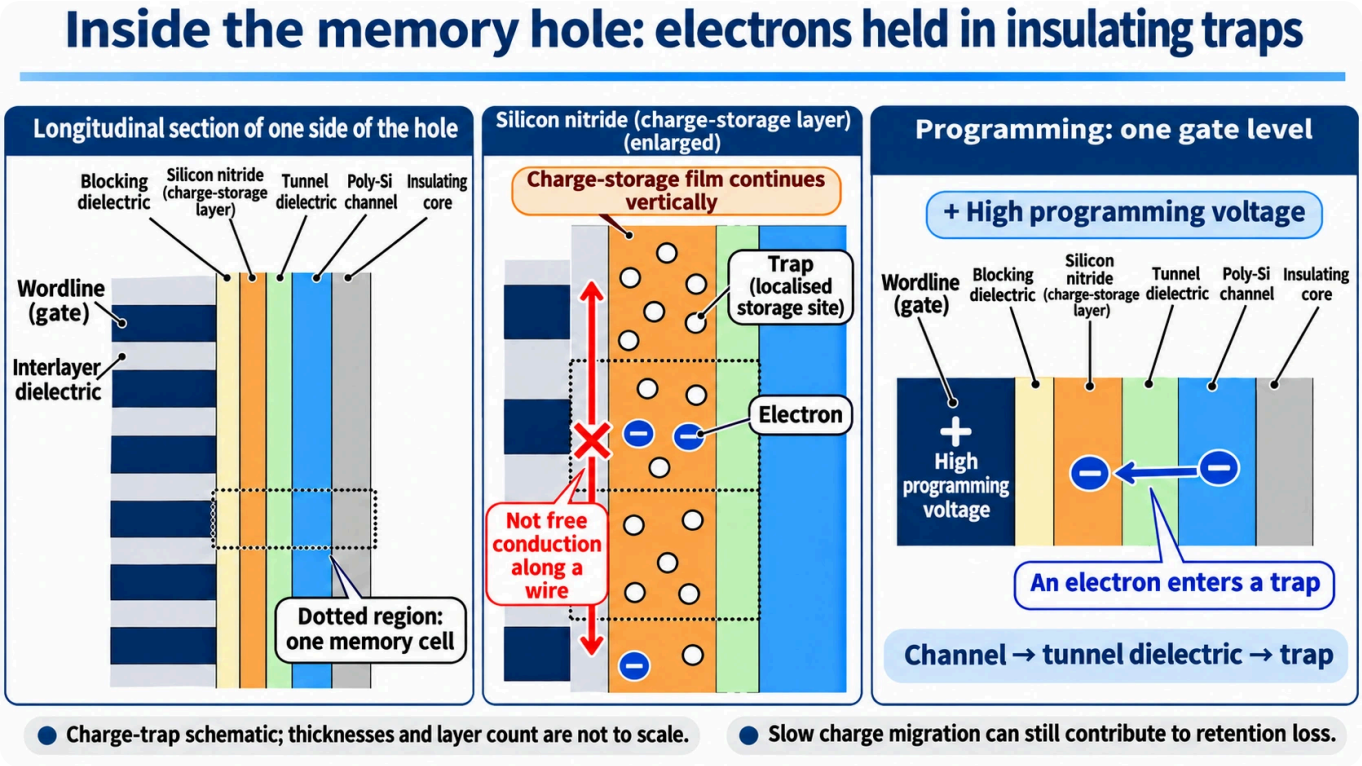


Figure 2 **Inside the memory hole: electrons held in insulating traps** (schematic). Layer thicknesses and gate count are illustrative; the red cross indicates the absence of free wire-like conduction, not zero long-term charge migration.

Retention is finite

Trapping does not freeze every electron in place forever. Slow redistribution along the storage film can contribute to lateral charge loss. The abstract of the cited 2026 study identifies thinning of silicon-nitride charge-trap layers as a retention challenge, before investigating dopants in an alternative HfO_2 storage material. That research does not establish a universal lifetime or leakage rate for all NAND products. [33]

One hole creates a series string of memory cells

Each wordline controls a different section of the vertical channel. Those transistor sections are connected in series along one **NAND string**. More memory levels can therefore provide more cells within the same lateral footprint, but they also demand deeper or more carefully connected holes. Channel continuity and gate isolation must both survive the process. [13]

The economic advantage is easier to see by imagining the alternative: patterning and processing each complete memory layer separately. A 2011 Toshiba analysis estimated that this would stop reducing cost per bit beyond roughly four to eight layers under its assumptions. Batch formation avoids repeating the same lithography and hole-patterning work for every level. Deposition, tier formation and other integration work still grow with layer count. [13]

Kioxia's published milestones include 48-layer products in 2015, 96 in 2018, 112 in 2020 and 162 in 2022. In July 2026 it announced sampling of tenth-generation, 332-layer BiCS FLASH. That is about seven times the layer count of the 48-layer example, although it does not imply seven times the depth or an unchanged process. [11][14]

Keeping a similar hole diameter while increasing depth makes mask survival, gas chemistry and plasma/profile control increasingly important. Tokyo Electron illustrates the scale with an enlarged analogy: roughly two trillion hair-width holes, 8 mm deep, formed uniformly over an area comparable to Tokyo Dome in 33 minutes. It is an analogy for simultaneous precision, not the physical dimensions of a wafer. [12][18]

DRAM, silicon vias and micromachines

- **DRAM capacitors** need substantial charge-storage surface area within a very small footprint. Tall capacitor structures are one application of deep-feature etching; Lam lists capacitor-cell processing alongside NAND holes, slots and contacts [21]. Explanation
- **Deep silicon trenches** appear in image sensors and power devices. Through-silicon vias, or **TSVs**, provide connections through silicon for stacked structures [21]. Reported
- **MEMS**, such as miniature mechanical sensors, use deep silicon processing to define three-dimensional structures. Research literature identifies deep reactive ion etching, **DRIE**, as important for both MEMS and TSV fabrication [9]. Reported

3. What changes inside a deep feature?

Wall interactions dominate transport over short distances

The **mean free path** is the average distance a particle travels before colliding with another particle. Berkeley's notes give an approximate argon ion-neutral relation of **λ (cm) = 1/(330p)**, with pressure p in Torr [3]. At 30 mTorr this gives about 0.1 cm, or 1 mm. Calculation

A hypothetical 0.1 µm-wide hole is about ten thousand times smaller than that distance. Calculation The relation is for the stated argon collision model, not every reactive species, but it illustrates the scale: inside a tiny feature, interactions with walls can be far more important than collisions between gas particles. Explanation

For neutral species this is a **Knudsen-transport** problem. Particles may reflect from walls, adsorb, react or return towards the opening. Some reach the bottom without a wall collision; nearly vertical ions can also follow that direct route. Gas transport is therefore better understood through individual trajectories and wall interactions than as a continuous draught of air flowing down the hole [1][6]. Reaction products must also find a way out. Explanation

ARDE and RIE lag

Aspect-ratio-dependent etching, ARDE, means that etch behaviour depends on feature geometry. The common case in which deeper, narrower features etch more slowly is called **RIE lag**. The Texas lecture discusses four contributing mechanisms [1]. Reported

Mechanism	What limits delivery to the bottom?
Neutral shadowing	Oblique neutral species encounter upper walls. Some are consumed by adsorption or reaction before they reach the bottom.
Ion shadowing	Even a small angular spread sends ions into sidewalls instead of onto the bottom.
Differential charging	Unequal electron and ion access creates local potentials that change ion trajectories and energies.
Knudsen transport	Repeated wall interactions and the probability of returning to the opening restrict effective transport through the feature.

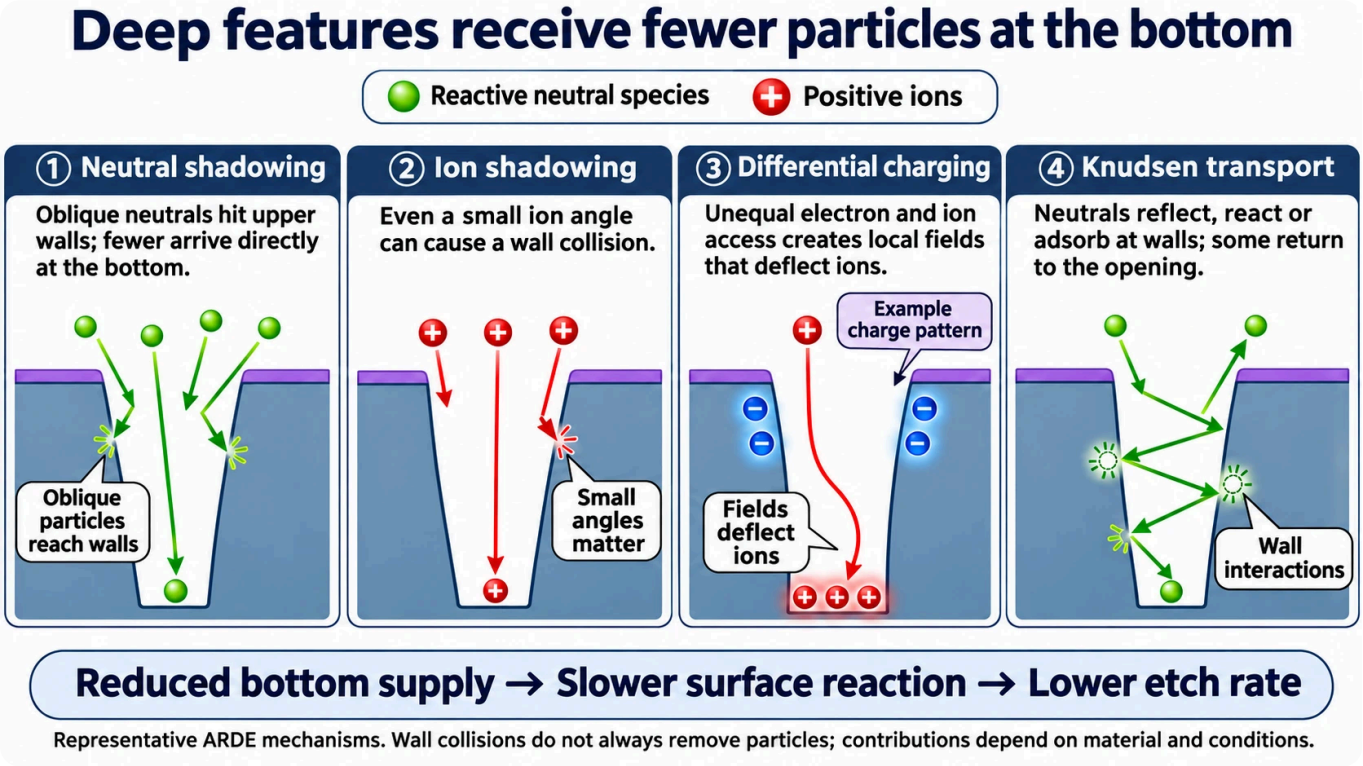


Figure 3 **Four mechanisms that change particle delivery in deep features** (schematic)

Reading the figure

These mechanisms can act together. A neutral hitting a wall is not automatically lost: it may reflect and continue, or be consumed at the surface. The charge pattern is one illustrative case, not a fixed polarity map for every feature. Particle counts and angles are schematic. The cited lecture identifies differential charging as dominant in the dielectric-etch study it discusses, rather than in every possible etch [1].

The opening occupies a very small part of the sky

Imagine looking upwards from the centre of a cylindrical hole's bottom. The opening lies within a cone of half-angle θ, measured from the vertical:

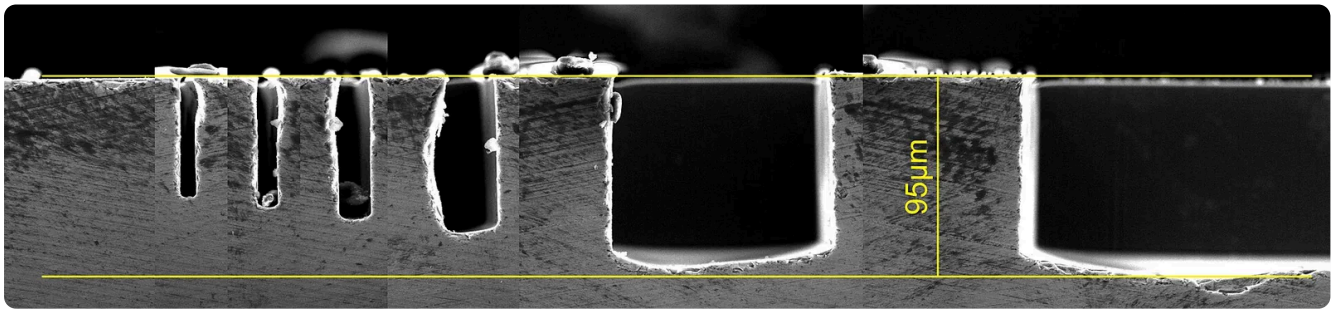
tan θ = radius/depth = 1/(2AR).

For an isotropic neutral population above a flat surface, the incident flux follows cosine weighting. The fraction within that angular cone is **sin²θ**. The following calculation estimates direct access to the bottom centre, before wall reflections or reactions. **Calculation**

Aspect ratio	Cone half-angle θ	Direct-access fraction, sin²θ
1:1	About 27°	About 20%
10:1	About 2.9°	About 0.25%
50:1	About 0.57°	About 0.01%
100:1	About 0.29°	About 0.0025%

At large AR, increasing aspect ratio tenfold reduces this direct geometric fraction by approximately a factor of one hundred. Reflected particles can still contribute, so the table is not a prediction of total bottom flux or etch rate. **Explanation**

A straight ion entering at the opening's centre faces the same geometric limit if it is to reach the bottom without hitting a wall. At AR = 50, an angle of only about 0.6° is enough to matter. Real trajectories also depend on entry position and electric fields. **Explanation**



Cross-section of silicon microchannels made in an ICP deep-etch process. According to the Commons description, the narrower channels receive radicals less efficiently and therefore etch more slowly. The different depths after the same processing time provide a direct example of geometry-dependent removal. **Explanation**

Image: MgerIt / Wikimedia Commons / CC BY-SA 4.0. Resized and converted to WebP.

Charging can change both the direction and energy of ions

Lesson 3-8 introduced sheath acceleration. Positive ions tend to arrive near the surface normal, while electrons have a broader angular distribution and can reach the surface more readily when the RF sheath barrier is low. Their access to a deep feature therefore differs [1]. **Explanation**

In one representative insulating-feature case, upper surfaces receive electrons more readily while the bottom receives a larger relative positive-ion contribution. The upper region can become relatively negative and the bottom positive. That distribution can repel incoming positive ions, reduce their impact energy or deflect them towards a wall. The actual potential depends on materials, electron supply and operating conditions. Explanation

The lecture cites an example with approximately 30% ion-energy reduction at an aspect ratio around three [1]. Deflected ions can also contribute to excessive removal near bottom corners. Charging is therefore a profile-control problem as well as a delivery problem. Explanation

- **Sometimes a narrower feature etches faster**

The opposite trend, **inverse ARDE**, is possible. A narrow feature may restrict the supply of polymer-forming species as well as etchants. If its protective film becomes thinner, removal can become faster under some conditions [1]. The important variable is the balance between deposition, protection and removal, not aspect ratio alone. Explanation

- **What can the process engineer adjust?**

  - **Pressure:** lower pressure can reduce ion scattering in the sheath, but also changes neutral supply and discharge conditions.
  - **Wafer bias:** sufficient ion energy helps bottom reactions and film clearance. Excess energy increases mask erosion and damage; source power and wafer bias have different roles.
  - **Gas mixture:** etching and film-forming species must remain balanced as the feature deepens.
  - **Pulsing and separated steps:** changes to plasma generation, bias timing or cyclic processing can alter charging and surface conditions [1][4].

Berkeley's notes describe pulsing as a way to reduce aspect-ratio effects and charging damage [4]. Charge relaxation depends on the pulse scheme; switching off power does not guarantee that every feature receives exactly the electrons it needs. ALE or other separated steps may help in suitable applications, but their transport and throughput constraints still need to be addressed. Explanation

4. Deep enough is not enough: the profile must be right

A feature that reaches the target depth can still be unusable. The walls must stay within the required dimensions, the entrance must remain open and the mask must survive. The lecture identifies several characteristic profile defects [1]. Reported

Defect	Appearance	Contributing mechanisms in the teaching examples
Bowing	The middle widens like a barrel	Scattered ions, inadequate sidewall protection or changes in passivation with depth
Necking	The entrance narrows	Excess polymer near the opening or redeposition of scattered material
Faceting	Mask corners become bevelled	Angle-dependent sputtering erodes exposed corners
Microtrenching	Bottom corners become deeper than the centre	Ion reflection from sloping walls or deflection by local charging

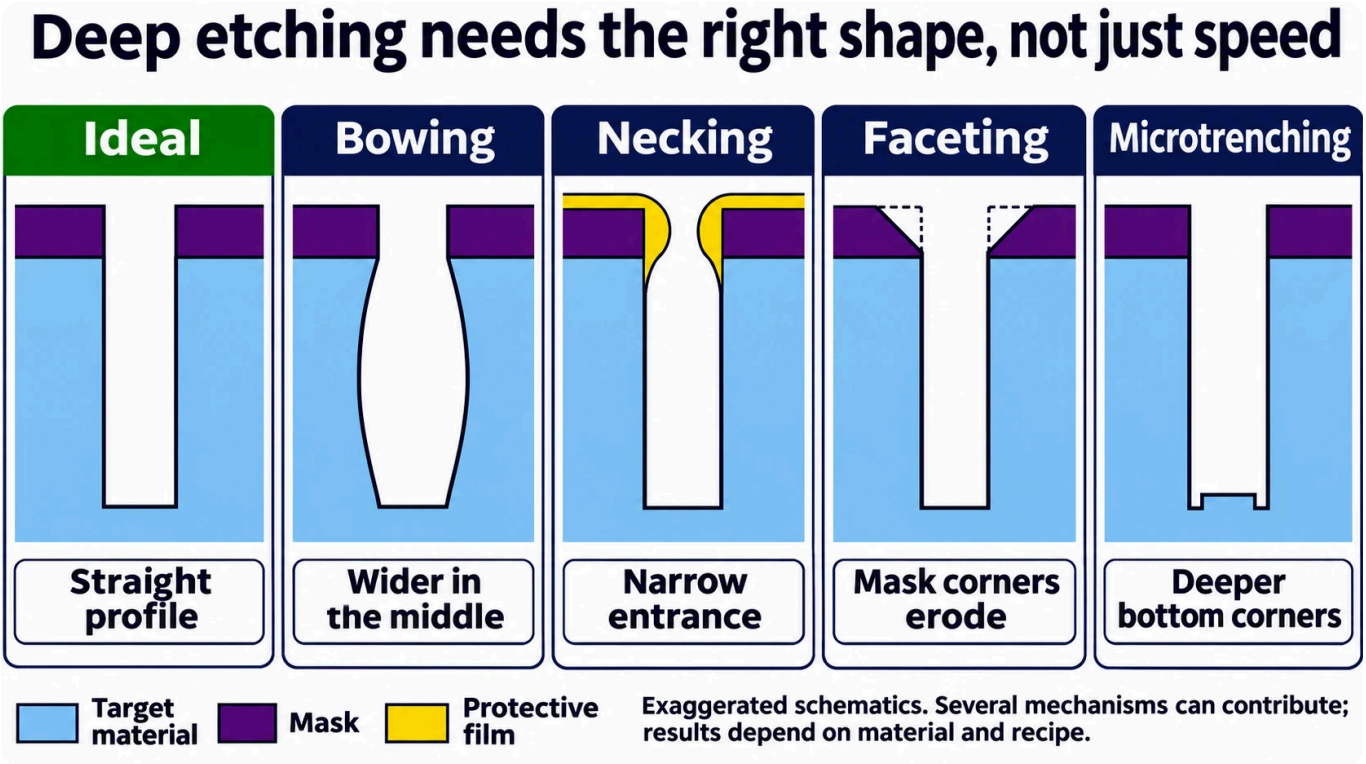


Figure 4 **An ideal profile compared with four common defects** (schematic)

Reading the figure

White represents removed material. Bowing is a widening below the entrance; necking restricts the entrance; faceting changes the mask; microtrenching cuts deeper at bottom corners. Shapes are exaggerated to make the differences visible. More than one mechanism can produce or worsen a defect [1].

In a NAND channel, profile differences can change the properties of cells at different heights. Lam's 2024 announcement reports channels up to 10 µm deep with a profile-deviation metric below 0.1% [20]. The denominator matters: Lam defines this as **maximum critical dimension minus minimum critical dimension, divided by channel depth**. It is not a claim that the diameter varies by less than 0.1% of the diameter. Explanation

5. Deep silicon etching with the Bosch process

- **Separate etching from protection in time**

Fluorine radicals can remove silicon quickly, but without sufficient protection they also attack sideways. The **Bosch process** alternates a silicon-removal step with a polymer-deposition step. At the next etch step, directed ions help clear the film at the bottom while the sidewalls remain protected [9][10]. Explanation

Franz Laermer and Andrea Schilp at Robert Bosch developed the approach described in US patent 5,501,893. Its priority date is 5 December 1992; the US patent was granted on 26 March 1996 [10]. The basic sequence is to etch, coat the newly exposed surfaces with a temporary protective layer, and repeat. Reported

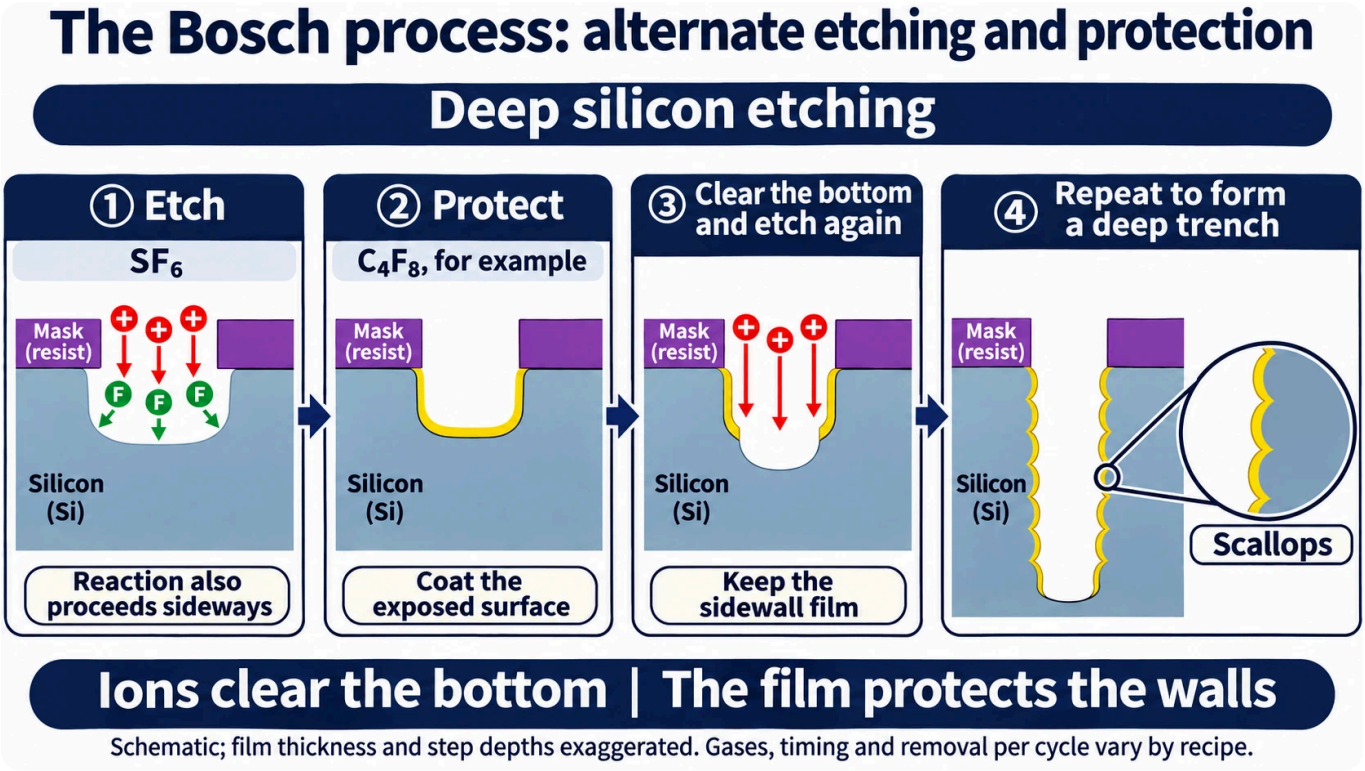


Figure 5 **The Bosch cycle: etch, protect, clear the bottom and repeat** (schematic)

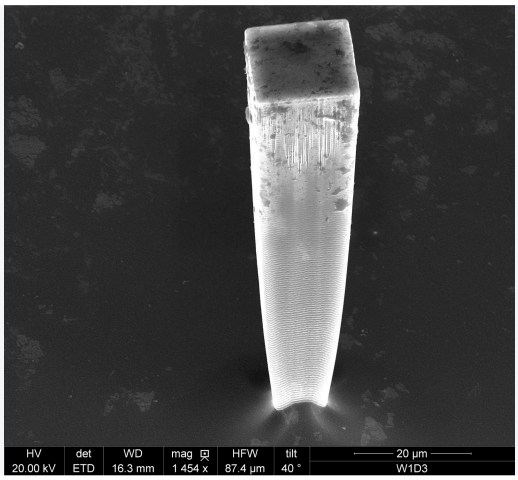
Reading the figure

The etch step produces a shallow rounded cavity. Protection covers the exposed walls and bottom. Ion bombardment then opens the bottom so removal can continue underneath, while the wall film persists. Repetition produces one connected trench with small sidewall undulations. Film thickness and removal depth are exaggerated [9][10].

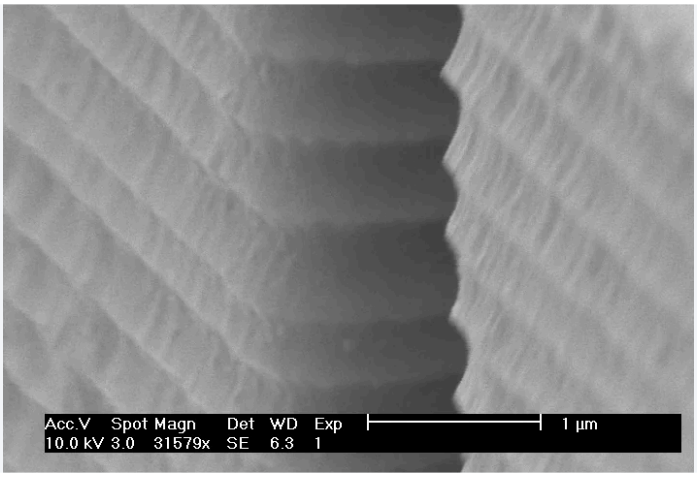
The patent's examples use SF_6/argon for removal and CHF_3/argon for polymer formation. One example removes 2-3 µm, then deposits approximately 50 nm of protective material over about a minute, with bottom clearing occurring in seconds [10]. Those numbers describe the example, not the timing of every modern Bosch process. A common later implementation alternates SF_6 etching and C_4F_8 passivation [9]. Reported

The cycles leave a trace: scallops

Each short removal step produces a little lateral recess. Repeating the cycle leaves a sequence of small undulations called **scallops**. Shorter etch steps can reduce their size [9]. The recipe must trade profile smoothness against removal rate, switching overhead and protection. Explanation



Silicon micropillar fabricated by ICP-DRIE. The Commons description attributes the fine grooves to the Bosch process and notes that the pillar becomes narrower towards its base. The repeating texture is a visible record of cyclic removal and protection. Explanation
Image: MgerIt / Wikimedia Commons / CC BY 4.0. Resized and converted to WebP.



Scanning electron micrograph of a silicon structure fabricated by photolithography and Bosch-process deep reactive ion etching, according to Commons. The enlarged wall makes the repeating scallop shape visible. Explanation
Image: Pgalajda / Wikimedia Commons / Public domain. Converted to WebP.

Polymer also deposits on chamber surfaces, so cleaning is part of maintaining repeatable processing [9]. Lam's filing describes deep-silicon equipment that supports rapidly alternating processes as well as conventional single-step etching [21]. Reported

6. Cryogenic etching and tiered NAND structures

Low temperature changes the protection mechanism

Cryogenic silicon etching has roots in the work of S. Tachi, K. Tsujimoto and S. Okudaira, published in 1988 [7]. The review by Dussart and colleagues traces the method's early introduction to a Japanese team [8]. The origin is relevant history; the subsequent technology has developed through research and manufacturing work across countries. Reported

Early experiments aimed to suppress lateral silicon reactions by cooling the wafer. Later understanding identified an important role for a thin $\mathbf{SiO_xF_y}$ layer, initially associated with oxygen impurities, in protecting the walls [9]. Reported

In a conventional cryogenic silicon example, an SF_6/O_2 plasma is used with the wafer around −100°C. Low-temperature surface chemistry supports protection while etching continues. Unlike the alternating fluoropolymer Bosch example, this continuous route can produce smooth walls without the same polymer-deposition cycle [9]. Explanation

The protective layer forms more readily on a cold surface, and much of it desorbs on warming. The cited paper also identifies practical challenges including liquid-nitrogen use, reproducibility and very uniform substrate cooling [9]. These help explain its more limited industrial adoption relative to Bosch processing in the silicon applications discussed. Explanation

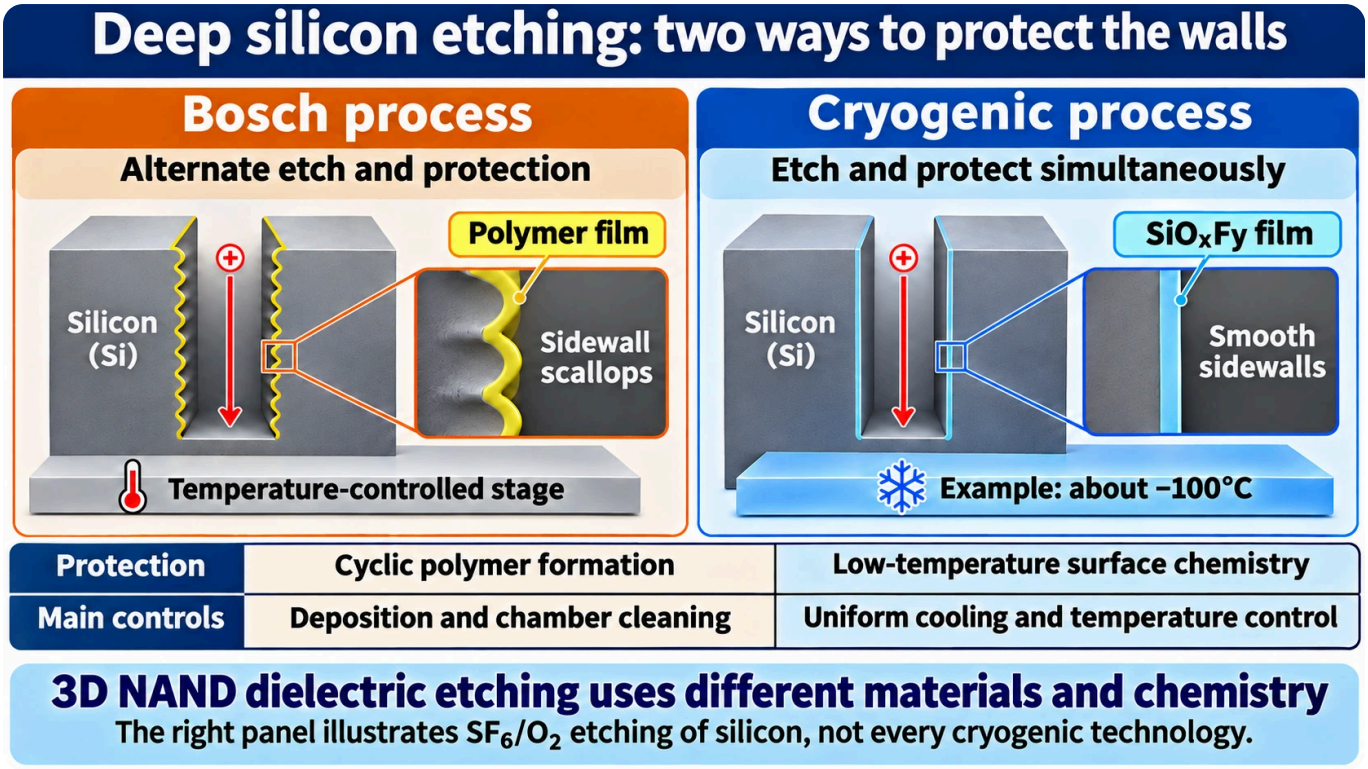


Figure 6 **Sidewall protection in Bosch and cryogenic silicon etching** (schematic)

Reading the figure

Both panels concern silicon. The left uses cyclic polymer protection; the right illustrates low-temperature SF_6/O_2 chemistry with SiO_xF_y protection. Exposed bottom regions allow removal to continue. The −100°C example and blue film must not be transferred directly to 3D NAND dielectric etching, which involves different materials and chemistry [9][17][20].

Cryogenic dielectric etching for 3D NAND

NAND channel holes pass through multilayer film stacks, not simply a solid silicon block. Equipment suppliers have also developed low-temperature **dielectric** etching for this task. Sharing the word “cryogenic” does not make it the same process as silicon SF_6/O_2 etching. Explanation

Lam Research states that it brought a cryogenic etch offering into volume production in 2019. Its July 2024 announcement reports that approximately 1,000 of more than 7,500 of its HAR dielectric-etch chambers used in NAND production employed cryogenic technology, about 13% on those approximate figures [20]. Calculation

For Lam Cryo 3.0, the same announcement reports an etch rate 2.5 times that of conventional dielectric processes, 40% lower energy consumption per wafer and up to 90% lower emissions. These are supplier comparisons; the announcement explicitly says the estimated emissions reduction was not independently verified [20]. Lam's filing describes low temperature as enabling new chemistries that improve HAR capability [21]. Reported

Tokyo Electron announced a cryogenic dielectric-etch development in June 2023 aimed at channel holes for NAND beyond 400 layers. It reported a 10 μm etch depth in 33 minutes and an 84% reduction in the stated greenhouse-gas impact comparison [17]. The depth and time imply an average rate of about 0.3 μm/min, or 5 nm/s; this average does not show how rate varies throughout the etch. Calculation

Its 2024 blog describes coolants at negative tens of degrees Celsius, compared with 0-80°C coolant ranges in its conventional examples. Coolant temperature is not automatically the same as the wafer's actual surface temperature. The article says that its latest generation replaced 91% of the fluorocarbon gas with HF [18]. Its 2026 integrated report gives per-wafer reductions of 84% in CO_2-equivalent emissions and 43% in electricity use relative to its first-generation equipment [22]. These figures retain the supplier's comparator and do not imply a reduction across every etch process. Explanation

Why can cooling help?

In a simple surface-residence model, lower temperature can reduce thermal desorption, allowing an adsorbed species to remain longer. That can change surface coverage, protection and available reaction pathways. Explanation

The cited supplier descriptions do not provide a complete surface-reaction mechanism for every proprietary dielectric process. Cooling alone does not guarantee a higher rate: reaction kinetics, product removal and passivation also change. The useful result comes from the combination of chemistry, plasma control and temperature, not from temperature in isolation. Interpretation

Split the stack when one full-depth etch is too difficult

A taller stack can be divided into **tiers**. Each tier is patterned and processed, with alignment and connection steps creating the final continuous structure. This reduces the depth tackled in one etch, but adds integration work. Explanation

SK hynix's November 2024 announcement of 321-layer NAND describes a **three-plug** process, forming and electrically connecting the structure in three stages. It also describes changing the plug-filling material to reduce deformation [16]. Samsung's ninth-generation V-NAND announcements describe **double-stack** integration and channel-hole etching; the cited April 2024 release does not give a numerical layer count [15][30]. Reported

Tokyo Electron explains that reducing three etch stages to two can reduce manufacturing cost [18]. The objective is therefore not only to make a deeper hole: it can also be to eliminate a whole tier of associated processing. Explanation

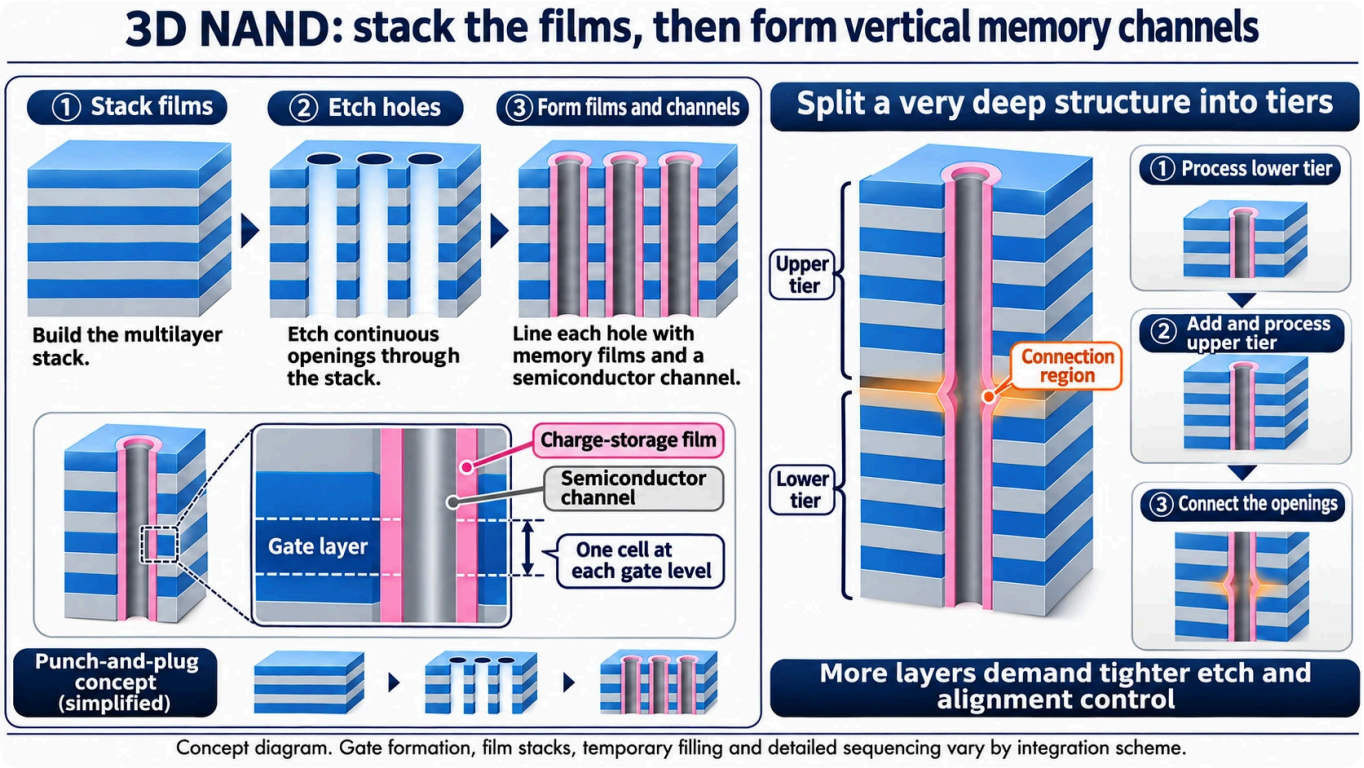


Figure 7 **Punch-and-plug formation and connected tiers in 3D NAND** (schematic)

Reading the figure

The empty openings in step 2 become lined with films and a semiconductor channel in step 3. The right-hand panel shows connected tiers. Real integration can include temporary filling, alignment, gate replacement and other steps not drawn here. Film stacks and sequencing vary; the diagram explains the concept rather than one complete production recipe [11][15][16].

7. Memory makers: the demand behind the etch

- **A sourced market snapshot**

A December 2025 METI presentation gives the following DRAM and NAND shares, based on company-hearing data [23]. The chart does not identify the market-data year, so 2025 is treated here as the publication year. The figures are context for the source article, not an independently updated market ranking. Reported

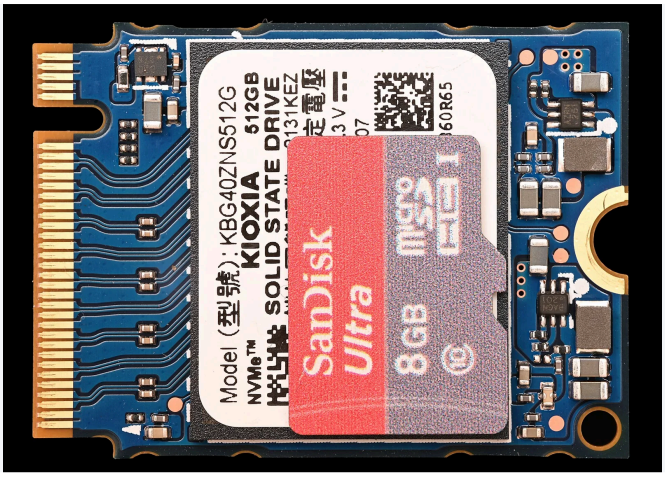
DRAM supplier	Share	NAND supplier	Share
Samsung, South Korea	39.3%	Samsung, South Korea	32.9%
SK hynix, South Korea	33.6%	SK hynix, South Korea	19.7%
Micron, United States	21.6%	Kioxia, Japan	14.9%
		Micron, United States	11.9%
		Sandisk, United States	10.1%
		YMTC, China	8.9%

The two South Korean entries sum to 72.9% in DRAM and 52.6% in NAND. The NAND entries for the United States total 22.0%, while Kioxia and YMTC account for the stated 14.9% and 8.9%. **Calculation** The same source gives an HBM split of SK hynix 57%, Micron 35% and Samsung 8% [23]. HBM is a distinct category; those percentages should not be substituted for the broader DRAM figures. **Explanation**

- **Layer counts are milestones, not a complete comparison**

Company	Dated announcement	Reported milestone
Kioxia	July 2026	Sampling of tenth-generation, 332-layer, 1 Tb TLC BiCS FLASH; production at Kitakami Fab 2; 59% higher bit density than the eighth generation [14]
Samsung	April 2024	Volume production of ninth-generation, 1 Tb TLC V-NAND with double-stack integration; no layer count in that release [15]
SK hynix	November 2024	Volume production of 321-layer, 1 Tb TLC NAND using three-plug processing [16]

Kioxia's tenth generation was jointly developed with Sandisk, and its 332-layer description refers to word-line layers [31]. **Reported** Layer-count conventions may differ, and the table mixes sampling with volume-production announcements from different dates. Cell design, usable density, speed, yield and cost also matter. A larger number alone is not a complete measure of technical superiority. **Explanation**



A 512 GB M.2 2230 Kioxia/Toshiba BG4 SSD compared with a SanDisk Ultra 8 GB microSD card, according to Commons. The SSD package contains both an NVMe controller and NAND flash. The deep structures discussed in this lesson become part of the memory inside storage devices like these. **Explanation**

Image: Phiarc / Wikimedia Commons / CC BY-SA 4.0. Resized and converted to WebP.

8. Equipment suppliers and their roles

The METI source gives a broader etching-equipment market of ¥2.3383 trillion, including Applied Materials at 33%, Lam Research at 30% and Tokyo Electron at 20%, without specifying the data year in the chart [23]. That category is broader than NAND channel-hole etching. Its shares cannot establish a separate ranking for HAR dielectric tools. **Explanation**

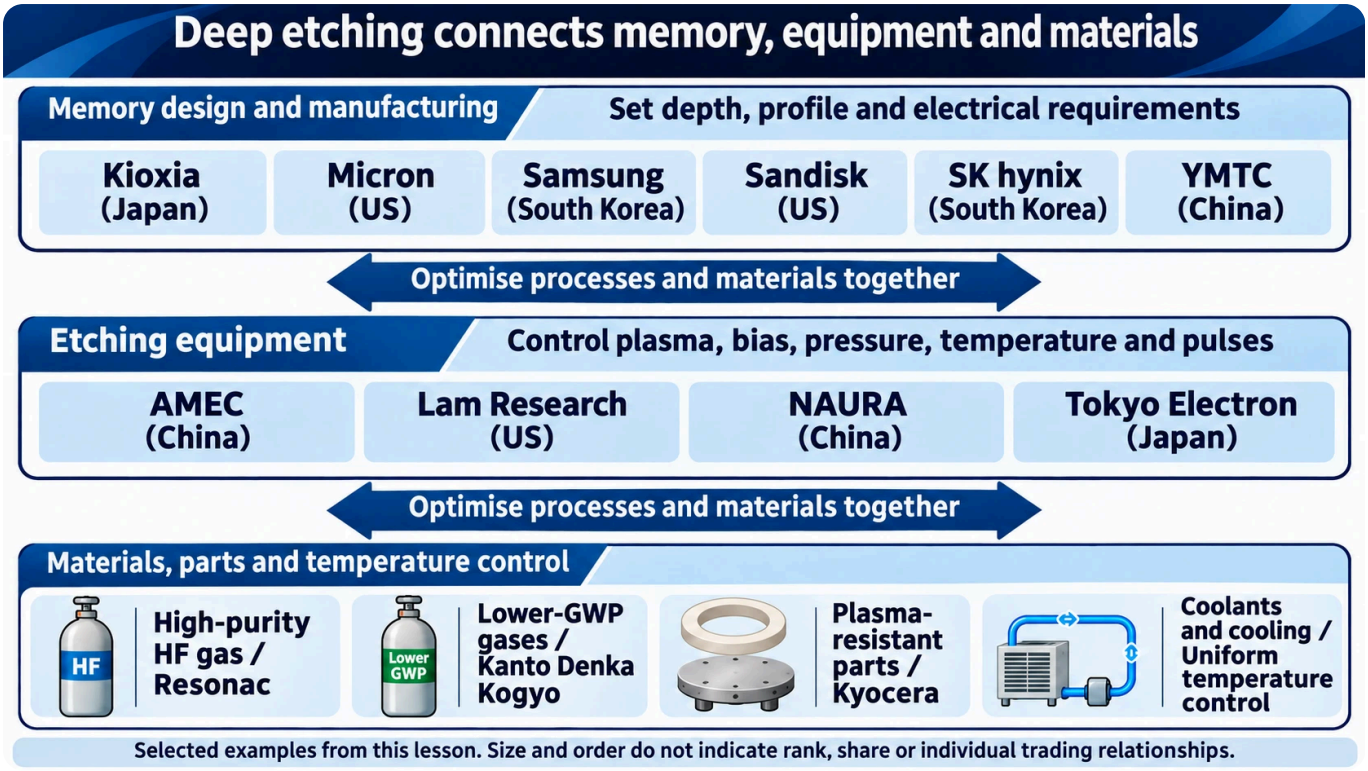


Figure 8 **Memory, equipment, materials and temperature control** (schematic)

Reading the figure

The bands show complementary roles. Memory makers specify the structure and electrical requirements; equipment controls the process; gases, parts and cooling support it. Names are selected examples from this lesson. Equal boxes and connecting arrows do not establish share, rank, complete market coverage or individual commercial relationships [14–29].

Selected equipment profiles, in alphabetical order

AMEC (China). Its 2025 annual report describes 60:1 dielectric etching as a domestic standard application for its equipment and reports customer qualification and repeat orders for the Nanova LUX-Cryo ICP product [24]. These are company-reported application milestones, not a directly comparable worldwide share measure. Reported

Lam Research (United States). Its 2024 announcement says that Flex HAR dielectric etchers are used by all major memory manufacturers for 3D NAND volume production, and that five million wafers had already been processed using its cryogenic technology [20]. Its filing identifies Vantex applications including NAND holes, slots and contacts, together with capacitor-cell processing [21]. The wording and installed-use figures are Lam's dated statements. Reported

NAURA (China). Its 2025 report identifies memory holes and trenches as applications for CCP etching and describes low-temperature and multiple-pulse development for 12-inch HAR CCP equipment [25]. The described approach should not be assumed to have identical materials, specifications or qualification status to another supplier's cryogenic product. Reported

Tokyo Electron (Japan). The company dates the start of its new-etch development to around 2014 and announced its cryogenic dielectric work in 2023 [18]. In February 2025 it reported one customer's selection as a volume-production **process of record, POR**, with evaluations continuing elsewhere. At that time it expected pilot-line investment in 2025 and volume-production investment in 2026, and estimated a US$2 billion market in 2027 [19]. These were dated expectations, not confirmation of later investment or market results. Reported

- **Memory investment affects more than one tool category**

Applied Materials' FY2025 semiconductor-systems revenue mix was 67% foundry, logic and other, 26% DRAM and 7% NAND [26]. This is a business-segment mix, not the mix of its etching revenue alone. It illustrates how memory investment connects to a broader equipment portfolio without establishing a HAR-specific position. Explanation

9. Gases, cooling and chamber materials

- **A successful recipe needs suitable materials around it**

  - **Lower-GWP process gases:** Kanto Denka Kogyo reports adoption of KSG-14 for Kioxia's NAND memory-channel-hole etching, describing a lower GWP than conventional c-C_4F_8 [28]. This is a specific adoption announcement, not a universal replacement for every fluorocarbon recipe. Reported
  - **Plasma-resistant components:** Kyocera describes ceramics for semiconductor equipment, including electrostatic chucks, with resistance to plasma erosion and particle generation [29]. Uniform wafer contact and temperature control are especially important in cryogenic processing [9]. Reported
  - **High-purity HF:** Resonac's June 2026 announcement planned additional hydrogen-fluoride gas production in Tokuyama during 2026, alongside Kawasaki, citing demand from advanced processing including cryogenic etching [27]. The cited plan is not treated as proof that the new line is already operating. Reported
  - **Coolants and cooling systems:** Tokyo Electron discusses replacing PFAS used in cooling fluids and fluorinated refrigerants while maintaining stable low-temperature processing [18]. Cooling capability, fluid properties and environmental impact have to be considered together. Explanation

These are examples from the source material, not a complete international supplier list. Japanese companies have documented roles in these specialised materials; that does not require treating other regions as absent from the wider supply chain. Explanation

Where materials engineering makes a difference

A suitable molecule must reach the feature, support removal or protection and leave manageable products. High purity limits contamination. A durable mask must survive while the deep structure is formed. Chamber ceramics must resist erosion without creating defects. The chuck and cooling system must keep conditions uniform, and tier-connection materials must remain stable during integration.

Deep etching brings these tasks together: success is measured at the bottom of the feature, not only at the gas inlet or power supply. Explanation

10. What further development must achieve

The next challenge is not simply a bigger aspect-ratio number. Manufacturers want accurate profiles with fewer processing stages, acceptable damage, useful throughput and lower environmental impact. Tokyo Electron's cited development goal is AR = 200 in one etch; it also describes the cost benefit of reducing three stages to two [18]. These are objectives tied to that publication. Explanation

Lower-GWP chemistries, more effective gas use and suitable exhaust treatment must preserve the required profile. Cold processing also adds demands on cooling materials and energy. A useful advance has to improve the complete manufacturing route, rather than one isolated rate or temperature. Explanation

11. Recap and the next lesson

Topic	Key point
Aspect ratio	Depth divided by width; a small angular error becomes important in a long, narrow feature.
3D NAND	Batch formation creates many memory levels, while tall stacks make etching and tier connection harder.
Feature transport	Wall interactions, return paths and surface losses matter when the mean free path greatly exceeds feature width.
ARDE	Geometry changes removal through neutral and ion shadowing, charging and transport.
Profile defects	Bowing, necking, faceting and microtrenching describe different failures.
Bosch process	Alternate silicon removal and polymer protection; repeated lateral recesses produce scallops.
Cryogenic silicon etching	Low-temperature SF6/O2 chemistry can sustain SiOxFy sidewall protection.
Cryogenic dielectric etching	Different materials and chemistry are used for deep NAND stacks; silicon conditions cannot simply be copied across.
Tiering	Splitting the stack reduces individual etch depth but adds alignment and connection work.
Industry	Memory, equipment, gases, parts and cooling contribute different capabilities; dated claims need matching scopes.

Lesson **3-10, Ion Implantation and Annealing**, moves from shaping material to changing its electrical behaviour: accelerated dopant ions introduce atoms such as boron or phosphorus, and subsequent heat treatment helps establish the intended properties.

12. Check your understanding

1. What is the aspect ratio of a hole 5 µm deep and 0.1 µm in diameter?

> **▼ Show answer**
>
> Depth divided by diameter gives 5/0.1 = 50, or 50:1. Both dimensions must use the same units.

2. Why form many NAND memory levels by etching a stack rather than processing each complete planar memory layer separately?

> **▼ Show answer**
>
> Batch formation avoids repeating the same lithography and hole-patterning work at every level. It can reduce cost per bit, although deposition, tiering and other integration steps still add work as the structure grows.

3. Why does a continuous nitride storage film not behave like a wire connecting the stored charge in every cell?

> **▼ Show answer**
>
> Electrons occupy localised traps in an insulating material, so they cannot conduct freely along it as in a wire. Slow charge migration can still occur and contribute to retention loss.

4. Why are wall interactions so important inside a low-pressure, narrow feature?

> **▼ Show answer**
>
> The mean free path can greatly exceed the feature width. Neutrals are therefore more likely to encounter a wall than another gas particle. Some particles reflect, react or adsorb; nearly vertical particles can still reach the bottom directly.

5. Name four mechanisms discussed in connection with ARDE.

> **▼ Show answer**
>
> Neutral shadowing, ion shadowing, differential charging and Knudsen transport. They can act together, and their relative importance changes with materials and conditions.

6. How can different electron and ion arrival angles affect a deep insulating feature?

> **▼ Show answer**
>
> They can create unequal charging between upper surfaces and the bottom. The resulting local fields may reduce ion energy or deflect trajectories, changing bottom removal and sometimes causing profile defects. The polarity pattern is condition-dependent.

7. How does the Bosch process preserve sidewalls, and what trace can it leave?

▼ **Show answer**

A polymer layer coats the exposed surfaces. At the next etch step, directed ions help clear the bottom while sidewall protection remains. Repeating the cycle leaves small undulations called scallops.

8. What protects the walls in the cryogenic silicon example, and why is cooling demanding?

▼ **Show answer**

A thin SiOxFy layer supports sidewall protection in low-temperature SF6/O2 processing, around −100°C in the example. Uniform temperature, reproducibility and the cooling infrastructure are important practical constraints.

9. Why can a cryogenic NAND dielectric process have a lower greenhouse-gas impact?

▼ **Show answer**

Suitable low-temperature chemistry can reduce the use of high-GWP fluorocarbon gases. Tokyo Electron reports replacing 91% with HF in its cited generation. The result depends on the actual recipe, comparator, gas use and exhaust treatment; it is not an automatic property of every cold process.

10. What must be checked before comparing suppliers' layer counts, market shares or etch-performance claims?

▼ **Show answer**

The date, market definition, metric and operating conditions, plus whether the statement concerns sampling, volume production, a forecast or an attributed supplier estimate. A chamber count, a layer count and a market share measure different things.

13. Glossary

Memory cell
A region storing a data state; in a vertical NAND string, a wordline controls one channel section.

Charge-storage film
Material that retains charge to change the cell threshold voltage.

Charge trap
A localised electronic storage site in a dielectric; trapping is different from free conduction in a metal.

NAND string
A series connection of memory-cell transistors along a semiconductor channel.

Aspect ratio
Feature depth divided by width; hole width is commonly its diameter.

High-aspect-ratio etching (HAR)
Etching features that are deep relative to their width.

3D NAND
NAND flash with memory cells arranged vertically at multiple levels.

Punch-and-plug
A batch-processing concept that etches openings through a stack and forms memory films and vertical channels inside.

Memory channel hole
An opening through a NAND stack used to form the vertical memory-channel structure.

Through-silicon via (TSV)
A connection formed through silicon to link structures or stacked chips.

MEMS
Microelectromechanical systems, including miniature mechanical sensors and actuators.

DRIE
Deep reactive ion etching, commonly used to form deep silicon structures.

Mean free path
The average distance travelled before collision with another particle, for a specified collision process.

Knudsen transport
Transport dominated by particle interactions with boundaries rather than collisions between gas particles.

ARDE
Aspect-ratio-dependent etching; RIE lag is the common case of slower removal in deeper, narrower features.

Inverse ARDE
Conditions under which a narrower or higher-aspect-ratio feature etches faster.

Neutral shadowing
Restricted direct access of oblique neutral species to a feature's bottom.

Differential charging
Unequal charge accumulation caused by differing electron and ion access.

Bowing
Widening of a feature below its entrance.

Necking
Narrowing near the entrance to a feature.

Faceting
Bevel-like erosion of mask corners.

Microtrenching
Excessive removal near bottom corners.

Bosch process
Cyclic deep silicon etching that alternates removal with protective-film formation.

Scallops
Repeated sidewall undulations left by cyclic etch steps.

Cryogenic etching
Etching at low substrate temperature to obtain useful surface-reaction and protection behaviour.

SiOxFy
A silicon-oxygen-fluorine surface layer used for protection in the cryogenic silicon example.

Double-stack / three-plug
Integration approaches that form and connect a tall NAND structure in multiple stages.

Process of record (POR)
A process or equipment choice selected for a specified production application.

Electrostatic chuck
A wafer holder that uses electrostatic attraction and also supports thermal control.

14. Sources and further reading

Reference numbers match the Japanese edition. English descriptions identify each publication; some original sources are in Japanese, Korean or Chinese. Company comparisons and forecasts retain the publication dates and scope indicated in the text.

1. **S. Sirard, Lam Research / University of Texas at Austin** — Introduction to Plasma Etching, Day 2 (2017; pp. 16-27) — Read source
2. **S. Sirard, Lam Research / University of Texas at Austin** — Introduction to Plasma Etching, Day 1 (2017; p. 7) — Read source
3. **M. A. Lieberman, UC Berkeley** — A Short Course on the Principles of Plasma Discharges and Materials Processing, Day 1 (2015; PDF p. 46) — Read source
4. **M. A. Lieberman, UC Berkeley** — The same course, Day 2 (2015; PDF p. 115) — Read source
5. **K. J. Kanarik et al.** — Overview of atomic layer etching in the semiconductor industry, Journal of Vacuum Science & Technology A 33, 020802 (2015) — Read source
6. **J. W. Coburn and H. F. Winters** — Conductance considerations in the reactive ion etching of high aspect ratio features, Applied Physics Letters 55, 2730-2732 (1989; discussed through the reproduction in ref. 1) — Read source
7. **S. Tachi, K. Tsujimoto and S. Okudaira** — Low-temperature reactive ion etching and microwave plasma etching of silicon, Applied Physics Letters 52, 616-618 (1988) — Read source
8. **R. Dussart, T. Tillocher, P. Lefaucheux and M. Boufnichel** — Plasma cryogenic etching of silicon: from the early days to today's advanced technologies, Journal of Physics D 47, 123001 (2014; HAL abstract) — Read source
9. **T. Tillocher et al.** — Comparison between Bosch and STiGer Processes for Deep Silicon Etching, Micromachines 12(10), 1143 (2021; Section 1) — Read source
10. **F. Laermer and A. Schilp, Robert Bosch GmbH** — US Patent 5,501,893: Method of anisotropically etching silicon (granted 26 March 1996) — Read source
11. **Kioxia** — What is 3D flash memory BiCS FLASH? (technology explainer; Japanese) — Read source
12. **Kioxia** — RIE technology supporting BiCS FLASH (13 June 2019; Japanese) — Read source
13. **R. Katsumata, Y. Fukuzumi and H. Aochi, Toshiba** — Three-dimensional BiCS flash memory for high-capacity nonvolatile storage, Toshiba Review 66(9) (2011; Japanese) — Read source
14. **Kioxia** — Sampling of tenth-generation BiCS FLASH for high performance, capacity and low power (3 July 2026; Japanese) — Read source
15. **Samsung Electronics** — Samsung Electronics Begins Industry's First Mass Production of 9th-Gen V-NAND (23 April 2024) — Read source
16. **SK hynix** — Start of volume production of 321-layer NAND (21 November 2024; Korean announcement) — Read source
17. **Tokyo Electron** — Memory channel-hole etch technology enabling ultra-fast 10 μm-deep etching for 3D NAND beyond 400 layers (9 June 2023) — Read source
18. **Tokyo Electron** — Cryogenic Etching: Tokyo Electron's Digital and Green Transformation of Semiconductor Process Equipment (corporate blog, 21 October 2024) — Read source
19. **Tokyo Electron** — Q3 FY2025 Earnings Briefing Q&A (10 February 2025; Q10) — Read source
20. **Lam Research** — Lam Research Introduces Lam Cryo 3.0 Cryogenic Etch Technology to Accelerate Scaling of 3D NAND for the AI Era (31 July 2024) — Read source
21. **Lam Research** — Form 10-K, fiscal year ended June 2026 (pp. 6-7) — Read source
22. **Tokyo Electron** — Integrated Report 2026 (PDF p. 55; Japanese edition) — Read source
23. **Japan, Ministry of Economy, Trade and Industry** — Future direction of semiconductor and digital industry strategy (23 December 2025; pp. 4-5; Japanese) — Read source
24. **AMEC** — Annual Report 2025 (pp. 43, 55; Chinese) — Read source
25. **NAURA** — Annual Report 2025 (pp. 19-20; Chinese) — Read source
26. **Applied Materials** — Form 10-K, fiscal year ended October 2025 (p. 30) — Read source
27. **Resonac** — Strengthening high-purity hydrogen-fluoride gas production for semiconductors (25 June 2026; Japanese) — Read source
28. **Kanto Denka Kogyo** — KSG-14 (product page; Japanese) — Read source
29. **Kyocera** — Components for semiconductor manufacturing equipment (product page; Japanese) — Read source
30. **Samsung Electronics** — Samsung Begins Industry's First Mass Production of QLC 9th-Gen V-NAND for AI Era (12 September 2024) — Read source
31. **Kioxia** — Design and development of tenth-generation 1 Tb, 3-bit-per-cell BiCS FLASH (18 June 2025; Japanese) — Read source
32. Kioxia — What is NAND Flash Memory? Read source
33. Ji-yeon Lee and Yun-Heub Song — First-principles dopant screening to suppress shallow traps in HfO_2 charge-trap layers for 3D NAND flash memory, Journal of Applied Physics 140, 035701 (15 July 2026). Retention discussion based on the abstract, verified through Crossref metadata. Read source

15. Claims and evidence

Claim or group of claims	Supporting source	Treatment
Aspect ratio, ARDE mechanisms, differential charging, inverse ARDE, controls and profile defects	Sirard Day 2 [1]	Teaching examples; mechanisms may coexist
Features above 40:1 and 60:1	Sirard Day 1 [2]; Kanarik et al. [5]	Dated examples, not universal thresholds
Argon ion-neutral mean-free-path relation	Lieberman Day 1 [3]	Approximation for the stated collision model
Pulsing and reduction of geometry effects or charging damage	Lieberman Day 2 [4]	Benefits depend on pulse scheme and application
Conductance and high-aspect-ratio feature transport	Coburn and Winters [6], discussed through [1]	Original work identified; teaching explanation retained
Early cryogenic silicon etching	Tachi et al. [7]; Dussart et al. [8]	Research history
DRIE applications, Bosch gases and scallops, SiOxFy protection and cryogenic challenges	Tillocher et al. [9]	Silicon processes distinguished from NAND dielectric etching
Bosch inventors, patent dates, alternating sequence and example process values	US Patent 5,501,893 [10]	Patent example, not a modern universal recipe
2007 batch-processing concept and 48/96/112/162-layer milestones	Kioxia [11]	Supplier historical account
Deeper holes at similar diameter and the importance of masks, gases and plasma control	Kioxia [12]	Supplier technical explanation
Four-to-eight-layer cost crossover in simple stacking	Toshiba Review [13]	2011 model under its assumptions
Tenth-generation 332-layer sampling, Kitakami production and density comparison	Kioxia [14]	July 2026 company announcement; sampling distinguished from volume production
Ninth-generation V-NAND, double stack and channel-hole etching	Samsung [15][30]	Dated announcements; no numerical layer count inferred
321-layer production, three-plug processing and material change	SK hynix [16]	November 2024 company announcement
10 µm in 33 minutes and stated emissions comparison	Tokyo Electron [17]	Supplier development result and comparator
Scale analogy, coolant ranges, 91% gas substitution, AR 100/200, tier reduction and cooling-fluid concerns	Tokyo Electron blog [18]	Dated description and objectives; coolant and wafer temperatures distinguished
One-customer POR, investment timing and 2027 market estimate	Tokyo Electron Q&A [19]	February 2025 statements and forecasts
Cryogenic production introduction, chamber figures, rate/energy/emissions claims, profile metric, Flex use and processed wafers	Lam Research [20]	Dated supplier claims; emissions estimate not independently verified; profile denominator retained
Vantex and deep-silicon applications, rapid alternation and new cryogenic chemistries	Lam FY2026 filing [21]	Supplier product description
84% CO2-equivalent and 43% electricity comparison	Tokyo Electron report [22]	Per-wafer comparison with first-generation equipment
DRAM, NAND, HBM and broader etch-equipment shares	METI [23]	Chart data year not specified; publication year is 2025
AMEC 60:1 applications and LUX-Cryo qualification	AMEC 2025 report [24]	Company-reported milestones
NAURA HAR CCP, low-temperature and multiple-pulse development	NAURA 2025 report [25]	Company description; qualification not assumed equivalent to competitors

Claim or group of claims	Supporting source	Treatment
67/26/7 revenue mix	Applied Materials FY2025 filing [26]	Semiconductor-systems business, not etch-only revenue
Added HF production and cryogenic demand	Resonac [27]	June 2026 plan; completion not inferred
KSG-14 adoption in NAND channel-hole etching	Kanto Denka [28]	Named supplier adoption claim
Plasma-resistant ceramics and electrostatic chucks	Kyocera [29]	Selected component examples
Kioxia/Sandisk joint development and word-line count	Kioxia [31]	Supplier technical account
50:1 worked example, 1 mm free path, 10,000-fold size ratio, angular cone and fractions, approximate sevenfold layer count, average removal rate and chamber/market sums	Stated inputs and equations in the text	This article's calculations
Particle-access explanation, charging relaxation, surface residence, cell-property links and comparison cautions	Sources above with explanatory reasoning	Teaching synthesis; proprietary mechanisms not inferred as established fact
NAND storage, continuous charge-trap films, programming and the vertical series string.	Sources 13 and 32; explanatory schematics.	Source-based explanation.
Slow lateral charge loss despite localised storage.	Source 33, abstract. No universal retention-rate claim.	Research context.

Updated 20 November 2026. Technical explanations draw on university lectures, research papers, patents and manufacturer publications. Company figures and performance comparisons are attributed to their dates and scope; plans are distinguished from results. Reference numbers match the Japanese edition. The English text and diagram labels were written for this edition.

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