SEMICONDUCTOR FRONT-END · PART 3-11

CMP
Chemistry and motion create a flat surface for the next layer

Building a chip leaves an uneven landscape of films, trenches and interconnects. Each new layer needs a controlled starting surface. Chemical mechanical polishing, or CMP, combines a reactive liquid with a moving polishing pad to remove material and reduce those height differences. This lesson follows the process from the polishing station to the surface chemistry, then explains how manufacturers control defects and how equipment and materials suppliers contribute.

Semiconductor manufacturing series · Intermediate introduction

Suggested preparation: deposition and basic photolithography · Updated 19 November 2026

What you will learn

- Why lithography and multilayer wiring need planar surfaces.
- How the carrier head, pad, slurry and conditioner work together.
- How pressure, relative speed and surface chemistry affect removal.
- How stop layers, endpoint control and dummy fill help protect the result.
- How equipment, abrasives, pads and cleaning fit into the global CMP supply chain.

1. The process in three ideas

First, create a level starting point. Deposited films can reproduce the steps underneath them. Accumulating topography makes it harder to expose the next pattern sharply and to form reliable wiring over steps.

Second, make removal depend on contact. The slurry changes the surface chemistry, while abrasive particles and the pad remove material where they contact it. Raised areas initially carry more load, so they tend to be removed faster.

Third, control where removal ends. A useful CMP recipe removes the unwanted film quickly while limiting attack on the material that should remain. Polishing, endpoint detection and post-CMP cleaning all contribute to the final result.

2. Why a chip needs a flat surface

- **Small steps become a manufacturing problem**

After transistors are formed, insulating films and metal interconnects are built above them. A deposited film may follow the underlying shape. If that shape contains steps, later films inherit them. A metal film crossing a steep corner can become thin there. Its smaller cross-section raises the electrical resistance of that part of the wire. [3]

Lithography adds another constraint. The depth of focus is the limited range of surface heights over which a pattern can be imaged acceptably. Its familiar scaling is proportional to **λ/NA²**, where λ is wavelength and NA is numerical aperture. Increasing NA to print smaller features reduces this height allowance. A surface with large peaks and valleys can place different parts of the same exposure outside the usable focus range. [4]

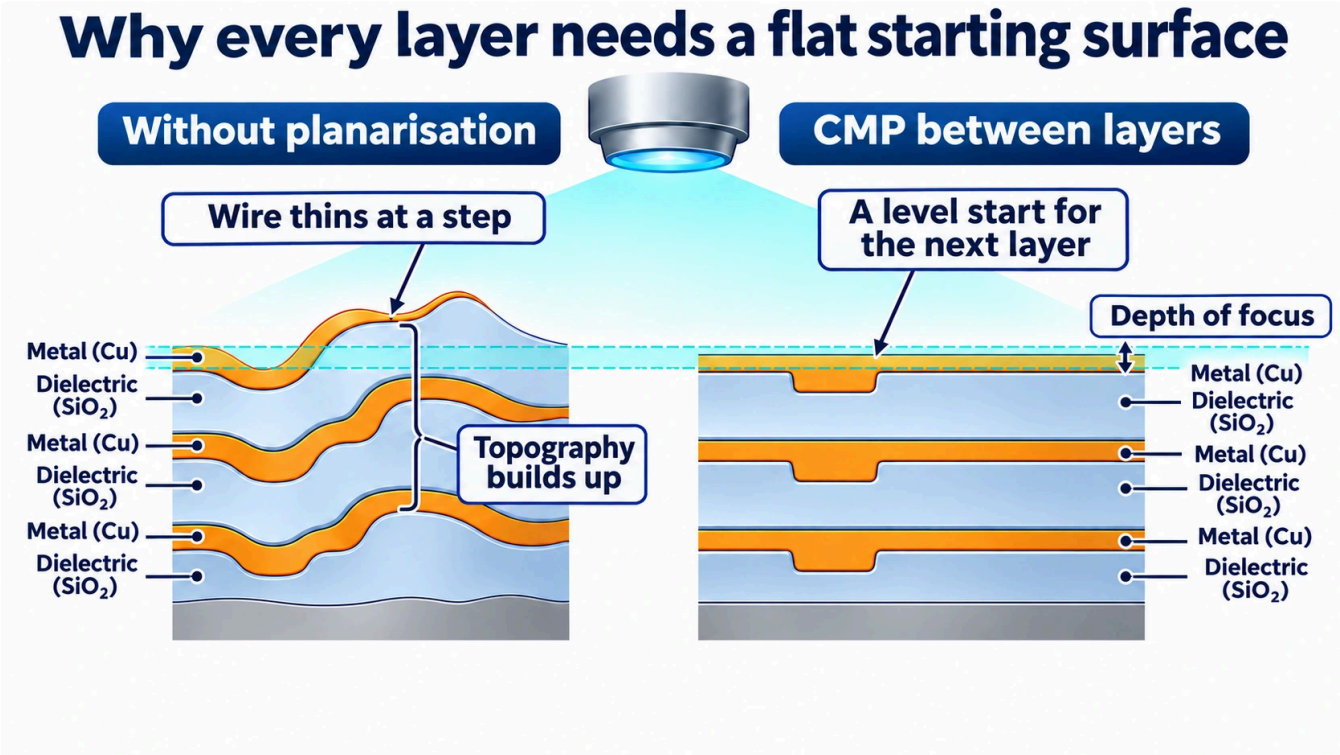


Figure 1. CMP reduces the topography that would otherwise be passed to the next layer. The vertical dimensions and optical field are schematic.

Planarisation can be described at different scales. Rounding a sharp corner helps locally. Reducing height differences across regions of a die is a broader task. CMP can address both local and larger-scale topography by depositing excess material and polishing it back. The step-height ratio, meaning the final step height divided by its initial value, gives one measure of the improvement. [S3, S4]

A historical comparison

Cornell's 2007 introduction describes a transition from roughly three or four wiring levels before CMP to seven or eight with CMP. Those numbers describe the technology discussed in that historical source. They provide context for the importance of planarisation. [3]

- **Earlier approaches to planarisation**

Approach	How it works	Limitation
BPSG reflow	Boron and phosphorus lower the softening temperature of a glass film. A high-temperature treatment allows it to redistribute.	The smoothing distance is limited. The original teaching example uses about 1,000 °C.
Spin-on glass	A liquid precursor spreads across the wafer and is cured into an oxide-like film.	Film quality and unequal shrinkage in thick and thin regions can leave residual steps.
Etchback	A coating fills depressions before material is etched back across the surface.	Matching removal rates and controlling the final profile are difficult.

These methods could smooth local features while leaving different pattern-density regions at different heights. The source material presents this as a major motivation for adopting CMP. [S1, S3, S4]

3. How polishing became a device process

Polishing glass and silicon was already established when manufacturers began considering it for patterned device wafers. The obstacle was contamination. A slurry full of abrasive particles appeared difficult to reconcile with a clean semiconductor process.

In an account reproduced in a 2024 CMP user-group presentation, former IBM scientist Klaus Beyer describes the experiment he performed in January 1983. He took a glass-covered, trenched wafer to an existing wafer-polishing operation. After polishing and megasonic cleaning, he found a broadly level surface. His earlier work on cleaning and polishing-related scratches helped him assess whether the contamination could be removed. [1]

Beyer's account says that he initially kept the result to himself for two weeks, then used IBM's internal open-door route to raise the idea. A small team evaluated device wafers for approximately ten months before the process was accepted for production. The story illustrates how a surface-treatment technique became a practical device-manufacturing step when polishing and cleaning were developed together. [1]

IBM's patent application filed on 28 October 1985 became US 4,944,836 on 31 July 1990. Its central idea was selective chemical mechanical removal of an upper film until it became substantially coplanar with the underlying material. One example fills openings in an insulator with metal and removes the metal above the field. This anticipates the logic of damascene processing. [2]

The broader polishing tradition predates these device applications. Preston's removal-rate relationship originated in glass polishing in 1927. Fujimi's corporate history, for example, records ceria abrasives for optical glass in 1960 and silicon-wafer abrasives in 1967. These are part of the materials background from which device CMP developed. [S4, S12]

4. What happens in a CMP station

The wafer is held **with its device surface facing down** against a pad attached to a rotating platen. The carrier head also rotates. Slurry flows onto the pad, and a conditioner renews the pad surface. [S3, S4]



Figure 2. A single polishing station. The magnified contact region exaggerates particle size and spacing. Production tools can contain several polishing and cleaning stations.

Part	Job	Why its design matters
Platen	Supports and rotates the pad.	Its motion helps establish the relative sliding speed.
Polishing pad	Transfers load and carries slurry at the interface.	Hardness, pores, grooves and compliance affect contact and defects.
Carrier head and retaining ring	Hold the wafer and apply controlled pressure.	The pressure distribution and edge restraint affect uniformity.
Slurry	Supplies reactive chemistry and abrasives.	It must suit the film being removed and the material that should remain.
Diamond conditioner	Renews the pad's surface texture.	A glazed pad can lose its intended removal behaviour.



A pad-conditioning disc, identified as a Chiaping CMP-108 in the source description. Image by cpxmn, Wikimedia Commons, CC BY-SA 2.0. Resized and converted to WebP. Original image and licence

- **Pressure and consumables depend on the process**

The 2007 Cornell primer gives a teaching range of 4–10 psi, or approximately 28–69 kPa. It discusses poor contact at low pressure and wafer damage at high pressure in that context. Actual operating limits depend on the head, film stack and recipe. Pressure is a load per unit area, so it must also be distributed appropriately across the wafer. [3]

Purdue's lecture contrasts example oxide and metal recipes. The oxide example uses silica with alkaline chemistry, particles of 100–250 nm, pH 10.5–11.3 and flow rates of 250–1,000 mL/min. Its metal example uses alumina and ferric nitrate, particles of 180–280 nm, pH 4.1–4.4 and 50–100 mL/min. These are illustrative teaching conditions. They show how strongly slurry design can change with the target film. [4]

- **Polishing is followed by cleaning**

The wafer leaves the pad with slurry residues and particles on it. Keeping it wet until cleaning helps prevent dried deposits from becoming difficult to remove. Soft PVA brushes, cleaning chemistry and rinsing are used to detach residues while limiting scratches and corrosion. Dilute ammonia is one example described in the historical teaching material. [S3, S14]

Integrated production tools combine these steps. Applied Materials describes its Reflexion LK Prime with four polishing pads, six heads, eight cleaning chambers and two drying chambers. It reports increased throughput relative to the preceding system, with gains depending on the application. [8]

5. Why pressure and motion affect removal

- **Preston's relationship**

A common first approximation is **RR = Kp × P × V**. RR is the removed thickness per unit time, P is contact pressure, V is relative sliding speed, and Kp is an empirical coefficient associated with the film, slurry, pad and operating conditions. It describes a useful trend within a suitable process range. A complete prediction of patterned-wafer behaviour requires more detail. [4]

For a fixed recipe, stronger contact or more sliding distance per second often increases removal. However, changing pressure also changes how the pad deforms, and changing speed can affect slurry transport and temperature. Process engineers therefore optimise removal rate alongside uniformity and defectivity.

Why turn the head and platen in the same direction?

Consider the idealised geometry used in the lecture. Let **d** be the vector from the platen centre to the carrier centre and **r** the vector from the carrier centre to a point on the wafer. Their angular velocities are ωp and ωw. The relative velocity is

vrel = ωp × d + (ωp − ωw) × r
Here × denotes the vector cross product. With equal angular velocities in the same direction, the term containing r vanishes. For fixed centre separation, the ideal relative speed has the same magnitude everywhere on the wafer.

This removes one source of speed variation. Pressure, pad condition, chemistry and wafer-edge effects still influence removal. Modern heads use features such as compliant membranes and controlled retaining-ring pressure to help manage those variations. [4]

Worked example. For an assumed centre separation of 0.20 m and a rotation rate of 70 rpm, the ideal relative speed is 2π × 70/60 × 0.20 ≈ **1.5 m/s**. The separation is an assumption for this calculation.

6. Why the high areas disappear first

The slurry changes the surface being polished

For silicon dioxide, water and hydroxide participate in surface reactions. Hydrolysis converts bridging Si–O–Si groups into hydroxylated surface species. Abrasives under load help detach material, and the flowing liquid carries reaction products away. $Si(OH)_4$ is one species discussed in the source treatment of oxide removal. The mechanical and chemical actions are coupled. [S4, S5]

Metal CMP uses different chemistry. Oxidants and other additives control oxidation, dissolution and passivation. Contact can remove a reacted surface film at exposed high areas, allowing the cycle to continue. The formulation must also limit unwanted attack on recessed regions. [4]

Ceria and the “chemical tooth” model

Ceria, CeO_2, has a particular affinity for silica surfaces. In the chemical-tooth model discussed in the STI review, surface cerium groups form Ce–O–Si connections that help detach silicon-containing species. Other proposed mechanisms involve larger fragments or the role of Ce^{3+} surface sites. The microscopic mechanism remains a subject of study. [5]

The review contrasts silica slurries using more than 10 wt% abrasive with ceria examples that achieve useful removal at about 0.25 wt%. These figures illustrate particular reported formulations. Particle concentration alone does not determine performance, and ceria can also introduce defects. Particle size, aggregation, surface chemistry and additives all matter. [5]

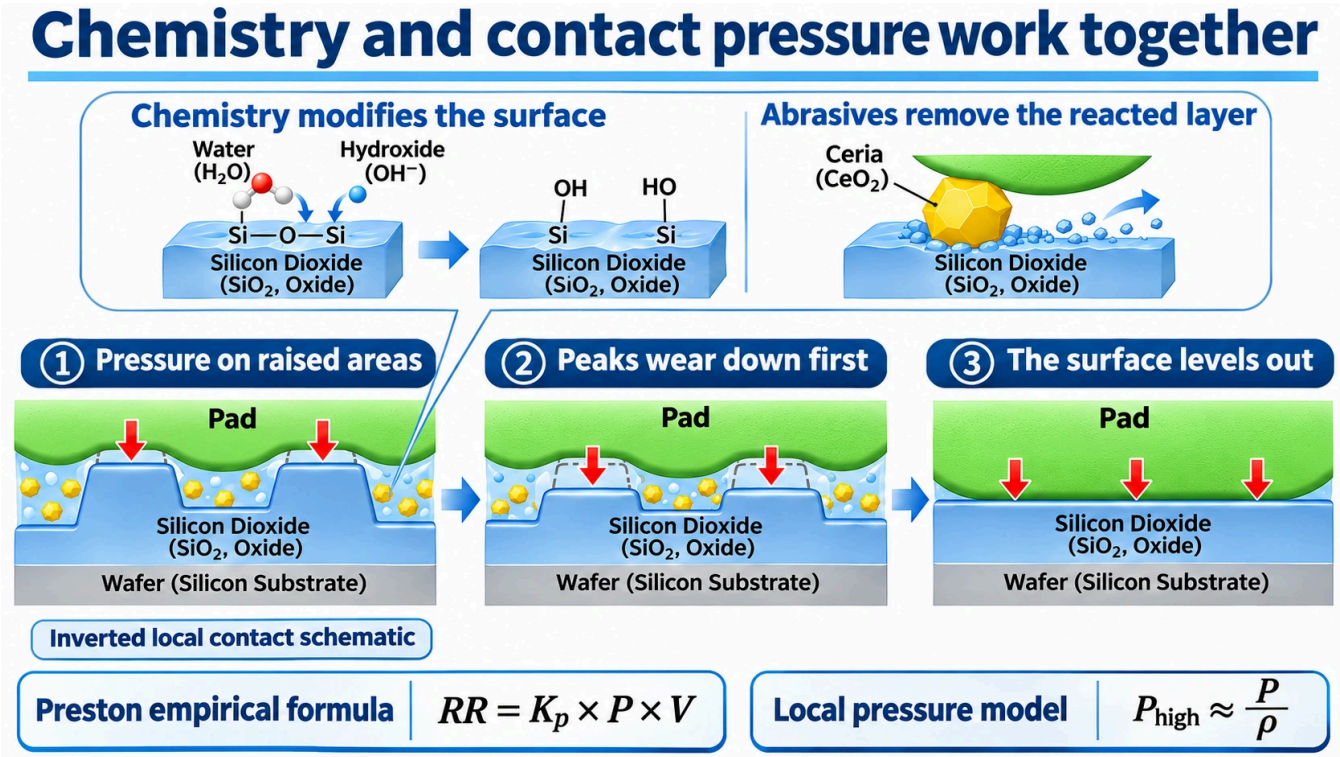


Figure 3. An inverted local contact view puts the wafer below the pad for readability. In the actual station the wafer faces down. The surface chemistry and pressure model are simplified.

A simple load-sharing calculation

Suppose a force F is spread over wafer area A. Its nominal pressure is P = F/A. If the pad initially touches only the raised fraction ρ of that area, an ideal load balance gives **Phigh = F/(ρA) = P/ρ**.

For ρ = 0.5, this model gives twice the nominal pressure on the high areas. For ρ = 0.25, it gives four times the pressure. Combined with Preston's relationship, that predicts faster initial removal at raised areas. This is a teaching calculation that assumes all the load is carried by the peaks and other factors stay fixed. A real pad deforms and can also contact lower regions.

Pattern density therefore affects the outcome. Isolated raised features and dense arrays can polish differently. As the surface levels out, contact spreads over more area and the original concentration of load decreases.

Rate, flatness and defects must be balanced

The lecture describes trends in which higher pressure increases rate but can worsen planarisation as the pad conforms to recesses. A stiffer pad can bridge topography more effectively while increasing defect risk. Higher platen speed can improve planarisation under the conditions discussed. These trends guide recipe development, while the final result must be measured for the specific film stack. [4]

7. Removing the excess and keeping the structure

Selectivity is the ratio of removal rates for two materials. A stop layer is deliberately removed more slowly than the overlying material. It creates a useful process window for clearing excess film while protecting the underlying structure. [S2, S3, S5]

Shallow trench isolation

STI electrically separates neighbouring devices. A thin pad oxide and a nitride mask are formed, trenches are etched into silicon, and oxide fills the trenches and covers the field. CMP clears the oxide above the field while the nitride acts as a relatively slow-polishing stop. The nitride is subsequently stripped in a separate chemical step. Additives that suppress nitride removal can increase oxide-to-nitride selectivity. Bulk removal and finishing may use different stages. [5]

Tungsten plugs and copper damascene

For a tungsten plug, a hole in a dielectric is filled and the excess tungsten above it is polished away. Damascene copper wiring follows the same broad logic at the interconnect level. Pattern the dielectric, deposit the necessary liner and copper, then remove the overburden so that the conductor remains in the recess. [S2, S3]

Copper is difficult to pattern by conventional subtractive dry etching because suitably volatile reaction products are difficult to obtain under practical conditions. Filling a patterned dielectric and using CMP therefore became central to copper interconnect integration. Barrier and liner removal also need control, so production copper CMP commonly involves more detail than the simplified drawing.

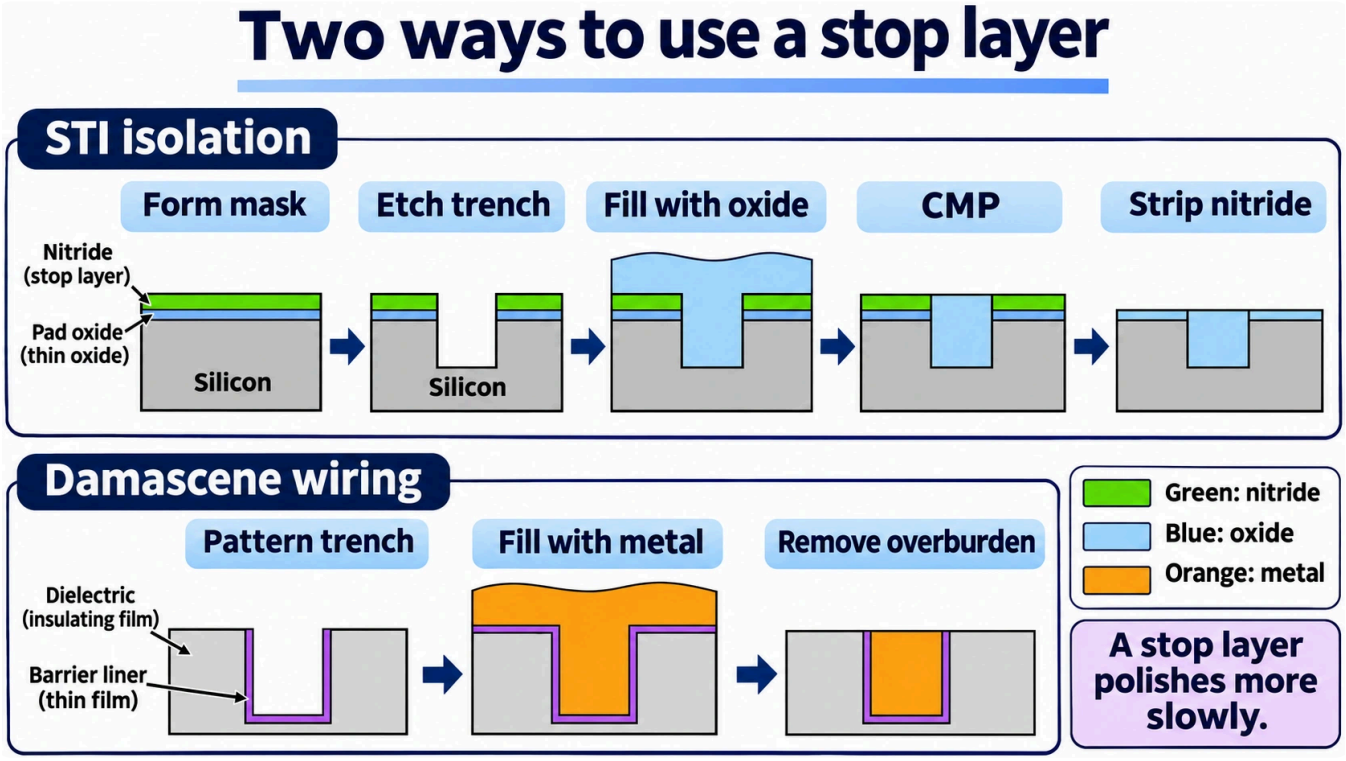
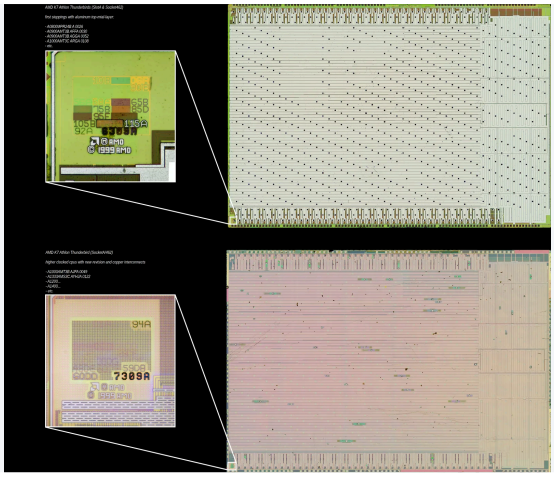


Figure 4. In STI, nitride stripping follows CMP. In damascene, metal and liner over the field are removed while material remains in the trench. Film thicknesses are schematic.



Aluminium and copper interconnect versions of AMD Athlon Thunderbird, as identified in the source description. The comparison connects the polishing process to a familiar class of electronic device. Image by FritzchensFritz, Wikimedia Commons, CC0. Resized and converted to WebP. Original image

8. How a good polishing step can go too far

A slow-polishing stop film still has a finite removal rate. Patterned regions also redistribute contact pressure. Continuing after the overburden has cleared can therefore change the structure that was meant to remain. [3][4][5]

Effect	What the cross-section shows	What contributes
Recess	A filled feature ends below its surroundings.	The filled material may remove faster or experience chemical attack.
Dishing	A broad feature develops a concave top.	Pad deformation and continued removal within the wide feature.
Erosion	A dense patterned region loses both conductor and intervening dielectric.	Pattern-dependent contact and removal during overpolishing.

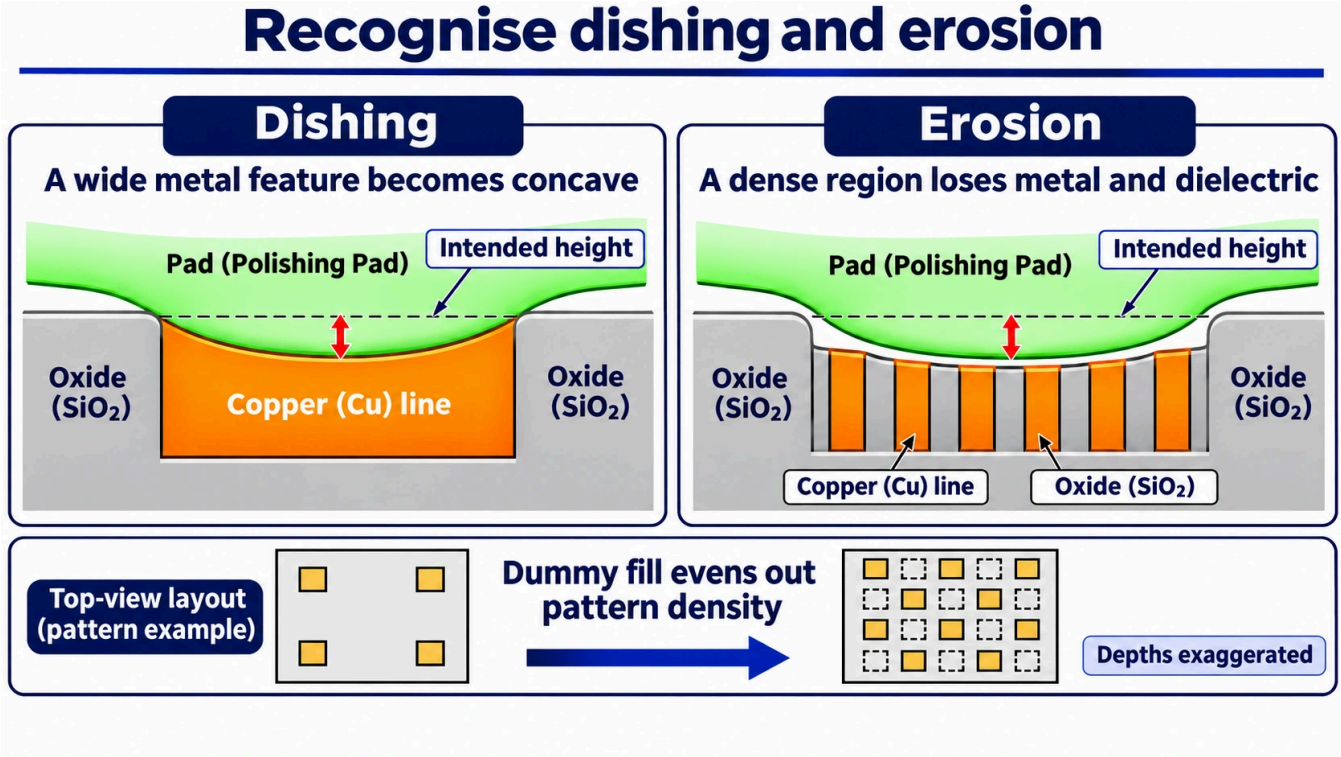


Figure 5. Dishing concerns the profile within a feature. Erosion concerns the loss of a patterned region relative to its surroundings. Depths are exaggerated.

Blanket-film selectivity does not by itself predict what a patterned wafer will do. The Cornell primer gives a 300:1 polysilicon-to-oxide example but cautions that erosion can reduce the effective selectivity seen in patterned structures. [3]

Dummy fill adds non-functional features to sparse areas to make pattern density more consistent. Layout decisions can therefore affect polishing results. **Endpoint detection** provides another control. Changes in motor current or optical signals can indicate that the exposed material has changed, helping determine when to move to the next stage or stop. [S3–S5, S9]

Scratches and residues are equally important. Agglomerated abrasives, pad defects and contamination can produce microscratches. Cleaning must remove particles and residues without adding damage. This connects CMP directly to the cleaning processes introduced in lesson 3-1. [S3, S5, S14]

9. The global CMP supply chain

CMP performance depends on a combination of equipment, slurry, pad, conditioner and cleaning. Suppliers contribute different parts of that combination. The following overview groups them by function.

- **Equipment and process integration**

The METI presentation cited by the Japanese article reports a CMP equipment market of **¥424.2 billion**, with Applied Materials at 51%, EBARA at 34% and Hwatsing Technology at 11%. The equipment chart does not state its measurement year. These figures should be read as the source's reported market snapshot. The two largest shares add to 85%; the 4% remainder in Figure 6 is calculated by subtraction. [6]

Supplier	Base	Examples of contribution
Applied Materials	United States	Integrated polishing, cleaning and drying. Its Reflexion LK Prime can split long polishing tasks across multiple platens. [8]
EBARA	Japan	CMP systems within a broader precision-machinery business. The company reports cumulative CMP shipments above 4,000 systems and describes itself as the second-largest supplier. [7]
Hwatsing Technology	China	300 mm CMP systems, endpoint control and applications extending into advanced packaging. Its annual report describes adoption in memory production. [9]

Productivity and adoption statements are attributed to the companies concerned. Hwatsing's reported share above 90% concerns domestically produced CMP equipment in its stated market context. It is a different measure from the global equipment shares above. [9]

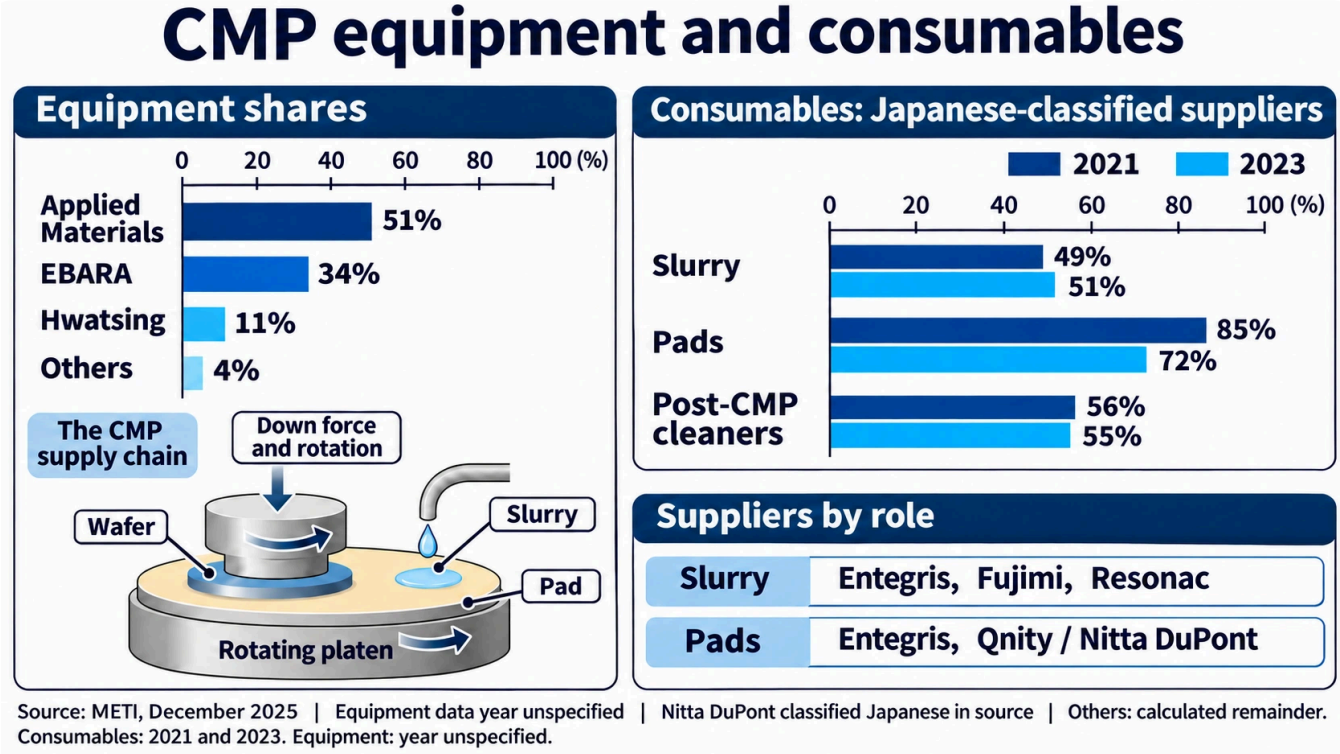


Figure 6. Market figures carried over from the Japanese article's cited METI presentation. Equipment data year unspecified. Consumables compare 2021 and 2023. The source classifies the Osaka-based Nitta DuPont joint venture as Japanese. Supplier examples identify roles and do not indicate rankings or purchasing relationships. [6]

Slurry, pads and cleaning materials

Entegris supplies CMP slurries, pads, post-CMP cleaning chemistry, PVA brushes and filtration. Its acquisition of CMC Materials in July 2022 brought the former Cabot Microelectronics business into the group. Its reporting describes film-specific products and development for emerging interconnect materials. [14]

Fujimi developed its PLANERLITE CMP slurry line in 1995. Its product range distinguishes oxide, tungsten, polysilicon, copper and barrier-film applications, showing why one slurry recipe cannot be assumed to suit every film. [S12, S13]

Resonac supplies CMP slurries including ceria-based formulations. It reports leading positions for ceria slurry and STI slurry in specified market studies and years. Its nano-ceria materials are presented as a way to combine polishing performance with lower scratch risk. These are company-attributed product and market statements. [S10, S11]

Qnity, separated from DuPont's electronics business on 1 November 2025, supplies pad families including IC1000. Its filings describe pads for a range of planarisation applications, with groove designs and other features adapted to customer needs. Nitta DuPont is also relevant to pad supply and to the classification used in METI's historical data. [S6, S15, S16]

The Japanese suppliers' significant position in consumables remains relevant to a global account. METI's data show Japanese-classified suppliers at 49% then 51% of CMP slurry, 85% then 72% of pads, and 56% then 55% of post-CMP cleaning chemicals in 2021 and 2023 respectively. The pad change is a decrease of 13 percentage points. The joint-venture classification and the historical dates are important when interpreting these shares. [6]

Where materials engineering matters
Abrasive composition, particle size and aggregation affect both removal and scratches. Additives tune reactions and selectivity. Pad structure controls contact and slurry transport. Cleaning formulations and filters help manage residues. These materials must work together with the tool and the film stack.

10. What makes CMP increasingly demanding?

Thicker stacks. Large topography and thick films in 3D NAND can require extended removal. Multiple controlled polishing stages are one response described by equipment suppliers. [8]

Advanced packaging. Hybrid bonding, through-silicon vias and wafer thinning introduce demanding surface-preparation tasks. Hwatsing's reporting discusses CMP across bonding-surface preparation, thinning and TSV metallisation. The inference for integration is that surface planarity and cleanliness become increasingly consequential as bonding requirements tighten. [9]

New materials. Molybdenum and ruthenium interconnects, and hard semiconductor substrates such as SiC and GaN, require appropriate polishing chemistry and materials. The film, abrasive and pad must be evaluated together. [14]

Smaller defect budgets. A small scratch or particle can compromise a fine structure. Removal rate, selectivity, uniformity and post-CMP cleanliness therefore need to improve together. [5]

11. Bringing the process together

CMP creates a usable surface for the next manufacturing step by controlling both reaction and contact. Raised areas initially carry more load, selective chemistry helps clear the intended film, and endpoint control limits further removal. Cleaning completes the operation.

Lesson 3-12 follows the conductor left inside the dielectric. It examines damascene copper wiring, multilayer interconnects and the idea of delivering power from the back of a transistor wafer.

12. Check your understanding

▼ Why can uneven films cause trouble in both lithography and wiring?

Different surface heights can exceed the usable depth of focus. Metal deposited over steps can also thin at corners, raising local resistance.

▼ Which surface of the wafer faces the polishing pad?

The device surface faces down. The carrier holds and loads the wafer while slurry and the moving pad act at the interface.

▼ Why was device CMP initially considered difficult to introduce?

The abrasive slurry created contamination and scratch concerns. Practical adoption required effective cleaning as well as controlled polishing.

▼ What do P, V and Kp mean in Preston's relationship?

P is contact pressure, V is relative sliding speed and Kp is an empirical coefficient associated with the materials and process conditions.

▼ What follows from equal head and platen angular velocities in the ideal model?

The position-dependent term cancels. With fixed centre separation, the ideal relative speed is uniform across the wafer. Other causes of removal non-uniformity still require control.

▼ If only one quarter of the area carries the load, what does the simple pressure model predict?

The local pressure is four times the nominal value. Applying Preston's approximation would predict four times the removal rate if all other factors stayed fixed.

▼ What does the nitride do during STI CMP?

It polishes more slowly than the oxide and acts as a stop layer while the oxide overburden is removed. It is stripped separately afterwards.

▼ How do dishing and erosion differ?

Dishing makes the top of an individual broad feature concave. Erosion lowers a dense patterned region, including its intervening dielectric.

▼ Why add dummy fill to a circuit layout?

It reduces pattern-density differences that would otherwise contribute to uneven polishing.

▼ Why should the market chart be read with its footnotes?

The equipment measurement year is unspecified, consumables refer to 2021 and 2023, and a joint venture is classified as Japanese in the source. Different market definitions are not directly interchangeable.

13. Terms used in this lesson

Term	Meaning
CMP	Chemical mechanical polishing, also called chemical mechanical planarisation.
Planarisation	Reducing surface-height differences over a useful lateral range.
Depth of focus	The permitted focus range for an acceptable lithographic image.
Step-height ratio	Final step height divided by initial step height.
BPSG / SOG	Boron- and phosphorus-doped glass / spin-on glass.
Slurry / abrasive	The polishing liquid formulation / its solid polishing particles.
Pad / conditioner	The contact sheet on the platen / the disc that renews its texture.
Retaining ring	The ring around a wafer in a carrier head that helps restrain it and manage edge contact.
Preston coefficient	The empirical factor Kp in a pressure–speed removal model.
Pattern density	The fraction of a chosen area occupied by a specified type of feature.
Selectivity / stop layer	A ratio of removal rates / a relatively slow-polishing layer used for process control.

Term	Meaning
STI	Shallow trench isolation, which uses dielectric-filled trenches to separate devices.
Damascene	Forming conductors by filling patterned recesses and removing excess material above them.
Dishing / erosion	Concavity within a broad feature / loss across a patterned region.
Dummy fill	Non-functional layout features added to help control local pattern density.
Endpoint detection	Using a measured signal to help identify the end of a polishing stage.
Post-CMP cleaning	Removing polishing residues and particles before the wafer proceeds.

14. Sources

The references retain the numbering used throughout this lesson. Historical teaching examples, supplier statements and calculations are identified in the text.

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14. Entegris, Form 10-K for the year ended December 2024, Item 1. Source document

15. Qnity Electronics, IC1000 CMP Polishing Pads. See also the English-language Qnity registration disclosure for pad families. Source document

16. DuPont, DuPont Completes Separation of Qnity Electronics, 3 November 2025. Source document

17. EBARA, corporate website and company history. Source document

Additional primary source for pad families Qnity registration disclosure, June 2025.

15. How the evidence is used

Topic	Basis	How to read it
IBM history and selective polishing patent	S1, S2	Historical account and patent claims
Focus, earlier planarisation and tool components	S3, S4	Teaching material with historical examples
Preston relationship, motion and pattern effects	S4	Empirical model and lecture examples
Oxide chemistry, ceria and STI	S5	Review of reported mechanisms and formulations
Pressure amplification and 1.5 m/s example	Calculations in this lesson	Explicit idealisations and assumed centre separation
Equipment and consumables shares	S6	Historical source data with measurement-year and classification caveats
Equipment products, adoption and capabilities	S7–S9	Attributed company reporting
Materials, product ranges and corporate changes	S10–S17	Company disclosures and product information
Growing importance of bonding-surface preparation	S9 and interpretation in this lesson	Application reporting followed by a stated inference

Illustrations created with ImageGen. Film thicknesses, particle sizes, surface profiles and optical fields are schematic. The article retains the supplied lesson's market data and source definitions.

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