SEMICONDUCTOR FRONT-END · PART 3-12

Interconnects
Building the wires that make billions of transistors work together

A transistor can switch, but a useful chip needs connections. Signals must travel between devices, clocks must arrive at the right time, and power must reach the circuits with an acceptable voltage loss. This lesson follows the multilayer wiring stack, explains copper dual damascene and low-k dielectrics, then examines the limits of narrow metal lines and the move towards backside power delivery.

Semiconductor manufacturing series · Advanced introduction

Suggested preparation: sputtering, electroplating and CMP · Updated 19 November 2026

What you will learn

- How local, intermediate and global wiring divide the task of connecting a chip.
- Why resistance and capacitance make long, narrow interconnects difficult to scale.
- How dual damascene forms a trench and its connecting via in one metal-fill operation.
- Why lower permittivity, thinner barriers and alternative metals involve trade-offs.
- How electromigration damages wires and why backside power changes the routing architecture.

Contents

1. The lesson in three ideas
2. Why there are so many wiring layers
3. Why a smaller wire can be a slower wire
4. How dual damascene makes copper wiring
5. Making the insulation store less charge
6. What happens when copper gets extremely narrow?
7. Electromigration and the movement of atoms
8. Power delivery from the back of the wafer
9. The equipment chain behind an interconnect
10. Materials and interfaces across the supply chain
11. How the challenges connect
12. Check your understanding
13. Terms used in this lesson
14. Sources
15. How the evidence is used

1. The lesson in three ideas

The wiring has a hierarchy. Fine lines close to the transistors connect nearby devices. Higher layers use larger conductors for longer distances and power distribution. Many layers are needed to accommodate all these functions.

Interconnect performance depends on both metal and dielectric. Copper reduces resistance compared with the aluminium systems it displaced. Low-k insulation reduces capacitive loading. At very small dimensions, scattering, barrier thickness and reliability become increasingly important.

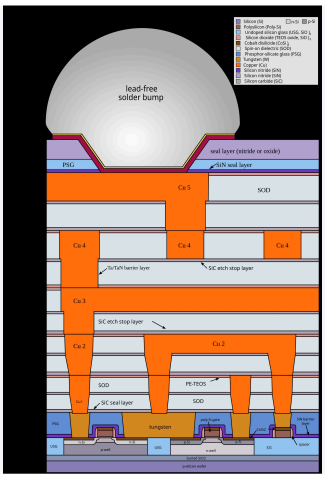
Power delivery is changing sides. A backside power network can bring power towards the devices through a separate route, leaving more frontside resources for signals. Bonding, thinning, alignment and thermal design become central parts of that integration.

2. Why there are so many wiring layers

- **Above the transistors**

The front-end-of-line, or FEOL, creates the transistor structures. Contacts and local connections link them to the back-end-of-line, or BEOL, where successive metal and dielectric layers form the wiring network. In this series, BEOL is still part of wafer fabrication. Assembly and packaging follow later.

The historical CMOS cross-section below shows how the pieces fit together. It contains transistors, tungsten plugs, copper layers, diffusion barriers, etch-stop films and a solder bump at the top. Its five copper levels are an example from an earlier technology generation. [8]



CMOS chip structure from the early 2000s. The source labels the copper barrier as Ta/TaN and interlayer etch stops as SiC. Image by Cepheiden, Wikimedia Commons, CC BY 2.5, rendered and converted to WebP. Original and licence

More recent stacks can be much deeper. Imec uses 15–20 BEOL levels when explaining the path of frontside power delivery. The 2024 IRDS roadmap also projects an increase in interconnect layer count from 15 to 19 over its tabulated horizon. These are source-specific examples rather than a fixed layer count for every chip. [5][7]

- **Different distances need different conductors**

Stanford's lecture groups wires by reach into local, intermediate and global interconnects. It also distinguishes signal, clock, and power-and-ground functions. A short connection between nearby transistors has different requirements from a conductor spanning a large part of the die. [2]

IBM's account of copper integration describes a hierarchy with fine lower wires and wider, thicker upper wires. The lower levels prioritise density and manageable capacitance. The upper levels reduce resistance over long paths. In the 1999 example, the finest wires were about 0.25 µm wide and the upper wires roughly an order of magnitude wider. Those dimensions describe that historical implementation. [1]

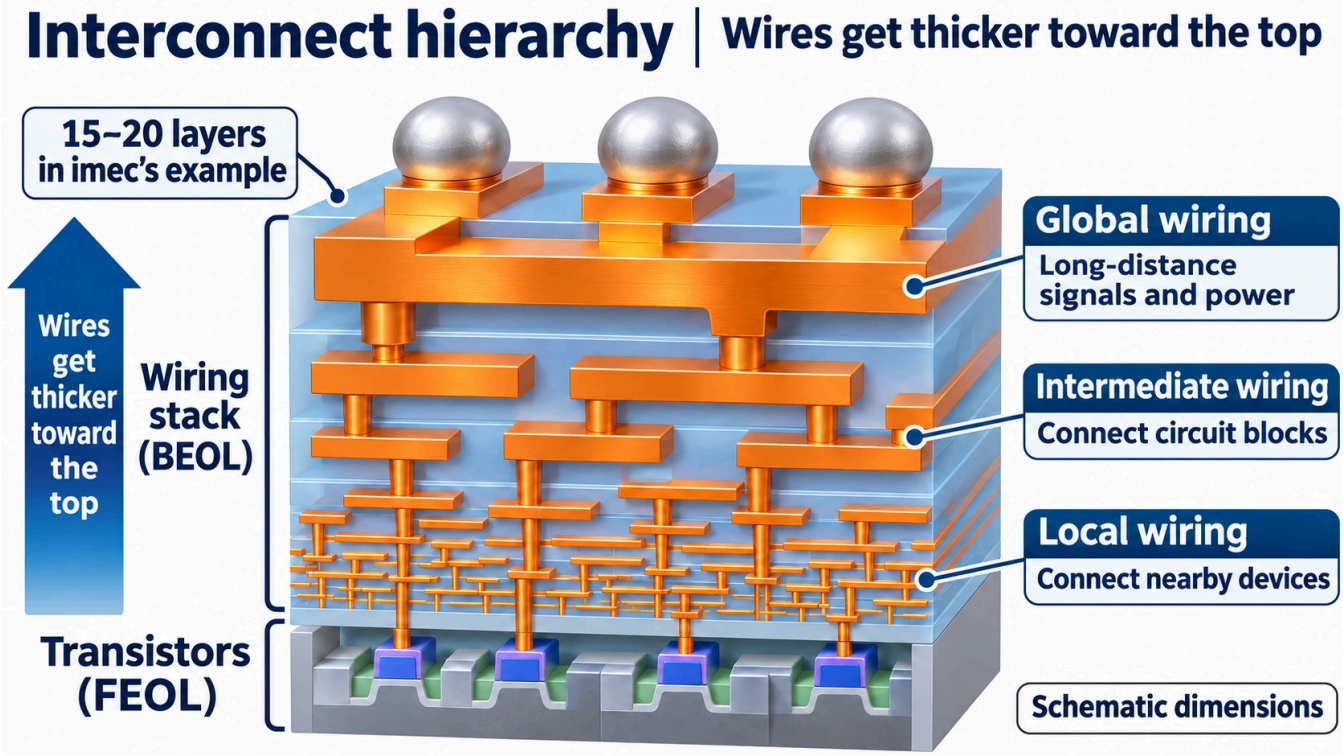
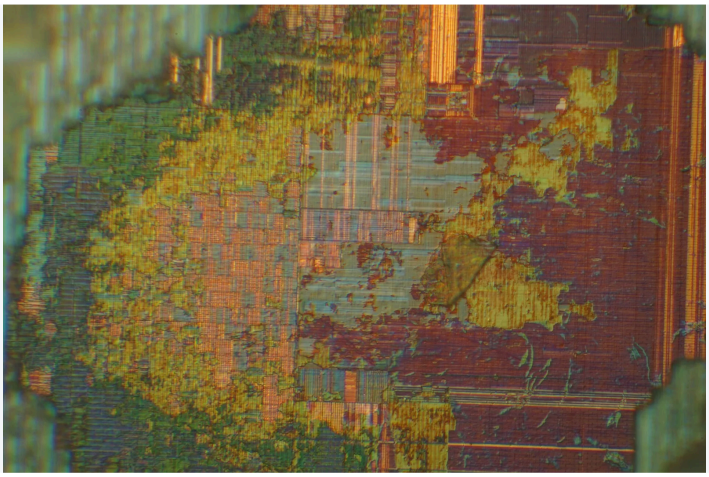


Figure 1. A wiring hierarchy. Individual layers and their connections are simplified. The layer-count example comes from imec's discussion of frontside power delivery. [1][2][7]



A Core i5-6600K with portions of the upper wiring layers removed, as described by the source. The photograph makes the multilayer structure visible. Image by cole8888, Wikimedia Commons, CC BY-SA 2.0, resized and converted to WebP. Original and licence

3. Why a smaller wire can be a slower wire

Resistance meets capacitance

Changing a logic signal means charging or discharging capacitance along a resistive path. A useful first estimate of interconnect delay therefore involves the product **RC**. The complete delay also depends on the driver, receiver, wire distribution and coupling to nearby conductors.

Simple geometric relationships
$R = \rho L/(WH)$

$C_{side} \approx \kappa\varepsilon_0 HL/S$, and **$C_{vertical} \approx \kappa\varepsilon_0 WL/X$**

L is wire length, W is width, H is thickness, S is lateral spacing, X is vertical dielectric separation, ρ is metal resistivity, κ is relative permittivity and ε_0 is vacuum permittivity. The capacitance expressions are parallel-plate approximations. Fringing fields and real stack geometry add further contributions. [2]

Closely spaced neighbours can contribute substantially to capacitance. The lecture gives an example in which lateral coupling accounts for about 70% of the total. That proportion depends on the geometry. Coupling affects delay, switching energy and crosstalk, so the insulation is part of the electrical design. [2]

A scaling example with a fixed wire length

Keep the length L unchanged, and halve W, H, S and X. Also keep ρ and κ fixed. The cross-sectional area WH becomes one quarter as large, making resistance four times greater. The ratios H/S and W/X stay unchanged, so the capacitance in this simplified model remains approximately constant. The resulting RC product is about four times larger.

This calculation captures a particular problem for long wires that cannot shrink with the transistor. If a local wire's length also shrinks, its scaling behaves differently. The historical trend in the lecture shows transistor delay improving while long-wire delay becomes increasingly restrictive. It is a useful explanation of the interconnect bottleneck. [2]

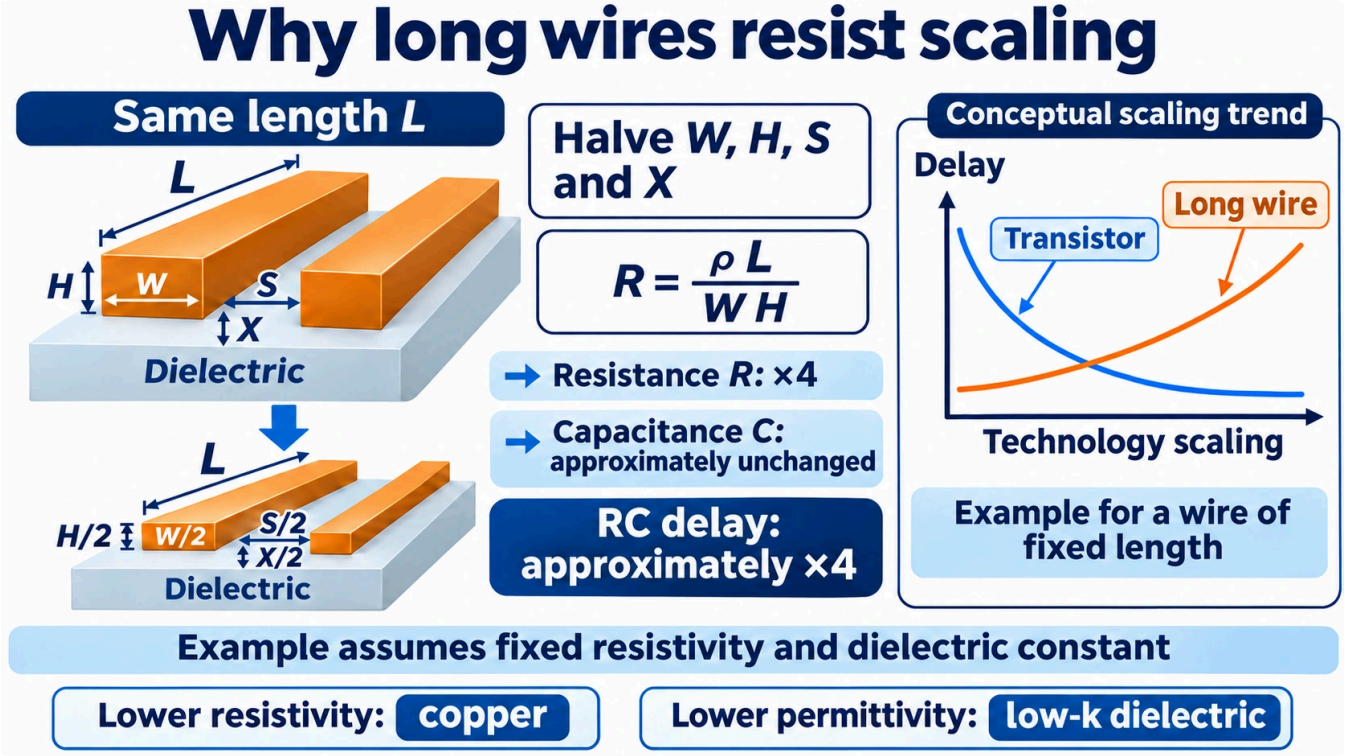


Figure 2. A worked scaling example, with every stated transverse dimension halved. The trend chart is conceptual and has no numerical time scale.

The equations suggest two material approaches. A lower-resistivity conductor reduces R. A lower-permittivity dielectric reduces C. Copper and low-k materials were introduced to address these different parts of the same problem.

4. How dual damascene makes copper wiring

- **Pattern the dielectric, then fill it**

Aluminium wiring could be made by depositing a blanket metal film and etching it into the desired shape. Copper created a different integration challenge. IBM's account identifies deposition, patterning and containment as three linked problems. Copper is difficult to pattern by conventional subtractive reactive-ion etching under practical conditions, and its diffusion into neighbouring material must be controlled. [1]

Damascene reverses the patterning sequence. Trenches are made in the dielectric first. Copper is deposited to fill them, and CMP removes the excess above the field. The copper left in the trenches becomes the wiring.

Dual damascene extends the idea to the trench and its vertical connection, the **via**. Both cavities are filled in one metal-deposition sequence and planarised together. The lithography and etch steps can still involve several operations. “Dual” describes what is filled together. [1]

- **The sequence**

1. **Build the dielectric stack.** Place a cap or etch-stop film above the previous wiring level, followed by the required dielectric films.

2. **Etch the via and trench.** The via must reach the intended lower conductor. The local cap is opened at the connection.
3. **Deposit barrier, liner and seed as required.** A TaN/Ta-based system is a familiar copper example. A conductive seed provides the starting surface for electroplating.
4. **Electroplate copper.** Controlled chemistry and deposition conditions fill the cavity without leaving a void. Excess copper also forms above the field.
5. **Use CMP.** Remove the copper overburden and field barrier, leaving the conductor and its buried liner in the patterned recess.
6. **Cap the level.** Seal the copper before building the next interconnect level.

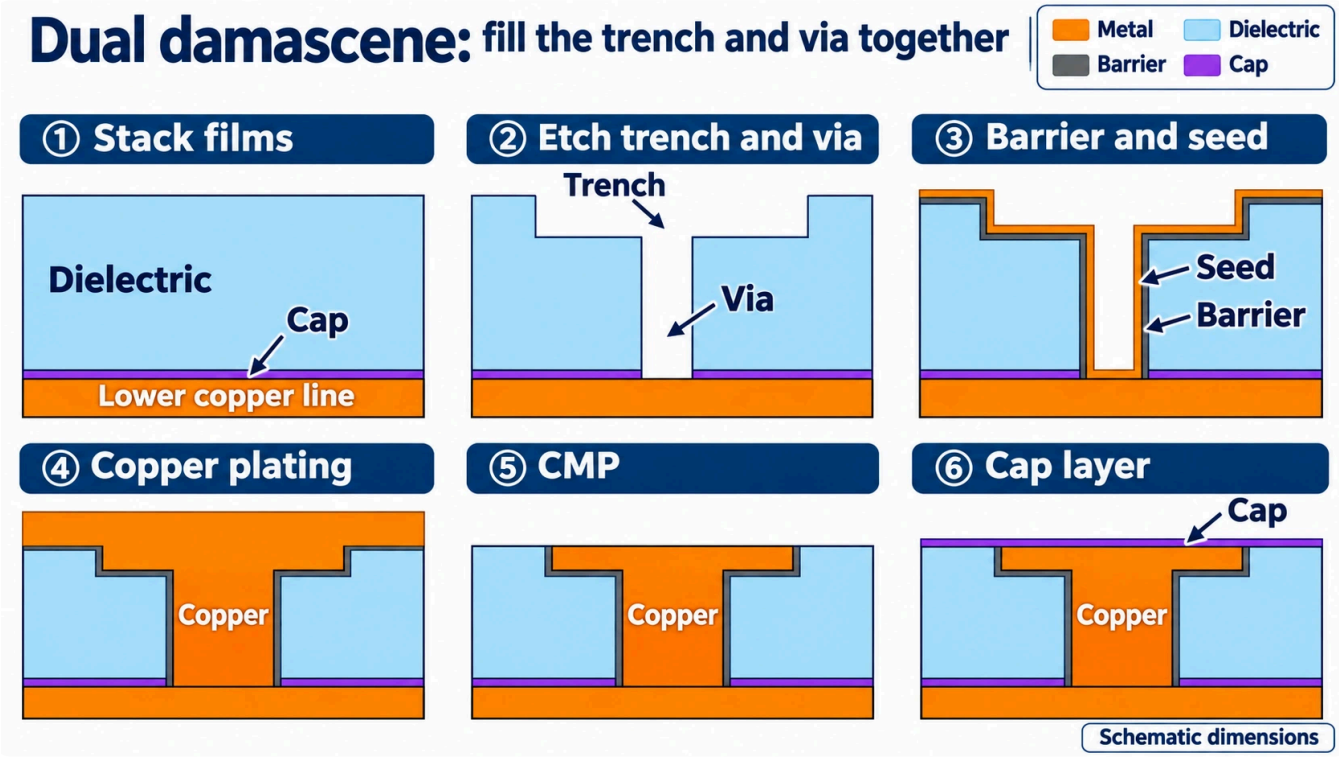


Figure 3. Read the numbered panels from the top row to the bottom row. The via passes through the lower cap to connect to the previous copper level. Trench-first and via-first integrations, film stacks and deposition methods vary. [1]

Why the thin surrounding films matter

The barrier limits copper diffusion into the dielectric or silicon. The top cap closes the conductor and can also contribute to etch control for the next level. Interfaces influence adhesion and reliability as well as diffusion. IRDS highlights barrier and interface quality as important to electromigration lifetime. [5]

These surrounding layers occupy physical space. As the line gets narrower, a liner that cannot be proportionally thinned leaves a smaller fraction of the nominal opening available for low-resistance copper.

The transition to copper

IBM's technical account describes early damascene plating wafers in late 1989 and early 1990, followed by a programme reorganisation in 1994 that selected dual damascene for cost and integration advantages. It records the public copper announcement in September 1997 and product shipments in June 1998, with manufacturing at Burlington. The change required the metal, deposition, patterning and reliability scheme to work together. [1]

5. Making the insulation store less charge

What a lower κ changes

A dielectric polarises in an electric field. Its relative permittivity κ describes that response. For a fixed geometry, capacitance is proportional to κ. At the same applied voltage, **Q = CV** means that a lower capacitance stores less charge. This reduces the charge that a driver must move when a signal switches.

Lower κ can be achieved by changing chemical composition, reducing network density, introducing pores and avoiding absorbed water. Stanford's examples progress from dense silicon dioxide through modified oxides to porous films and air gaps. [3]

Material or structure	Illustrative κ	What changes
SiO_2	About 4	A relatively dense oxide network.
Fluorinated oxide, SiOF	About 3.7; a cited range is 3.3–3.9	Composition changes the dielectric response.
Carbon-modified oxide, SiOC(H)	2.8–3.5	Groups such as CH_3 modify and terminate parts of the network.
Porous oxide	1.8–2.5	Small voids reduce the effective permittivity.
Air gap	Approximately 1 in the cavity	A deliberately formed space replaces some solid dielectric between conductors.

The effective permittivity of a complete interconnect stack also includes liners, caps, surrounding material and geometry. An air cavity with κ near 1 does not make the whole stack's effective κ equal to 1.

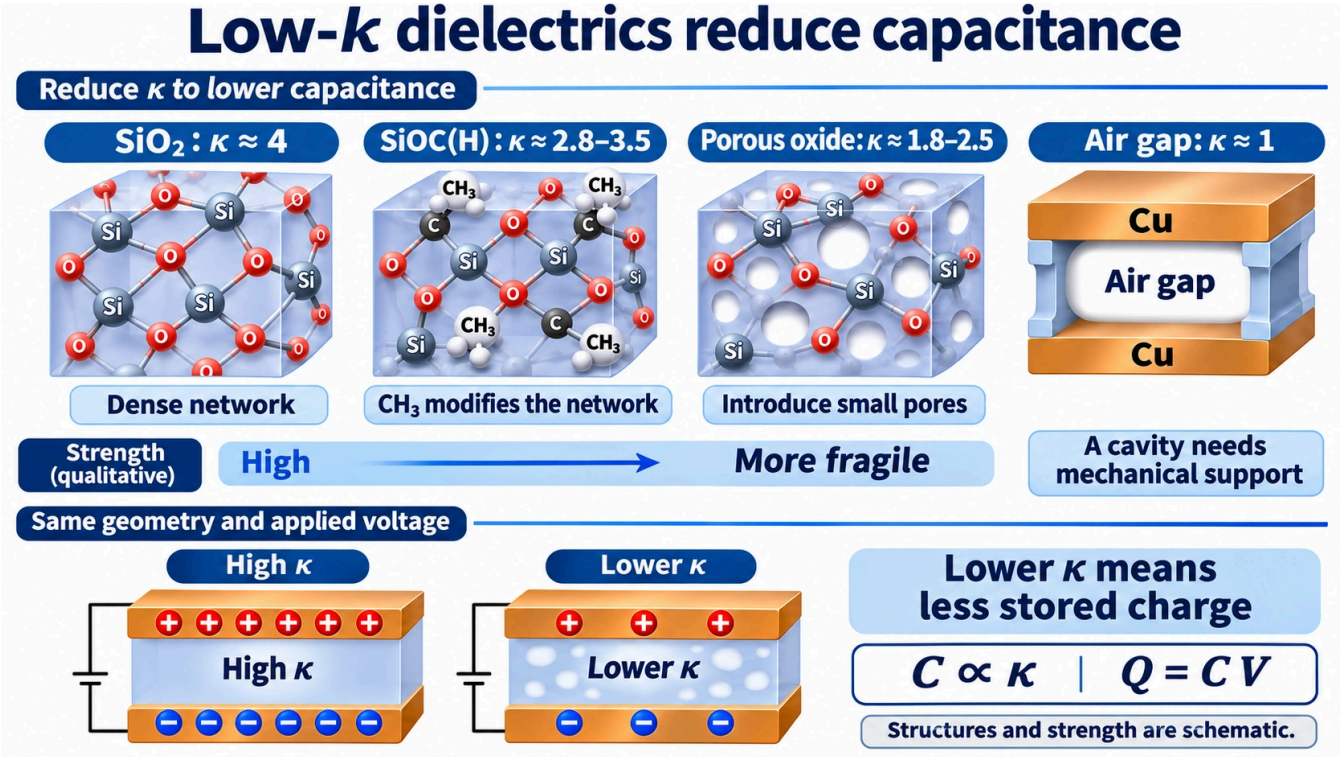


Figure 4. The charge symbols compare equal geometry and voltage. The structural drawings are conceptual. The κ ranges come from teaching material and the roadmap, and are not specifications for every commercial film. [3][5]

- **The mechanical cost**

A more open network can be mechanically weaker and less robust during processing. The lecture cites examples with thermal and mechanical properties substantially below those of dense SiO_2. The roughly tenfold comparison in that material describes particular low-k examples, not a universal factor for every film. [3]

IRDS describes adhesion, CMP damage and package-induced stress as obstacles to further κ reduction. Introducing extensive porosity becomes difficult, making intentional air gaps an alternative integration route. The surrounding structure must still support the conductors and survive later processing. [5]

Applied Materials' Black Diamond family illustrates a tool-and-film approach. Its product description gives an early dense film near κ = 3.0 and a nanoporous Black Diamond II example near κ = 2.55. A porogen-containing film is deposited and ultraviolet treatment removes the pore-forming organic material. The supplier describes both the dielectric benefit and the need to maintain mechanical strength. [10]

6. What happens when copper gets extremely narrow?

- **Resistivity becomes size-dependent**

The expression R = ρL/A is still useful, but the resistivity ρ need not remain equal to its bulk value. A room-temperature mean free path of about 39 nm is commonly used for copper in the cited study. When wire dimensions and grain sizes approach this scale, surfaces and grain boundaries provide additional opportunities for electron scattering. [6]

The liner fraction adds another penalty. A very narrow opening can contain a significant proportion of barrier and liner material, leaving less copper area than its outside dimensions suggest. A lower bulk-resistivity metal alone therefore cannot settle the resistance of the integrated line.

A grain-boundary calculation

The cited paper discusses the Mayadas–Shatzkes model. One approximate expression used in the lesson is

$$\rho/\rho_0 \approx 1 + 1.5 \times r/(1 - r) \times \lambda/D$$

Here ρ_0 is bulk resistivity, λ is mean free path, D is average grain size and r is the assumed grain-boundary electron-reflection probability. The lower-case r distinguishes this probability from electrical resistance R.

Taking λ = 39 nm, D = 20 nm and r = 0.3 gives $1 + 1.5 \times 0.3/0.7 \times 39/20 \approx$ **2.25**. This is an illustrative estimate from the stated approximation. It omits surface scattering and barrier-volume effects and is not a measurement of a particular manufactured wire. [6]

- **Why consider cobalt, ruthenium or molybdenum?**

An alternative metal may offer a different combination of scattering behaviour, grain structure, liner requirements, deposition behaviour and reliability. Bulk resistivity is only one part of the comparison.

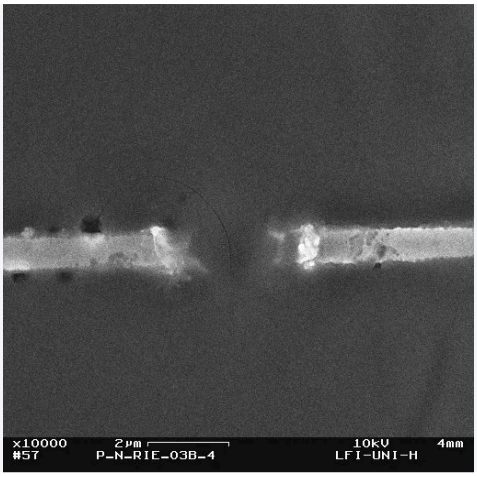
The 2022 study compares grain-boundary reflection in several face-centred-cubic metals. It estimates copper's random-boundary reflection probabilities at about 0.28–0.39 and finds larger reflection probabilities for several other metals in that group. Its conclusions do not establish that every metal beats copper when made small. Grain structure and crystal class matter. Cobalt and ruthenium are outside that particular face-centred-cubic comparison. [6]

The 2024 IRDS roadmap expects copper to remain important through at least 2029 while considering non-copper materials for the lowest interconnects and vias. It discusses cobalt, ruthenium and molybdenum in the relevant roadmap context. A chip can therefore combine materials chosen for different levels rather than require one conductor for the entire stack. [5]

7. Electromigration and the movement of atoms

At high current density, electrons transfer momentum to the metal system. Atomic transport can accumulate material in some places and deplete it in others. This is **electromigration**, often explained using the image of an electron wind. A void can grow in a depleted region until the conducting path fails. The actual failure site depends on geometry, interfaces, current direction and material transport paths. [1][5]

IBM's historical comparison reported copper lifetimes more than 100 times those of a titanium-clad aluminium alloy under its stated accelerated test conditions of 295 °C and 2.5 million A/cm². This is a comparison under those test conditions, rather than a universal lifetime multiplier for all copper wiring. [1]



Electromigration failure in a copper interconnect. The source notes that the upper protective films were removed for observation. Image by Patrick-Emil Zörner, Wikimedia Commons, public domain, converted to WebP. Original image

A scaling model for lifetime

IRDS discusses a model in which lifetime scales approximately as **wh/j**, with width w, thickness h and current density j. If current I is held fixed, j = I/(wh), making the model's lifetime proportional to **$(wh)^2/I$**.

Halving both w and h reduces wh to one quarter. Squaring that area gives a factor of **1/16**. This result follows from the chosen fixed-current model. Real reliability also depends strongly on temperature, diffusion paths, stress, geometry and how operating current changes. [5]

IRDS discusses measures such as alloyed copper seed layers and thin cobalt-containing caps at the copper–SiCN interface. They address the paths along which atoms can move. Barrier and cap engineering, grain control and current-density limits all contribute to reliability. [5]

8. Power delivery from the back of the wafer

- **The frontside routing problem**

Traditional frontside wiring carries both signals and power. Power enters through relatively large conductors, then travels through the stack towards smaller connections near the transistors. Resistance along the delivery path causes a voltage loss, often described as **IR drop**. The time-dependent supply behaviour can include additional effects as well.

In imec's account, power routing uses at least 20% of the routing resources in the discussed architecture. The article also describes the difficulty of maintaining its stated 10% voltage-loss budget. These figures describe that source's design context. [7]

Give power a separate route

A backside power delivery network moves major power-distribution wiring to the wafer's other side. Wider, lower-resistance conductors can bring power towards the devices through short connections. Frontside routing space is released for signal connections, and some standard-cell designs can be made more compact. [7]

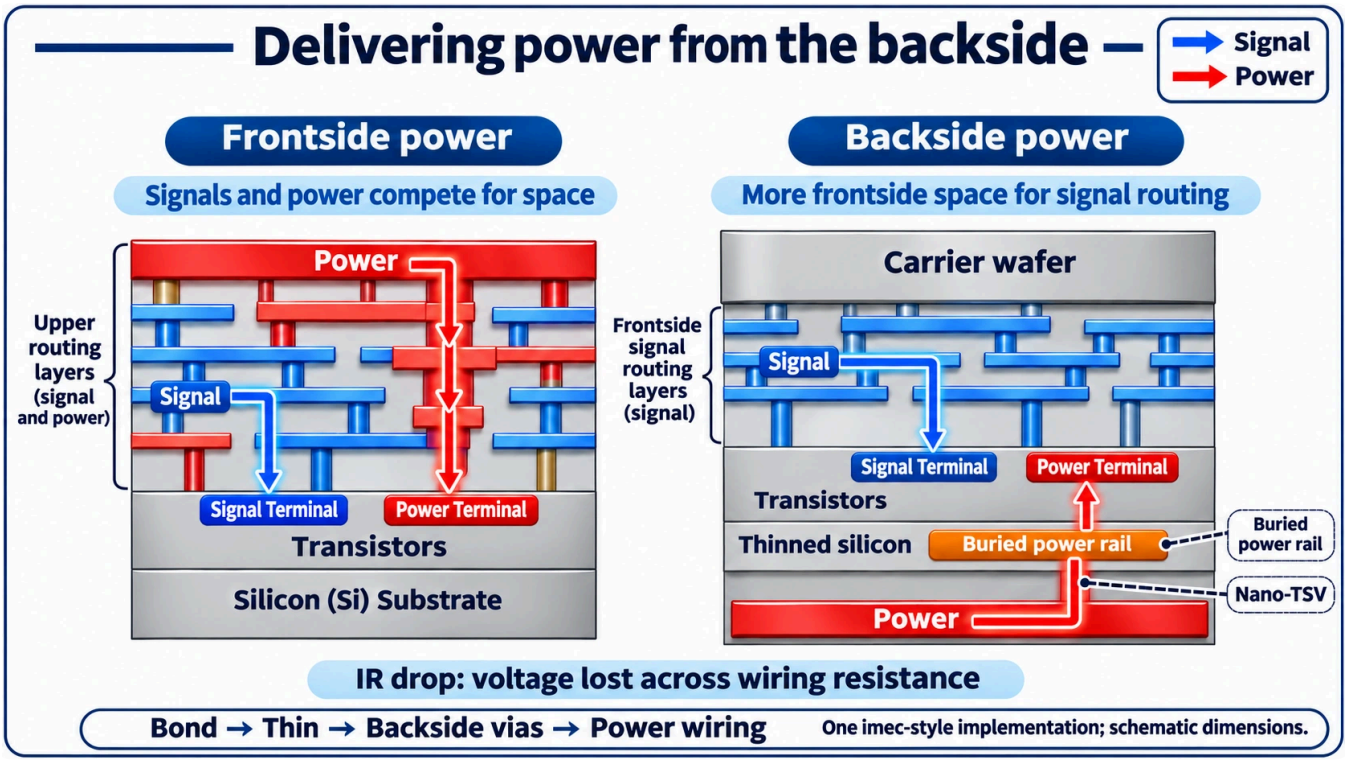


Figure 5. One imec-style buried-power-rail implementation. The drawing keeps a common viewing orientation for comparison. Actual Intel, TSMC and research integrations can use different landing structures, materials and process sequences. [7][11][12]

One research process flow

Imec's example combines a **buried power rail**, or BPR, with a **nano-through-silicon via**, or nTSV. The BPR lies near the devices, partly in silicon and partly in the isolation region. The small backside via lands on it through the thinned substrate. [7]

1. Prepare the device wafer, including a suitable thinning-stop scheme. Form the transistors and buried rails. The research example cites rails about 30 nm wide at approximately 100 nm pitch, using refractory metal options such as tungsten or ruthenium.
2. Complete the frontside wiring and bond that side to a support wafer. The cited example uses SiCN bonding with a subsequent 250 °C treatment.
3. Remove most of the original substrate by grinding, CMP and etching. The remaining silicon is a few hundred nanometres thick in the example, with a thickness variation below 40 nm.
4. Align and form backside vias to the intended rail locations. The example discusses alignment below 10 nm and tungsten-filled vias a few hundred nanometres deep.
5. Build the backside power wiring.

Those dimensions are details of a particular research implementation. Their value is to show why thinning and alignment are critical, and why a backside connection differs from a much larger packaging TSV. [7]

An imec–Arm simulation reported at IEDM 2019 compared conventional frontside delivery, frontside delivery with buried rails, and backside delivery with nTSVs landing on buried rails. In that study the combined backside scheme reduced IR drop by about a factor of seven relative to the conventional case. The benefit is tied to the evaluated design. Thermal behaviour also needs attention when most of the original silicon support has been removed. [7]

- **Different industrial implementations**

Intel's PowerVia. Intel's 2023 test-chip announcement reported more than 90% standard-cell utilisation, over 30% improvement in its voltage-droop metric and a 6% frequency benefit. Its current Intel 18A page describes high-volume production in the United States. The page attributes up to a tenfold reduction in worst-case dynamic voltage droop and up to 11% block-area compaction to the evaluated PowerVia implementations. These are Intel's stated results under its documented conditions. [9][11]

TSMC's Super Power Rail. TSMC announced A16 in April 2024, combining nanosheet transistors with backside power. That announcement targeted production in 2026 and reported, relative to N2P, an 8–10% speed improvement at the same voltage, 15–20% lower power at the same speed and up to 1.10 times chip density. Its June 2026 shareholder material also scheduled A16 volume production for the second half of 2026. These are company targets and comparisons cited to their announcement dates. [12][14]

The two sets of percentages use different baselines and conditions, which must accompany each comparison. The architectural lesson is the separation of signal routing from major power distribution. Bonding, thinning, backside patterning and thermal management determine how that idea is implemented.

9. The equipment chain behind an interconnect

Dual damascene brings together processes introduced earlier in the series. Dielectrics and caps are deposited, trenches and vias are etched, liners and seed layers are added, copper is plated, and CMP clears the field. Each step has different equipment and materials requirements.

Step	Equipment category	Selected shares reported in the source
Dielectric and cap deposition	CVD	Applied Materials 47%, Lam Research 16%, ASM International 12%, Tokyo Electron 7%
Trench and via pattern transfer	Etch	Applied Materials 33%, Lam Research 30%, Tokyo Electron 20%
Barrier and seed deposition	Sputtering	Applied Materials 85%, ULVAC 10%
Copper fill	Electrochemical deposition	The supplied market chart gives no share. Lam's SABRE is an example product family.
Overburden removal	CMP	Applied Materials 51%, EBARA 34%

The percentages are carried over from the lesson's cited METI presentation. They describe broad equipment categories, rather than the subset used only for interconnects. The equipment chart does not state its measurement year, and the selected suppliers do not sum to the entire market. [4]

The same source gives category market sizes of ¥2,021.8 billion for CVD, ¥2,338.3 billion for etch, ¥564.3 billion for sputtering and ¥424.2 billion for CMP. These category totals should be interpreted with the same scope and date limitations. [4]

Lam describes SABRE as an electrochemical-deposition family for copper damascene, including control of void-free filling, defects and resistivity. A product example identifies a supplier's role without implying an exclusive supplier relationship for every damascene flow. [13]

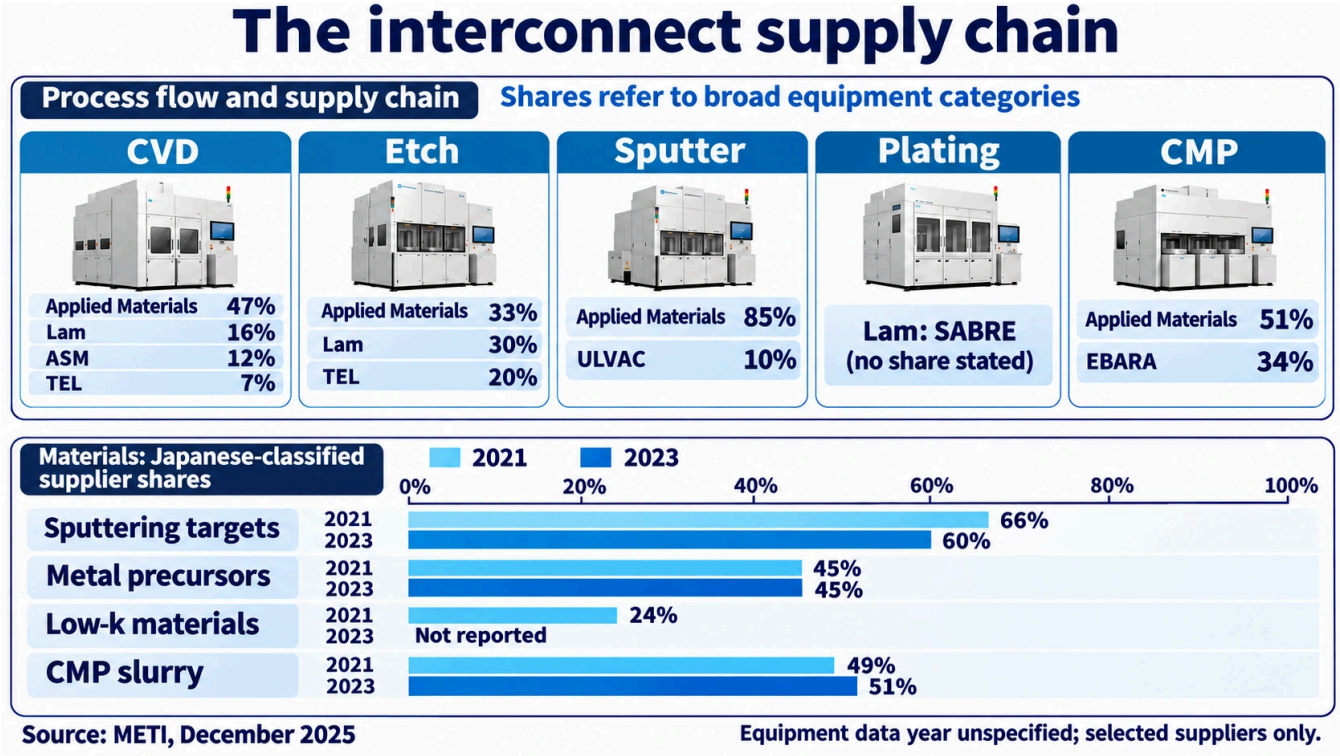


Figure 6. Process roles and a historical market snapshot. Equipment shares refer to broad categories with no stated measurement year. Materials data compare 2021 and 2023; the source does not report a 2023 low-k share. [4][13]

10. Materials and interfaces across the supply chain

Interconnect integration depends on the conductor, dielectric and the interfaces between them. Sputtering targets provide source material for physical deposition. Metal precursors support CVD and ALD. Low-k formulations and deposition processes determine the insulation. Slurry and pad choices help CMP reach a controlled final profile.

The Japanese suppliers' substantial presence in some materials categories remains part of a global account. The METI data reproduced in the supplied lesson give the following shares for Japanese-classified suppliers. [4]

Category	2021	2023
Sputtering targets	66%	60%
Metal precursors	45%	45%
Low-k materials	24%	Not reported
CMP slurry	49%	51%

These figures describe the source's historical country classification and market definitions. A supplier's role in one category does not determine the complete set of materials used by a particular fab.

The Stanford lecture distinguishes CVD low-k solutions associated with equipment suppliers from spin-on approaches associated with materials suppliers. Applied Materials' Black Diamond is one example in which deposition equipment and film design are developed together. [3][10]

Where materials engineering makes a difference

- **Conductors.** Compare size-dependent resistance, deposition, liner needs and reliability for copper and alternative metals.
- **Barriers and caps.** Limit diffusion while preserving useful conductor area and robust interfaces.
- **Low-k dielectrics.** Balance capacitance, adhesion, moisture resistance and mechanical strength.
- **Precursors.** Enable thin, conformal films in small features.
- **Backside integration.** Develop suitable bonding surfaces, rail metals, thinning stops and thermal paths.

11. How the challenges connect

At the finest levels, alternative metals and thinner surrounding films address resistance and available cross-section. In the dielectric, porosity and air-gap structures address capacitance while creating mechanical constraints. Backside power changes the routing architecture itself. Reliability and process integration decide which combinations are useful in manufacturing.

The next lesson, 3-13, turns to metrology, inspection and yield. Once hundreds of processing steps have created a multilayer structure, manufacturers need to determine whether its dimensions, materials and connections are within specification and where defects originated.

12. Check your understanding

▼ Why are lower wires fine and upper wires often larger?

Lower levels connect nearby devices at high density. Wider and thicker upper conductors reduce resistance on longer paths and major distribution routes.

▼ What determines resistance in the simplest wire model?

R = ρL/(WH). Length and resistivity increase resistance; a larger conducting cross-section reduces it.

▼ When does the fourfold RC example apply?

Length, resistivity and dielectric constant stay fixed while width, thickness, lateral spacing and vertical separation are all halved. Resistance rises by four and the simplified capacitance stays approximately unchanged.

▼ What does dual damascene fill together?

The lateral trench and the via connecting it to a lower conductor. The cavities are prepared before the metal-fill and CMP sequence.

▼ What do the barrier and cap do?

They help contain copper and maintain appropriate interfaces. The cap or related films can also provide etch control for subsequent processing.

▼ Why can a low-k film be difficult to integrate?

A less dense or porous structure can be mechanically weaker, less adhesive or more susceptible to damage and moisture. It must survive CMP and packaging stress.

▼ Why can narrow copper have a higher resistivity than bulk copper?

Surfaces and grain boundaries scatter electrons more strongly when their characteristic dimensions approach the electron mean free path. Barriers also reduce the available copper area.

▼ How does electromigration cause failure?

Current-driven atomic transport can deplete a region and form a void, interrupting the conductor. Interfaces, temperature, geometry and current density affect the process.

▼ What are two intended benefits of backside power?

A lower-resistance power path can reduce voltage loss, and moving major power distribution away from the frontside releases routing resources for signals.

▼ **Why does backside integration require a carrier wafer?**

Most of the original substrate is removed to allow short backside connections. A bonded carrier supports the very thin device structure during processing.

13. Terms used in this lesson

Term	Meaning
Interconnect	A conductor and its vertical connections linking devices and other conductors.
FEOL / BEOL	Device formation / the subsequent multilayer wafer-level wiring processes.
Local, intermediate and global wiring	Connections grouped by their physical reach and integration role.
Via	A vertical connection between wiring levels, including its opening and conductive fill.
RC delay	A delay associated with charging capacitance through resistance.
Relative permittivity, κ	A dielectric's permittivity relative to vacuum.
Low-k dielectric / air gap	Low-permittivity insulation / an intentional cavity that reduces capacitive coupling.
Damascene / dual damascene	Filling patterned dielectric recesses with metal and removing overburden / filling trench and via together.
Barrier / cap	A film limiting diffusion and controlling interfaces / a film covering a conductor, sometimes also used for etch control.
Mean free path / grain-boundary scattering	Average distance between scattering events / electron scattering at interfaces between crystallites.
Electromigration	Current-driven atomic transport that can cause voids and interconnect failure.
IR drop	Voltage lost across resistance in a current-carrying supply path.
BSPDN	Backside power delivery network.
BPR / nano-TSV	Buried power rail / a small through-silicon connection in a thinned wafer.
Standard cell	A reusable logic-layout building block with defined dimensions and interfaces.

14. Sources

Technical teaching material, research results, roadmap projections, historical market figures and supplier statements are distinguished in the text.

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15. How the evidence is used

Topic	Sources	Type of evidence
Hierarchy, copper history and dual damascene	S1, S2	Historical technical account and teaching material.
Resistance, capacitance and scaling	S2	Approximate geometric models. The fourfold RC example is calculated in this lesson.
Low-k composition and mechanical trade-offs	S3, S5, S10	Teaching examples, roadmap and attributed product information.
Scattering and alternative metals	S5, S6	Roadmap and research model. The 2.25 resistivity ratio is an illustrative calculation.

Topic	Sources	Type of evidence
Electromigration	S1, S5	Accelerated historical test and a roadmap scaling model. The 1/16 result is conditional on fixed current.
Backside power process and simulated benefit	S7	One research integration and a specific design simulation.
PowerVia and A16	S9, S11, S12, S14	Company-attributed tests, product statements and dated production targets.
Equipment and materials shares	S4	Historical data retained from the supplied lesson. Equipment measurement year unspecified.
Copper electroplating equipment	S13	Product-family example.

Illustrations created with ImageGen. Dimensions, molecular structures, charge symbols and profiles are schematic. The market figures retain the supplied lesson's data and category definitions.

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