SEMICONDUCTOR FRONT-END · PART 3-4

Sputtering and Electroplating
From metal targets to copper wiring

A copper wire inside a chip is not laid into place as a ready-made wire. Engineers first form a trench, coat it with thin underlayers, fill it with copper and polish away the excess. This lesson follows two complementary methods: sputtering, which releases atoms from a solid target, and electroplating, which turns dissolved metal ions into a solid film. Along the way, we explain what magnets actually do, why deep features are difficult to coat, and how a few additives can make copper grow faster at the bottom.

Semiconductor Front-End Series · Part 3-4 · Intermediate introduction · Helpful background: Lesson 3-3 · Updated 7 November 2026

In this lesson

1. Three ideas to keep in mind
2. Why use physical deposition for metal films?
3. Sputtering: a collision cascade at the target
4. Magnetrons: what the magnets actually do
5. Getting material into deep features
6. From a trench to a copper interconnect
7. Electroplating: charge becomes deposited metal
8. Superfilling: make the bottom advance first
9. Smaller wires and a wider role in packaging
10. Equipment suppliers: different strengths in different processes
11. Targets and plating chemistry: the materials behind the tools
12. What future processes ask of materials and equipment
13. A compact comparison
14. Check your understanding
15. Glossary
16. Sources and further reading
17. Claim-to-source notes

How to read this lesson

Begin with the main text. The shaded physics boxes add optional detail and worked estimates. Figures are conceptual and not to scale. Numbered links lead to the supporting sources.

What you will learn

- Explain how ion–atom collisions release material from a sputtering target.
- Distinguish the roles of magnetic confinement, collimation, long throw and ionised PVD.
- Use Faraday's law to estimate copper deposition and explain additive-assisted bottom-up filling.
- Identify representative equipment, target and plating-chemistry suppliers without confusing their different market categories.

1. Three ideas to keep in mind

- **Sputtering starts with a solid source.** Argon ions strike a target and release metal atoms. The atoms travel towards the wafer and form a film. A magnetron keeps electrons near the target for longer, increasing ionisation; the magnet does not pull copper atoms onto the wafer.
- **Electroplating starts with dissolved ions.** Copper ions accept electrons at a conducting surface and become metal. Charge passed determines the amount deposited, while local current distribution and chemistry determine where it grows.
- **The methods work together.** In a representative copper damascene process, a barrier limits copper diffusion, a seed layer carries plating current, electroplating fills the feature and CMP removes the excess. Advanced processes can combine PVD with CVD or ALD where required.

2. Why use physical deposition for metal films?

- **A suitable gas-phase precursor is not always the easiest route**

CVD and ALD, covered in Lesson 3-3, rely on appropriate precursor chemistry. For some metal-film requirements, it is more practical to start with the solid material itself, release atoms and transport them to the wafer. This is **physical vapour deposition, or PVD**. Sputtering and evaporation belong to this family Explanation .

Stanford's 1999 lecture material gives the following representative choices [1]:

Film	Process described in the lecture
Aluminium	Magnetron sputtering
Titanium and titanium–tungsten	Conventional, collimated or ionised sputtering; CVD described as difficult
Titanium nitride	Reactive sputtering in a nitrogen-containing plasma
Copper	Electroplating described as the most common method

These are historical teaching examples, not a complete specification for every present-day device. Material choice, feature shape and integration requirements govern the actual process.

Evaporation and sputtering

Evaporation heats a material in high vacuum so that vapour reaches the substrate. Stanford uses pressures below **10^{-5} Torr** as an example. Different constituents of an alloy may evaporate at different rates, and line-of-sight arrival gives poor coverage in recessed features [1] Reported .

The lecture consequently gives evaporation a limited role in its integrated-circuit context. That should not be read as saying evaporation has disappeared from research or other thin-film industries.

Sputtering instead uses energetic particle impacts to release material. Stanford gives a **1–100 mTorr** range and explains why this method is generally better suited than evaporation to depositing alloys and compounds [1]. Preferential sputtering, re-sputtering and other effects can still change film composition: matching the target composition is not automatic Explanation .

3. Sputtering: a collision cascade at the target

Two particle journeys in opposite directions

A basic sputtering system places a target and wafer opposite one another in a vacuum chamber. Argon enters the chamber, and a discharge produces electrons, neutral argon and positive **Ar^+ ions**. A negative target attracts the ions across the near-target sheath. Their impacts release target atoms, which then travel through the chamber and can deposit on the wafer [1] Reported .

It helps to follow the two journeys separately: **ions towards the target; released metal towards the wafer**. An argon ion does not turn into a copper atom. Most deposited metal in conventional sputtering travels as neutral atoms Explanation .

MIT's lecture gives **10–100 mTorr** and roughly **1 kV** as typical teaching conditions, and about **16 eV** for argon's ionisation energy [2]. These numbers describe different quantities. The ionisation energy is the energy needed to remove an electron from an argon atom; it is not the same as the electrical operating voltage or every ion's impact energy.

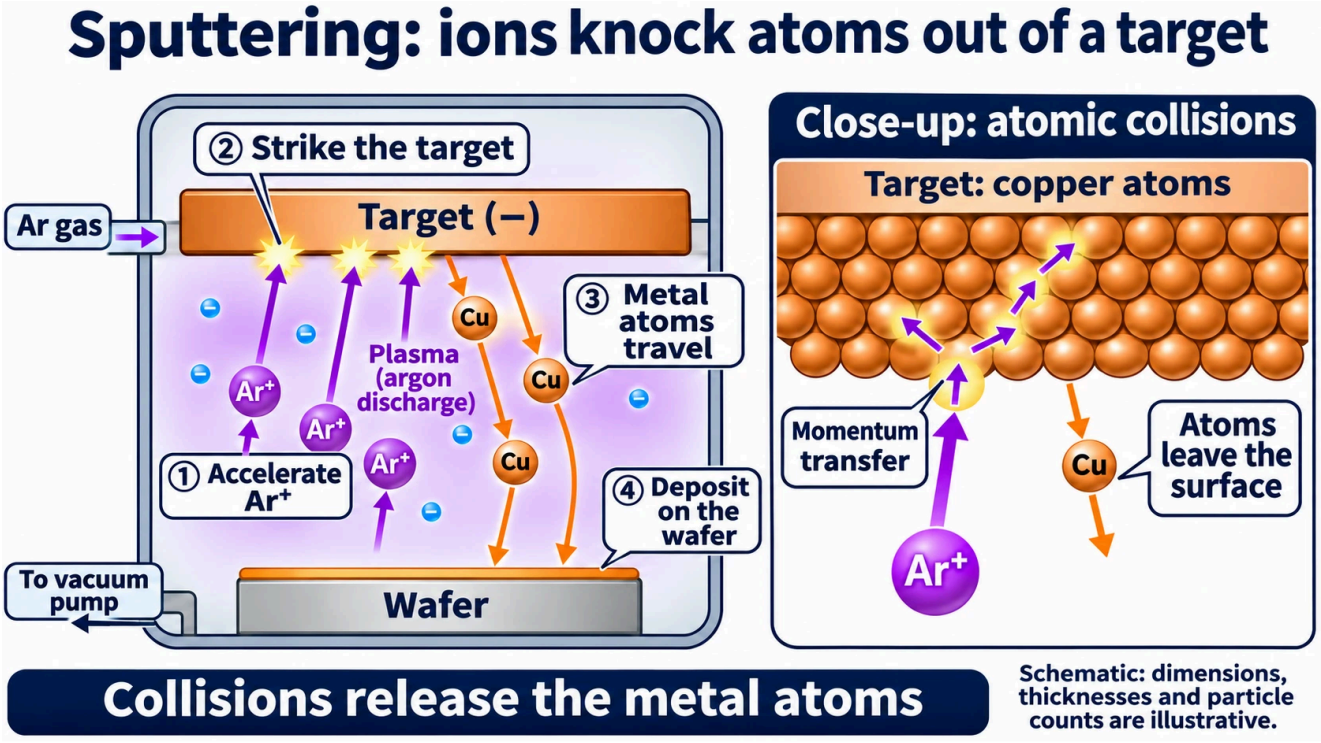


Figure 1 **Ions release target atoms; metal atoms form the film** (schematic)

Reading the figure

The close-up shows collisions transferring momentum through the target. Particle sizes and counts are illustrative. The coloured arrows distinguish ion acceleration from the subsequent flight of released metal atoms.

- **Sputter yield: an average number, not a fixed outcome**

The **sputter yield, Y**, is the number of target atoms released per incident ion. MIT gives a representative range of **0.1–3** [2]. A value below one is an average over many impacts, not a fraction of a physical atom leaving after each collision.

Yield depends on ion energy and mass, target material and angle of incidence. Stanford notes that differences in yield between target materials are less extreme than differences in vapour pressure, which helps with alloy deposition [1] Reported .

Why mass matching helps transfer energy

In a simple two-body elastic collision, a moving particle of mass M_1 strikes a stationary particle of mass M_2. The maximum transferred energy fraction, for a head-on collision, is [2]:

$$E_2/E_1 = 4M_1M_2/(M_1 + M_2)^2$$

Using relative atomic masses, an argon projectile of about 40 gives the following values Calculation :

- Copper, 63.5: approximately **0.95**.
- Aluminium, 27: approximately **0.96**.
- Tantalum, 181: approximately **0.59**.

Similar masses permit a larger energy transfer in this model. Actual sputtering also depends on binding at the surface, impact geometry and the collision cascade inside the solid. The energy fraction alone does not predict the final yield.

An electron is roughly **73,000 times lighter than an argon atom** Calculation . It transfers little energy to such a heavy particle in an elastic collision. In the discharge, electrons are important for excitation and ionisation; heavy ions do the main work of knocking target atoms out Explanation .

Conducting targets: DC; insulating targets: RF

A conducting target can use **direct current, or DC**, sputtering [1]. With a dielectric target, positive charge accumulates at the surface and disrupts the discharge. MIT gives a **1–10 µs** timescale for this charging problem in its example [2].

Radio-frequency, or RF, sputtering allows electrons to reach the surface during part of the cycle and neutralise accumulated charge. Because electrons and ions respond differently, the target can develop a negative time-averaged self-bias relative to the plasma. **13.56 MHz** is a commonly used frequency [2] Reported . This is more than simply reversing the direction of a steady DC current.

4. Magnetrons: what the magnets actually do

Keep electrons in the useful region

Stanford's EE311 notes present magnetron sputtering as the dominant semiconductor PVD approach in their teaching context [3]. Magnets behind the target shape a field in front of its surface. Electrons spend longer near that region, encounter more argon atoms and support more ionisation.

The notes compare current densities around **10–100 mA/cm² for magnetrons** with roughly **1 mA/cm² for a conventional RF example**, and give **5–10 cm** target–wafer spacing, **2–10 mTorr** and several hundred volts as representative conditions [3] Reported . These are examples, not universal operating ranges.

Gyroradius is not distance from the target

A charged particle's velocity component perpendicular to a magnetic field produces circular motion. The gyroradius is:

$$r = mv_{\perp}/(|q|B)$$

Using the MIT example of $v_{\perp} \approx 6\times10^{6}$ m/s and B = 0.1 T [2], an electron's radius is approximately **0.34 mm** Calculation .

That is the radius of motion around a magnetic field line. It does **not** mean that the electron always stays within 0.34 mm of the target surface. Electric fields, magnetic geometry and collisions jointly determine its trajectory and residence time.

The much heavier Ar^{+} ions are less readily magnetised under typical magnetron conditions. They are accelerated mainly by the electric field towards the negative target. Magnetic confinement primarily acts on electrons; it is not a magnetic conveyor carrying copper to the wafer Explanation .

- **The racetrack left in the target**

Where ionisation and ion bombardment concentrate, the target erodes more quickly. The resulting ring-shaped track is commonly called the **racetrack** [3]. Field direction, geometry and electric fields matter as well as magnetic-field strength.

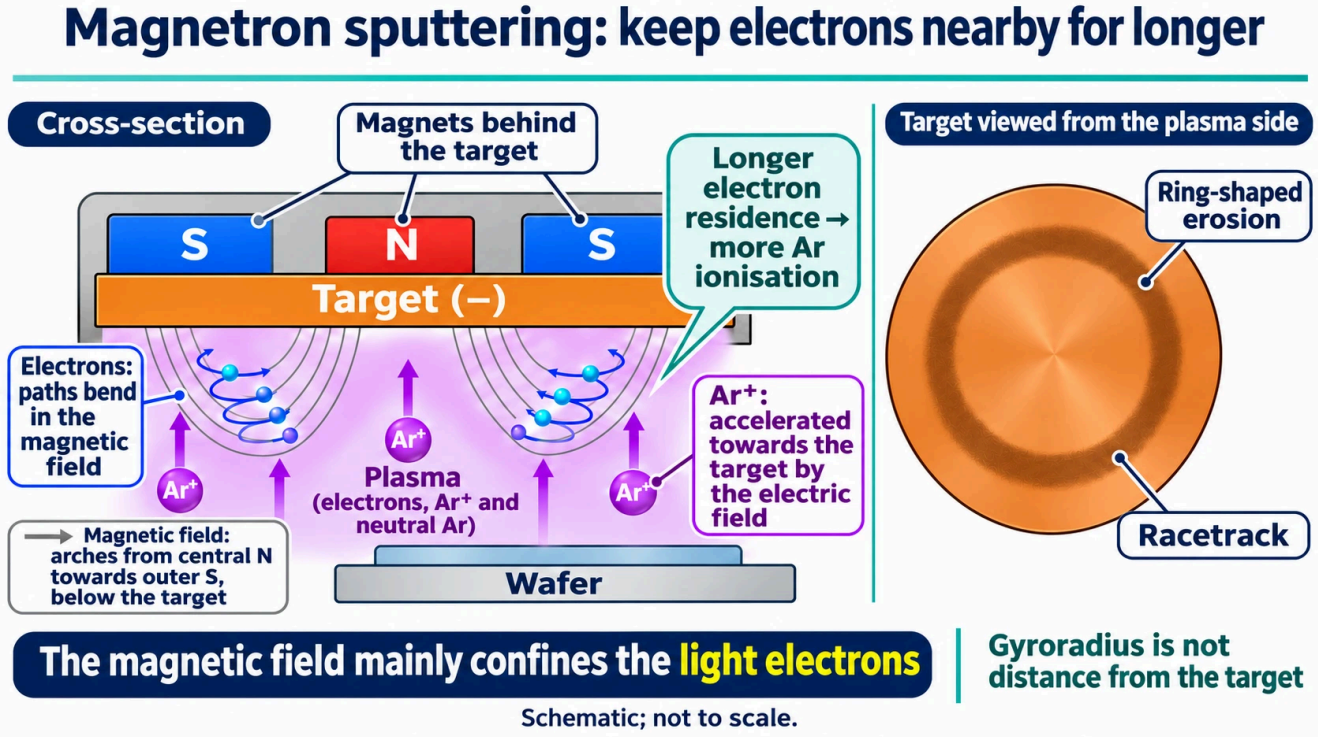
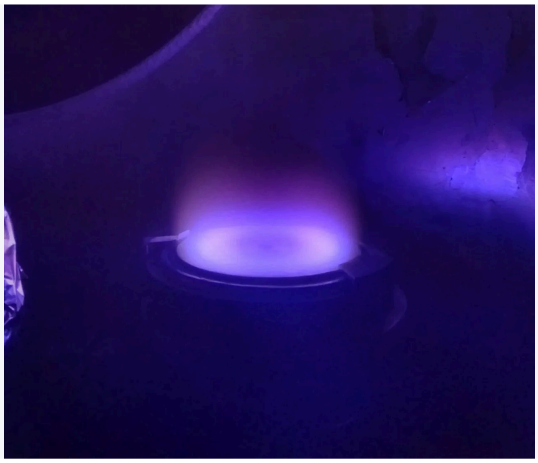


Figure 2 **Electron confinement and racetrack erosion** (schematic)

Reading the figure

The target is drawn flat in the left schematic; the right-hand disc shows the erosion pattern. The magnetic field arches in front of the target. Some production systems move or rotate the magnet assembly to distribute erosion over a larger area.



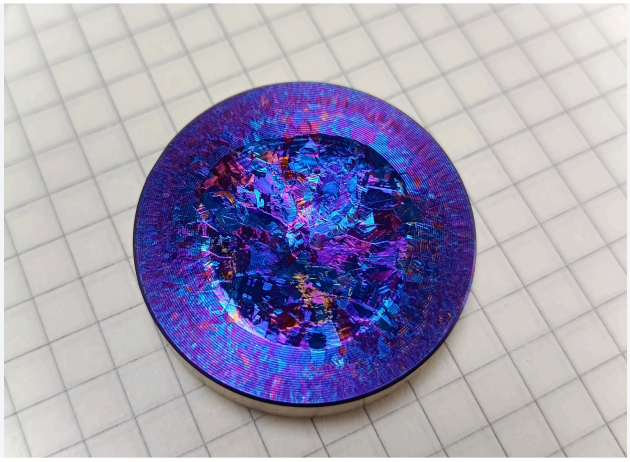
The Commons description identifies a magnetron sputtering cathode with a glowing argon plasma. The bright ring corresponds to the region of enhanced discharge near the target.

Photo: Inmodus / Wikimedia Commons / CC BY-SA 3.0. Resized and converted to WebP.

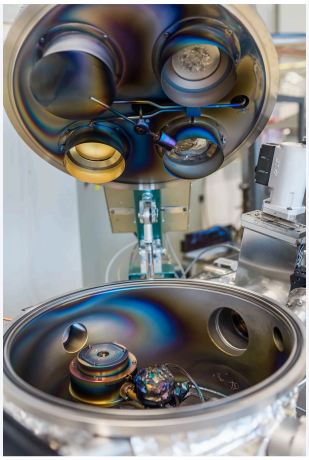


A circular planar target used in DC magnetron sputtering, according to the Commons description. The ring-shaped erosion track is clearly visible.
Photo: Axelfusillo / Wikimedia Commons / Public domain. The photograph was cropped from the original image, resized and converted to WebP.

A target must be replaced before its deepest erosion region compromises the plate, even if substantial material remains elsewhere. A patent addressing large-area coating gives utilisation examples of **40% or less for planar targets** and **above 90% for rotating cylindrical targets** [4]. Those figures belong to that coating context and should not be applied to every semiconductor wafer tool. Another patent describes rotating magnets behind a wafer-processing target to spread erosion [5] **Reported** .



According to its Commons description, surface oxidation caused by heating has produced blue and purple interference colours on this titanium target.
Photo: 范皓程 (Fan Haocheng) / Wikimedia Commons / CC BY 4.0. Resized and converted to WebP.



The Commons description identifies gold, titanium and palladium targets in a system at the Institute of Physics of the Czech Academy of Sciences. Several sources are mounted in the lid. This research installation differs from a high-volume production tool.
Photo: Czech Academy of Sciences (Pavlína Jáchimová) / Wikimedia Commons / CC BY-SA 3.0. Resized and converted to WebP.

- **Reactive sputtering: adding chemistry to PVD**

Adding nitrogen or oxygen allows a sputtering process to form a compound. MIT describes **titanium nitride, TiN**, using titanium or titanium nitride targets with argon/nitrogen mixtures [2]. A 1990s patent also describes reactive sputtering of titanium in nitrogen-containing gas for a TiN barrier [6] Reported . PVD therefore describes how material is released and transported; it does not exclude chemical reactions during film formation.

5. Getting material into deep features

- **Arrival direction and sticking both matter**

Lesson 3-3 explained why low effective sticking can help a precursor reach the bottom of a deep feature. In a representative PVD model, arriving metal is instead readily captured at its first surface encounter. Stanford uses a sticking coefficient near one for its PVD examples [1]. Actual coefficients depend on material, surface and temperature.

Lecture-model example	Arrival distribution exponent, n	Sticking coefficient
Conventional sputtering	1–4	1
Ionised or collimated sputtering	8–80	1
LPCVD SiO_2 from TEOS	1	0.05–0.1

The angular distribution is represented as $\cos^n\theta$: a larger n favours arrival close to the surface normal [1]. This is a modelling comparison, not a fixed law for every reactor.

Applied Materials' patent describes conventional PVD as predominantly neutral metal transport with a broad angular distribution, and cites ion densities below 10^9 cm^{-3} in that context [5] Reported .

Shadowing and overhangs

Atoms arriving obliquely accumulate near the opening. The growing **overhang** shadows lower regions; if it closes the entrance, it can trap a **void**. A closed opening also blocks subsequent plating access [5]. Stanford notes poor coverage near bottom corners [3]. One patent gives an example with **135 nm on the top surface but only 40 nm at the bottom** [6] Reported .

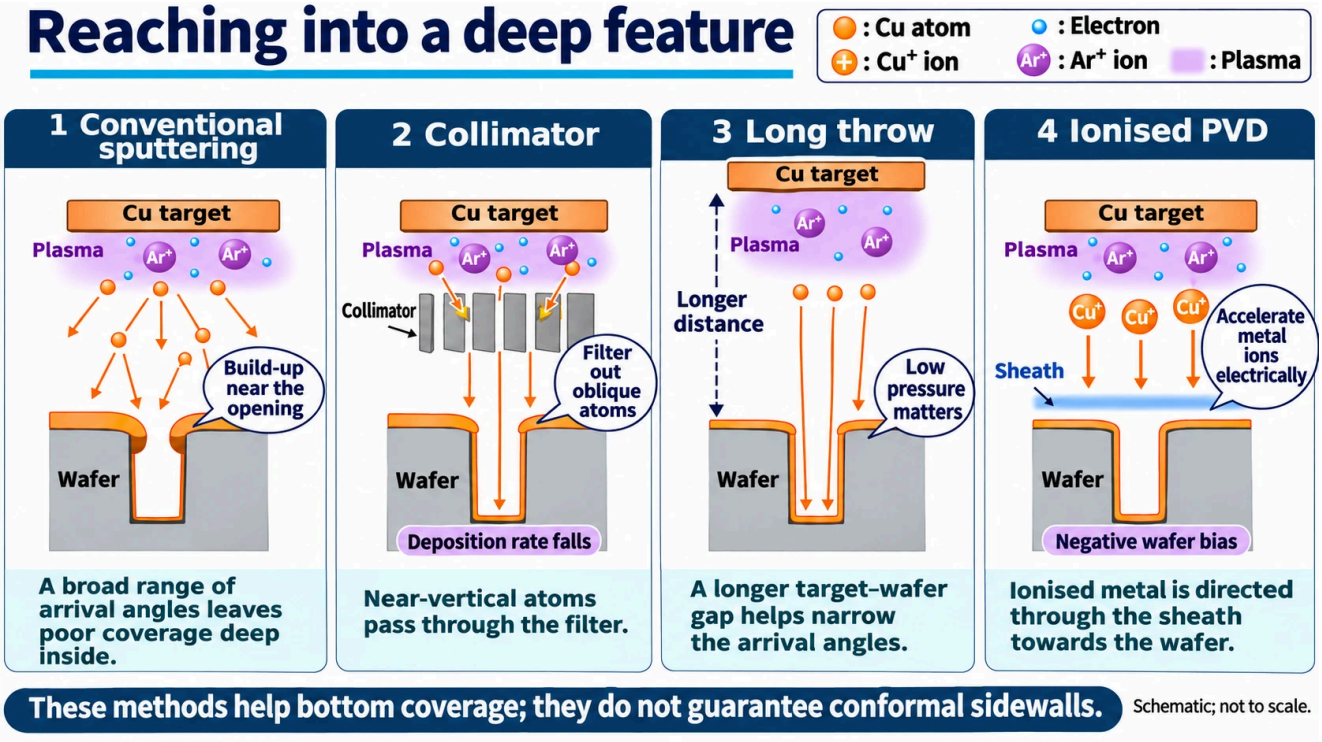


Figure 3 **Three ways to improve delivery into a feature** (schematic)

Reading the figure

Collimation and long throw select arrival directions geometrically. Ionised PVD adds electrical control of charged metal species. These approaches can improve bottom coverage without guaranteeing a uniformly coated sidewall. Neutral atoms are not accelerated by the wafer's electric field.

Collimation: reject oblique trajectories

A **collimator** is a perforated plate between target and wafer. Oblique atoms strike the channel walls, while near-vertical atoms can pass through. A patent filed in 1991 describes a **1 cm thick** honeycomb steel plate [6].

For an aspect-ratio-two feature, the patent reports bottom coverage improving from about **4%** of top-surface thickness without collimation to **11%** and **17%** for two collimator geometries. Changing the collimator channel aspect ratio from one to two reduced deposition rate to **one quarter** in the reported comparison [6] Reported . Better directionality costs throughput because much of the released material lands on the filter.

Long throw: increase the spacing

A longer target–wafer distance can narrow the range of trajectories that reach a particular feature. Applied Materials' patent discusses distances exceeding **50%, preferably 90%, and more preferably 140% of wafer diameter**. It also notes lower deposition rates and limitations in lower-sidewall and bottom coverage [5] Reported .

Lower pressure helps preserve direction by reducing gas collisions. Stanford gives an approximate gas mean-free-path relation of **1/(260P) cm**, with P in Torr [3]. This gives about **0.8 cm at 5 mTorr** and **3.8 cm at 1 mTorr** Calculation . Those distances make collisions relevant over centimetre-scale gaps. The collision path of a sputtered metal atom through argon also depends on its energy and collision cross-section, so the gas estimate is not a precise collision count for every metal atom.

- **Ionised PVD: steer charged metal through the sheath**

If metal atoms are ionised in a dense plasma, a negative wafer bias can accelerate them through the near-wafer sheath. A **1996 IBM paper** reports approximately **85% copper ionisation** in its process and describes electrostatic collimation towards the substrate [7] Reported .

The Applied Materials patent discusses high-density plasma examples above **10^{11} cm^{-3}**, often at pressures above **30 mTorr**, and warns that ion bombardment and heating can promote copper dewetting on barriers even around **50–75°C** [5]. These are limitations of the processes discussed in that patent, not universal limits of ionised PVD.

The same patent proposes **self-ionised plasma, or SIP**: copper is ionised and some ions return to sputter the target. A copper self-sputter yield above one can help sustain the process, but adequate ionisation and return fractions are also necessary. The patent describes operation below **5 mTorr**, preferably below **1 mTorr**, and combinations with long throw [5] Reported .

Another option is **bias sputtering**, in which ions re-sputter some deposited material from the wafer. Controlled removal can reduce entrance overhangs and improve coverage [1]. As in HDP-CVD, adding and removing material together can be more useful than deposition alone.

6. From a trench to a copper interconnect

- **Barrier first, seed second**

Copper must be kept from diffusing into surrounding dielectric material. A **barrier** provides that protection. Stanford's copper-interconnect notes discuss transition-metal compounds including **TaN and TiN** [8].

Electroplating also needs a conducting surface. In the conventional process described by the lectures, direct plating onto the barrier is difficult, so a thin **copper seed layer** provides a suitable surface and current path. PVD is a principal method for the barrier/liner and seed in those examples [8][9]. Advanced structures can combine these methods with CVD or ALD.

A representative sequence is:

1. Etch a trench or via into the dielectric.
2. Deposit a thin barrier.
3. Add a continuous copper seed layer.
4. Electroplate copper to fill the feature and leave an overburden.
5. Remove excess copper and field barrier by **chemical–mechanical polishing, CMP**.

This is the **damascene** approach: form a recess, fill it and remove the excess, rather like metal inlay. Lessons 3-11 and 3-12 cover polishing and interconnect integration in more detail.

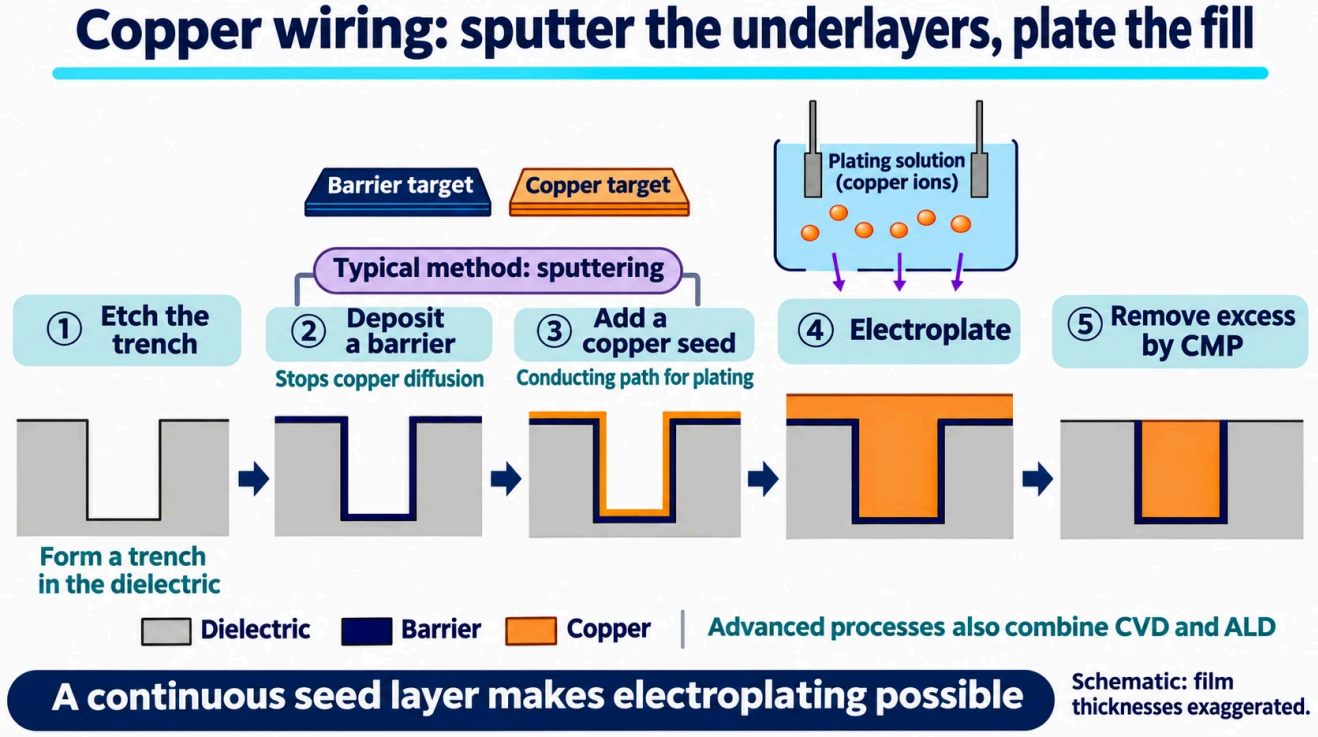


Figure 4 **Underlayers, copper fill and polishing** (schematic)

Reading the figure

The barrier protects the surrounding material; the seed supplies a continuous conducting path for plating. The two are different layers with different jobs. Their thicknesses are exaggerated so that the sequence remains visible.

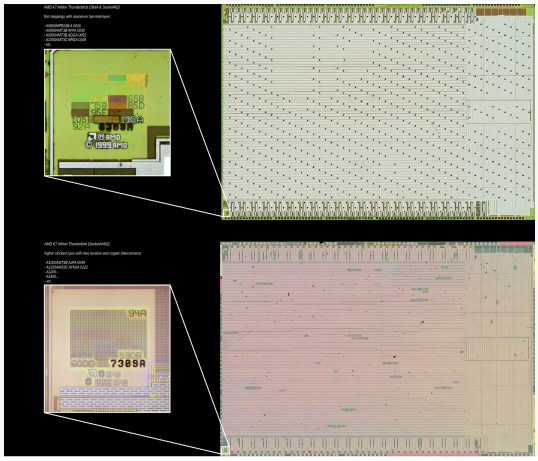
Why the industry moved from aluminium to copper

Aluminium, and later aluminium–copper alloys, had been widely used for on-chip wiring. IBM's **September 1997** announcement and **June 1998** shipments marked a major transition to copper [11].

Stanford's lecture compares bulk resistivities as follows [9] Reported :

Metal	Resistivity in the lecture, μΩ·cm
Silver	1.63
Copper	1.67
Gold	2.35
Aluminium	2.67
Tungsten	5.65

Copper offers low resistance and useful reliability characteristics. The lecture also lists melting points of **1,083°C for copper** and **660°C for aluminium**, and an electromigration-test example with copper lifetime over **110 times** that of an aluminium alloy [9]. That lifetime ratio is a particular test result, not a guarantee for every copper wire. Actual nanoscale resistivity also depends on surfaces, grain boundaries and surrounding layers.



The Commons description and image annotations compare AMD Athlon dies: an early version with aluminium upper-level wiring above a later version using copper. The image illustrates the historical materials transition, rather than a controlled comparison of all processing variables.

Image: FritzchensFritz / Wikimedia Commons / CC0. Resized and converted to WebP.

7. Electroplating: charge becomes deposited metal

- **Follow the electrode reactions**

In a simple copper-plating example, the wafer's seed layer is the **negative cathode**, and a soluble copper plate is the **positive anode**. The electrolyte contains copper ions. Stanford writes the corresponding reactions [8]:

$$CuSO_4 \rightarrow Cu^{2+} + SO_4^{2-}$$

$$\text{Cathode: } Cu^{2+} + 2e^- \rightarrow Cu$$

$$\text{Soluble anode: } Cu \rightarrow Cu^{2+} + 2e^-$$

Copper ions accept two electrons at the cathode and join the metal film. At a soluble copper anode, copper enters solution and replenishes ions. Production baths also contain acid, chloride and additives. Some tools use insoluble anodes, with different anode reactions and copper-replenishment arrangements **Explanation** .

Electrons travel through metallic wires and electrodes. In the liquid, ions carry charge. It is not a stream of free electrons crossing the bath from one electrode to the other.

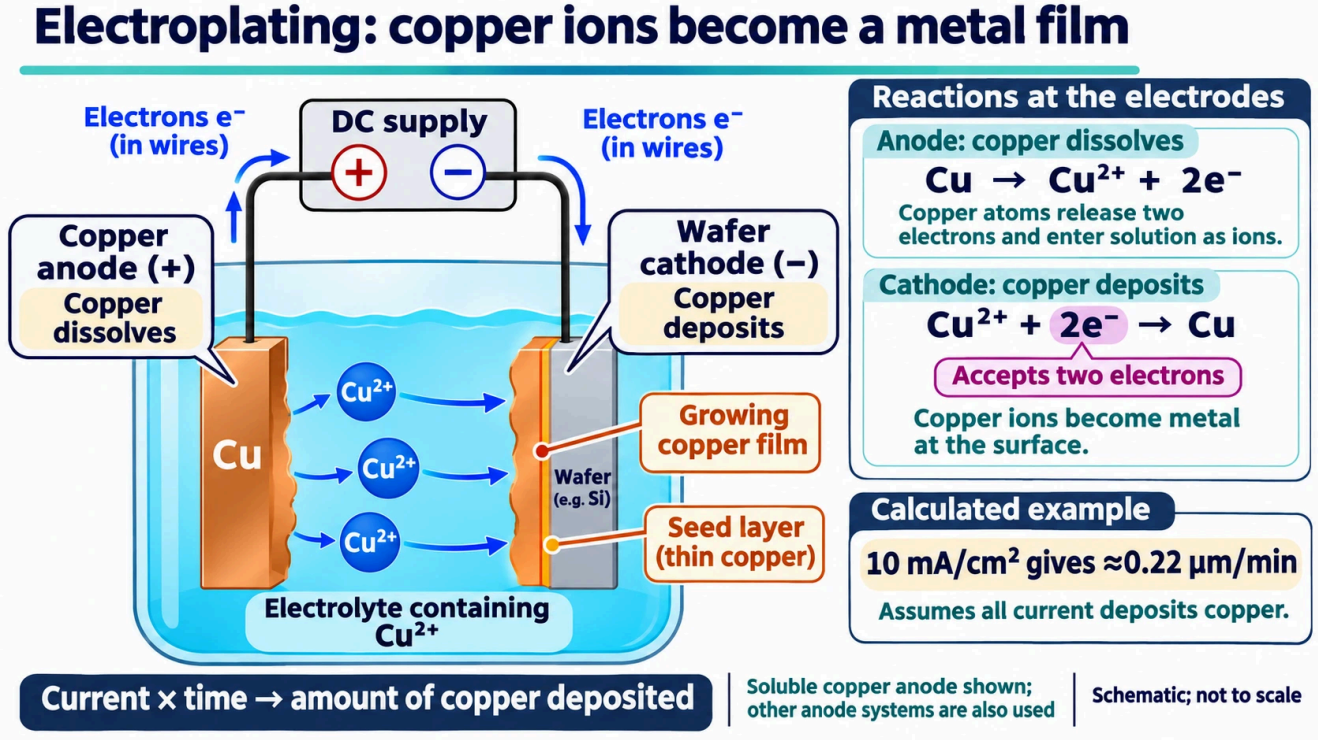
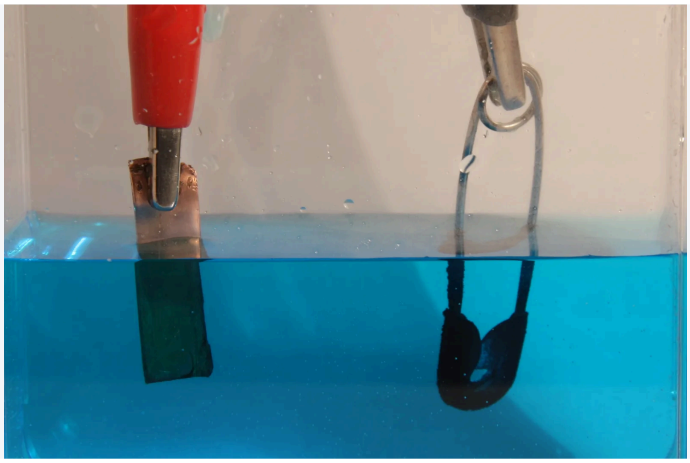


Figure 5 **Copper ions accept electrons at the wafer surface** (schematic)

Reading the figure

The arrows for electrons stay in the wires. Cu^{2+} appears in the electrolyte and becomes copper at the cathode surface. The soluble-anode arrangement illustrates the principle; production equipment can use other arrangements.



The Commons description identifies copper plating onto a safety pin in copper sulphate solution. The copper anode is on the left and the pin is the cathode on the right. Semiconductor plating uses the same basic cathodic reduction, with much tighter process control.
Photo: Richard Wheeler (Zephyris) / Wikimedia Commons / CC BY-SA 3.0. The final frame was cropped from a five-frame sequence, resized and converted to WebP.

Why seed continuity matters

IBM's 1998 paper describes the seed as the conducting path from contacts at the **wafer edge** to the full plating surface [10]. Discontinuities or excessive sheet resistance can disrupt current delivery and deposition. That is why coating a deep feature with a thin but continuous seed is such an important task for the preceding deposition process.

Faraday's law: estimating the growth rate

The amount of electrochemical reaction is proportional to charge passed. The University of Utah lecture writes the deposited mass as [12]:

$$W = AQ/(nF), \text{ with } Q = It$$

Here A is molar mass in g/mol, n is the number of electrons per deposited atom, and F is the Faraday constant, approximately **96,485 C/mol**. For copper, n = 2. IBM likewise relates local deposition rate to local current density [10].

For **10 mA/cm²**, copper molar mass **63.55 g/mol**, density **8.96 g/cm³** and **100% current efficiency**, the thickness increase per second is:

$$0.010 \times 63.55 / (2 \times 96{,}485 \times 8.96)$$

$$\approx 3.7\times10^{-7} \text{ cm/s} \approx 3.7 \text{ nm/s}$$

That is about **0.22 µm/min**, or **0.44 µm/min at twice the current density** Calculation .

The calculation predicts deposited amount under its assumptions. A uniform film also requires uniform local current, sufficient ion supply, appropriate additives and controlled flow. Passing the right total charge does not by itself guarantee equal thickness everywhere Explanation .

8. Superfilling: make the bottom advance first

Uniform coating can leave a seam

If copper grows at the same rate on every wall, opposite sidewalls can meet in the middle and leave a **seam**. If the opening closes before the interior fills, a void can remain. IBM's paper explains why defect-free filling requires preferential growth towards the bottom and describes **superfilling** enabled by additives [10] Reported .

Three additive roles

Stanford lists accelerators, suppressors, levellers and chloride ions [8]. NIST's 2023 review describes representative acid copper-sulphate systems combining halide, polyether suppressor, sulphur-containing accelerator and, frequently, a nitrogen-containing cationic leveller [14].

- **Suppressor:** reduces deposition through an adsorbed inhibiting layer. NIST's 2002 study uses polyethylene glycol of molecular mass 3,400 with sodium chloride [13].
- **Accelerator:** competes with inhibiting species and promotes growth. SPS, a sulphonate-terminated disulphide, is a common example [13].
- **Leveller:** limits excessive growth and protrusions. It does not suddenly switch on only after the feature is full; adsorption and growth interactions can occur throughout deposition [14].

CEAC: the surface area changes while adsorbates remain

Imagine accelerator molecules as labels attached to the growing copper surface. As a **concave surface segment advances**, its area can shrink. If strongly adsorbed accelerator remains on that segment, the same population occupies a smaller area and its coverage rises. Greater accelerator coverage then promotes faster local growth Explanation .

This is the **curvature-enhanced accelerator coverage, or CEAC, mechanism**. NIST's 2002 paper describes quantitative modelling of bottom-up growth using this principle [13]. The 2023 review explains the enrichment of strongly bound adsorbates on shrinking concave surfaces [14].

The explanation concerns adsorbed molecules on a moving interface. It does not mean that accelerator falls to the bottom under gravity, or that every flat trench floor must shrink in area. Competition between additives, potential and transport also matter. CEAC is a representative explanation for the relevant small-feature systems, not the only mechanism of bottom-up filling at every scale.

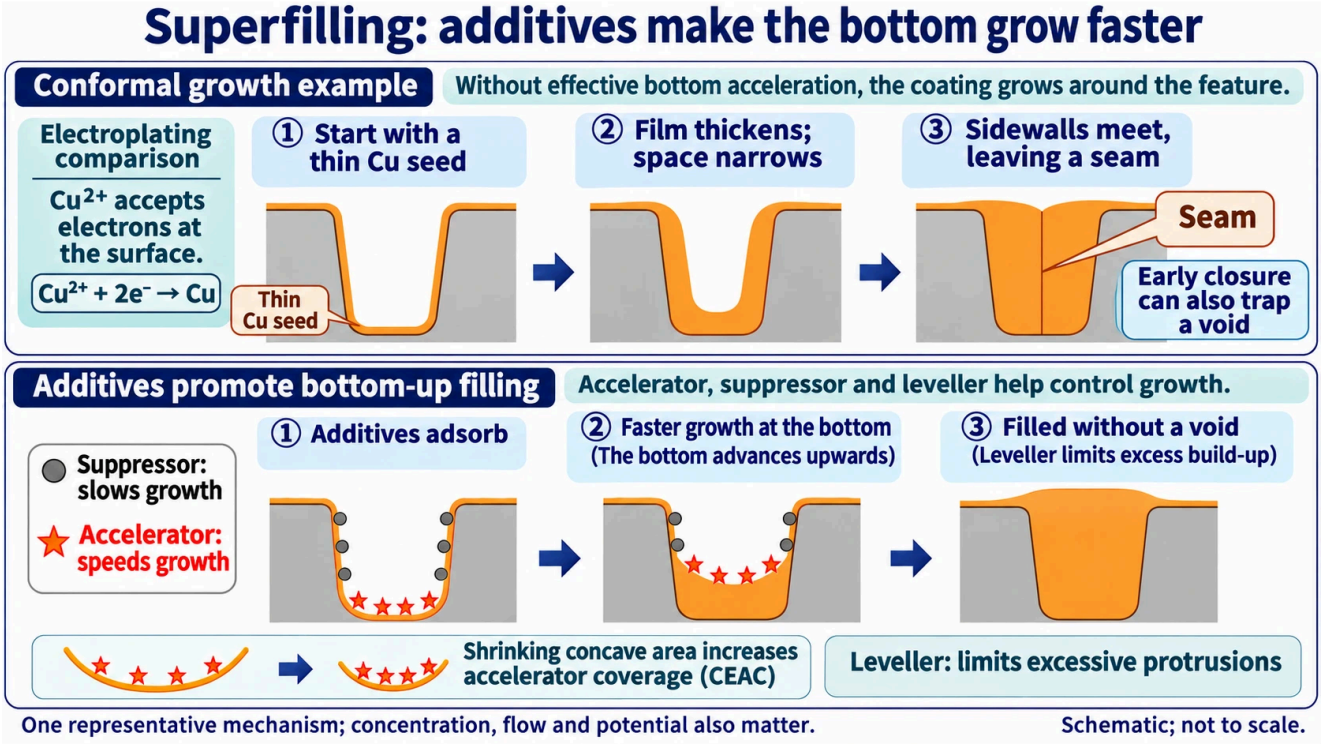


Figure 6 **Conformal growth versus additive-assisted filling** (schematic)

Reading the figure

Grey circles and red stars represent additive functions, not actual molecular sizes or counts. The inset keeps the same number of stars on a shorter concave arc to illustrate increased coverage. The leveller limits excessive build-up after filling as well as interacting during growth.

- **Electroplating was not the obvious choice at first**

In his 1999 account, IBM's Panos Andricacos recalls that PVD, CVD and electroless methods were initially considered for copper, while electrolytic copper was outside the team's early mainstream thinking [11].

IBM's 1998 paper dates its first damascene copper-plating demonstration to **1989**, a working microprocessor using the technology to **1997**, and manufacturing introduction to **1998** [10]. The 1999 account places the announcement in **September 1997**, shipments in **June 1998**, and production at Burlington, Vermont [11]. The early demonstration-to-production interval was roughly **nine years** Calculation . IBM reported a **40–45% resistance reduction** relative to aluminium-alloy interconnects in that development context [10].

9. Smaller wires and a wider role in packaging

- **The barrier takes up valuable cross-section**

A barrier prevents copper diffusion, but it is usually much less conductive than copper. If its thickness cannot shrink in proportion to the line width, it occupies a growing share of the conducting cross-section [8]. Surface and grain-boundary scattering also increase copper's resistivity as dimensions fall [9].

IRDS's **2024** roadmap identifies rising interconnect resistance, new barrier materials, ALD barriers and alternatives to copper as important issues. Its M1/Mx table shows barrier targets of **1.5 nm in 2024**, **1.0 nm in 2025**, **0.5 nm in 2027**, and a **barrierless** direction from **2029**. Ruthenium and molybdenum appear among candidate conductors; cobalt and ruthenium are discussed for local wiring [15] Reported .

These are roadmap targets, not a statement that every factory or product changes material in the indicated year. A 1.5 nm film is only a few atomic spacings thick, yet must remain sufficiently continuous and effective. That is one reason highly controlled deposition methods matter Explanation .

- **Plating also connects chips to one another**

Applied Materials identifies electrochemical deposition as a key process in advanced packaging, including **TSVs, pillars, redistribution layers, bumps, pads and hybrid-bonding structures**. Its page also lists gold, nickel, silver and tin alongside copper [17]. Lam's SABRE 3D family addresses TSVs, copper pillars, redistribution and microbumps [20].

AI accelerators and stacked HBM need dense connections within the package as well as inside each chip. Plating therefore spans on-chip wiring and the larger structures that join dies and package substrates. The dimensions and filling mechanisms are not identical across those applications Explanation .

10. Equipment suppliers: different strengths in different processes

Sputtering platforms

Applied Materials describes its **Endura** platform as a widely used interconnect-deposition system, stating that it has been involved in making the majority of microchips produced over the preceding two decades. Its product page describes configurations with up to **nine process chambers**, including two pre-clean chambers [16] Reported . These are the supplier's statements, not an independently calculated market share.

NAURA reports delivery of its **1,000th PVD tool** and lists applications including copper interconnects, aluminium pads, metal hard masks, metal gates and silicides on 300 mm wafers [23]. **ULVAC** highlights its experience in metal-film processes and high-volume manufacturing support [24].

The source article did not establish a recent, comparable primary-source market-share dataset for sputtering tools. Product descriptions are therefore used to explain supplier positions, without turning them into a numerical ranking.

Lam's deposition page lists ECD, CVD and ALD, while Tokyo Electron's 2026 report discusses oxidation, CVD and ALD in its deposition coverage [18][32]. Absence of a particular term or product from one page or report is not sufficient evidence that a company has no activities in the field Explanation .



The Commons description identifies an AJA International system in Cornell University's Nanoscale Science and Technology Facility. A research and prototyping installation differs in scale and configuration from a high-volume fab tool.
Photo: a13ean / Wikimedia Commons / CC BY-SA 3.0. Resized and converted to WebP.

Electroplating tools

Lam describes **SABRE** as a platform that helped lead the transition to copper interconnects [19], while SABRE 3D serves packaging structures [20]. Applied Materials describes filling features **below 20 nm** with **aspect ratios above 5:1**, suppressing sidewall growth while favouring bottom-up filling [17]. These are supplier descriptions of capability under their process conditions.

ACM Research is headquartered in **Fremont, California**, with most development and manufacturing in **China**, according to its 2025 Form 10-K [21]. Its Shanghai subsidiary's annual report quotes **Gartner's 2025 data** for an **8.2% global electroplating-equipment share and third place**, and claims a leading position in China's 300 mm copper-interconnect plating market [22] Reported .

ACM estimates a **US$1.5 billion electroplating-tool market in 2025**, compared with about **US$5.3 billion for PECVD**, using third-party research and customer information [21]. These are company estimates. NAURA reports introducing a 300 mm plating system [23]. **Uyemura** reports that sales of higher-value semiconductor wafer plating equipment supported improved equipment-business profit for the year ended March 2026 [29].

- **Keep the comparisons on the same basis**

The table is alphabetical by company and separates equipment from materials.

Company	Location or operating context	Example reported position
ACM Research / ACM Shanghai	US headquarters; much development and manufacturing in China	8.2%, third in plating equipment; Gartner data quoted by the subsidiary [22]
Applied Materials	United States	Broad installed use of Endura; company product statement [16]
JX Advanced Metals	Japan	About 65% of semiconductor sputtering targets; company estimate [25]
Konfoong Materials	China	RMB2.85 billion ultra-high-purity target revenue in 2025 [27]
Lam Research	United States	SABRE interconnect plating and SABRE 3D packaging applications [19][20]
NAURA	China	Reports delivery of its 1,000th PVD tool [23]
Solstice Advanced Materials	United States	Describes itself as the largest semiconductor-target manufacturer [26]
ULVAC	Japan	Metal-film equipment and powder-metallurgy targets [24]
Uyemura	Japan	Plating chemicals and wafer-plating equipment [29]

For context, **all semiconductor manufacturing equipment**, rather than these two processes alone, recorded **US$135.1 billion** of worldwide sales in 2025 in SEAJ/SEMI statistics. China accounted for **US$49.3 billion**, Taiwan **US$31.5 billion**, South Korea **US$25.8 billion** and Japan **US$9.5 billion** [30]. A Japanese government summary gives Japan-headquartered equipment suppliers about **28% of the worldwide equipment market in 2023** [31]. Neither dataset is a sputtering-only or plating-only national share table.

11. Targets and plating chemistry: the materials behind the tools

- **A target is an engineered material**

A sputtering target is not simply a metal plate cut to size. **Konfoong Materials**, also known as Jiangfeng Electronics, lists demanding purity requirements in its 2025 annual report [27]:

Target material	Purity example reported by Konfoong
Aluminium	At least 99.9995%, or 5N5
Copper	At least 99.9999%, or 6N
Tungsten	At least 99.999%, or 5N; specified harmful impurities such as sodium and potassium below one part in ten million

The same report identifies grain size and orientation control, bonding, precision machining, inspection, cleaning and packaging as core technologies. It highlights the difficulty of copper–manganese alloy targets and the importance of tantalum for barriers [27]. Uniform composition and microstructure contribute to repeatable erosion and film behaviour Explanation .

High-purity targets and competing supplier claims

JX Advanced Metals reports approximately **65% global share in semiconductor sputtering targets** and about **50% in high-purity tantalum powder** in its 2026 integrated report; both are company estimates [25]. It identifies purification, composition and microstructure control, surface treatment, analysis and equipment-maker relationships as strengths.

The report describes plans to raise target capacity to about **1.3 times fiscal-2025 levels**, centred on its Hitachinaka plant, and local finishing capacity to **1.4 times in Taiwan** and **twice the level in South Korea**, with additions coming progressively from fiscal 2027 [25]. These are capacity plans, not completed-output figures.

JX also highlights **99.9999999% purity copper, or 9N** [25]. The corresponding impurity fraction is on a **one-part-per-billion scale** Calculation . The purity basis and measured elements matter: a purity percentage cannot automatically be reinterpreted as exactly one impurity atom per billion copper atoms.

Solstice Advanced Materials, formed through the 2025 separation of Honeywell's advanced-materials business, calls itself the world's largest manufacturer of semiconductor sputtering targets. It highlights **6N copper** and fine-grain processing [26]. JX's share estimate and Solstice's largest-manufacturer claim are both supplier statements. Their scope or measurement basis may differ; this lesson does not independently reconcile them Explanation .

Other participants appear in **Materion's 2024 annual report**, which names competitors including Honeywell, Praxair, Solar Applied Materials Technology, Grikin and Tanaka Holdings [28]. Those names belong to the report's period. ULVAC reports favourable orders for targets made using powder-metallurgy technology [24].

Konfoong reports **RMB2.85 billion** in ultra-high-purity metal-target revenue for 2025, up **22%**, describes itself among leading global wafer-fabrication target suppliers, and discusses localisation of its raw-material supply chain [27]. It does not provide a matching global share percentage in the cited discussion.

Plating chemicals and the packaging market

Uyemura reports chemical sales, including internal sales, of **¥55.8 billion** for the year ended March 2026. Wafer- and package-related chemicals accounted for **¥44.49 billion** [29], or roughly **80%** Calculation .

Its reported regional wafer/package chemical sales were **Japan ¥13.5 billion**, **Taiwan ¥13.2 billion**, **China ¥12.4 billion**, **South Korea ¥2.83 billion**, **North America ¥1.59 billion** and **ASEAN ¥0.87 billion**. It identifies demand related to generative-AI servers as a contributor and discusses formaldehyde-free **electroless copper** chemistry for wafers [29]. Electroless deposition is a different process from the externally powered electroplating explained earlier.

These figures cover a broader wafer/package chemical business. They should not be presented as a market share for on-chip copper electroplating additives; the source article did not establish such a primary-source share dataset.

12. What future processes ask of materials and equipment

- **Thinner barriers, and potentially barrierless conductors.** The 2024 IRDS roadmap points towards 0.5 nm barriers and later barrierless directions [15]. Continuity, copper containment and electrical resistance must be balanced, with PVD, ALD and other methods selected for the structure.
- **Alternatives to copper at the smallest dimensions.** Cobalt, ruthenium, molybdenum and tungsten appear in discussions of local or advanced interconnects [15]. Different metals create new target, precursor and integration requirements Interpretation .
- **Reliable filling with very thin seeds.** Applied Materials describes sub-20 nm, high-aspect-ratio filling [17]. ACM describes plating developments for ultrathin seeds and advanced nodes including 28 nm, 14 nm and beyond [21]. Continuous current delivery and controlled additive action remain central.
- **More demanding package connections.** TSVs, pillars, redistribution and hybrid-bonding structures extend the importance of deposition beyond the transistor fab [17][20][29]. Dimensions, metals and reliability requirements vary across those applications.

Where materials expertise contributes

Useful skills include ultra-high-purity refining; grain and texture control; alloy design; target-to-backing-plate bonding; additive molecular design and bath analysis; new barrier materials; and reliable copper, tin, silver or nickel deposition. Japan has strong specialist suppliers in several of these areas, alongside major suppliers elsewhere. The common challenge is translating materials control into repeatable manufacturing performance.

13. A compact comparison

Topic	Key idea
PVD	Releases material from a solid source; evaporation and sputtering are different methods
Sputtering	Ions transfer momentum to the target; released atoms travel to the wafer
Magnetron	Magnetic fields increase electron residence and ionisation; electric fields accelerate ions
Deep-feature coverage	Directionality and sticking cause shadowing; collimation, long throw and ionisation offer different improvements
Barrier and seed	Barrier limits copper diffusion; seed provides a suitable conducting plating surface
Electroplating	$Cu^{2+} + 2e^- \rightarrow Cu$; deposited amount follows charge passed
Superfilling	Additives favour bottom-up growth; CEAC explains one important small-feature mechanism
Industry	Equipment, target and chemical markets have different leaders and share definitions
Next requirements	Thinner barriers, alternative metals, ultrathin seeds and advanced packaging

Next is **3-5: Photolithography fundamentals**. Having explored ways to create films, we turn to transferring circuit patterns into them using light and resist.

14. Check your understanding

1. Why does the lecture favour sputtering over evaporation for many integrated-circuit metal films?

▼ Show answer

Different alloy constituents can evaporate at very different rates, and line-of-sight evaporation has poor step coverage. Sputtering is generally better suited to alloy and compound deposition in this context. Evaporation remains useful elsewhere.

2. In the simple head-on collision model, does argon transfer a larger energy fraction to copper or tantalum?

▼ Show answer

Copper. The maximum fraction is $4M1M2/(M1+M2)^2$: about 0.95 for argon/copper and 0.59 for argon/tantalum. Similar masses improve energy transfer. Actual sputter yield also depends on binding and the collision cascade.

3. Why use RF rather than steady DC for an insulating target?

▼ Show answer

Positive charge accumulates on a dielectric surface under DC. During part of an RF cycle, electrons can neutralise that charge. Different electron and ion responses support a negative time-averaged target bias and sustained sputtering.

4. How does a magnetron increase sputtering rate, and why is a racetrack left behind?

▼ Show answer

Magnetic confinement keeps electrons in the target region longer, increasing argon ionisation. Ion bombardment concentrates in particular regions and erodes a track. The electron gyroradius is not its distance from the target surface.

5. Why can conventional sputtering leave poor coverage or a void in a deep feature?

▼ Show answer

A broad range of arrival angles and ready capture at the surface cause build-up near the opening. The walls shadow lower regions. If an overhang closes the entrance before filling is complete, an enclosed void can remain.

6. What does a collimator improve, and what does it cost?

▼ Show answer

It rejects oblique atoms and increases the near-normal component reaching the feature bottom. The cited patent reports about 4% bottom coverage without collimation versus 11–17% in its collimated examples. Capturing material in the filter reduces deposition rate.

7. Why add a copper seed before electroplating?

▼ Show answer

The dielectric does not provide a conducting plating surface, and conventional direct plating onto the barrier is difficult. A continuous copper seed distributes current from wafer-edge contacts and supports copper growth throughout the feature.

8. At 20 mA/cm², what approximate copper thickness is deposited per minute at 100% current efficiency?

▼ Show answer

About 0.44 µm/min, twice the approximately 0.22 µm/min value at 10 mA/cm². This assumes sufficient supply and the stated copper properties; total charge alone does not ensure uniform local thickness.

9. How does CEAC help explain bottom-up filling?

▼ Show answer

Accelerator remains on a concave growing surface as its area shrinks, increasing coverage and local growth rate. It is not settling under gravity. Suppressor competition, potential and transport also matter, while levellers limit excessive build-up.

10. Why do barriers become a larger electrical problem as wires shrink?

▼ Show answer

They are less conductive than copper and can occupy an increasing fraction of the line's cross-section. Copper also suffers stronger size-dependent scattering. Roadmaps therefore explore thinner barriers and alternative or barrierless conductors; their dates are targets, not universal production transitions.

15. Glossary

PVD
Physical vapour deposition; material is physically released from a source and transported to the substrate.

Evaporation
Heating a material in vacuum so its vapour can deposit on another surface.

Sputtering
Using energetic particle impacts to eject target atoms for deposition.

Target
The source plate supplying material in a sputtering system.

Sputter yield
Average number of target atoms released per incident ion.

DC sputtering
Sputtering using a direct-current supply, generally with a conducting target.

RF sputtering
Sputtering driven by radio-frequency power; suitable for insulating targets as well as conducting materials.

Magnetron
A sputtering source whose magnetic field increases electron confinement near the target.

Racetrack
The preferentially eroded region of a magnetron target.

Lorentz force
Force on a moving charge in an electromagnetic field; the magnetic part bends its trajectory.

Reactive sputtering
Sputtering in a reactive gas mixture to form a compound film.

Sticking coefficient
Probability that an arriving species is captured at a surface; process- and material-dependent.

Overhang
A deposit protruding near a feature opening and shadowing the interior.

Void
An unwanted enclosed empty region remaining in a deposited fill.

Collimator
A channelled filter that rejects particles travelling at large angles to the surface normal.

Long throw
Increased source–substrate separation used to improve arrival directionality.

Ionised PVD
PVD in which deposited metal is ionised, allowing electrical control near the substrate.

SIP
Self-ionised plasma; metal ions help sustain target sputtering when ionisation and return are sufficient.

Barrier
A film that limits copper diffusion into surrounding material.

Seed layer
A thin conducting layer supporting current distribution and subsequent plating.

Damascene
Forming a metal feature by filling a dielectric recess and polishing away excess material.

Electroplating
Depositing metal electrochemically using an external current.

Faraday's law
Relates electrochemical reaction amount to charge passed.

Faraday constant
Charge per mole of electrons, approximately 96,485 C/mol.

Electromigration
Current-driven atomic transport that can cause interconnect damage.

Superfilling
Preferential filling of recessed features from the bottom, enabled by appropriate chemistry and conditions.

Suppressor
An additive that inhibits local deposition.

Accelerator
An additive that promotes deposition relative to the inhibited surface.

Leveller
An additive that limits excessive growth and surface protrusions.

CEAC
Curvature-enhanced accelerator coverage; enrichment of adsorbed accelerator as a concave surface segment shrinks during growth.

16. Sources and further reading

1. **Stanford EE212, Plummer, Deal and Griffin; hosted by University of Washington EE528** — Chapter 9: Thin Film Deposition, pp.14–21, 23–24, 34 — Read source
2. **MIT OpenCourseWare, 6.152J, 2005** — PVD: Sputter Deposition, pp.2, 10–11, 14, 20–21, 24–25 — Read source
3. **K. Saraswat, Stanford EE311** — Deposition & Planarization, pp.6, 17–18 — Read source
4. **T. Deppisch et al.** — US7531071: Magnet arrangement for a planar magnetron, granted 2009, p.7 — Read source
5. **Applied Materials** — EP1091016A2: Self ionized plasma for sputtering copper, 2001, pp.1, 4–5 — Read source
6. **Lee et al.** — US5401675: Method of depositing conductors in high aspect ratio apertures using a collimator, granted 1995, pp.6, 8 — Read source
7. **S. M. C. A. Nichols, S. M. Rossnagel and S. Hamaguchi** — Ionized physical vapor deposition of Cu for high aspect ratio damascene trench fill applications, J. Vac. Sci. Technol. B 14, 3270, 1996; Osaka University repository — Read source
8. **K. Saraswat, Stanford EE311** — Copper Interconnect, pp.6, 10, 13, 17–18 — Read source
9. **K. Saraswat, Stanford EE311** — Cu Interconnect, lecture slides, PDF pp.2–3, 10–11, 16 — Read source
10. **P. C. Andricacos et al., IBM** — Damascene copper electroplating for chip interconnections, IBM J. Res. Dev. 42(5), 567, 1998, pp.567–570 — Read source
11. **P. C. Andricacos, IBM** — Copper On-Chip Interconnections, The Electrochemical Society Interface, Spring 1999, pp.32–37 — Read source
12. **B. K. Gale, University of Utah** — Electro Chemical Deposition, MEMS Lecture 12, p.3 — Read source
13. **T. P. Moffat, D. Wheeler, C. Witt and D. Josell, NIST** — Superconformal Electrodeposition Using Derivitized Substrates, Electrochem. Solid-State Lett. 5(12), C110, 2002 — Read source
14. **T. P. Moffat, T. M. Braun, D. Raciti and D. Josell, NIST** — Superconformal Film Growth: From Smoothing Surfaces to Interconnect Technology, Acc. Chem. Res., 2023 — Read source
15. **IRDS** — 2024 Edition, More Moore, pp.8, 20–21, Table MM-13 — Read source
16. **Applied Materials** — Endura PVD, product page, source article accessed 7 November 2026 — Read source
17. **Applied Materials** — Plating, product page — Read source
18. **Lam Research** — Deposition — Read source
19. **Lam Research** — SABRE Product Family — Read source
20. **Lam Research** — SABRE 3D Product Family — Read source
21. **ACM Research** — SEC Form 10-K, fiscal 2025, Items 1 and 2 — Read source
22. **ACM Research Shanghai** — Annual Report 2025, pp.20, 26, 46; Chinese edition — Read source
23. **NAURA** — Annual Report 2025, pp.17–18, 21–22; Chinese edition — Read source
24. **ULVAC** — Integrated Report 2025, pp.4, 28, 34; Japanese edition — Read source
25. **JX Advanced Metals** — Integrated Report 2026, PDF pp.8, 35–36; Japanese edition — Read source
26. **Solstice Advanced Materials** — Sputtering Targets and Coil Sets — Read source
27. **Konfoong Materials International** — Annual Report 2025, pp.11–13, 15; Chinese edition — Read source
28. **Materion** — Annual Report 2024, including Form 10-K, PDF p.13 — Read source
29. **Uyemura** — Results presentation for the year ended March 2026, 15 May 2026, pp.2, 13, 21; Japanese edition — Read source
30. **SEAJ and SEMI, 8 April 2026** — Worldwide semiconductor manufacturing equipment sales by region for 2025 — Read source
31. **Japan's Ministry of Economy, Trade and Industry** — Semiconductor and Digital Industry Strategy, Executive Summary, 23 December 2025, p.3; Japanese edition — Read source
32. **Tokyo Electron** — Integrated Report 2026, p.11 and report-wide terminology review; Japanese edition — Read source

17. Claim-to-source notes

Claim group	Basis and scope	Type
Film choices, evaporation/sputtering comparison, yield and angular/sticking models	Stanford EE212 [1]; historical teaching context, not universal modern specifications	Reported
Collision-energy model, DC/RF distinction, electron-motion example and reactive sputtering	MIT lecture [2]; representative parameters	Reported
Magnetron conditions, racetrack, shadowing and gas mean free path	Stanford EE311 [3]; lecture estimates	Reported
Planar/cylindrical target utilisation	Patent [4]; large-area coating context	Reported
Conventional PVD, long throw, plasma limitations and SIP	Applied Materials patent [5]; claims refer to its process context	Reported
Collimator geometry, coverage and rate comparisons	Patent [6]; particular reported examples	Reported
Approximately 85% copper ionisation	Nichols, Rossnagel and Hamaguchi [7]; 1996 experimental context	Reported
Barrier/seed roles, copper properties, electrochemical reactions and additive categories	Stanford copper lectures [8][9]	Reported
Seed current distribution, superfilling and development chronology	IBM paper [10] and author account [11]	Reported
Faraday's law and conducting-surface requirements	University of Utah lecture [12]	Reported
CEAC, competitive adsorption and bottom-up filling	NIST papers/review [13][14]; not a universal description of every feature scale	Reported
Barrier thickness and alternative-conductor directions	IRDS 2024 [15]; roadmap targets, not guaranteed production dates	Reported
Endura use and chamber configurations	Applied Materials product page [16]; supplier statement	Reported
Packaging plating and fine-feature capability	Applied Materials [17] and Lam [20]; product descriptions	Reported
Lam deposition portfolio and SABRE role	Lam pages [18][19]	Reported
ACM headquarters, operations, market estimates and ultrathin-seed processes	ACM 2025 Form 10-K [21]	Reported
Plating share and rank	ACM Shanghai report quoting Gartner [22]; category and period retained	Reported
NAURA PVD shipments, applications and plating	Annual report [23]	Reported
ULVAC equipment and powder-metallurgy target business	Integrated report [24]	Reported
JX share, purity and capacity plans	Integrated Report 2026 [25]; company estimates and plans	Reported
Solstice formation and target claims	Corporate product information [26]; supplier claim	Reported
Konfoong purity, capabilities and revenue	Annual Report 2025 [27]	Reported
Competitor names in target materials	Materion Annual Report 2024 [28]; names belong to that period	Reported
Uyemura sales, regional mix and chemical development	Results presentation [29]; broader wafer/package chemicals, not only on-chip additives	Reported

Claim group	Basis and scope	Type
Equipment purchases by region and Japan-headquartered suppliers' share	SEAJ/SEMI [30] and METI [31]; all equipment	Reported
TEL report terminology	Japanese source's review of [32]; absence of a term does not establish absence of a business	Reported
Energy fractions, mass ratio, gyroradius, free paths, plating rates, purity fraction and revenue proportion	Calculations from stated inputs; assumptions identified in the text	Calculation
Possible differences behind supplier rankings; demand for new source materials	Interpretation, not harmonised market datasets or guaranteed forecasts	Interpretation
Particle paths, electrical versus magnetic roles, coating versus filling and additive illustrations	General explanations; diagrams are schematics, not quantitative process simulations	Explanation

Updated 7 November 2026. This English edition presents the same technical material in prose written for an international readership. Historical lecture examples and company figures retain their stated dates and scope. Reported information, calculations, interpretation and explanation are labelled separately. All six Image Gen diagrams are teaching schematics. The seven existing photographs retain their individual credits and licences.

© 2026 Troy Technical. Original text and illustrations: all rights reserved, subject to applicable legal exceptions. The credited photographs retain their stated licences. Links to this article are welcome.
Teaching diagrams localised with the built-in Image Gen tool for this English edition.