SEMICONDUCTOR FRONT-END · PART 3-3

Deposition: CVD and ALD
Building a chip, one thin film at a time

A chip needs more than silicon and its oxide. It needs conductors, insulators and protective layers, often inside features much deeper than they are wide. Chemical vapour deposition turns gas-phase precursors into solid films. Atomic layer deposition separates the reactions to gain finer control. This lesson explains what pressure, plasma and surface chemistry each contribute, then connects those ideas to logic, memory and the global equipment and materials supply chain.

Semiconductor Front-End Series · Part 3-3 · Intermediate introduction · Helpful background: Lesson 3-2 · Updated 7 November 2026

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How to read this lesson

Begin with the main text. The shaded physics boxes add optional detail and worked estimates. Figures are conceptual and not to scale. Numbered links lead to the supporting sources.

What you will learn

- Explain how gas transport and surface chemistry jointly determine CVD growth.
- Describe what lower pressure, plasma assistance and self-limiting ALD reactions each make possible.
- Connect thin-film requirements in logic and memory to the equipment and precursor companies serving them.

1. Three ideas to keep in mind

- **A film grows only as fast as its slowest essential step.** In CVD, the bottleneck may be the surface reaction or delivery of fresh precursor. The distinction tells engineers whether to focus on temperature, gas flow or reactor geometry.
- **ALD controls growth by separating and saturating reactions.** With adequate exposure and purge, it can coat deep features remarkably evenly. A cycle usually should not be imagined as placing one complete atomic layer on the wafer.
- **Equipment and chemistry are inseparable.** Leading suppliers operate across the United States, Europe and Asia. Market shares describe particular equipment or materials categories; they are not directly interchangeable measures of national strength.

2. Why a chip needs deposited films

Oxidation cannot supply every material

Lesson 3-2 showed how thermal oxidation consumes silicon to grow silicon dioxide. That is valuable, but a working chip also needs silicon nitride, metals and high-permittivity dielectrics. It may need a new film on top of an existing insulator or metal rather than on exposed silicon.

Lam Research describes CVD and ALD as precision methods for small tungsten connections and barrier films, while PECVD, high-density plasma CVD and ALD provide important insulating layers [5] Reported .

Film	Example function	Example process
Polycrystalline silicon	Electrodes and conducting features	LPCVD, 575–650°C [1]
Silicon nitride, Si_3N_4	Oxidation masks and surface protection	LPCVD, 650–800°C; PECVD, 200–400°C [1]
Silicon dioxide, SiO_2	Insulation between conductors and gap filling	CVD, 200–800°C; TEOS-based plasma processes include 25–400°C examples [1]
Tungsten, W	Contacts and vias	LPCVD, 250–500°C [1]
Hafnium-based high-k oxides	Gate insulation	ALD [12]

The temperature ranges are **teaching examples from Stanford's 1999 course material**, not universal specifications for today's tools. Precursor chemistry, reactor design, substrate and required film properties change the usable range Explanation .

Supplying the material from outside

In thermal oxidation, the Si/SiO_2 interface moves into the silicon while the oxide also extends above the original surface. In CVD and ALD, the principal film-forming material arrives from an external source as a gas or vapour. This expands the range of possible films and underlying surfaces.

It does not make every material compatible with every substrate. The precursor must react appropriately, nucleation must begin where required, and the substrate must tolerate the temperature and chemistry. Interfacial reactions and contamination can still determine whether a nominally correct film is useful Explanation .

3. CVD: the journey from gas to solid

- **Seven steps, not one event**

CVD stands for **chemical vapour deposition**. Stanford's lecture notes divide the process into seven steps [1] Reported :

1. Deliver precursor gas to the deposition region.
2. Transport precursor through the near-surface boundary layer, where diffusion becomes important.
3. Adsorb precursor species onto the surface.
4. React at the surface to form the solid film.
5. Desorb gaseous reaction by-products.
6. Transport those by-products away through the boundary layer.
7. Carry them out of the reactor.

For example, silane can decompose thermally to deposit silicon [2]:

$$SiH_4 \rightarrow Si\ (film) + 2H_2$$

Another teaching example forms silicon nitride from dichlorosilane and ammonia at about 750°C [2]:

$$3SiH_2Cl_2 + 4NH_3$$

$$\rightarrow Si_3N_4 + 6H_2 + 6HCl$$

These equations describe overall reactions. The actual surface mechanism involves intermediate species and several individual reaction steps Explanation .

Two resistances in series: transport and reaction

A simple model separates delivery to the surface from incorporation into the film [1]:

- **Transport flux:** $F_1 = h_G(C_G - C_S)$.
- **Surface-reaction flux:** $F_2 = k_S C_S$.

C_G is precursor concentration in the bulk gas, C_S is its concentration at the surface, h_G is a mass-transfer coefficient and k_S is a surface-reaction coefficient. At steady state, $F_1 = F_2$. Stanford draws a parallel with the Deal–Grove oxidation model from Lesson 3-2 [1]. MIT explains the two processes using **electrical resistances in series** [2] Reported .

If $\mathbf{k_S \ll h_G}$, precursor arrives faster than it reacts. Growth is **surface-reaction-limited**. The reaction coefficient follows an Arrhenius dependence, $k_S = k_0 \exp(-E_A/k_B T)$, so temperature is especially important.

If $\mathbf{h_G \ll k_S}$, the surface can consume precursor faster than it is replenished. Growth is **mass-transport-limited**. Flow and reactor geometry become particularly important. Transport still depends on temperature, but generally less strongly than the exponential reaction term [1] Reported .

A worked example. Using the lecture's 1.6 eV activation energy for silicon epitaxial growth, increasing temperature from 600°C (873 K) to 650°C (923 K) changes the reaction coefficient by $\exp[(1.6/8.617\times10^{-5})(1/873 - 1/923)] \approx$ **3.2 times** Calculation . A 50°C difference can therefore produce a large growth difference in a reaction-limited process. Temperature uniformity matters across a wafer and across a batch.

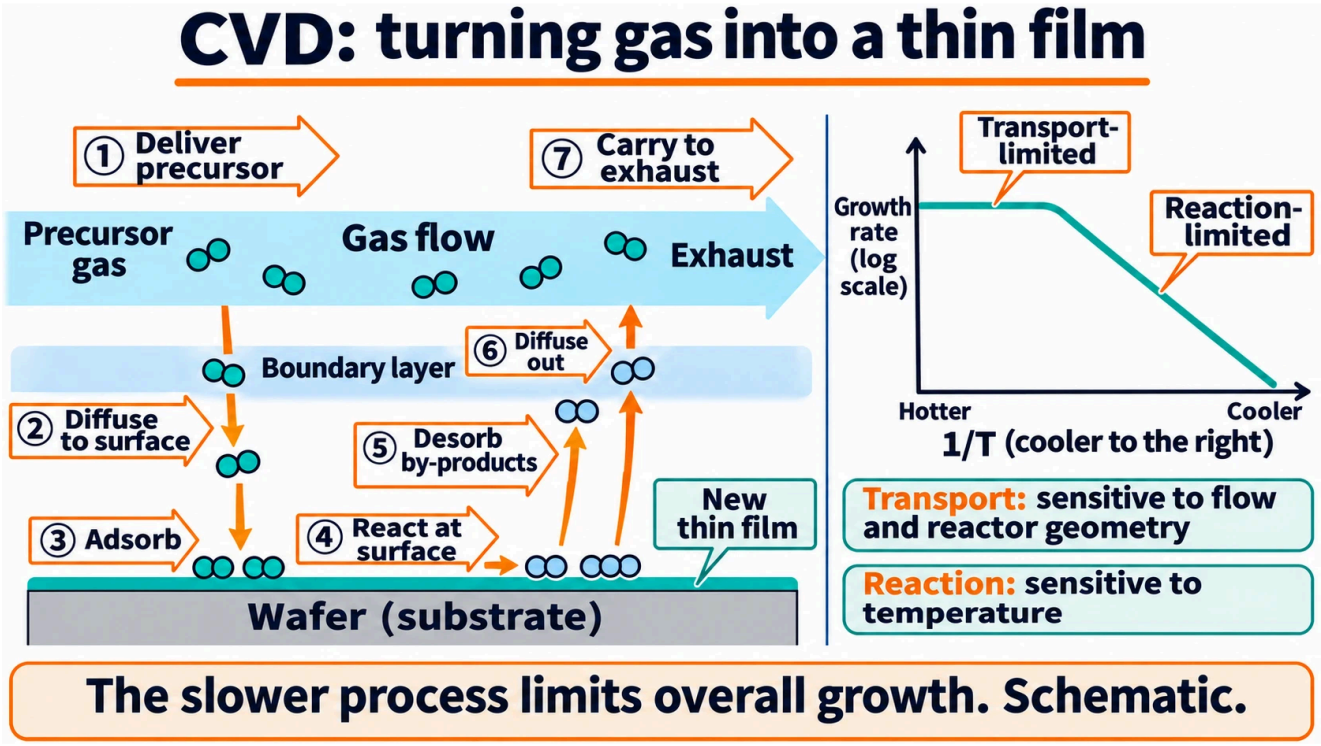


Figure 1 **From precursor delivery to film growth** (schematic)

Reading the figure

The graph uses **1/T**, so the hotter end is on the left. Its plateau is a simplified illustration of relatively weak temperature dependence in the transport-limited regime. The curve is conceptual, not a measured process recipe.

4. LPCVD: what lower pressure changes

Molecules travel farther between collisions

In a transport-limited process, differences in precursor delivery can become differences in film thickness. **Low-pressure CVD, or LPCVD**, reduces some of those transport constraints.

The **mean free path** is the average distance a gas molecule travels before colliding with another molecule. MIT gives the kinetic-theory relation [3]:

$$\lambda = k_B T / (\sqrt{2}\, \pi\, d^2 p)$$

Here d is molecular collision diameter and p is pressure. For the same gas at the same temperature, **λ is inversely proportional to pressure**.

Pressure	Approximate mean free path in the lecture
1 atmosphere	10^{-5} cm, or 0.1 μm
1 Torr, about 1/760 atmosphere	10^{-2} cm, or 0.1 mm
1 mTorr	10 cm

These are order-of-magnitude teaching values [3]. A calculation specifically for **nitrogen at 300 K**, taking d ≈ 0.37 nm, gives **about 68 nm at one atmosphere** and **52 μm at 1 Torr** Calculation . The two sets of values have different precision and should not be mistaken for inconsistent measurements of one specified gas.

Longer mean free path is part of a transport story

MIT gives the approximate scaling $D_{gas} \propto T^{3/2}/p$ [3]. In Stanford's illustrative boundary-layer model, reducing pressure to 1 Torr raises the diffusion coefficient by 760 times. The boundary layer becomes about seven times thicker, leaving a roughly **100-fold improvement in h_G** [1] Reported .

This is a model estimate, not a promise that every modern LPCVD reactor improves by exactly that factor. It shows why reduced pressure can make surface-reaction-limited conditions easier to obtain. Lower pressure does not have to mean a thinner boundary layer Explanation .

Uniform temperature and adequate supply enable batch processing

When transport becomes less restrictive, engineers can place more emphasis on controlling the surface reaction. A **hot-wall reactor** heats the reaction tube as well as the wafers. Stanford explains that this provides good temperature control and permits closely spaced wafer loading [1]. MIT lists reduced gas-phase reactions and good step coverage among LPCVD's advantages, and describes hot-wall LPCVD as a representative polysilicon process in its 2005 course [2] Reported .

In a vertical batch furnace, the wafers are stacked vertically, but **each wafer itself is horizontal**. Many wafers can be processed together. Temperature alone does not ensure uniform films: precursor concentration, flow and depletion as material is consumed must also be controlled Explanation .

Batch deposition systems from companies including KOKUSAI ELECTRIC and Tokyo Electron build on these reactor principles.

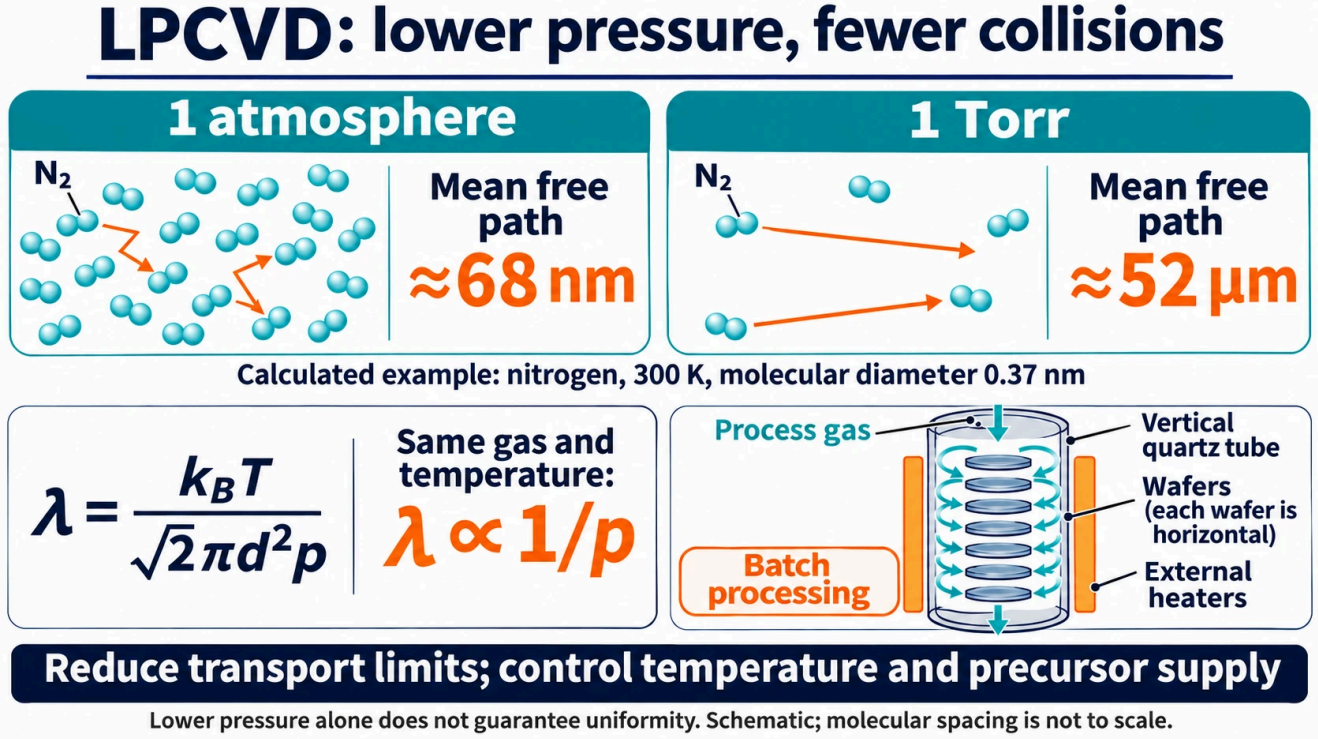


Figure 2 **Lower pressure reduces molecular collisions** (schematic)

Reading the figure

Longer free paths help explain reduced transport constraints. They do not mean that molecules never collide, or that a batch automatically receives identical precursor doses. The molecular spacing and furnace dimensions are schematic.

5. PECVD: helping chemistry without heating everything equally

- **Why temperature becomes a constraint**

Once temperature-sensitive structures exist, later steps have less freedom to heat the wafer. MIT uses aluminium interconnects as a teaching example: temperatures below about **450°C** help avoid unwanted aluminium–silicon reactions, and a plasma can supply energy for deposition [2]. That is a historical process example, rather than a universal temperature limit for all modern chips.

Plasma-enhanced CVD, or PECVD, uses energetic electrons to excite and dissociate precursor molecules. Reactive fragments, radicals and ion interactions can assist film growth at lower wafer temperatures [1]. Stanford's silicon nitride examples compare **650–800°C for thermal LPCVD** with **200–400°C for PECVD** [1] Reported .

Electron energy is not wafer temperature

University of Siegen teaching material describes low-pressure, non-equilibrium plasmas at roughly **0.1–10 Torr**, with representative electron energies of **0.5–10 eV** [4] Reported .

Using E/k_B, 1 eV corresponds to an energy scale of about 11,600 K. Thus 0.5–10 eV corresponds to roughly **5,800–116,000 K** Calculation . Those numbers describe an energy scale for electrons. They are **not the temperature of the wafer or of the whole gas**, and a precise electron-temperature interpretation depends on the distribution and definition used.

Light electrons gain energy readily from an electric field. Elastic collisions transfer relatively little of that energy to much heavier particles, while inelastic collisions can excite or dissociate molecules. The populations need not be in thermal equilibrium. Useful chemical activation can therefore occur without heating the entire system to the corresponding electron energy scale Explanation .

Lower temperature still comes with trade-offs. Film density, retained hydrogen, stress, electrical properties and plasma damage must be managed. A lower-temperature film with the same nominal composition is not automatically equivalent to a high-temperature one Explanation .

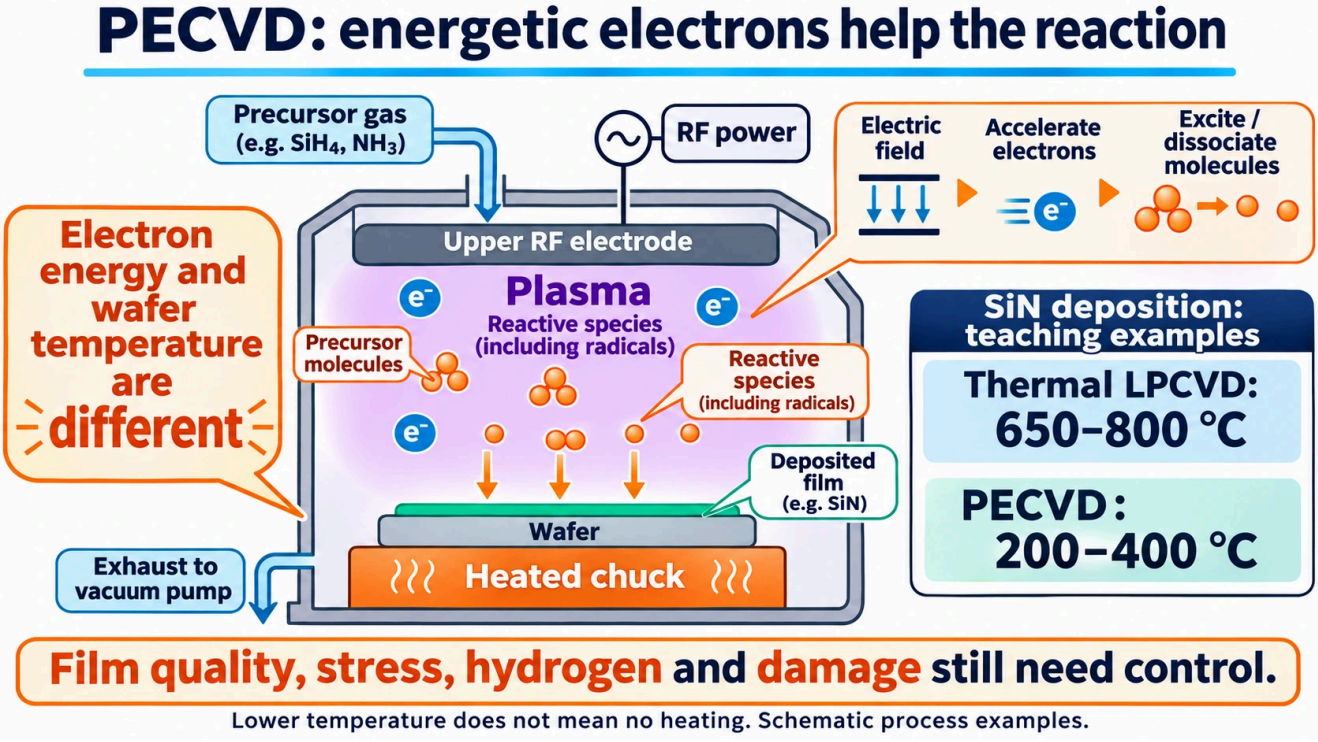


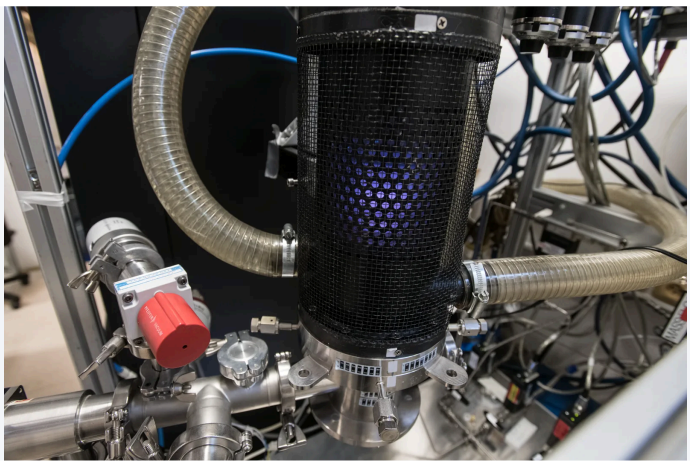
Figure 3 **Energetic electrons assist lower-temperature deposition** (schematic)

Reading the figure

The two silicon nitride temperature ranges are lecture examples. The important distinction is between electron energy and wafer temperature. PECVD can reduce the required wafer temperature without eliminating heating or damage-control requirements.

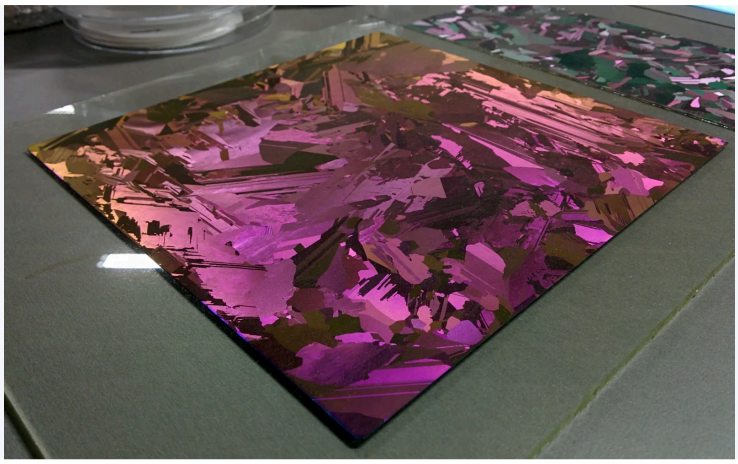


The Commons description identifies this as an STS multiplex PECVD system in the LAAS research facility in France. The equipment has a PECVD label on its front panel.
Photo: Guillaume Paumier (user:guillom) / Wikimedia Commons / CC BY-SA 3.0. Resized and converted to WebP.



A detail of a low-temperature plasma research system at the Institute of Physics of the Czech Academy of Sciences, according to its Commons description. A blue-violet glow is visible behind the mesh.
Photo: René Volfík, Institute of Physics of the Czech Academy of Sciences / Wikimedia Commons / CC BY-SA 4.0. Resized and converted to WebP.

- **What the colours of a film can reveal**



According to the Commons description, this multicrystalline silicon wafer from a photovoltaic laboratory at the University of New South Wales carries a PECVD silicon nitride coating of roughly 100 nm or less. It is an unsuccessful, non-uniform coating. It is not a circular single-crystal wafer for integrated-circuit production.
Photo: Radiotrefoil / Wikimedia Commons / CC BY-SA 4.0. Resized and converted to WebP.

Light reflected from the film's top and bottom surfaces interferes, rather like light reflected from a soap bubble. Different thicknesses can strengthen different colours. The patchwork in this example makes non-uniformity visible. Colour also depends on refractive index and viewing angle, so it is not a unique thickness measurement on its own Explanation .

- **HDP-CVD: depositing and removing material together**

High-density plasma CVD combines deposition with ion-driven sputtering. Stanford describes its use for silicon dioxide gap filling in interconnect processing: directional ions remove protrusions near a gap's entrance while deposition continues, helping prevent void formation [1] Reported . The useful idea is that a good filling process may need controlled removal as well as addition.

6. Coating a deep feature without sealing its entrance

- **Conformality and gap filling are different requirements**

The **aspect ratio** of a hole or trench is its depth divided by its width. **Step coverage** compares film thickness on its walls or bottom with thickness on the top surface. A **conformal** coating closely follows the underlying shape.

If material accumulates near the entrance, the opening can close before the interior fills. Lam describes how this can leave voids in tungsten features, raising resistance and compromising connections [6] Reported .

A conformal coating need not fill the hole. Often the aim is a thin insulating liner with an open centre, as in a capacitor. In other applications the goal really is complete metal or dielectric gap filling. Those tasks require different process choices Explanation .

Why a lower sticking probability can help

The **sticking coefficient** describes the probability that an arriving species is captured or incorporated at the surface. Stanford uses the following illustrative values [1] Reported :

Process example	Sticking coefficient in the teaching model
Physical deposition such as sputtering or evaporation	Modelled as 1
LPCVD silicon dioxide from silane	0.2–0.4
LPCVD silicon dioxide from TEOS	0.05–0.1
LPCVD tungsten	Below 0.01
LPCVD polysilicon	Below 0.001

Actual probabilities depend on species, surface state and temperature; **not every PVD process has a coefficient of one**.

A species that reacts at its first encounter is easily consumed near the opening. One that undergoes several surface encounters before incorporation has more opportunity to travel deeper. With adequate precursor supply, lower effective sticking can therefore improve coverage [1] Reported . ALD adds another useful mechanism: once the upper surface reaction saturates, additional precursor can continue towards unsaturated sites farther inside Explanation .

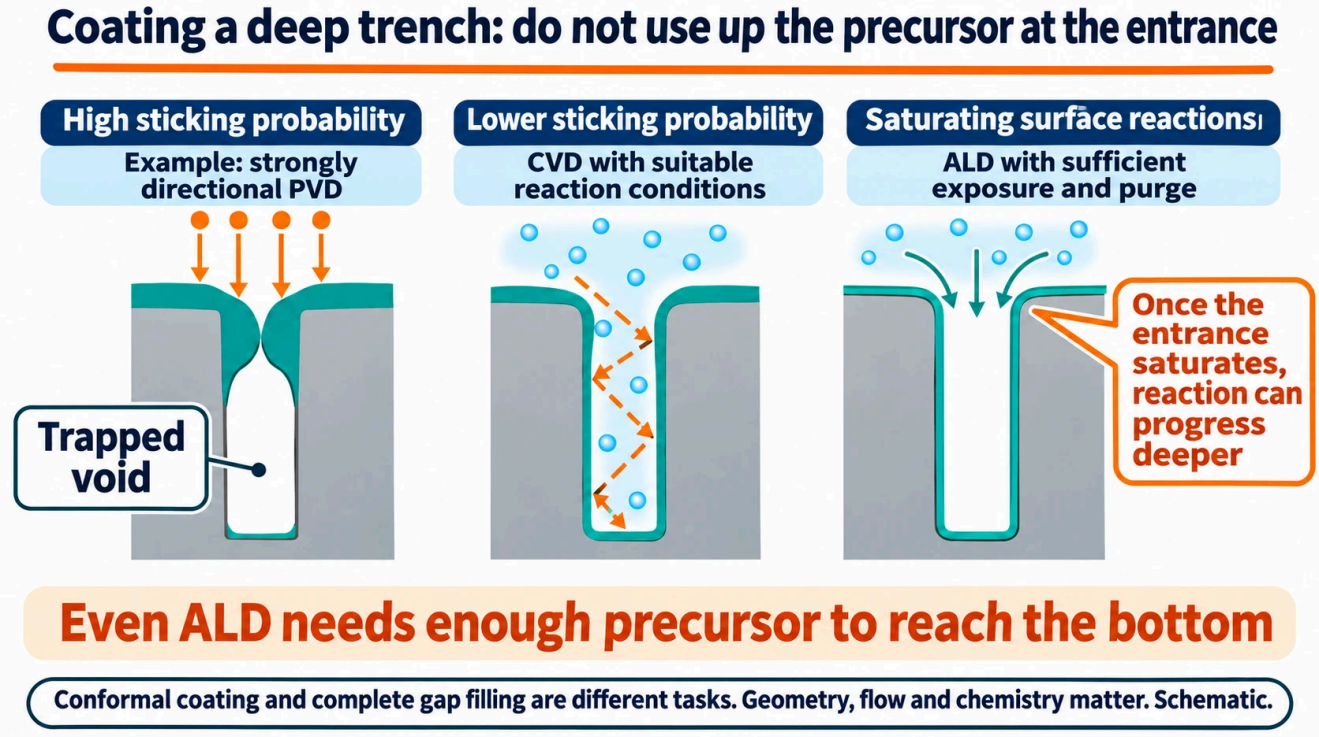


Figure 4 **Sticking, saturation and deep-trench coverage** (schematic)

Reading the figure

Only the left panel contains a trapped void caused by closure. The open centre of the ALD panel is intentional: it is a coating, not a completed fill. ALD still needs enough exposure and purge time to serve the deepest surface.

7. ALD: separating reactions to control each increment

- **Alternating doses, self-limiting surface chemistry**

Atomic layer deposition uses sequential, self-limiting gas–solid reactions. Puurunen's review identifies conformal coating of complex surfaces as a central capability [7]. ASM explains the repeated sequence of precursor pulses separated by inert-gas purges [8] Reported .

A familiar example deposits **aluminium oxide** using trimethylaluminium, **TMA, $Al(CH_3)_3$**, and water. One cycle has four steps [7]:

1. **Dose TMA.** It reacts with available surface groups. The half-reaction approaches saturation as the relevant sites or adsorption configurations become occupied.
2. **Purge.** Remove excess TMA and volatile by-products, while adsorbed species remain.
3. **Dose water.** Water reacts with the methyl-terminated surface, forms Al–O bonds and regenerates reactive surface groups. This half-reaction also saturates.
4. **Purge again.** Remove excess water and by-products before the next TMA dose.

The review's author-hosted full text provides a detailed treatment of the chemistry.

One cycle is not necessarily one atomic layer

For the TMA/water process at **300°C**, Puurunen gives an example growth increment of **about 0.09 nm per cycle**, around **30% of an alumina monolayer** [7] Reported .

For a 10 nm film, 10/0.09 ≈ **110 cycles** Calculation . This is a steady-growth estimate. Nucleation delay, substrate chemistry and changing initial growth can affect the actual cycle count.

Ligand crowding and the density of reactive surface groups help determine the increment. “Atomic layer” describes the scale and reaction control; it does not guarantee that every cycle deposits one complete sheet of atoms Explanation .

Temperature windows and precursor separation

An illustrative **ALD window** is a temperature range over which growth per cycle is comparatively stable [7]. At lower temperature, condensation or incomplete reactions can alter growth. At higher temperature, precursor decomposition may introduce CVD-like growth, while desorption may reduce incorporation. A flat window is not a compulsory feature of every valid ALD process Explanation .

Puurunen also describes how inadequate purging can leave TMA and water present together in the gas phase, introducing a CVD-like contribution and increasing growth per cycle [7] Reported . The aim is not simply to alternate valve signals. The reactor must actually separate the reactants sufficiently and deliver each to the required surfaces.

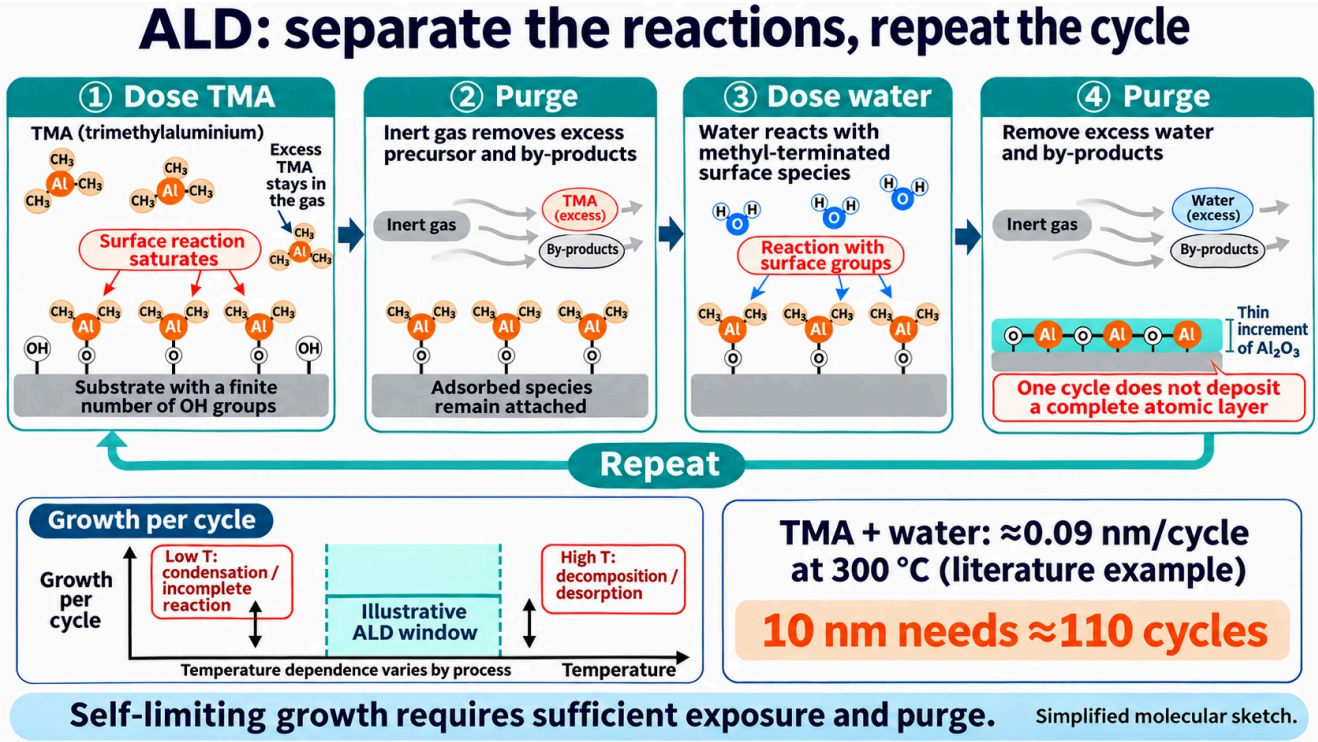


Figure 5 **An ALD cycle and its growth increment** (schematic)

Reading the figure

The 0.09 nm value is a literature example at 300°C, not a universal ALD constant. The temperature plot shows an illustrative window; arrows outside it indicate that growth can change in different directions for different mechanisms. Molecules and bonds are simplified.

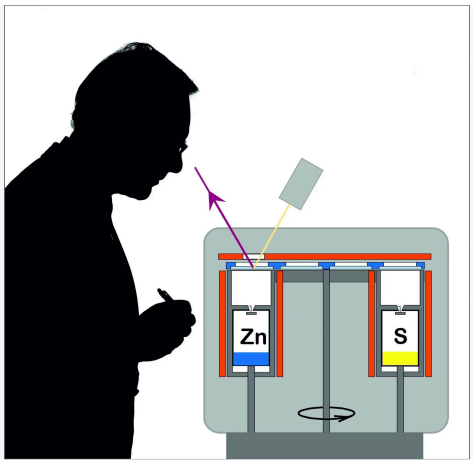


The Commons description identifies an ALD installation at the Institute of Physics of the Czech Academy of Sciences. The central stainless-steel vessel has a viewing window; gas lines are on the left and a glovebox on the right allows controlled-atmosphere handling.
Photo: René Volfík, Institute of Physics of the Czech Academy of Sciences / Wikimedia Commons / CC BY-SA 4.0. Resized and converted to WebP.

Two independent routes to the same principle

ALD's history includes **molecular layering in the Soviet Union in the 1960s** and **atomic layer epitaxy, or ALE, in Finland in the 1970s** [10]. Puurunen's 2005 review describes work by Aleskovskii's group on titanium tetrachloride/water reactions reported at a 1965 meeting and published in 1967 [7] Reported .

In Finland, **Tuomo Suntola** carried out initial experiments in **1974** [7]. The US patent by Suntola and Jorma Antson was granted in 1977, claiming priority from a Finnish application filed on **29 November 1974** [9] Reported .



This is a historical reconstruction, not a photograph of the original 1974 apparatus. The Commons description combines a 2014 silhouette of Suntola with a reactor sketch redrawn by Riikka Puurunen and Suntola from his original drawing. It depicts observation of purple interference colours as the film grows.
Image: Riikka Puurunen and Tuomo Suntola / Wikimedia Commons / CC BY-SA 4.0. Resized and converted to WebP.

Suntola received the **€1 million Millennium Technology Prize in 2018**. Technology Academy Finland highlighted ALD's importance in making the ultrathin films required by microprocessors and memory, and described the rapid expansion of semiconductor use from the early 2000s [11] Reported .



According to the Commons description, Suntola is presenting a talk on four decades of Finnish ALD development at an international ALD meeting in Helsinki in May 2014.
Photo: Riikka Puurunen / Wikimedia Commons / CC BY-SA 4.0. Resized and converted to WebP.

A major CMOS milestone: Intel's 2007 high-k gate

For its 45 nm generation in 2007, Intel introduced a hafnium-based high-k gate dielectric. Its engineers wrote that they evaluated sputtering, CVD and ALD before selecting ALD, and described this as the technology's first use in high-volume CMOS manufacturing [12] Reported .

That milestone came more than three decades after the 1974 Finnish experiments Calculation . It should not be read as the beginning of every industrial use of ALD: its earlier development and applications had a broader history.

Throughput and temperature: different improvements

ALD's repeated dose-and-purge sequence takes time. Two approaches address productivity:

- **Batch ALD** processes many wafers together. KOKUSAI ELECTRIC identifies this as a way to offset the time required by repeated gas sequences [14].
- **Spatial ALD** separates the reactants in space rather than relying only on temporal separation and purging. The substrate encounters different reaction zones [13].

Plasma-enhanced ALD, or PEALD, addresses a different requirement: plasma energy can enable reactions at lower wafer temperature, helping with temperature-sensitive applications [8]. It should not automatically be treated as a throughput improvement. Film quality, penetration and damage still need process-specific assessment Explanation .

8. Where the films go: logic, NAND and DRAM

Logic: gate dielectrics and spacers

ASM lists high-k metal gates, patterning spacers, gate spacers and metal–insulator–metal capacitors among ALD applications [8]. The film must have the right thickness and properties around a three-dimensional feature, rather than only on a flat test wafer.

In **spacer-based multiple patterning**, the thickness of a deposited sidewall film helps define a later feature's width. Lam identifies this as an important ALD application [15]. A line is first patterned; a thin conformal film is deposited around it; subsequent processing uses its sidewalls to create finer features. Lesson 3-6 will return to the patterning sequence Explanation .

3D NAND: many layers, then metal between them

NAND flash stores information in vertically stacked memory cells. IRDS's **2023** roadmap gives an example of **200 layers at roughly 50 nm per layer**, creating a stack about **10 µm** tall. It discusses production beyond 250 layers and the prospect of 500 or even 1,000 layers [17]. As a dated manufacturing milestone, SK hynix announced the start of **321-high NAND** mass production in **November 2024** [18] Reported .

Lam describes PECVD deposition of well over 100 alternating film pairs for 3D NAND [16]. Each layer's thickness, stress and defect level matters. Small stress contributions repeated many times can bow the wafer or destabilise the stack Explanation .

The structure also needs conducting **word lines**. These extend laterally between insulating layers; they are distinct from the vertical channel hole. Lam describes tungsten word-line filling and CVD/ALD processes for small tungsten and molybdenum features [6][25]. Tokyo Electron likewise discusses next-generation transition metals for NAND word lines [27] Reported .

- **DRAM: a thin dielectric between two deep electrodes**

DRAM stores charge in a capacitor. A deep structure provides more electrode area within a small footprint, while a thin high-k dielectric separates the electrodes. The introduction to a **2025** paper summarises prior work on zirconia/alumina/zirconia, **ZAZ**, dielectrics and trench aspect ratios above **100:1** [19] Reported . Those statements summarise earlier literature rather than reporting all such structures as that paper's own experiment.

Coating the full depth evenly helps control leakage and capacitance. Tokyo Electron identifies demanding DRAM capacitor deposition as a customer requirement [27].

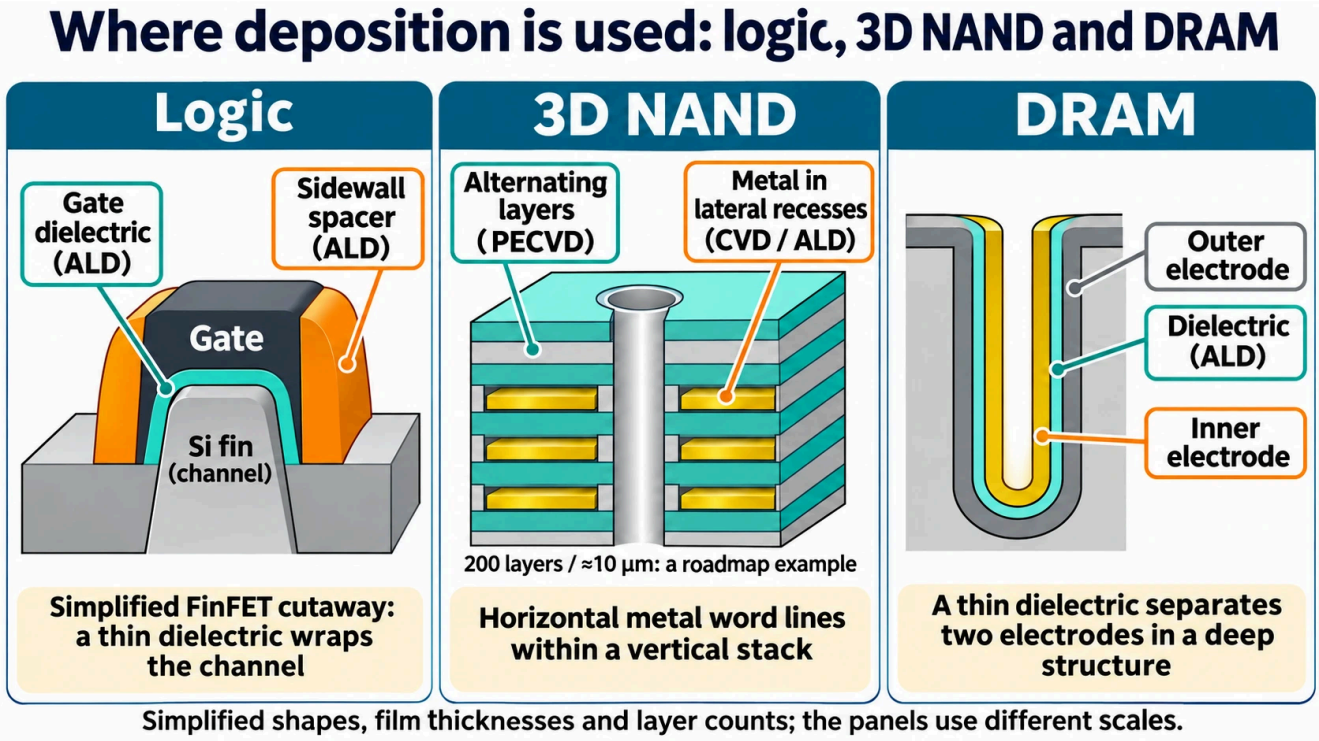


Figure 6 **Different devices, different deposition tasks** (schematic)

Reading the figure

The NAND metal word lines run horizontally, while the channel feature is vertical. In the DRAM panel, the teal dielectric is between the grey outer electrode and gold inner electrode. Layer counts, thicknesses and relative dimensions are simplified; the panels do not share a scale.

9. The equipment industry: several markets inside one label

Scale and definitions

Piotech's **2025 annual report**, published in 2026, estimates the global deposition equipment market at about **US$25.5 billion** for 2025. Citing industry data, it describes deposition as historically about **22% of front-end equipment spending**, with PECVD accounting for about **33%** and ALD about **11%** of deposition equipment [23] Reported .

These figures come from a supplier's report, including its use of external market research. They should be read with that attribution, rather than as independently reconstructed market totals.

A global supplier map

The table is alphabetical. It describes representative positions, not a single ranking of all suppliers.

Company	Headquarters	Deposition focus or reported position
Applied Materials	United States	Broad materials-engineering portfolio, including deposition [26]
ASM International	Netherlands	Single-wafer ALD; reports a share above 55% in that category [28]
KOKUSAI ELECTRIC	Japan	Batch deposition; reports 49% in batch deposition and about 80% in batch ALD-capable equipment [14]
Lam Research	United States	VECTOR PECVD, Striker ALD and ALTUS tungsten/molybdenum deposition [25]
NAURA	China	Broad deposition portfolio; reports deposition equipment revenue above RMB10 billion in 2025 [29]
Piotech	China	Specialises in PECVD and ALD [23]
Tokyo Electron	Japan	Batch and metal deposition; claims leading positions in its stated categories [27]

Piotech cites historical Gartner data in which **Applied Materials, Lam Research and Tokyo Electron together account for about 70% of CVD** [23]. Lam's fiscal-2026 filing names Applied Materials as its principal competitor in dielectric and metal deposition, and also identifies ASM and South Korea's Wonik IPS in ALD and PECVD competition [25] Reported .

Single-wafer ALD and batch processing

ASM was founded in the Netherlands in **1968**. Its annual report describes the acquisitions of Finland's **Microchemistry in 1999** and South Korea's **Genitech in 2004** as foundations for its ALD position. It estimates its single-wafer ALD share at **above 55%** [28] Reported .

ASM reports **€3.173 billion** revenue in 2025, with Asia accounting for **80%**. Its report estimates a single-wafer ALD market of about **US$3.0 billion in 2024**, rising to **US$5.1–6.1 billion in 2030**. It identifies gate-all-around logic and advanced DRAM, particularly beyond 2028, as growth drivers [28]. These are the company's estimates and outlook, not guaranteed outcomes.

Japan has strong suppliers in vertical batch processing. Tokyo Electron's **2026 integrated report** claims first place in diffusion furnaces, batch deposition and metal deposition, using its own category definitions and estimates. It says deposition represented about **20% of new-equipment sales** in the year ended March 2026 [27]. Applying that share to ¥1,775.4 billion of new-equipment sales gives roughly **¥355 billion** Calculation .

KOKUSAI ELECTRIC reports **49%** of batch deposition in 2025 and around **80%** of batch ALD-capable equipment [14]. Its figures should not be treated as directly contradicting Tokyo Electron's first-place claim: the categories, scope or measurement basis may differ Interpretation . The sound conclusion is that both companies have important positions in batch processing, while exact cross-company comparisons need matched definitions.

Chinese suppliers and equipment demand

NAURA reports **RMB39.35 billion** of total 2025 revenue, up **31%**, including more than **RMB10 billion** from deposition equipment. Its portfolio spans PVD, CVD, epitaxy, ALD and plating [29]. Piotech reports **RMB6.52 billion** revenue, up **59%**, with cumulative shipments exceeding **3,400 reaction chambers** to roughly **100 production lines** [23] Reported .

Supplier headquarters and customer location answer different questions. SEAJ/SEMI's **2025** equipment-sales statistics put the worldwide total at **US$135.1 billion**, including **US$49.3 billion in China**, **US$31.5 billion in Taiwan**, **US$25.8 billion in South Korea** and **US$9.5 billion in Japan** [24]. These are **all semiconductor manufacturing equipment**, not deposition alone. ASM reports that China represented more than 30% of its 2025 equipment sales [28].

For another distinct measure, Japan's economy ministry reports that Japan-headquartered companies held about **28% of the global semiconductor equipment market in 2023** [30] Reported . None of these statistics is a deposition-only national market-share table.

Read the denominator before comparing shares

A share of single-wafer ALD is not a share of all deposition equipment. A supplier's home country is not the location where its tools are installed. Ask **who measured what, for which year and using which definition**. Most rankings here are company estimates or market-research figures quoted by companies.

10. Precursors: chemistry before the reactor

Designing a molecule that can become a useful film

A **precursor** contains an element needed in the film, such as hafnium, zirconium, aluminium or tungsten. It must be deliverable as a vapour, sufficiently stable during storage and transport, and reactive under the intended surface conditions. Unwanted residues must be kept low. Those requirements can compete with one another Explanation .

The **2024 IRDS Yield Enhancement** report describes increasing ALD adoption and the challenge of stable delivery. Its examples include precursor delivery pressures around **5–100 Torr**, reactors often operating below **1 Torr**, and source containers sometimes heated above **90°C** [20] Reported . These are reported examples, not settings for every precursor. Delivering a repeatable dose from a liquid or solid source is itself an engineering problem.

Suppliers across the materials chain

The same industry includes broad chemical groups and specialist manufacturers. Germany's **Merck KGaA** completed its acquisition of US-based **Versum Materials in October 2019** [34]. Japanese specialists **ADEKA** and **Tri Chemical Laboratories** have significant positions in advanced memory precursors. Their strengths can be described directly without treating this geographically diverse market as a national contest Explanation .

ADEKA reports a share above **50% in high-permittivity materials for advanced semiconductor memory** in its 2026 integrated report [31]. That is a specific materials category, not half of all ALD chemicals. It entered semiconductor materials through TEOS in **1988**, began high-k materials production for DRAM in Japan in **2004** and South Korea in **2006**, and added a Taiwan plant for logic applications in **2024** [31].

ADEKA reports fiscal-2025 revenue of **¥416.5 billion**, with semiconductor materials at **8.6%** [31]. Multiplying those figures gives about **¥35.8 billion** Calculation . It also describes growing shipments of advanced-DRAM products from a new Korean ALD-materials plant. A February 2025 presentation set a semiconductor-materials revenue target above **¥110 billion for fiscal 2030** [32]. That is a company target.

Tri Chemical Laboratories, established in **1978**, reports record revenue of **¥23.88 billion** for the year ended January 2026. High-k materials accounted for **47.9%**, metal-film materials **22.5%** and etching materials **14.7%**; memory applications represented **58.8%** [33]. Its reported regional revenue mix was **China 34.0%, Taiwan 33.8%, Japan 18.8% and South Korea 9.2%**. Management identifies DRAM high-k materials as a major growth driver over the preceding decade [33] Reported .

Together, these examples show that a film's performance depends on more than the deposition tool. Molecular design, purification, analysis, packaging and vapour delivery all contribute to a repeatable process Explanation .

11. What the next processes must achieve

- **Deposit only where needed.** Area-selective deposition exploits differences in surface chemistry to favour growth on one material over another. A 2018 imec/KU Leuven presentation discussed its potential and noted limited industrial examples at that time [21]. A 2019 review explored how selective ALD could reduce alignment errors [22]. Unwanted nucleation and loss of selectivity remain central process questions; selectivity is not a guarantee of error-free patterning.
- **Use new interconnect materials.** IRDS discusses new barriers, ALD barriers and alternatives to copper as features shrink [17]. Tungsten and molybdenum deposition for small features and NAND word lines illustrate the importance of matching material choice to integration requirements [25][27].
- **Control more layers and deeper features.** The 2023 roadmap's 500- and 1,000-layer NAND prospects make thickness, stress, defects and precursor penetration increasingly consequential [17]. These are dated roadmap directions, not a claim that every such structure is already in production.
- **Obtain useful films at lower temperature.** KOKUSAI ELECTRIC links demand for lower-temperature deposition to scaling, multilayer integration and three-dimensional devices [14]. As Lesson 3-2 explained, the available thermal budget becomes tighter as more temperature-sensitive structures are added.

Where materials expertise makes a difference

Deposition creates opportunities well beyond reactor design: new precursor molecules; purification and trace analysis; stable source containers and delivery lines; inhibitors and surface treatments for selective growth; and chamber components or coatings that resist deposition and corrosion. Each connects molecular behaviour to manufacturing consistency Explanation .

12. A compact comparison

Approach	What it changes	What still needs control
Thermal CVD	Gas-phase precursors react to form a film	Delivery, surface chemistry, temperature and by-product removal
LPCVD	Lower pressure reduces transport constraints	Temperature uniformity, supply and depletion across the load
PECVD	Energetic electrons help activate chemistry	Film quality, stress, hydrogen, heating and plasma damage
Conformal CVD	Suitable sticking/reaction conditions improve penetration	Geometry, dose and the difference between coating and filling
ALD	Sequential, saturated half-reactions control growth increments	Exposure, purge, nucleation and surface chemistry
Batch / spatial ALD	Improves throughput by parallel processing or spatial separation	Uniform exposure and effective reactant separation
PEALD	Plasma supplies reaction energy at lower wafer temperature	Damage, penetration and material properties

The next lesson, **3-4: Deposition by sputtering and plating**, turns from gas-phase chemistry to physical ejection of atoms and electrochemical growth. These methods become particularly important when building metal interconnects.

13. Check your understanding

1. Why are CVD and ALD needed if silicon can already be thermally oxidised?

▼ Show answer

Oxidation grows silicon dioxide by consuming silicon. A chip also needs other materials, including nitrides, metals and high-k dielectrics, and films on other underlying surfaces. CVD and ALD supply film-forming precursors externally, subject to chemical and temperature constraints.

2. What is the practical difference between reaction-limited and transport-limited growth?

▼ Show answer

Reaction-limited growth is especially sensitive to temperature because the surface reaction is slow. Transport-limited growth is especially sensitive to delivery, flow and reactor geometry because the surface consumes precursor faster than it arrives.

3. How does LPCVD help make batch deposition practical?

▼ Show answer

Reduced pressure can lessen transport constraints and make reaction-limited operation easier to obtain. A hot-wall furnace can then control many wafers' temperatures. Precursor supply and depletion must also be controlled; low pressure alone does not ensure uniformity.

4. How can PECVD assist growth at a lower wafer temperature?

▼ Show answer

Electrons gain energy from an electric field and excite or dissociate precursor molecules, creating reactive species. The plasma is not in thermal equilibrium, so electron energy need not imply the same temperature for the wafer. Heating, film properties and damage still matter.

5. Can a lower sticking probability improve a deep trench's coating?

▼ Show answer

Yes, under suitable supply and reaction conditions. Species are less likely to be consumed at the entrance and have more opportunity to reach deeper surfaces. The coefficient is process-dependent, and good coating does not automatically mean complete gap filling.

6. Why does ALD offer precise thickness control, and what goes wrong with insufficient purging?

▼ Show answer

Saturated, separated half-reactions make the growth increment reproducible once growth is established. Too little purge can let reactants coexist and produce CVD-like growth. The relevant condition is actual exposure and separation in the reactor, not simply alternating valve commands.

7. Approximately how many cycles produce 10 nm at 0.09 nm per cycle?

▼ Show answer

About 110 cycles: 10/0.09 ≈ 111. This is the stated 300°C TMA/water example under steady-growth conditions, not a universal ALD rate.

8. What did Intel use ALD for in its 2007 45 nm CMOS generation?

▼ Show answer

The hafnium-based high-k gate dielectric. Its engineers describe evaluating sputtering, CVD and ALD before selecting ALD. This was a major CMOS manufacturing milestone, not the beginning of all industrial ALD applications.

9. What are two major deposition tasks in 3D NAND?

▼ Show answer

Depositing the many alternating layers that form the stack, and forming metal word lines in lateral spaces between insulating layers. These horizontal word lines are different from the vertical channel feature.

14. Glossary

Deposition
Forming a thin solid film on a surface.

CVD
Chemical vapour deposition; gas-phase precursors undergo reactions that form a solid film.

Boundary layer
A near-surface region with changing flow velocity or concentration, where diffusion matters to transport.

Surface-reaction-limited growth
Growth controlled mainly by the rate of surface chemistry; often strongly temperature-sensitive.

Mass-transport-limited growth
Growth controlled mainly by precursor delivery rather than surface consumption.

Arrhenius relation
An exponential relationship between a reaction coefficient, activation energy and absolute temperature.

Activation energy
The energy barrier associated with a reaction pathway.

LPCVD
Low-pressure CVD; reduced pressure can ease transport constraints and support batch processing.

Mean free path
Average distance travelled by a gas molecule between collisions with other molecules.

Hot-wall reactor
A reactor in which the chamber or tube walls are heated along with the wafer load.

PECVD
Plasma-enhanced CVD; plasma activation can reduce the required wafer temperature.

Plasma
A partially ionised gas containing electrons, ions and neutral species.

Radical
An atom or molecule with an unpaired electron; many radicals are highly reactive.

HDP-CVD
High-density plasma CVD, combining deposition with ion-driven sputtering for applications such as gap filling.

Aspect ratio
Feature depth divided by width.

Step coverage
Film thickness on a feature's walls or bottom relative to its top surface.

Void
An unwanted enclosed empty space remaining within a deposited fill.

Sticking coefficient
A measure of the probability that an arriving species is captured or incorporated at a surface.

ALD
Atomic layer deposition, based on sequential self-limiting surface reactions.

Self-limiting reaction
A half-reaction that approaches saturation because of available sites and surface chemistry; it need not occupy every atomic site.

Purge
Removal of excess reactant and by-products, commonly with inert gas and pumping.

ALD window
An illustrative temperature range with relatively stable growth per cycle; not every ALD process has a flat window.

TMA
Trimethylaluminium, $Al(CH_3)_3$, a common aluminium precursor.

ALE
Atomic layer epitaxy, the name used for the Finnish development associated with Suntola from 1974.

Molecular layering
The name used for the independent Soviet development of sequential self-limiting growth.

Spatial ALD
ALD that separates reactants into different physical zones.

PEALD
Plasma-enhanced ALD, using plasma energy to assist a cyclic deposition reaction.

Spacer
A thin sidewall feature; its thickness can define dimensions in multiple patterning.

3D NAND
NAND flash memory with cells arranged through a multilayer vertical structure.

Word line
A conductor used to select memory cells.

Precursor
A source molecule supplying material to a deposition reaction.

Area-selective deposition
Growth favoured on selected surfaces through differences in surface chemistry.

15. Sources and further reading

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16. Claim-to-source notes

Claim group	Basis and limits	Type
Film examples, temperatures, seven CVD stages, transport/reaction model, 1.6 eV example, LPCVD, HDP-CVD and sticking coefficients	Stanford teaching material [1]; process examples, not universal modern specifications	Reported
Silane decomposition, nitride reaction, series-resistance analogy and aluminium temperature constraint	MIT CVD lecture, 2005 [2]; historical teaching context retained	Reported
Mean free path and diffusion scaling	MIT vacuum lecture [3]; its tabulated values are approximate	Reported
Representative plasma pressure and electron energies	University of Siegen lecture [4]; electron energy is distinct from gas/wafer temperature	Reported
Film roles, tungsten voids and word-line filling	Lam deposition and ALTUS descriptions [5][6]	Reported
ALD surface chemistry, growth per cycle, temperature window and purge effects	Puurunen 2005 [7]; TMA/water is a specific example	Reported
ALD applications and plasma-assisted lower-temperature reactions	ASM technology description [8]	Reported
Finnish patent dates; independent Soviet and Finnish developments	Patent [9] and Puurunen history/review [7][10]	Reported
Suntola's 2018 prize and semiconductor relevance	Technology Academy Finland [11]	Reported
Intel's 45 nm high-k adoption	First-person Intel engineering account [12]; specific CMOS milestone	Reported
Spatial separation, batch throughput and lower-temperature needs	Poodt et al. [13], KOKUSAI report [14] and ASM [8]	Reported
Spacers, NAND multilayers, roadmap dimensions, DRAM capacitor context	Lam [15][16], IRDS [17], SK hynix [18], DRAM paper introduction [19]	Reported
Precursor delivery examples	IRDS Yield Enhancement, 2024 [20]; not a universal recipe	Reported
Area-selective deposition potential and difficulties	2018 presentation [21] and 2019 review [22]; dated research context	Reported
Deposition market size, quoted Gartner concentration and Piotech shipments	Piotech annual report [23]; company-reported or company-quoted market data	Reported
Equipment purchases by region	SEAJ/SEMI 2025 statistics [24]; all equipment, not deposition alone	Reported
Lam and Applied portfolios and competition	SEC filings [25][26]	Reported
TEL categories and sales; KOKUSAI market shares	Corporate reports [27][14]; definitions are not harmonised	Reported
ASM history, revenue, share estimate and outlook	ASM Annual Report 2025 [28]; forecast is not guaranteed	Reported
NAURA revenue and portfolio	NAURA Annual Report 2025 [29]	Reported
Japan-headquartered suppliers' 2023 equipment share	METI summary [30]; all equipment	Reported
ADEKA history, material-category share, revenue mix and target	ADEKA reports/presentation [31][32]	Reported
Tri Chemical revenue, product/application mix and regions	Integrated Report 2026 [33]	Reported

Claim group	Basis and limits	Type
Merck–Versum transaction	SEC filing [34]	Reported
3.2× temperature effect; 68 nm / 52 µm free paths; electron energy scale; ≈110 cycles; TEL and ADEKA revenue estimates	Calculations using the stated source inputs and assumptions	Calculation
Possible differences between batch-deposition market definitions	Interpretation; not independently reconciled market datasets	Interpretation
Intuitive explanations of transport, sticking, saturation and device structures	General principles illustrated schematically; not quantitative process simulations	Explanation

Updated 7 November 2026. This English edition is written for an international readership from the same technical material as the Japanese article. Historical teaching examples and company figures retain their source dates and definitions. Reported facts, calculations, interpretation and explanation are labelled separately. All six Image Gen diagrams are schematics, not process simulations. Photographs and the historical reconstruction retain their individual credits and licences.

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Teaching diagrams localised with the built-in Image Gen tool for this English edition.